Lab Report 8 – Design and Implementation of a Digital Up/Down Counter from 0 to 99

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1 First digit

BCD Up Counter State Transition Table (0 to 9 with Don't Cares)

Present State				Next State				T Inputs				Remark
Q_3	Q_2	Q_1	Q_0	Q_3^+	Q_2^+	Q_1^+	Q_0^+	T_3	T_2	T_1	T_0	
0	0	0	0	0	0	0	1	0	0	0	1	$0 \to 1$
0	0	0	1	0	0	1	0	0	0	1	1	$1 \to 2$
0	0	1	0	0	0	1	1	0	0	0	1	$2 \to 3$
0	0	1	1	0	1	0	0	0	1	1	1	$3 \to 4$
0	1	0	0	0	1	0	1	0	0	0	1	$4 \to 5$
0	1	0	1	0	1	1	0	0	0	1	1	$5 \to 6$
0	1	1	0	0	1	1	1	0	0	0	1	$6 \to 7$
0	1	1	1	1	0	0	0	1	1	1	1	$7 \to 8$
1	0	0	0	1	0	0	1	0	0	0	1	$8 \to 9$
1	0	0	1	0	0	0	0	1	0	0	1	$9 \to 0$
1	0	1	0	X	X	X	X	X	X	X	X	Don't Care
1	0	1	1	X	X	X	X	X	X	X	X	Don't Care
1	1	0	0	X	X	X	X	X	X	X	X	Don't Care
1	1	0	1	X	X	X	X	X	X	X	X	Don't Care
1	1	1	0	X	X	X	X	X	X	X	X	Don't Care
1	1	1	1	X	X	X	X	X	X	X	X	Don't Care

Karnaugh Maps for T Flip-Flop Inputs

Up Counter (Controlled by $B_u \cdot \overline{B_d}$)

T_0 **(Up)**

$$(T_0)_{up} = B_u \cdot \overline{B_d} \cdot 1 = B_u \cdot \overline{B_d}$$

	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

T_1 **(Up)**

$$(T_1)_{up} = Q_0 \cdot \overline{Q_3} \cdot B_u \cdot \overline{B_d}$$

	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	X	X	X	X
10	0	0	X	X

T_2 **(Up)**

$$(T_2)_{up} = Q_0 \cdot Q_1 \cdot B_u \cdot \overline{B_d}$$

	00	01	11	10
00	0	0	1	0
01	0	0	1	0
11	X	X	X	X
10	0	0	X	X

T_3 **(Up)**

$$(T_3)_{up} = Q_0 \cdot (Q_3 + Q_2 Q_1) \cdot B_u \cdot \overline{B_d}$$

	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	0	1	X	X

BCD Down Counter State Transition Table (9 to 0 with Don't Cares)

Present State				Next State				T Inputs				Remark
Q_3	Q_2	Q_1	Q_0	Q_3^-	Q_2^-	Q_1^-	Q_0^-	T_3	T_2	T_1	T_0	
1	0	0	1	1	0	0	0	0	0	0	1	$9 \to 8$
1	0	0	0	0	1	1	1	1	1	1	1	$8 \to 7$
0	1	1	1	0	1	1	0	0	0	0	1	$7 \to 6$
0	1	1	0	0	1	0	1	0	0	1	1	$6 \to 5$
0	1	0	1	0	1	0	0	0	0	0	1	$5 \to 4$
0	1	0	0	0	0	1	1	0	1	1	1	$4 \to 3$
0	0	1	1	0	0	1	0	0	0	0	1	$3 \to 2$
0	0	1	0	0	0	0	1	0	0	1	1	$2 \to 1$
0	0	0	1	0	0	0	0	0	0	0	1	$1 \to 0$
0	0	0	0	1	0	0	1	1	0	0	1	$0 \to 9$
1	0	1	0	X	X	X	X	X	X	X	X	Don't Care
1	0	1	1	X	X	X	X	X	X	X	X	Don't Care
1	1	0	0	X	X	X	X	X	X	X	X	Don't Care
1	1	0	1	X	X	X	X	X	X	X	X	Don't Care
1	1	1	0	X	X	X	X	X	X	X	X	Don't Care
1	1	1	1	X	X	X	X	X	X	X	X	Don't Care

Down Counter (Controlled by $\overline{B_u} \cdot B_d$)

T_0 **(Down)**

$$T_0 = \overline{B_u} \cdot B_d$$

	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

T_1 **(Down)**

$$T_1 = \overline{Q_0} \cdot (Q_1 + Q_2 + Q_3) \cdot \overline{B_u} \cdot B_d$$

	00	01	11	10
00	0	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

T_2 **(Down)**

$$T_2 = \overline{Q_1} \cdot \overline{Q_0} \cdot (Q_2 + Q_3) \cdot \overline{B_u} \cdot B_d$$

	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	X	X	X	X
10	1	0	X	X

T_3 **(Down)**

$$T_3 = \overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0} \cdot \overline{B_u} \cdot B_d$$

	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	X	X	X	X
10	1	0	X	X

Combined T Flip-Flop Expressions (Up and Down Modes)

T_0 **(Overall)**

$$T_0 = B_u \cdot \overline{B_d} + \overline{B_u} \cdot B_d$$

T_1 **(Overall)**

$$T_1 = Q_0 \cdot \overline{Q_3} \cdot B_u \cdot \overline{B_d} + \overline{Q_0} \cdot (Q_1 + Q_2 + Q_3) \cdot \overline{B_u} \cdot B_d$$

T_2 **(Overall)**

$$T_2 = Q_0 \cdot Q_1 \cdot B_u \cdot \overline{B_d} + \overline{Q_1} \cdot \overline{Q_0} \cdot (Q_2 + Q_3) \cdot \overline{B_u} \cdot B_d$$

T_3 **(Overall)**

$$T_3 = Q_0 \cdot (Q_3 + Q_2 Q_1) \cdot B_u \cdot \overline{B_d} + \overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0} \cdot \overline{B_u} \cdot B_d$$

2 Second Digit

We know that the state transition table and k-maps for the second digit will be same but we have to ensure that second digit only changes when first digit either transits form 9 to 0 or 0 to 9 i,e

Present State				Next State				T Inputs				Remark
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	T_3	T_2	T_1	T_0	
0	0	0	0	1	0	0	1	1	0	0	1	$0 \to 9$
1	0	0	1	0	0	0	0	1	0	0	1	$9 \to 0$

Therefore,

$$\begin{aligned}
T_0' &= (T_0)_{up} \cdot \overline{Q_3} \cdot \overline{Q_0} + (T_0)_{down} \cdot \overline{Q_3} \cdot \overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0} \\
T_1' &= (T_1)_{up} \cdot \overline{Q_3} \cdot \overline{Q_0} + (T_1)_{down} \cdot \overline{Q_3} \cdot \overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0} \\
T_2' &= (T_2)_{up} \cdot \overline{Q_3} \cdot \overline{Q_0} + (T_2)_{down} \cdot \overline{Q_3} \cdot \overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0} \\
T_3' &= (T_3)_{up} \cdot \overline{Q_3} \cdot \overline{Q_0} + (T_3)_{down} \cdot \overline{Q_3} \cdot \overline{Q_2} \cdot \overline{Q_1} \cdot \overline{Q_0}
\end{aligned}$$

3 Circuit Design

Mainly the circuit is built using logic gates and jk flip-flop

3.1 Components

- **Arduino Uno** – 1
  Provides 5V power and possibly input control (button pulse or clock).
- **Breadboards** – 3
  Two medium-sized for ICs and one large for extra wiring space.
- **74HC73 (JK Flip-Flop)** – 6
  Dual JK flip-flops with Clear; used for BCD counting and acts as T flip flop when J and K are shorted(4 bits per digit).
- **74HC00 (Quad 2-input NAND gate)** – 3
  Used for implementing logic conditions.

- **74HC08 (Quad 2-input AND gate)** – 3
  Used to enable logic outputs as per Karnaugh expressions.
- **74HC32 (Quad 2-input OR gate)** – 3
  Used to combine logic signals.
- **74HC04 (Hex Inverter / NOT gate)** – 2
  Used for inverting control and data signals.
- **CD4511 (BCD to 7-segment decoder)** – 2
  Drives 7-segment displays using 4-bit BCD input.
- **7-Segment Displays** – 2
  Likely common cathode; used to visually represent counter value.
- **Push Buttons** – 3
  Used for manual Up, Down, and Reset controls.
- **Resistors** – approximately 10–15
  Used for pull-down configurations and current limiting on LEDs.
- **Jumper Wires** – Multiple
  For all the required interconnections across components and breadboards.

3.2 Circuit Schematic

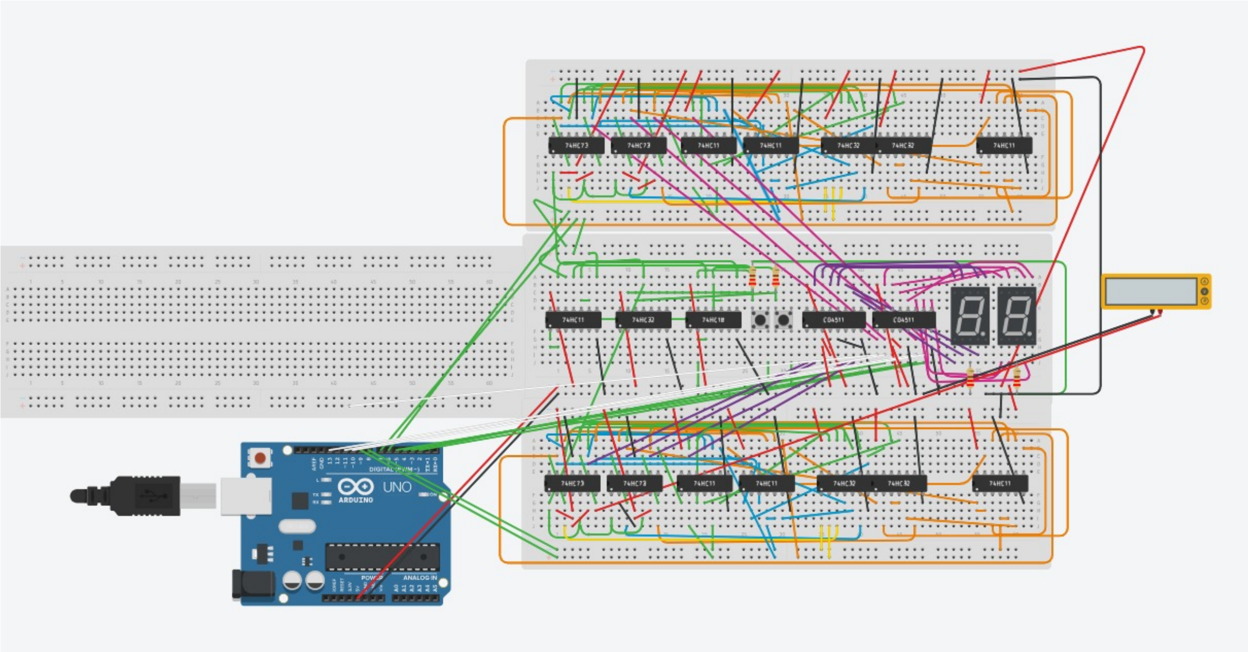
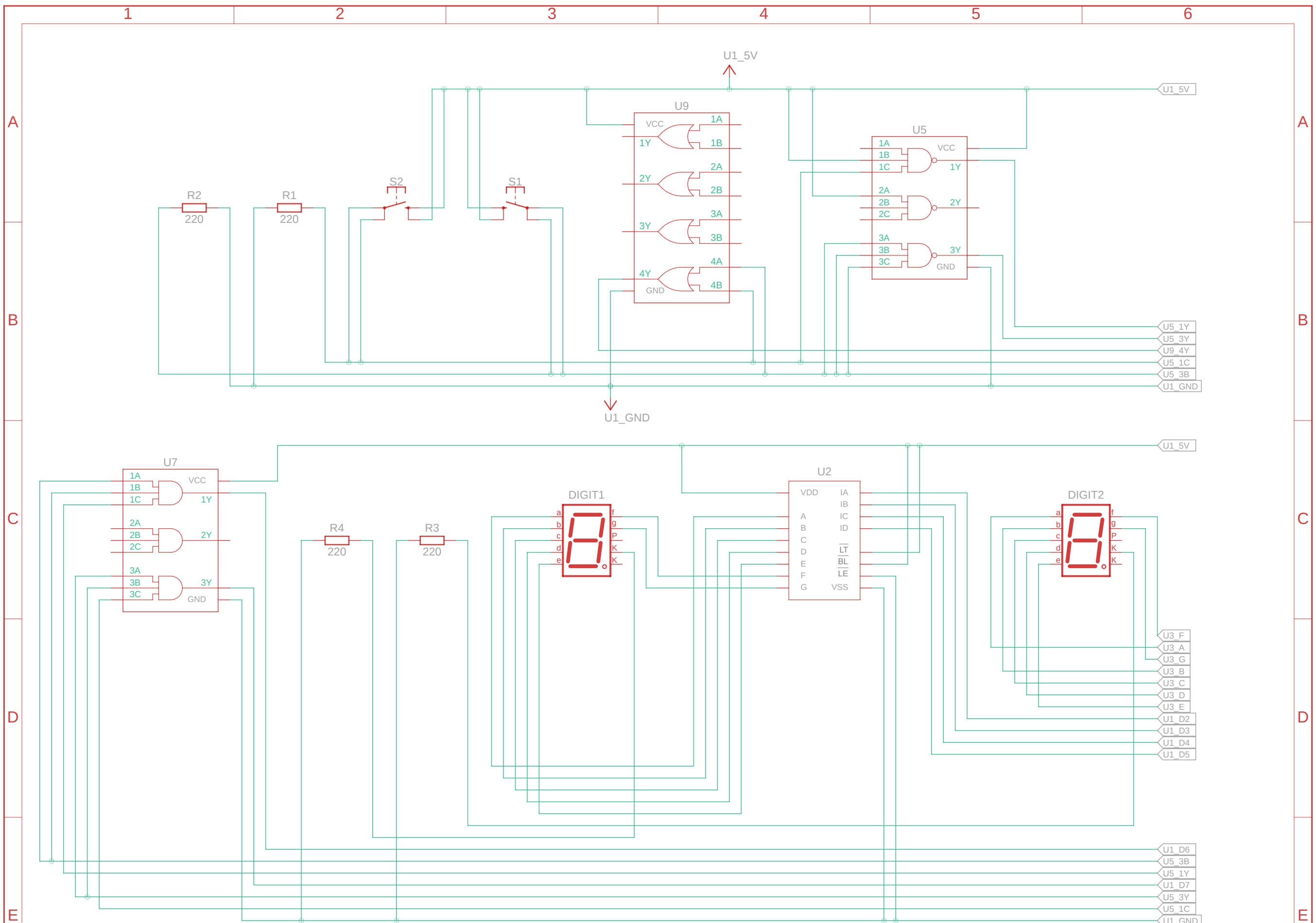


Figure 1: Breadboard implementation of a BCD up/down counter using T flip-flops and logic gates.

3.3 Wiring



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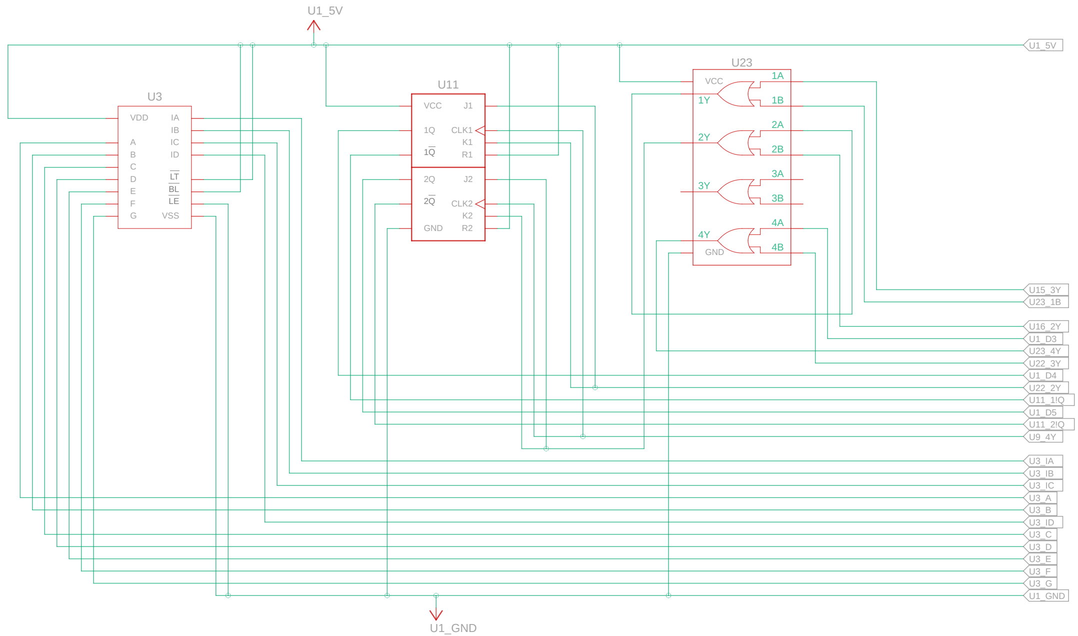

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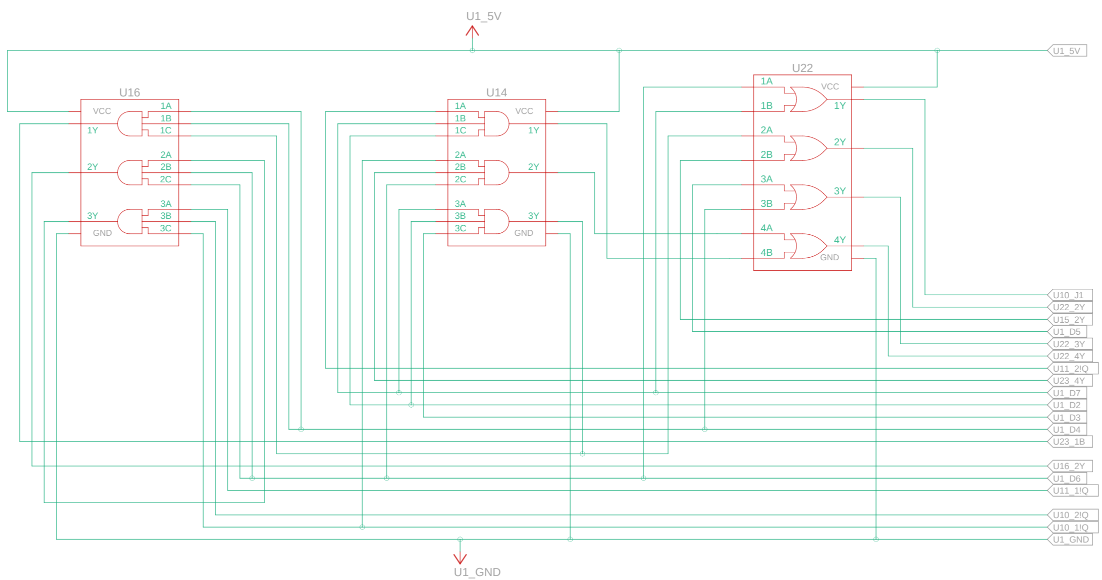

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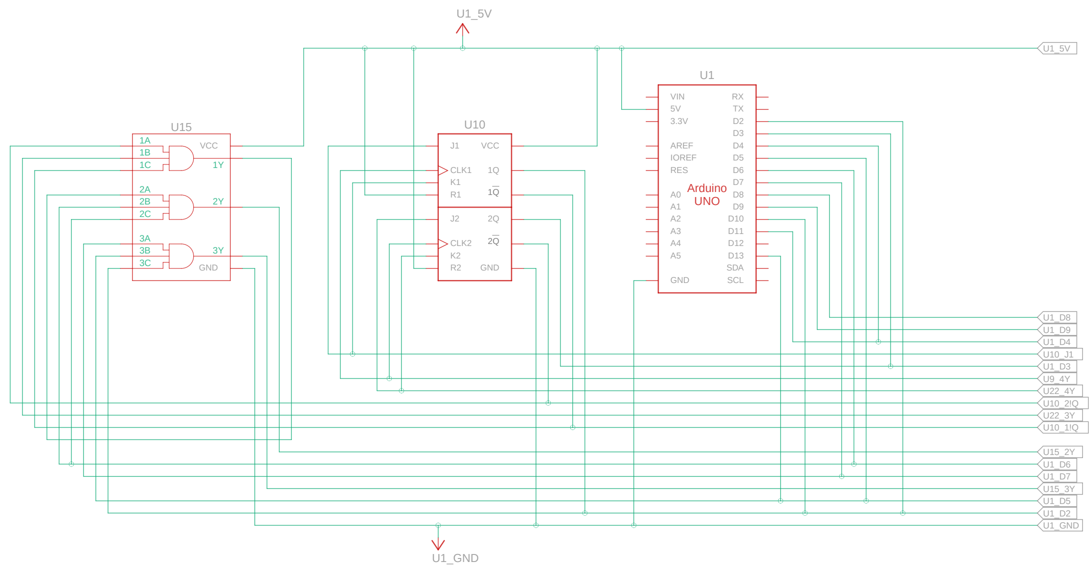

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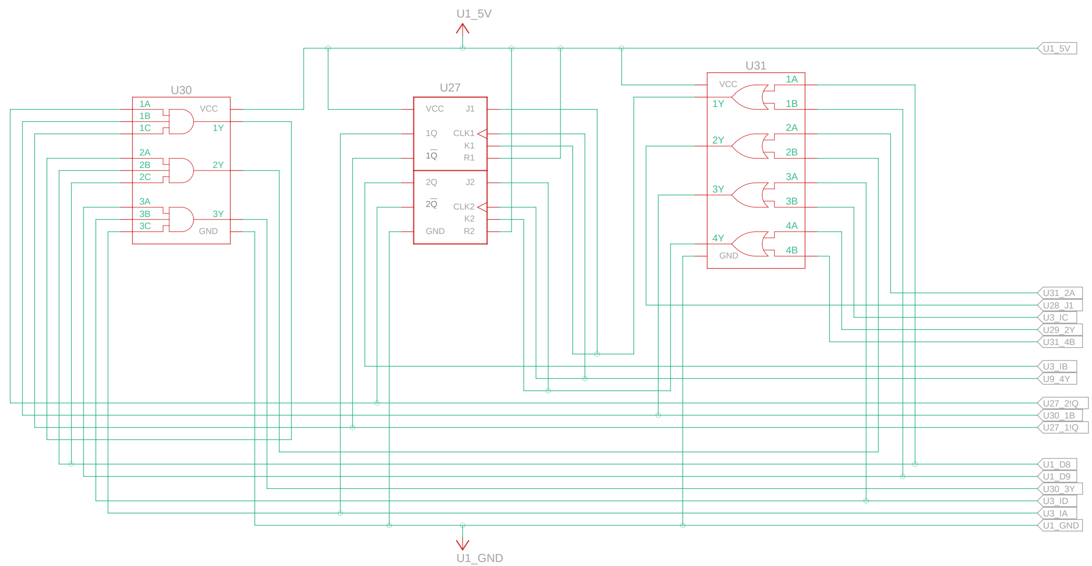

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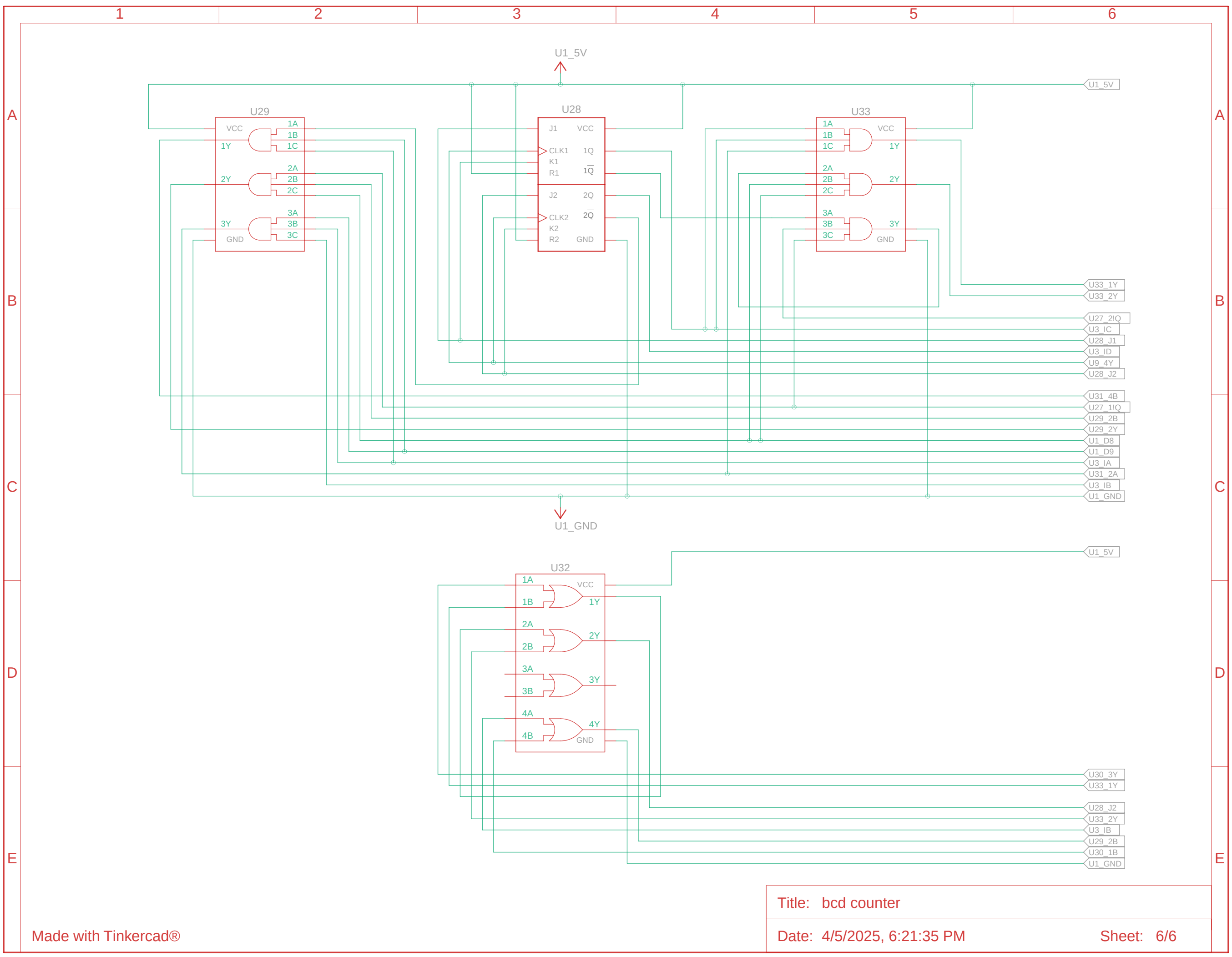
1
2
3
4
5
6
A
B
C
D
E
U1_5V
U29
U28
U33
U1_GND
U32
U33_1Y
U33_2Y
U27_2!Q
U3_IC
U28_J1
U3_ID
U9_4Y
U28_J2
U31_4B
U27_1!Q
U29_2B
U29_2Y
U1_D8
U1_D9
U3_IA
U31_2A
U3_IB
U30_3Y
U30_1B
Title: bcd counter
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3.4 Simulation

4 Conclusion

The above circuit performs number counting from 0 to 99.When up button is pressed the number increases by one and down button is pressed number decreases by one