Lab Report7

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1 Objective

To design a Mod-7 Asynchronous Counter using JK Flip-Flops (JK FFs) and demonstrate its performance using a CRO (Cathode Ray Oscilloscope) with a clock from an Arduino

2 Components Required

- IC 7476 (Dual JK Flip-Flop)
- IC 7410 (Triple 3-input NAND Gate)
- Arduino UNO(for clock signal)
- 7-segment Anode dispaly to show count
- 7447 IC (7-segement display decoder)
- 220Ω Resistor

3 Circuit

Component	Pin	Connection
Arduino Connections		
Arduino	Pin 13	Clock Input to First 7476 Flip-Flop
7476 (First Flip-Flop - Q1)		
7476 (IC1)	VCC (Pin 16)	+5V
7476 (IC1)	GND (Pin 8)	0V (Ground)
7476 (IC1)	J1, K1	+5V (HIGH)
7476 (IC1)	CLK1	Arduino Pin 13 (Clock)
7476 (IC1)	Q1 (Pin 15)	Clock for Second Flip-Flop
7476 (IC1)	PRE1, CLR1	+5V (HIGH)
7476 (IC1)	CLR1	Input from 7410 NAND Gate
7476 (Second Flip-Flop - Q2)		
7476 (IC2)	J2, K2	+5V (HIGH)
7476 (IC2)	CLK2	Q0 Output from First Flip-Flop
7476 (IC2)	Q2 (Pin 15)	Input to 7410 NAND Gate
7476 (IC2)	PRE2	+5V (HIGH)
7476 (IC2)	CLR2	Input from 7410 NAND Gate
7476 (Third Flip-Flop - Q3)		
7476 (IC3)	J3, K3	+5V (HIGH)
7476 (IC3)	CLK2	Q1 Output from First Flip-Flop
7476 (IC3)	Q3 (Pin 15)	Input to 7410 NAND Gate
7476 (IC3)	PRE3	+5V (HIGH)
7476 (IC3)	CLR3	Input from 7410 NAND Gate
7410 (NAND Gate for Reset)		
7410 (IC3)	Input 1	Q0 from 7476
7410 (IC3)	Input 2	Q1 from 7476
7410 (IC3)	Input 3	Q2 from 7476
7410 (IC3)	Output	CLR of Both 7476 Flip-Flops
7447 (BCD to 7-Segment Decoder)		
7447 (IC4)	A (Pin 7)	Q0 from Flip-Flop
7447 (IC4)	B (Pin 1)	Q1 from Flip-Flop
7447 (IC4)	C (Pin 2)	Q2 from Flip-Flop
7447 (IC4)	D (Pin 6)	GND (Always 0 for MOD-7 Counter)
7447 (IC4)	Outputs (a-g)	Corresponding Pins of 7-Segment Display
7447 (IC4)	VCC (Pin 16)	+5V
7447 (IC4)	GND (Pin 8)	0V (Ground)
7-Segment Display		
7-Segment	a-g	Corresponding Pins from 7447
7-Segment	Common Anode	+5V via 220Ω Resistor

Table 1: Connections for Mod-7 Asynchronous Counter with Display

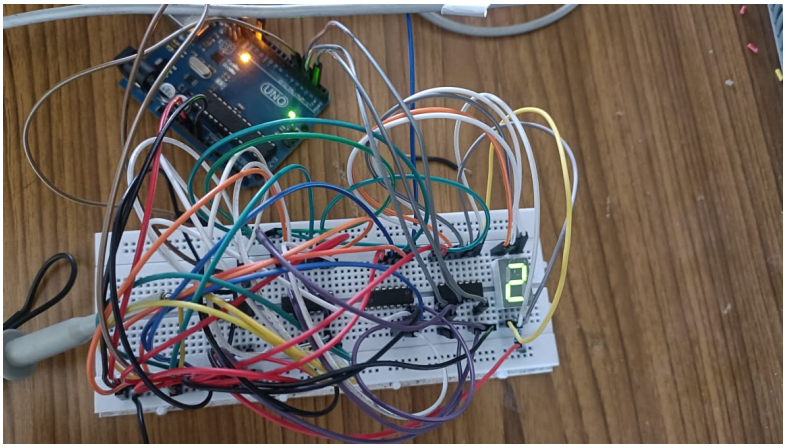

Figure 1: Circuit Diagram of Mod-7 Counter

4 Truth Table

J	**K**	**Q (Previous State)**	**Q (Next State)**
0	0	Q	Q (No Change)
0	1	Q	0 (Reset)
1	0	Q	1 (Set)
1	1	Q	$\overline{Q}$ (Toggle)

Table 2: Truth Table of JK Flip-Flop

Clock Cycle	Q2	Q1	Q0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0 (Reset)

Table 3: Truth Table for Mod-7 Counter

5 Observations and Results

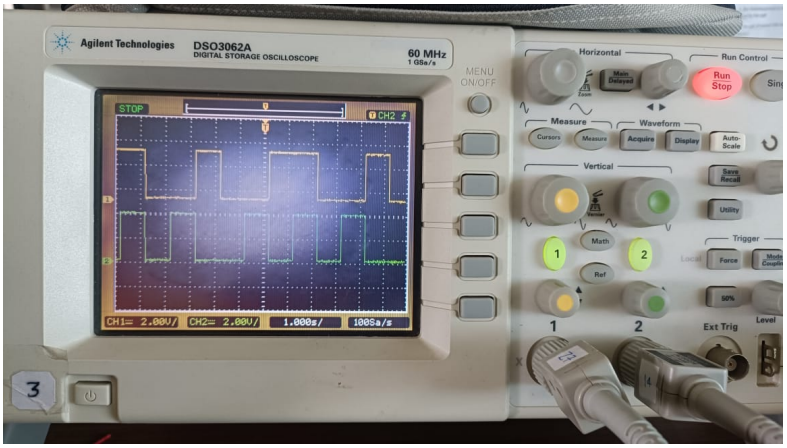

Figure 2: Channel1-Q2,Channel2-Q1

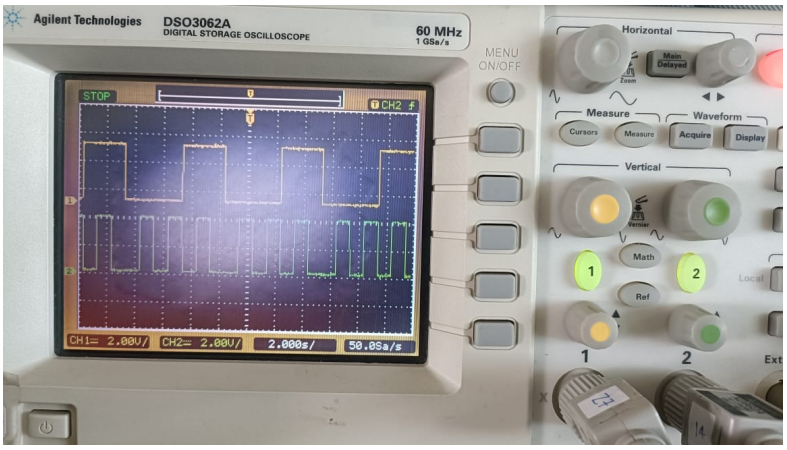

Figure 3: Channel1-Q3,Channel2-Q1

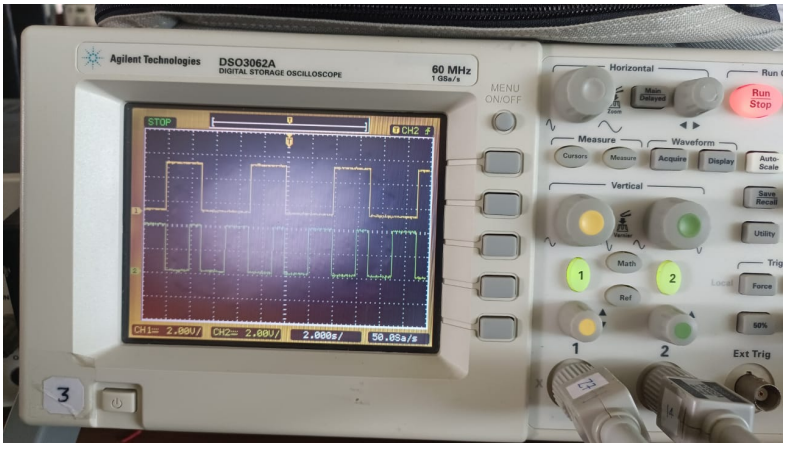

Figure 4: Channel1-Q3,Channel2-Q2

```
Q0:0 Q1:1 Q2:1 Test:0
Q0:0 Q1:0 Q2:0 Test:0
Q0:1 Q1:0 Q2:0 Test:0
Q0:0 Q1:1 Q2:0 Test:0
Q0:1 Q1:1 Q2:0 Test:0
Q0:0 Q1:0 Q2:1 Test:0
Q0:1 Q1:0 Q2:1 Test:0
Q0:0 Q1:1 Q2:1 Test:0
Q0:0 Q1:0 Q2:0 Test:0
Q0:1 Q1:0 Q2:0 Test:0
Q0:0 Q1:1 Q2:0 Test:0
Q0:1 Q1:1 Q2:0 Test:0
Q0:0 Q1:0 Q2:1 Test:0
Q0:1 Q1:0 Q2:1 Test:0
Q0:0 Q1:1 Q2:1 Test:0
Q0:0 Q1:0 Q2:0 Test:0
Q0:1 Q1:0 Q2:0 Test:0
Q0:0 Q1:1 Q2:0 Test:0
Q0:1 Q1:1 Q2:0 Test:0
Q0:0 Q1:0 Q2:1 Test:0
Q0:1 Q1:0 Q2:1 Test:0
Q0:0 Q1:1 Q2:1 Test:0
Q0:0 Q1:0 Q2:0 Test:0
Q0:1 Q1:0 Q2:0 Test:0
Q0:0 Q1:1 Q2:0 Test:0
Q0:1 Q1:1 Q2:0 Test:0
Q0:0 Q1:0 Q2:1 Test:0
Q0:1 Q1:0 Q2:1 Test:0
Q0:0 Q1:1 Q2:1 Test:0
Q0:0 Q1:0 Q2:0 Test:0
Q0:1 Q1:0 Q2:0 Test:0
Q0:0 Q1:1 Q2:0 Test:0
Q0:1 Q1:1 Q2:0 Test:0
Q0:0 Q1:0 Q2:1 Test:0
Q0:1 Q1:0 Q2:1 Test:0
Q0:0 Q1:1 Q2:1 Test:0
Q0:0 Q1:0 Q2:0 Test:0
Q0:1 Q1:0 Q2:0 Test:0
Q0:0 Q1:1 Q2:0 Test:0
Q0:1 Q1:1 Q2:0 Test:0
Q0:0 Q1:0 Q2:1 Test:0
Q0:1 Q1:0 Q2:1 Test:0
Q0:0 Q1:1 Q2:1 Test:0
```

Figure 5: ArduinoSerialMonitor

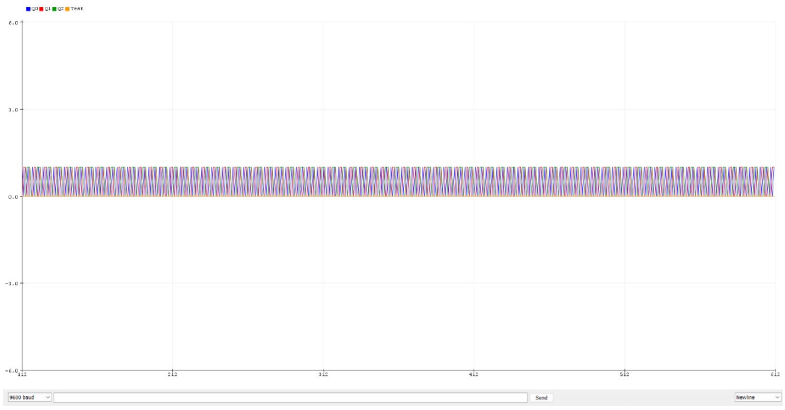

Figure 6: ArduinoSerialPlotter

- The counter correctly cycles through states 0 to 6 before resetting.
- The clock signal from Arduino successfully triggered the JK flip-flops.
- The video of the counter is in the github repository.

To check the codes, video etc. refer `https://github.com/ArnavYadnopavit/ElectricalLabEE1200/tree/main/LabReport7`

Thank You