Digital Clock Design in Verilog

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1 Overview

This project implements a complete digital clock system in Verilog HDL, featuring:

- A **timekeeper** module with support for 12h/24h modes and full date management (Jan 2020 to Apr 2025),
- A countdown **timer**,
- A configurable **alarm**, and
- A top-level FSM to switch between clock, timer, and alarm modes.

2 Timekeeper Module

The `timekeeper` module is the core of the clock system, maintaining current time and date. It is implemented as a 4-state finite state machine (FSM), where each state updates a different component of the clock:

2.1 States

- `S_SEC`: Increments seconds every clock tick.
- `S_MIN`: Rolls over seconds and increments minutes.
- `S_HR`: Increments hours and handles AM/PM toggling.
- `S_DATE`: Manages day, month, and year transitions including leap year handling.

2.2 AM/PM Mode

The module supports both 12-hour and 24-hour formats using the `AM_mode` signal. Transitions between formats are dynamically handled by converting the hour and setting the AM/PM bit accordingly.

2.3 Manual Adjustments

The `add_hour` and `add_minute` signals allow manual time adjustment. They increment the respective values, correctly handling overflows and AM/PM toggles.

2.4 Leap Year and Date Range

Leap years are computed using the standard Gregorian rules:

- Divisible by 4 and not 100, or divisible by 400.

The date is bounded between Jan 2020 and Apr 2025, and wraps back to Jan 2020 after 30-Apr-2025.

3 Timer Module

The `timer_module` implements a simple countdown timer:

- Takes minutes as input and counts down in seconds.
- A buzzer is activated when the countdown reaches zero.
- The timer is triggered using the `set_timer` input.

4 Alarm Module

The `alarm_module` allows users to set a daily alarm:

- The user provides `alarm_hr` and `alarm_min`.
- The alarm buzzer is triggered when the current time matches the set alarm time (with second = 0).

5 Digital Clock Integration

The `digital_clock` module integrates the timekeeper, timer, and alarm modules. It connects the outputs of the timekeeper to the alarm, and takes mode-specific control inputs for the timer and alarm settings.

6 Top-Level FSM: Mode Management

The `clock_with_mode_fsm` module manages high-level user interaction through a 3-state FSM:

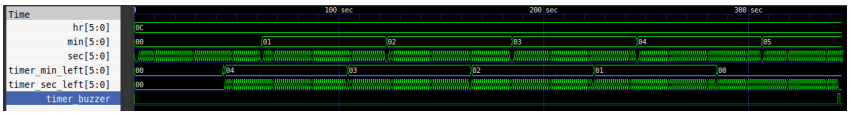
- `IDLE`: Regular clock mode; manual time setting is allowed.
- `SET_TIMER`: Timer configuration; minute increments adjust the timer duration.
- `SET_ALARM`: Alarm configuration; hours and minutes set the alarm time.

Transitions between states are triggered by a mode button. Each mode enables appropriate functionality while isolating input changes to relevant subsystems.

7 Timing Diagrams

7.1 Alarm

7.2 Timer



7.3 Display

For codes refer to `https://github.com/ArnavYadnopavit/FinalProjectDSLab`

Thank You