DRV5013 Digital-Latch Hall Effect Sensor

1 Features

- Digital Bipolar-Latch Hall Sensor
- Superior Temperature Stability
  - B_{OP} ±10% Over Temperature
- High Sensitivity Options (B_{OP} and B_{RP})
  - +2.3 / –2.3 mT (AD, see Figure 22)
  - +4.6 / –4.6 mT (AG, see Figure 22)
  - +9.2 / –9.2 mT (BC, see Figure 22)
- Supports a Wide Voltage Range
  - 2.5 to 38 V
  - Operation from Unregulated Supply
- Wide Operating Temperature Range
  - T_A = –40 to 125°C (Q, see Figure 22)
- Open Drain Output
  - Up to 30-mA Current Sink
- Fast Power-On
  - 35 µs
- Small Package and Footprint
  - Surface Mount 3-Terminal SOT-23 (DBZ)
    - 2,92 mm × 2,37 mm
  - Through-Hole 3-Terminal SIP (LPG)
    - 4,00 mm × 3,15 mm
- **Protection Features**
  - Reverse Supply Protection (up to –22 V)
  - Supports up to 40-V Load Dump
  - Output Short-Circuit Protection
  - Output Current Limitation

2 Applications

- Power Tools
- Flow Meters
- Valve and Solenoid Status
- BLDC Motors With Sensors
- Proximity Sensing
- Tachometers

3 Description

The DRV5013 device is a chopper-stabilized Hall Effect Sensor that offers a magnetic sensing solution with superior sensitivity stability over temperature and integrated protection features.

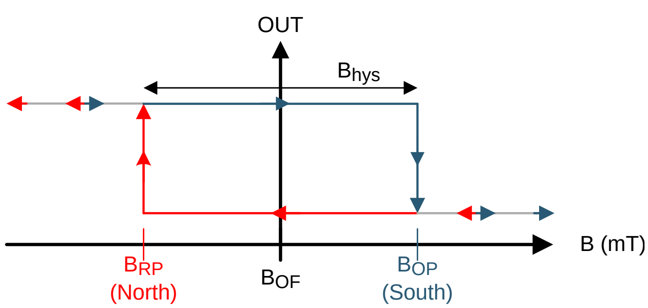
The magnetic field is indicated via a digital bipolar latch output. The IC has an open drain output stage with 30-mA current sink capability. A wide operating voltage range from 2.5 V to 38 V with reverse polarity protection up to –22 V makes the device suitable for a wide range of industrial applications.

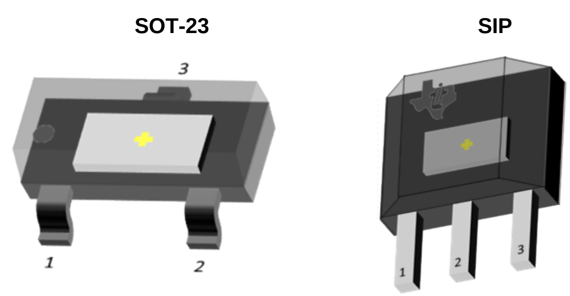
Internal protection functions are provided for reverse supply conditions, load dump, and output short circuit or over current.

Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV5013	SOT-23 (3)	2.92 × 2.37 mm
	SIP (3)	4.00 × 3.15 mm

4 Output State





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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2014) to Revision B — **Page**

- Changed I_{OCP} minimum and maximum values from 20 and 40 to 15 and 45 (respectively) in the *Electrical Characteristics* table 5
- Updated the hysteresis values for each device option in the *Magnetic Characteristics* table.......... 5
- Changed the MIN value for the +2.3 / – 2.3 mt B_{RP} parameter from –4 to –5 in the *Magnetic Characteristics* table 5

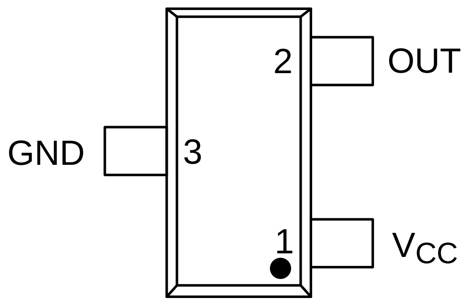
Changes from Original (March 2014) to Revision A — **Page**

- Changed the power-on value from 50 to 35 µs in the *Features* list 1
- Changed *RPM Meter* to *Tachometers* in the *Applications* list 1
- Changed all references to Hall IC to Hall Effect Sensor 1
- Changed the type of the OUT terminal from OD to Output in the *Terminal Functions* table 3
- Deleted the Output terminal current row in the *Absolute Maximum Ratings* table and changed V_{CC}max to V_{CC} after the voltage ramp rate for the power supply voltage 4
- Changed R_O to R1 in the test conditions for t_r and t_f in the *Switching Characteristics* table.......... 5
- Added the bandwidth parameter to the *Magnetic Characteristics* table 5
- Changed the MIN value for the +2.3 / – 2.3 mt B_{RP} parameter from +2.3 to –2.3 in the *Magnetic Characteristics* table 5
- Deleted the condition statement from the *Typical Characteristics* section and changed all references of T_J to T_A in the graph condition statements 6
- Deleted *Number* from the Power-On Time case names and added conditions to the captions of the case timing diagrams 10
- Added the R1 tradeoff and lower current text after the equation in the *Output Stage* section 12
- Added the C2 not required for most applications text after the second equation in the *Output Stage* section.......... 13
- Changed I_O to I_{SINK} in the condition statement of the FET overload fault condition in the *Reverse Supply Protection* section 14

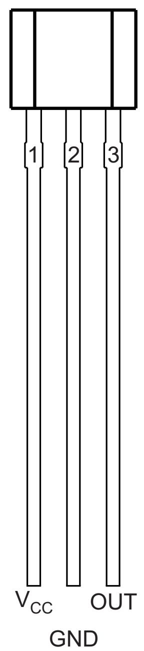
6 Terminal Configuration and Functions

For additional configuration information, see Device Markings and Mechanical, Packaging, and Orderable Information.

3-Terminal SOT-23
DBZ Package
(Top View)



3-Terminal SIP
LPG Package
(Top View)



Terminal Functions

TERMINAL			TYPE	DESCRIPTION
NAME	NUMBER			
	DBZ	LPG		
GND	3	2	GND	Ground terminal
OUT	2	3	Output	Hall sensor open-drain output. The open drain requires a resistor pullup.
V_{CC}	1	1	PWR	2.5 to 38 V power supply. Bypass this terminal to the GND terminal with a 0.01-µF (minimum) ceramic capacitor rated for V_{CC}.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–22 [2]	40	V
	Voltage ramp rate (V_{CC}), V_{CC} < 5 V	Unlimited		V/µs
	Voltage ramp rate (V_{CC}), V_{CC} > 5 V	0	2	
Output terminal voltage	OUT	–0.5	40	V
Output terminal reverse current during reverse supply condition	OUT	0	100	mA
Operating junction temperature, T_J		–40	175	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Ensured by design. Only tested to –20 V.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–65	150	°C
$V_{(ESD)}$	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [1]	–2.5	2.5	kV
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins [2]	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage	2.5	38	V
V_O	Output terminal voltage (OUT)	0	38	V
I_{SINK}	Output terminal current sink (OUT) [1]	0	30	mA
T_A	Operating ambient temperature	–40	125	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC [1]		DBZ (3 TERMINALS)	LPG (3 TERMINALS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	333.2	180	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.9	98.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	66.9	154.9	
ψ_{JT}	Junction-to-top characterization parameter	4.9	40	
ψ_{JB}	Junction-to-board characterization parameter	65.2	154.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (V_{CC})						
V_{CC}	V_{CC} operating voltage		2.5		38	V
I_{CC}	Operating supply current	V_{CC} = 2.5 to 38 V, T_A = 25°C		2.7		mA
		V_{CC} = 2.5 to 38 V, T_A = 125°C		3	3.5	
t_{on}	Power-on time			35	50	µs
OPEN DRAIN OUTPUT (OUT)						
$r_{DS(on)}$	FET on-resistance	V_{CC} = 3.3 V, I_O = 10 mA, T_A = 25°C		16		Ω
		V_{CC} = 3.3 V, I_O = 10 mA, T_A = 125°C		25	50	
$I_{lkg(off)}$	Off-state leakage current	Output Hi-Z			1	µA
PROTECTION CIRCUITS						
V_{CCR}	Reverse supply voltage		–22			V
I_{OCP}	Overcurrent protection level	Output current is clamped to this level	15	30	45	mA

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN DRAIN OUTPUT (OUT)						
t_d	Output delay time	B = B_{RP} – 10 mT to B_{OP} + 10 mT in 1 µs		13	25	µs
t_r	Output rise time (10% to 90%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V			0.5	µs
t_f	Output fall time (90% to 10%)	R1 = 1 kΩ, C_O = 50 pF, V_{CC} = 3.3 V			0.2	µs

7.7 Magnetic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT(1)
f_{BW}	Bandwidth		20			kHz
DRV5013AD: +2.3 / –2.3 mT						
B_{OP}	Operate point; see Figure 12	T_A = –40°C to 125°C	+1	+2.3	+5	mT
B_{RP}	Release point; see Figure 12		–5	–2.3	–1	mT
B_{hys}	Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$			5		mT
B_O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		–1.5	0	+1.5	mT
DRV5013AG: +4.6 / –4.6 mT						
B_{OP}	Operate point; see Figure 12	T_A = –40°C to 125°C	+2	+4.6	+8	mT
B_{RP}	Release point; see Figure 12		–8	–4.6	–2	mT
B_{hys}	Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$			9		mT
B_O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		–1.5	0	+1.5	mT
DRV5013BC: +9.2 / –9.2 mT						
B_{OP}	Operate point; see Figure 12	T_A = –40°C to 125°C	+4	+9.2	+16	mT
B_{RP}	Release point; see Figure 12		–16	–9.2	–4	mT
B_{hys}	Hysteresis; $B_{hys} = (B_{OP} – B_{RP})$			20		mT
B_O	Magnetic offset; $B_O = (B_{OP} + B_{RP}) / 2$		–1.5	0	+1.5	mT

(1) 1 mT = 10 Gauss

7.8 Typical Characteristics

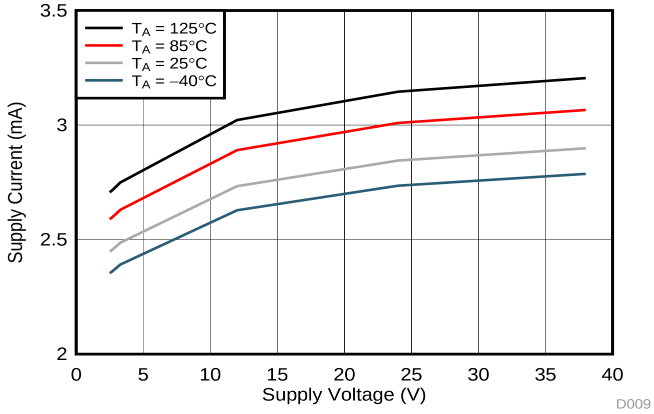


Figure 1. I_{CC} vs V_{CC}

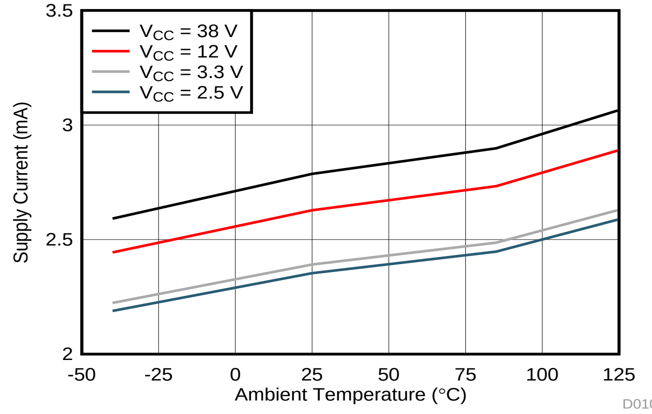
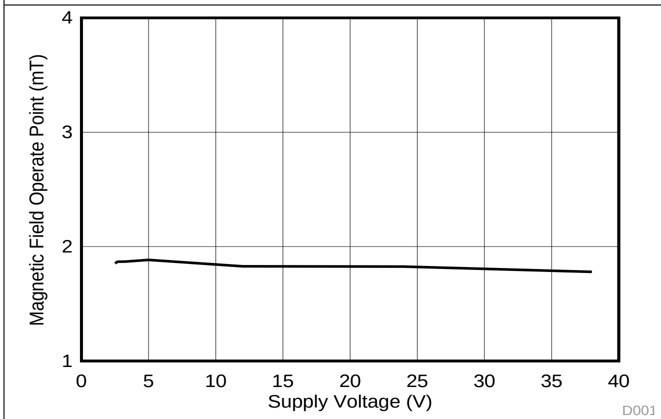
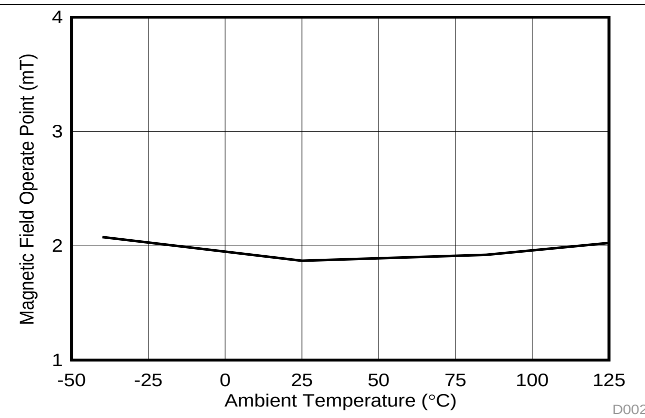


Figure 2. I_{CC} vs Temperature



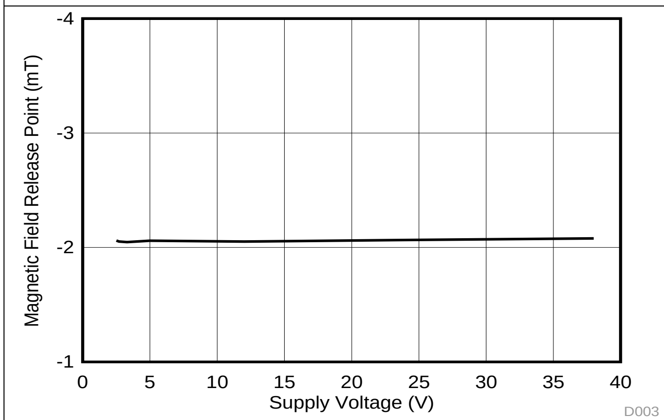
T_A = 25°C

Figure 3. DRV5013AD
B_{OP} vs V_{CC}



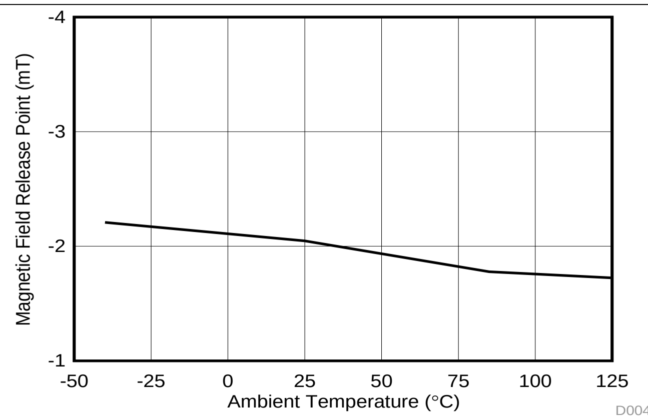
V_{CC} = 3.3 V

Figure 4. DRV5013AD
B_{OP} vs Temperature



T_A = 25°C

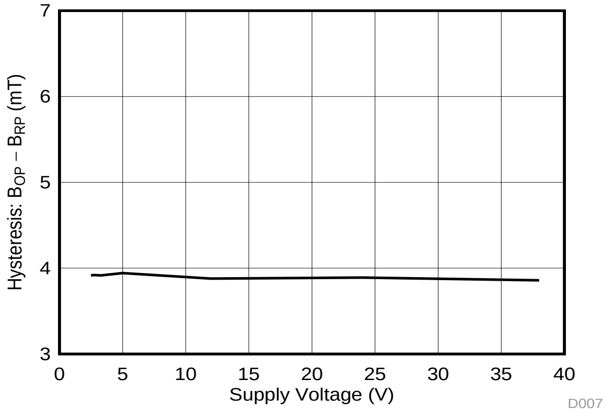
Figure 5. DRV5013AD
B_{RP} vs V_{CC}



V_{CC} = 3.3 V

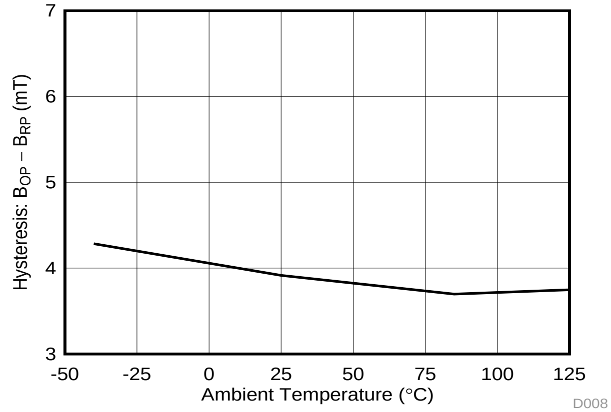
Figure 6. DRV5013AD
B_{RP} vs Temperature

Typical Characteristics (continued)



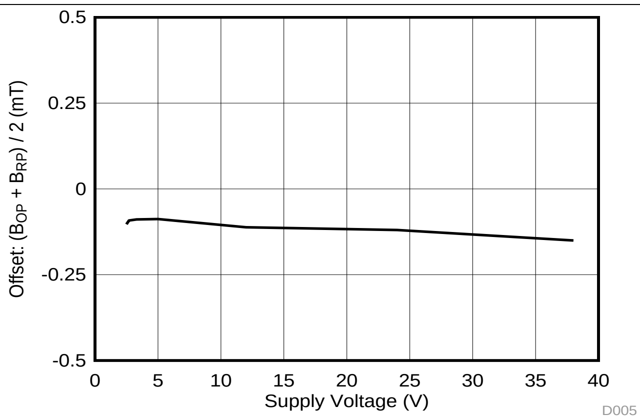
T_A = 25°C

Figure 7. Hysteresis vs V_{CC}



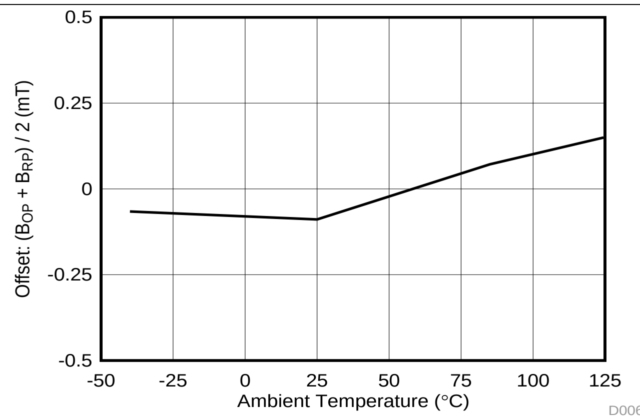
V_{CC} = 3.3 V

Figure 8. Hysteresis vs Temperature



T_A = 25°C

Figure 9. DRV5013AD Offset vs V_{CC}



V_{CC} = 3.3 V

Figure 10. DRV5013AD Offset vs Temperature

8 Detailed Description

8.1 Overview

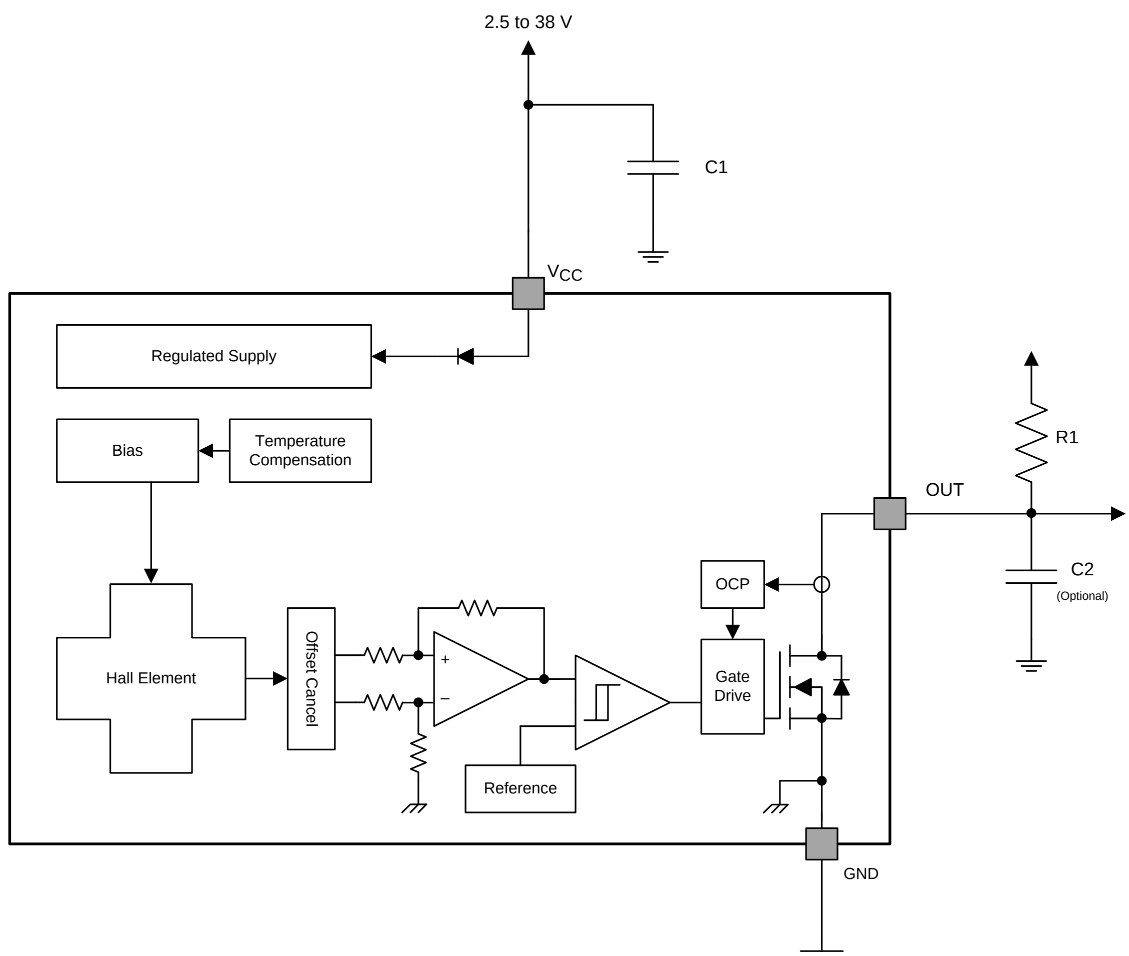
The DRV5013 device is a chopper-stabilized Hall sensor with a digital latched output for magnetic sensing applications. The DRV5013 device can be powered with a supply voltage between 2.5 and 38 V, and continuously survives continuous –22-V reverse-battery conditions. The DRV5013 device does not operate when –22 to 2.4 V is applied to the V_{CC} terminal (with respect to the GND terminal). In addition, the device can withstand voltages up to 40 V for transient durations.

The field polarity is defined as follows: a south pole near the marked side of the package is a positive magnetic field. A north pole near the marked side of the package is a negative magnetic field.

The output state is dependent on the magnetic field perpendicular to the package. A south pole near the marked side of the package causes the output to pull low (operate point, B_{OP}), and a north pole near the marked side of the package causes the output to release (release point, B_{RP}). Hysteresis is included in between the operate point and the release point therefore magnetic-field noise does not accidentally trip the output.

An external pullup resistor is required on the OUT terminal. The OUT terminal can be pulled up to V_{CC}, or to a different voltage supply. This allows for easier interfacing with controller circuits.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Field Direction Definition

A positive magnetic field is defined as a south pole near the marked side of the package as shown in Figure 11.

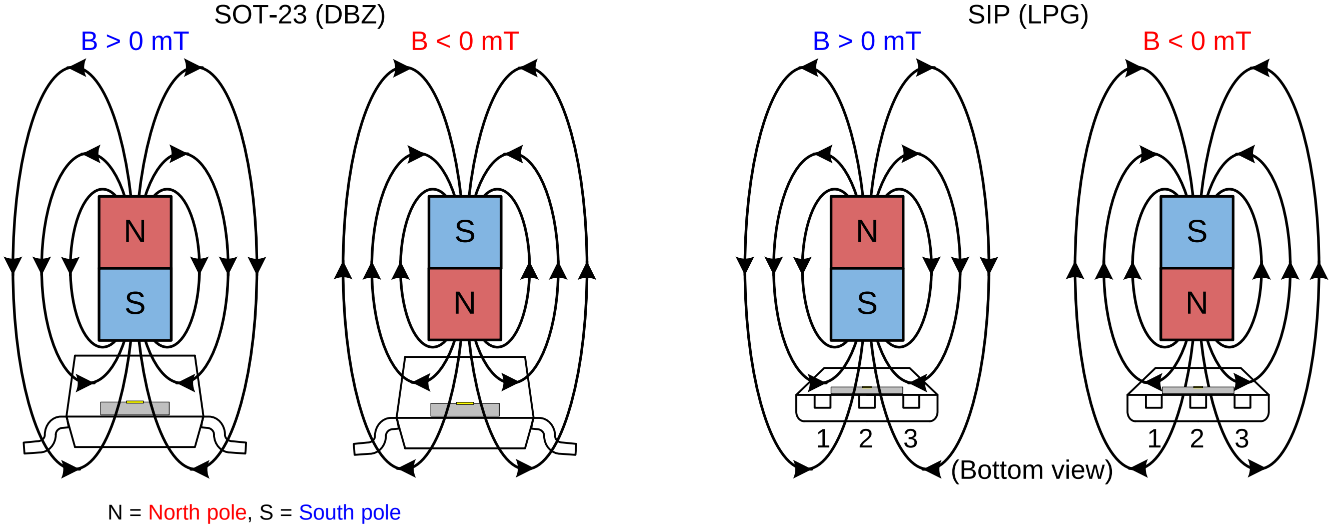


Figure 11. Field Direction Definition

8.3.2 Device Output

If the device is powered on with a magnetic field strength between B_{RP} and B_{OP}, then the device output is indeterminate and can either be Hi-Z or Low. If the field strength is greater than B_{OP}, then the output is pulled low. If the field strength is less than B_{RP}, then the output is released.

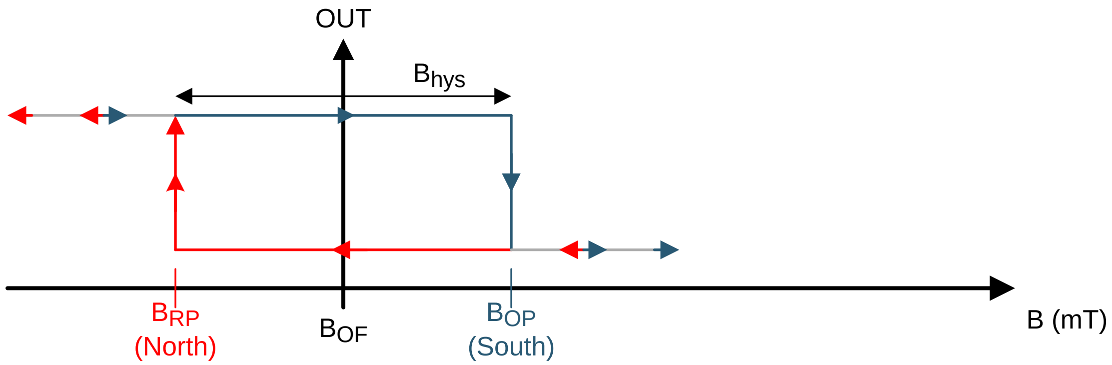


Figure 12. DRV5013—B_{OP} > 0

Feature Description (continued)

8.3.3 Power-On Time

After applying V_{CC} to the DRV5013 device, t_{on} must elapse before the OUT terminal is valid. During the power-up sequence, the output is Hi-Z. A pulse as shown in Figure 13 and Figure 14 occurs at the end of t_{on}. This pulse can allow the host processor to determine when the DRV5013 output is valid after startup. In Case 1 (Figure 13) and Case 2 (Figure 14), the output is defined assuming a constant magnetic field $B > B_{OP}$ and $B < B_{RP}$.

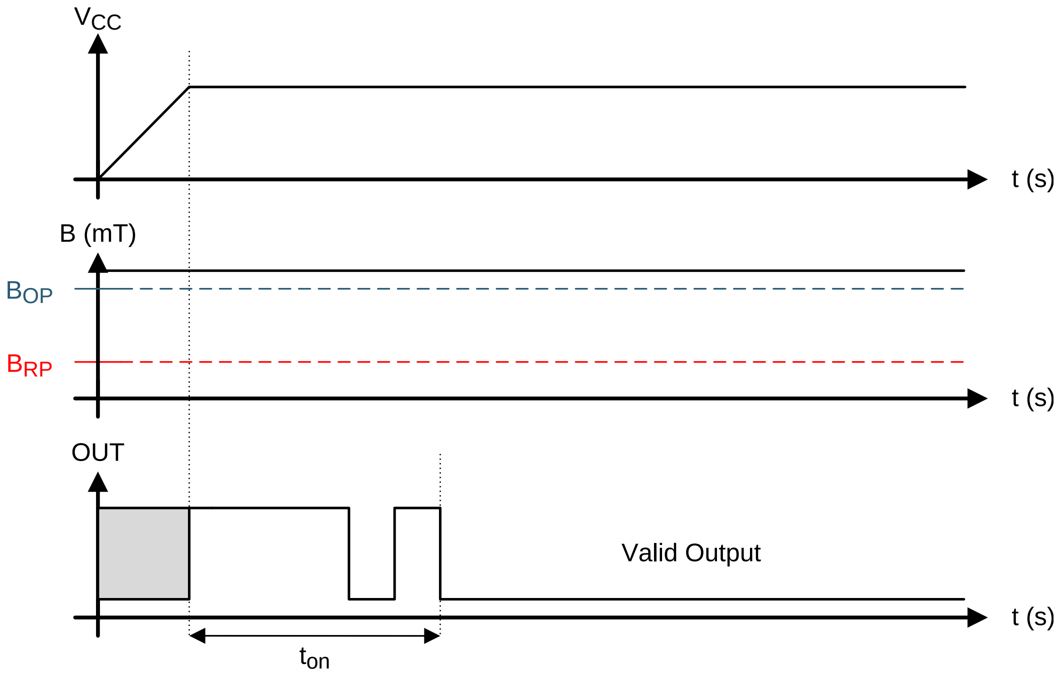


Figure 13. Case 1: Power On When $B > B_{OP}$

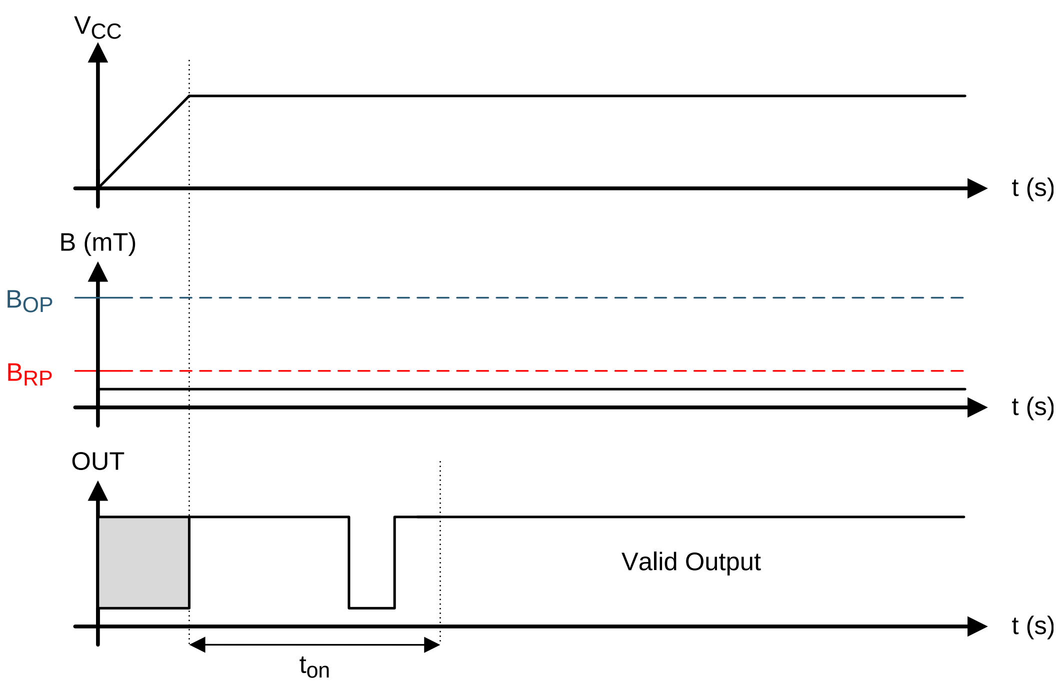


Figure 14. Case 2: Power On When $B < B_{RP}$

Feature Description (continued)

If the device is powered on with the magnetic field strength $B_{RP} < B < B_{OP}$, then the device output is indeterminate and can either be Hi-Z or pulled low. During the power-up sequence, the output is held Hi-Z until t_{on} has elapsed. At the end of t_{on}, a pulse is given on the OUT terminal to indicate that t_{on} has elapsed. After t_{on}, if the magnetic field changes such that $B_{OP} < B$, the output is released. Case 3 (Figure 15) and Case 4 (Figure 16) show examples of this behavior.

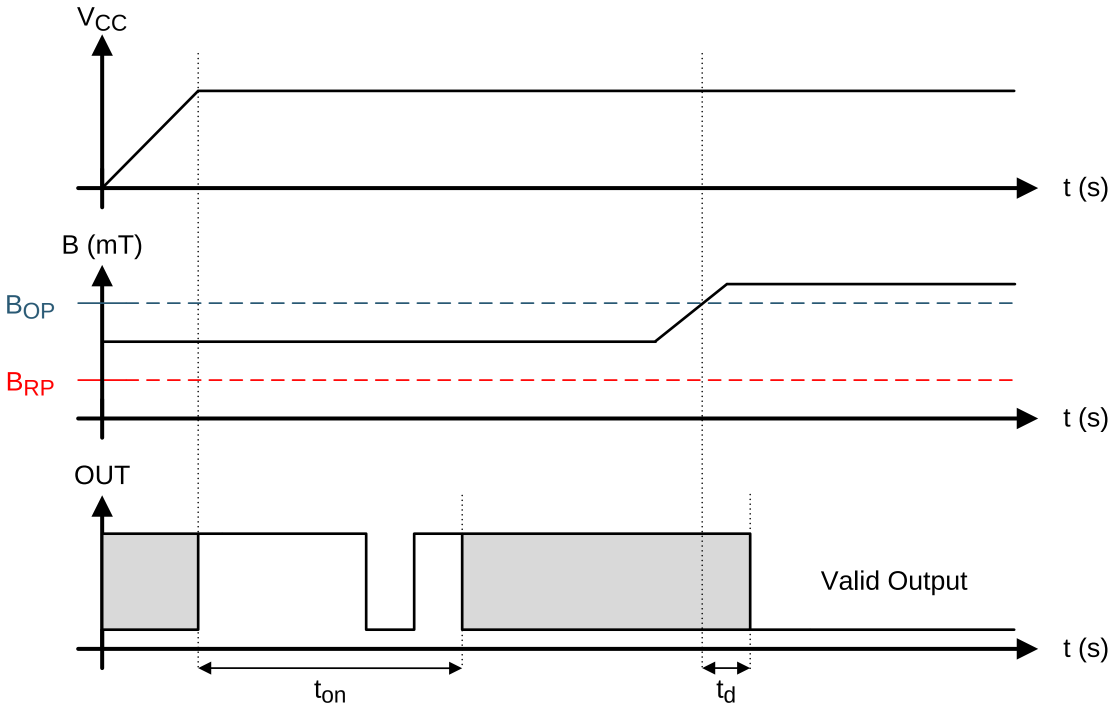


Figure 15. Case 3: Power On When $B_{RP} < B < B_{OP}$, Followed by $B > B_{OP}$

Feature Description (continued)

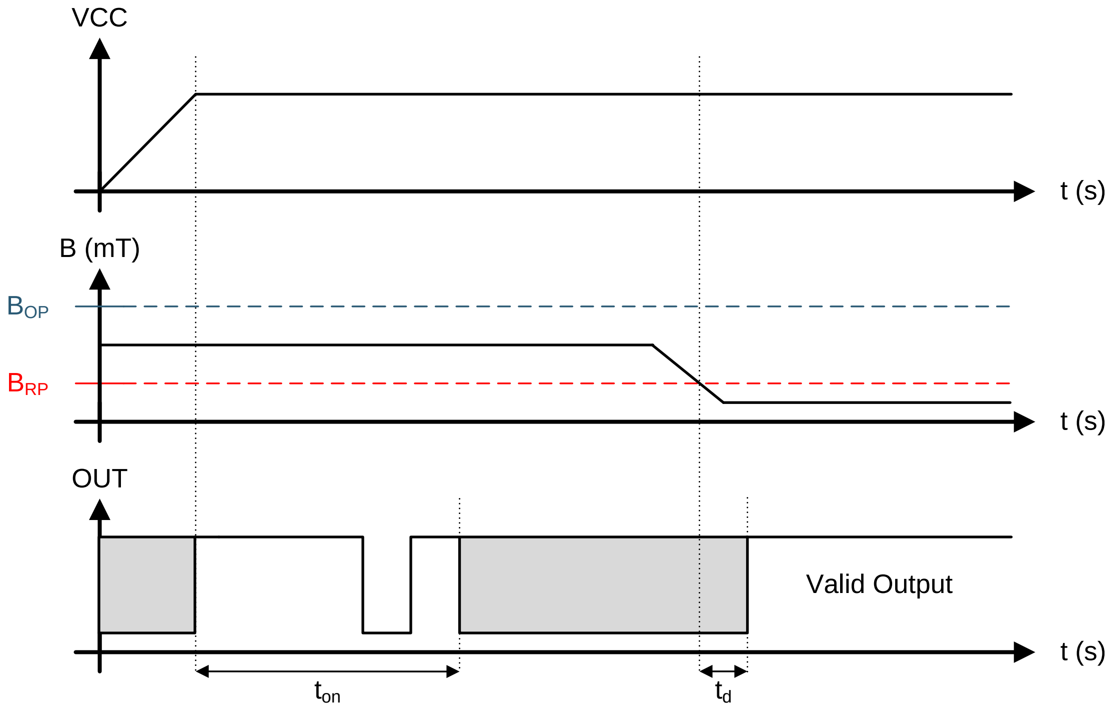


Figure 16. Case 4: Power On When $B_{RP} < B < B_{OP}$, Followed by $B < B_{RP}$

8.3.4 Output Stage

The DRV5013 output stage uses an open-drain NMOS, and it is rated to sink up to 30 mA of current. For proper operation, calculate the value of the pullup resistor R1 using Equation 1.

$$\frac{V_{ref}\ \text{max}}{30\ \text{mA}} \leq R1 \leq \frac{V_{ref}\ \text{min}}{100\ \mu\text{A}} \quad (1)$$

The size of R1 is a tradeoff between the OUT rise time and the current when OUT is pulled low. A lower current is generally better, however faster transitions and bandwidth require a smaller resistor for faster switching.

In addition, ensure that the value of R1 > 500 Ω to ensure the output driver can pull the OUT terminal close to GND.

NOTE

V_{ref} is not restricted to V_{CC}. The allowable voltage range of this terminal is specified in the *Absolute Maximum Ratings* section.

Feature Description (continued)

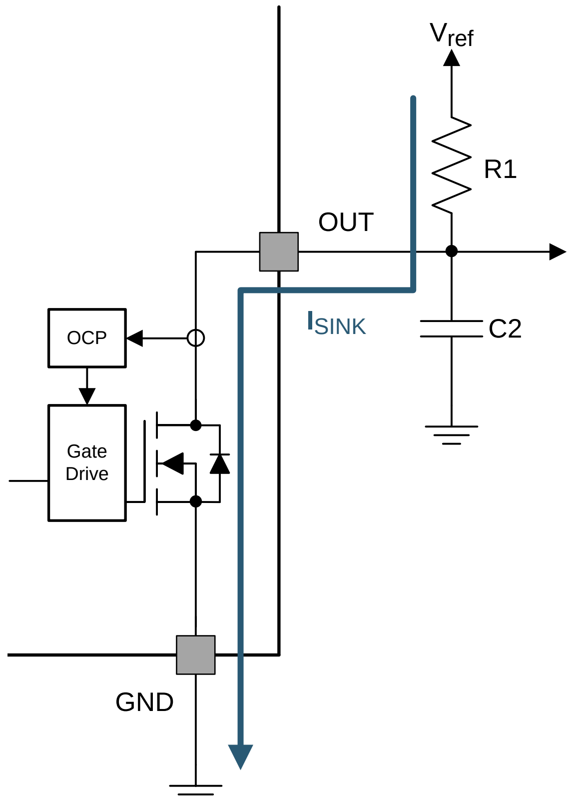


Figure 17.

Select a value for C2 based on the system bandwidth specifications as shown in Equation 2.

$$2 \times f_{BW}\ (\text{Hz}) < \frac{1}{2\pi \times R1 \times C2} \quad (2)$$

Most applications do not require this C2 filtering capacitor.

Feature Description (continued)

8.3.5 Protection Circuits

The DRV5013 device is fully protected against overcurrent and reverse-supply conditions.

8.3.6 Overcurrent Protection (OCP)

An analog current-limit circuit limits the current through the FET. The driver current is clamped to I_{OCP}. During this clamping, the $r_{DS(on)}$ of the output FET is increased from the nominal value.

8.3.7 Load Dump Protection

The DRV5013 device operates at DC V_{CC} conditions up to 38 V nominally, and can additionally withstand V_{CC} = 40 V. No current-limiting series resistor is required for this protection.

8.3.8 Reverse Supply Protection

The DRV5013 device is protected in the event that the V_{CC} terminal and the GND terminal are reversed (up to –22 V).

NOTE

In a reverse supply condition, the OUT terminal reverse-current must not exceed the ratings specified in the *Absolute Maximum Ratings* section.

FAULT	CONDITION	DEVICE	DESCRIPTION	RECOVERY
FET overload (OCP)	$I_{SINK} \geq I_{OCP}$	Operating	Output current is clamped to I_{OCP}	$I_O < I_{OCP}$
Load Dump	38 V < V_{CC} < 40 V	Operating	Device will operate for a transient duration	$V_{CC} \leq$ 38 V
Reverse Supply	–22 V < V_{CC} < 0 V	Disabled	Device will survive this condition	$V_{CC} \geq$ 2.5 V

8.4 Device Functional Modes

The DRV5013 device is active only when V_{CC} is between 2.5 and 38 V.

When a reverse supply condition exists, the device is inactive.

9 Application and Implementation

9.1 Application Information

The DRV5013 device is used in magnetic-field sensing applications.

9.2 Typical Application

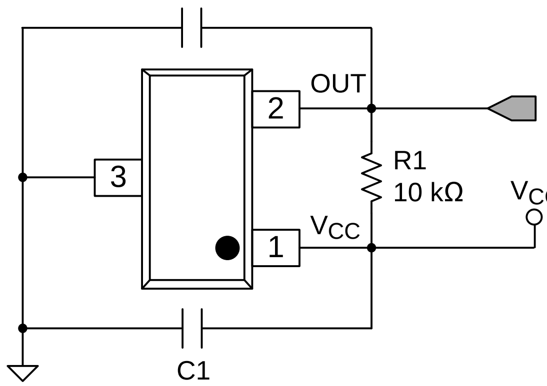


Figure 18. Typical Application Circuit

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{CC}	3.2 to 3.4 V
System bandwidth	f_{BW}	10 kHz

9.2.2 Detailed Design Procedure

Table 2. External Components

COMPONENT	TERMINAL 1	TERMINAL 2	RECOMMENDED
C1	V_{CC}	GND	A 0.01-µF (minimum) ceramic capacitor rated for V_{CC}
C2	OUT	GND	**Optional**: Place a ceramic capacitor to GND
R1	OUT	REF(1)	Requires a resistor pullup

(1) REF is not a terminal on the DRV5013 device, but a REF supply-voltage pullup is required for the OUT terminal; the OUT terminal may be pulled up to V_{CC}.

9.2.2.1 Configuration Example

In a 3.3-V system, 3.2 V ≤ V_{ref} ≤ 3.4 V. Use Equation 3 to calculate the allowable range for R1.

$$\frac{V_{ref}\ \text{max}}{30\ \text{mA}} \leq \text{R1} \leq \frac{V_{ref}\ \text{min}}{100\ \mu\text{A}} \quad (3)$$

For this design example, use Equation 4 to calculate the allowable range of R1.

$$\frac{3.4\ \text{V}}{30\ \text{mA}} \leq \text{R1} \leq \frac{3.2\ \text{V}}{30\ \text{mA}} \quad (4)$$

Therefore:

$$113\ \Omega \leq \text{R1} \leq 32\ \text{k}\Omega \quad (5)$$

After finding the allowable range of R1 (Equation 5), select a value between 500 Ω and 32 kΩ for R1.

Assuming a system bandwidth of 10 kHz, use Equation 6 to calculate the value of C2.

$$2 \times f_{BW}\ (\text{Hz}) < \frac{1}{2\pi \times \text{R1} \times \text{C2}} \quad (6)$$

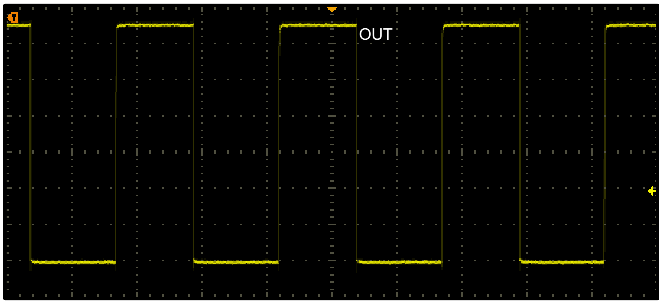
For this design example, use Equation 7 to calculate the value of C2.

$$2 \times 10\ \text{kHz} < \frac{1}{2\pi \times \text{R1} \times \text{C2}} \quad (7)$$

An R1 value of 10 kΩ and a C2 value less than 820 pF satisfy the requirement for a 10-kHz system bandwidth.

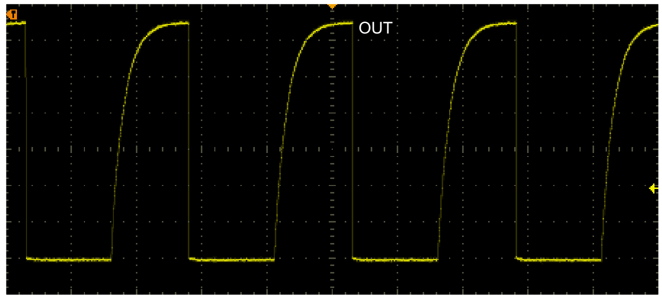
A selection of R1 = 10 kΩ and C2 = 680 pF would cause a low-pass filter with a corner frequency of 23.4 kHz.

9.2.3 Application Curves



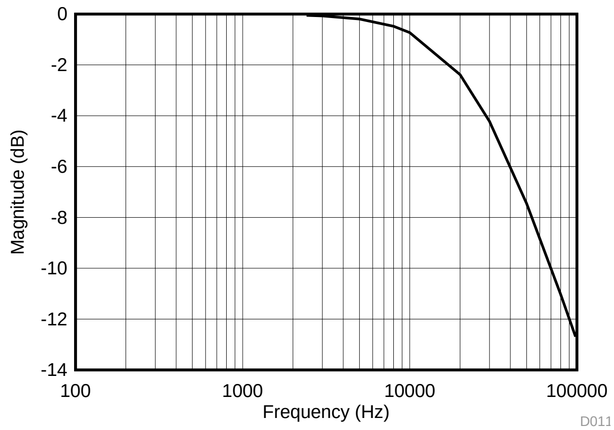
R1 = 10 kΩ pull-up   No C2

Figure 19. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pull-up   C2 = 680 pF

Figure 20. 10-kHz Switching Magnetic Field



R1 = 10-kΩ pull-up   C2 = 680 pF

Figure 21. Low-Pass Filtering

10 Power Supply Recommendations

The DRV5013 device is designed to operate from an input voltage supply (VM) range between 2.5 V and 38 V. A 0.01-µF (minimum) ceramic capacitor rated for V_{CC} must be placed as close to the DRV5013 device as possible.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

Figure 22 shows a legend for reading the complete device name for and DRV5013 device.

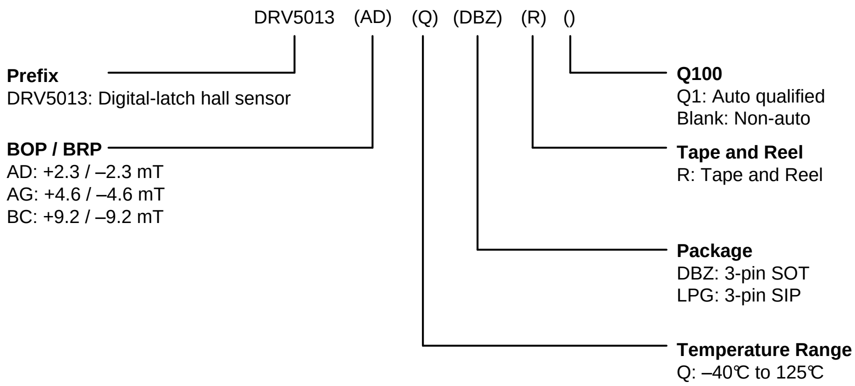
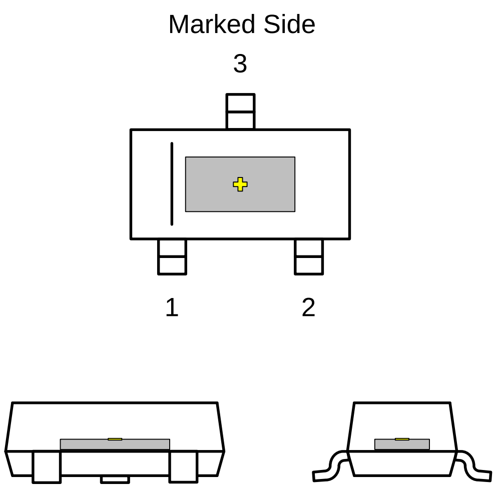


Figure 22. Device Nomenclature

11.1.2 Device Markings



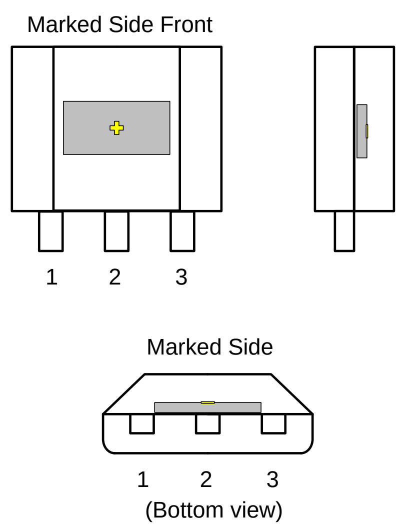


Figure 23. SOT-23 (DBZ) Package

Figure 24. SIP (LPG) Package

indicates the Hall Effect Sensor (not to scale). Located in the center of the package.

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5013ADQDBZR	ACTIVE	SOT-23	DBZ	3	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	+NLAD	Samples
DRV5013ADQLPG	PREVIEW	TO-92	LPG	3	1000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	-40 to 125	+NLAD	
DRV5013AGQDBZR	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		
DRV5013AGQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		
DRV5013BCQDBZR	PREVIEW	SOT-23	DBZ	3	3000	TBD	Call TI	Call TI	-40 to 125		
DRV5013BCQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		
PDRV5013ADQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		
PDRV5013AGQDBZT	PREVIEW	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 125		
PDRV5013AGQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		
PDRV5013BCQDBZT	PREVIEW	SOT-23	DBZ	3	250	TBD	Call TI	Call TI	-40 to 125		
PDRV5013BCQLPG	PREVIEW	TO-92	LPG	3	2000	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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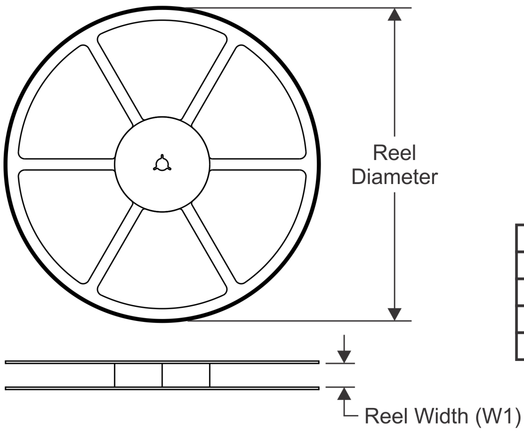
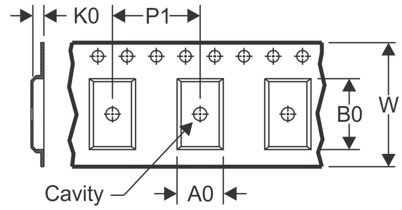
TAPE AND REEL INFORMATION

REEL DIMENSIONS

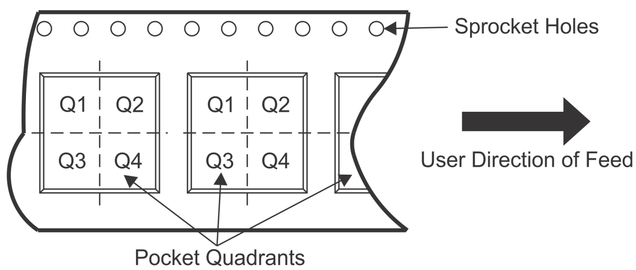


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

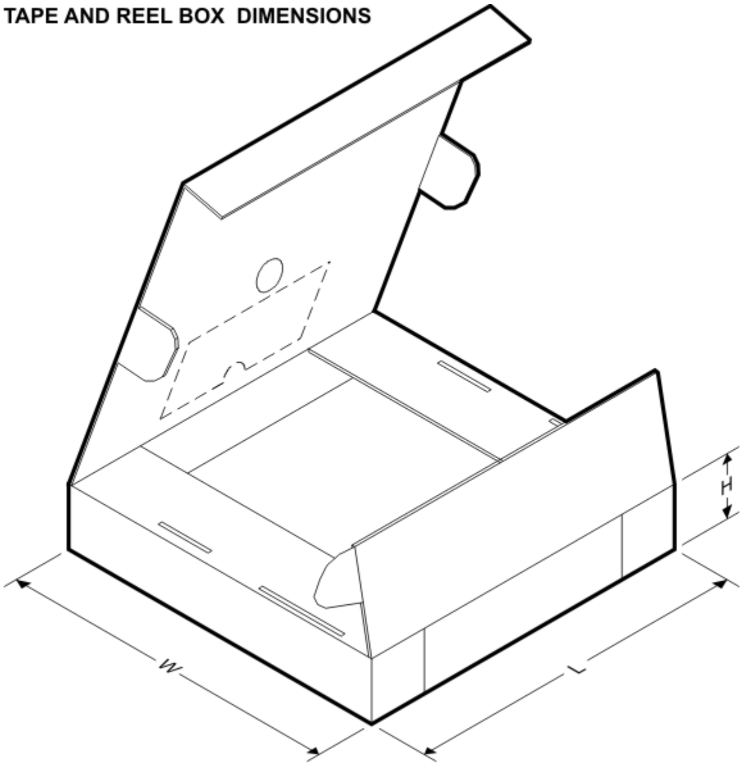
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

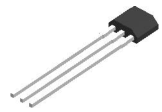
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5013ADQDBZR	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5013ADQDBZR	SOT-23	DBZ	3	3000	202.0	201.0	28.0

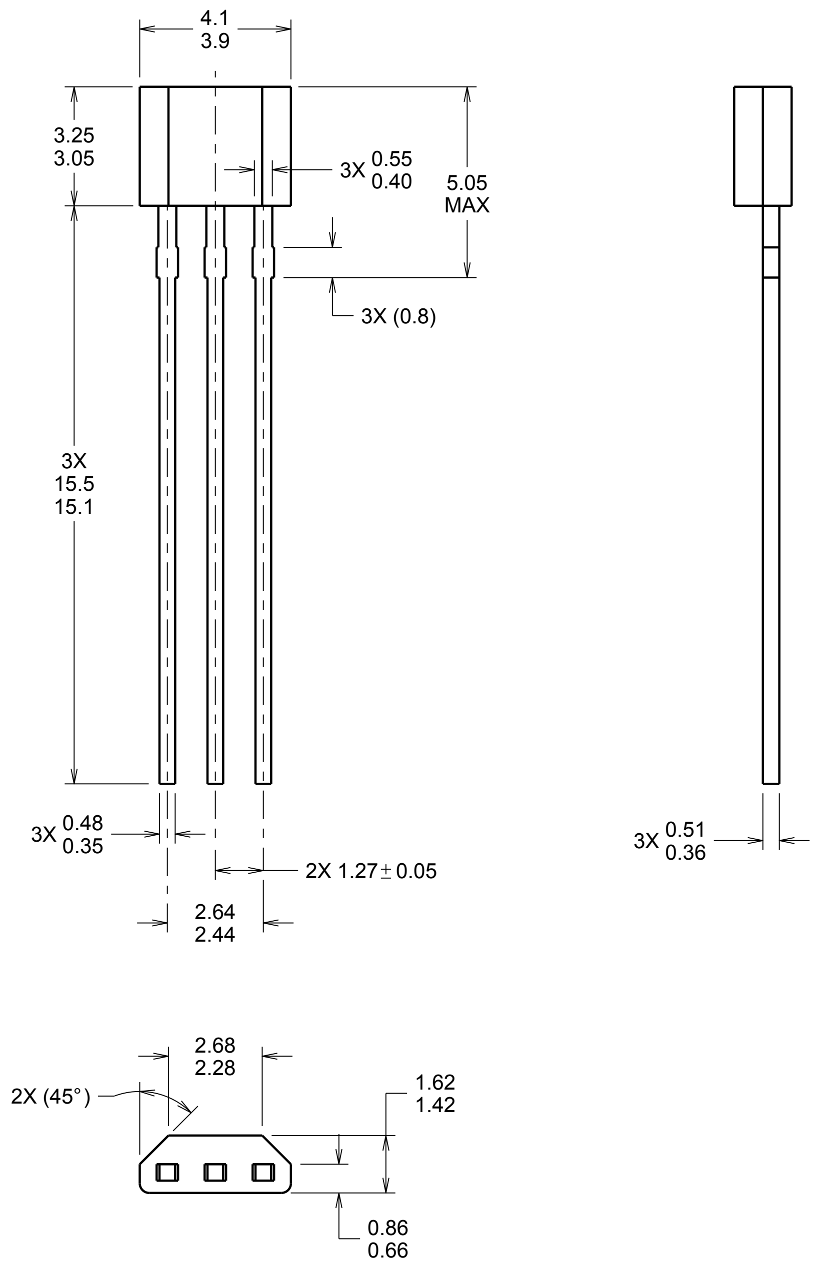


PACKAGE OUTLINE

LPG0003A

TO-92 - 5.05 mm max height

TO-92

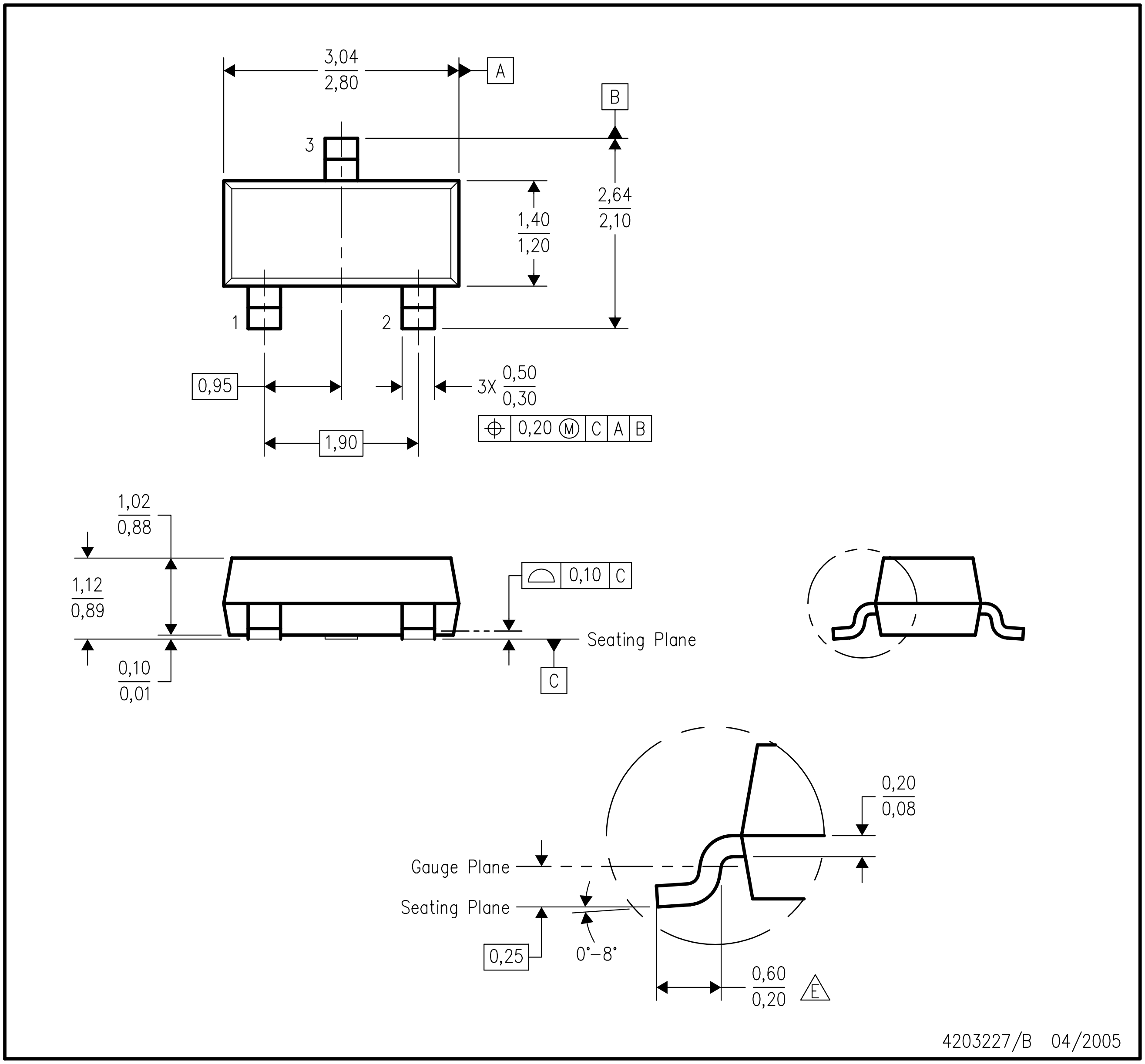


4221343/A 02/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

DBZ (R-PDSO-G3) PLASTIC SMALL-OUTLINE



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Lead dimensions are inclusive of plating.
- D. Body dimensions are exclusive of mold flash and protrusion. Mold flash and protrusion not to exceed 0.25 per side.
- E. Falls within JEDEC TO–236 variation AB, except minimum foot length.

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