KSZ8041TL-FTL Eval Board Revision 1.0

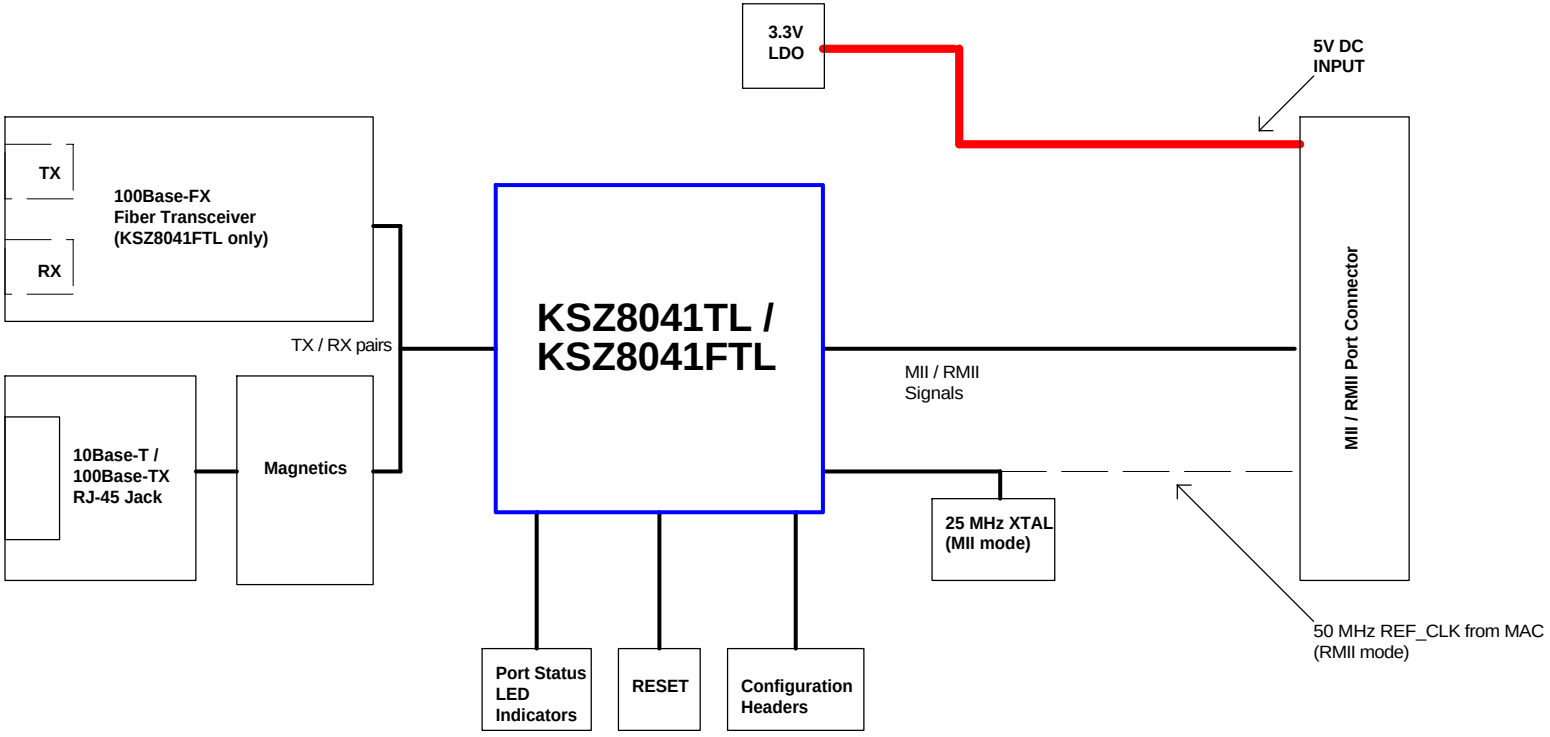
REVISION HISTORY

DATE	DESCRIPTION	REVISION
1/4/07	Initial Release	1.0
4/27/07	Added 100pF capacitor (C54) on REXT (pin 16) of KSZ8041TL/FTL.	1.1

Table of Contents

Title: KSZ8041TL-FTL Eval Board		
Size	Document Number: Revision History	Rev: 1.1
Date: Friday, April 27, 2007	Sheet 1 of 5	

KSZ8041TL_FTL EVAL BOARD - BLOCK DIAGRAM



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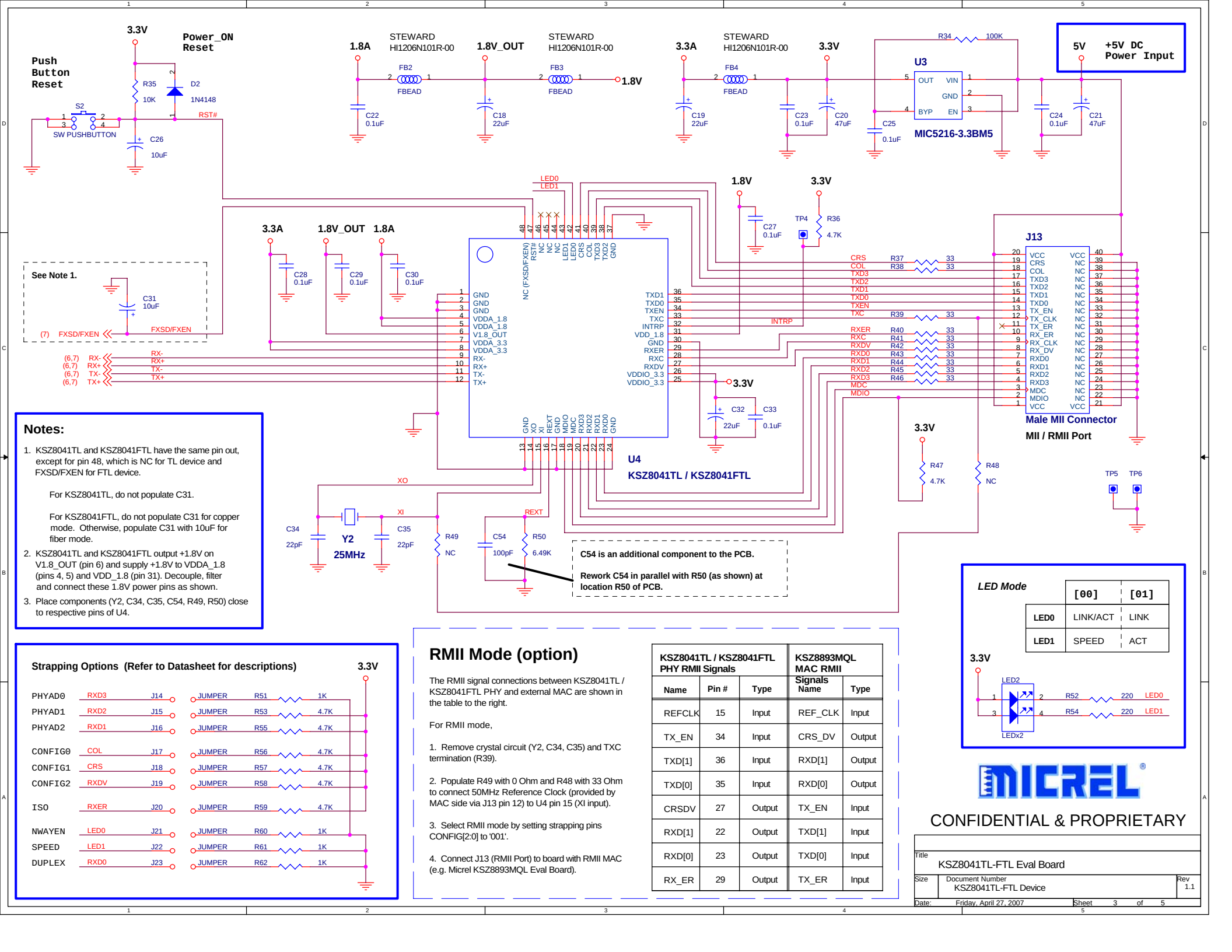
Title: KSZ8041TL-FTL Eval Board		
Size	Document Number: KSZ8041TL-FTL Board -- Block Diagram	Rev: 1.1
Date: Friday, April 27, 2007	Sheet 2 of 5	



Notes:

1. KSZ8041TL and KSZ8041FTL have the same pin out, except for pin 48, which is NC for TL device and FXSD/FXEN for FTL device.

   For KSZ8041TL, do not populate C31.

   For KSZ8041FTL, do not populate C31 for copper mode. Otherwise, populate C31 with 10uF for fiber mode.
2. KSZ8041TL and KSZ8041FTL output +1.8V on V1.8_OUT (pin 6) and supply +1.8V to VDDA_1.8 (pins 4, 5) and VDD_1.8 (pin 31). Decouple, filter and connect these 1.8V power pins as shown.
3. Place components (Y2, C34, C35, C54, R49, R50) close to respective pins of U4.

Strapping Options (Refer to Datasheet for descriptions)

PHYAD0	RXD3	J14	JUMPER	R51	1K	
PHYAD1	RXD2	J15	JUMPER	R53	4.7K	
PHYAD2	RXD1	J16	JUMPER	R55	4.7K	
CONFIG0	COL	J17	JUMPER	R56	4.7K	
CONFIG1	CRS	J18	JUMPER	R57	4.7K	
CONFIG2	RXDV	J19	JUMPER	R58	4.7K	
ISO	RXER	J20	JUMPER	R59	4.7K	
NWAYEN	LED0	J21	JUMPER	R60	1K	
SPEED	LED1	J22	JUMPER	R61	1K	
DUPLEX	RXD0	J23	JUMPER	R62	1K	

RMII Mode (option)

The RMII signal connections between KSZ8041TL / KSZ8041FTL PHY and external MAC are shown in the table to the right.

For RMII mode,

1. Remove crystal circuit (Y2, C34, C35) and TXC termination (R39).
2. Populate R49 with 0 Ohm and R48 with 33 Ohm to connect 50MHz Reference Clock (provided by MAC side via J13 pin 12) to U4 pin 15 (XI input).
3. Select RMII mode by setting strapping pins CONFIG[2:0] to '001'.
4. Connect J13 (RMII Port) to board with RMII MAC (e.g. Micrel KSZ8893MQL Eval Board).

KSZ8041TL / KSZ8041FTL PHY RMII Signals			KSZ8893MQL MAC RMII Signals	
Name	Pin #	Type	Name	Type
REFCLK	15	Input	REF_CLK	Input
TX_EN	34	Input	CRS_DV	Output
TXD[1]	36	Input	RXD[1]	Output
TXD[0]	35	Input	RXD[0]	Output
CRSDV	27	Output	TX_EN	Input
RXD[1]	22	Output	TXD[1]	Input
RXD[0]	23	Output	TXD[0]	Input
RX_ER	29	Output	TX_ER	Input

LED Mode

	[00]	[01]
LED0	LINK/ACT	LINK
LED1	SPEED	ACT

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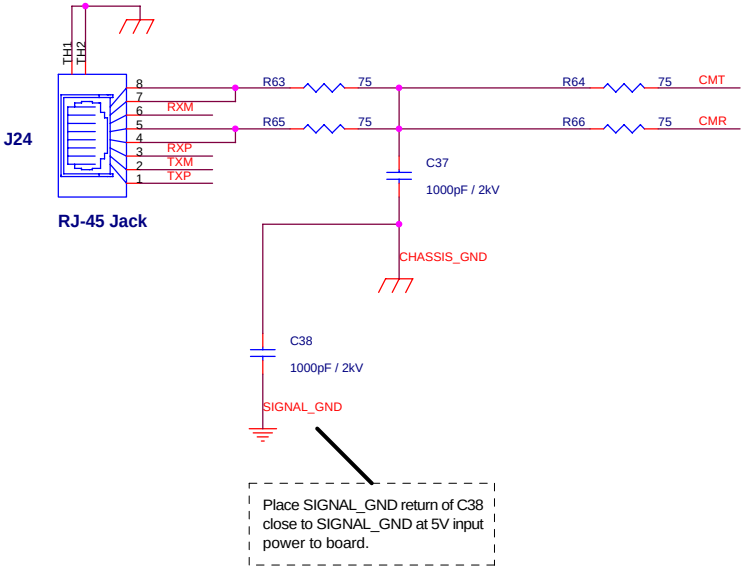
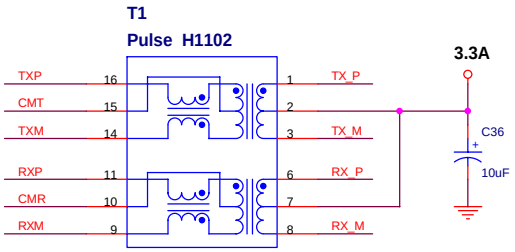
Title: KSZ8041TL-FTL Eval Board		
Size	Document Number: KSZ8041TL-FTL Device	Rev: 1.1
Date: Friday, April 27, 2007	Sheet 3 of 5	

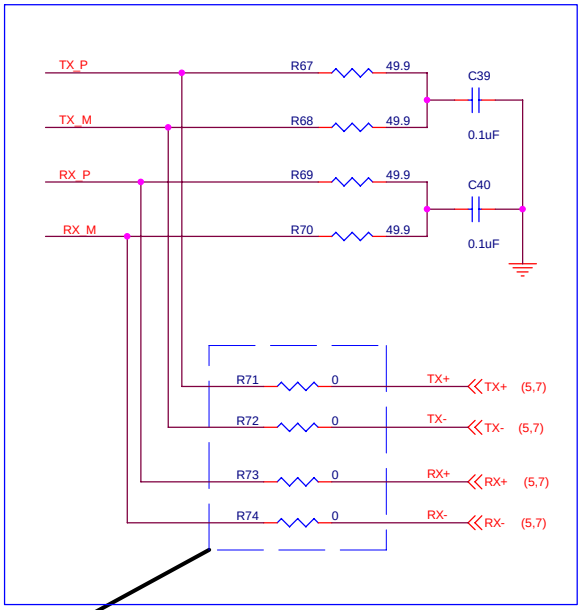


Place SIGNAL_GND return of C38 close to SIGNAL_GND at 5V input power to board.



Place components in box below close to KSZ8041

Route both traces of each differential pair as identical to each other as possible at 6mil width/6mil parallel spacing, and at least 18 mils away from all other signals

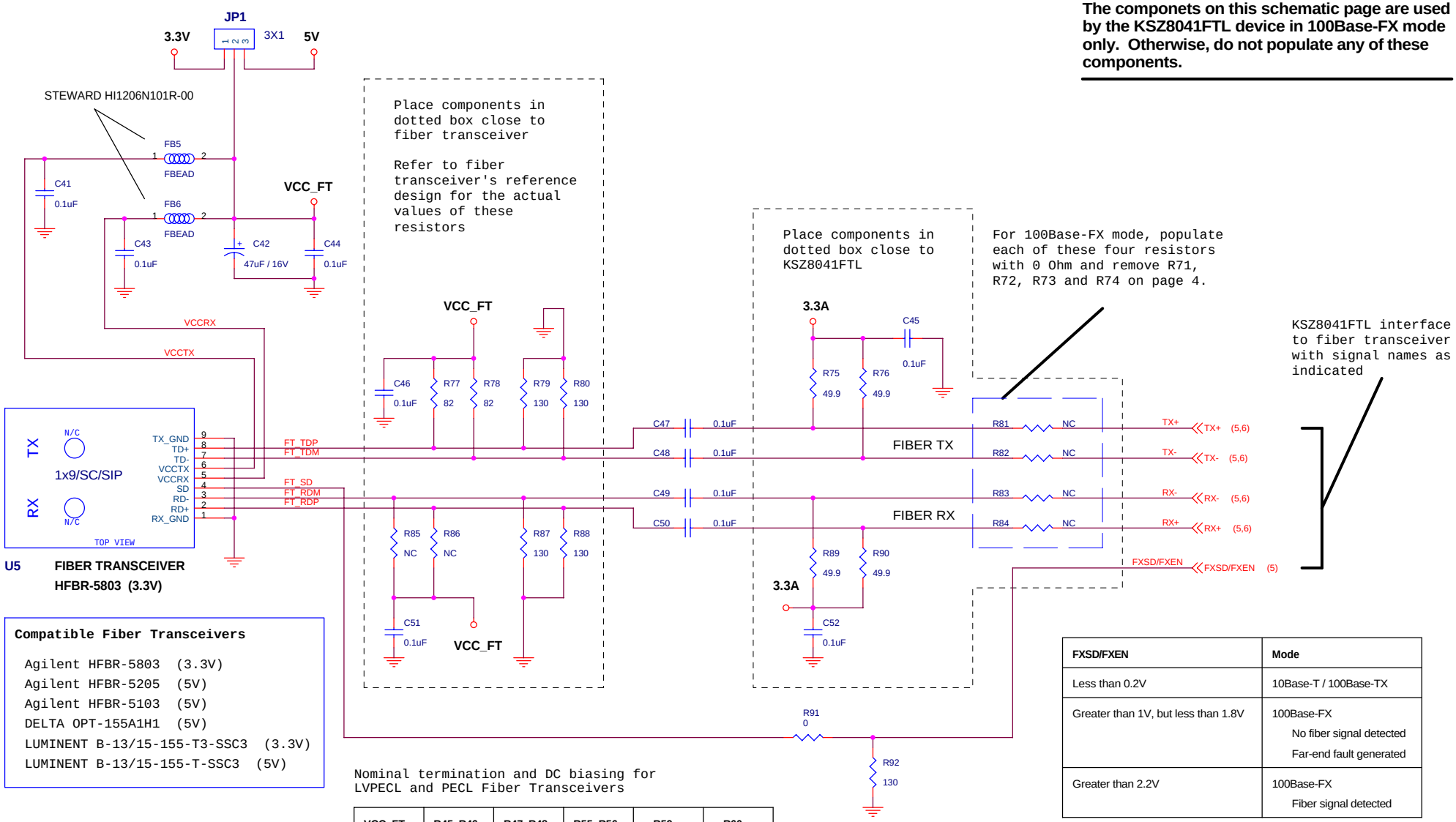


For 10Base-T and 100Base-TX modes, populate each of these four resistors with 0 Ohm and remove R81, R82, R83 and R84 on page 5.

CONFIDENTIAL & PROPRIETARY

Title: KSZ8041TL-FTL Eval Board		
Size	Document Number: KSZ8041TL-FTL UTP Interface	Rev: 1.1
Date: Friday, April 27, 2007	Sheet 4 of 5	

The componets on this schematic page are used by the KSZ8041FTL device in 100Base-FX mode only. Otherwise, do not populate any of these components.



Compatible Fiber Transceivers

Agilent HFBR-5803 (3.3V)
Agilent HFBR-5205 (5V)
Agilent HFBR-5103 (5V)
DELTA OPT-155A1H1 (5V)
LUMINENT B-13/15-155-T3-SSC3 (3.3V)
LUMINENT B-13/15-155-T-SSC3 (5V)

Nominal termination and DC biasing for LVPECL and PECL Fiber Transceivers

VCC_FT	R45, R46	R47, R48	R55, R56	R59	R60
+3.3V	82 Ohms	130 Ohms	130 Ohms	0 Ohm	130 Ohms
+5V	68 Ohms	191 Ohms	270 Ohms	4.75K 1%	5.62K 1%

FXSD/FXEN	Mode
Less than 0.2V	10Base-T / 100Base-TX
Greater than 1V, but less than 1.8V	100Base-FX No fiber signal detected Far-end fault generated
Greater than 2.2V	100Base-FX Fiber signal detected

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Title: KSZ8041TL-FTL Eval Board		
Size	Document Number: KSZ8041FTL Fiber Interface	Rev: 1.1
Date: Friday, April 27, 2007	Sheet 5 of 5	