# KSZ8041 rev_A3 Errata Sheet

## Single-Port Fast Ethernet PHY

The following erratum affects silicon revision A3 of the following products:

KSZ8041NL, KSZ8041TL, KSZ8041FTL

| Item # | Erratum (description of problem) | Solution / Workaround |
|---|---|---|
| 1 | In Digital Loop-back mode (register 0x0h bit 14 = 1) for 10Base-T full-duplex, the first loop-back packet sometimes has FCS error if clock and data are initially not synchronized.<br><br>This problem does not occur in normal PHY mode and in Digital Loop-back mode for 100Base-TX full-duplex. | Use PCS Loop-back by setting:<br>▪ Strapping pins CONFIG[2:0] to '100'.<br>▪ Register 0x1Fh bit 11 to '1' for Force Link.<br><br>or<br><br>Use RJ-45 Loop-back by shorting TX+/- pins to RX+/- pins, respectively, at the RJ-45 connector. |

For any questions about this errata and sample request, please contact your Micrel FAE or local Sales Representative.