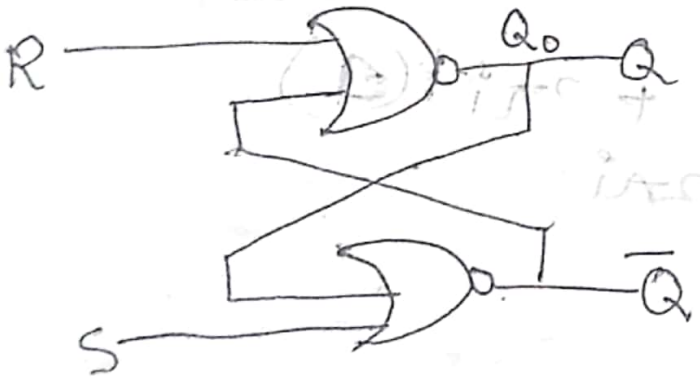
Assignment-02

SR LATCH (1st memory element)

Design: (NOR gate)



Set = ON = 1

Reset = OFF = 0

characterise table:

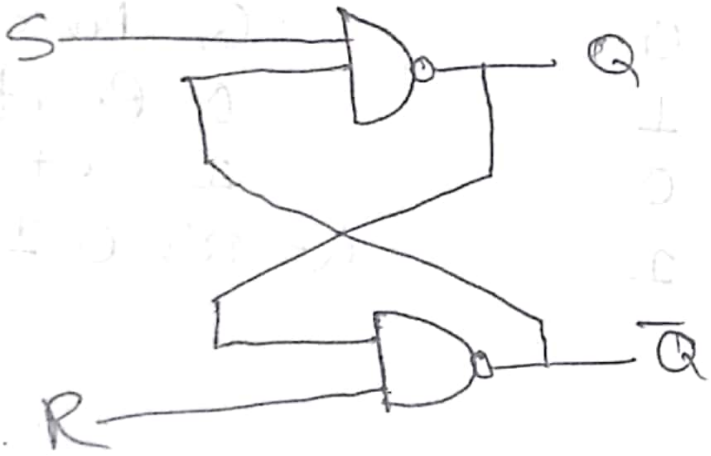
S	R	Q_0	Q	$\bar{Q}$	
0	0	0	0	0	$Q=Q_0$
0	0	1	1	1	
0	1	0	0	1	$Q=0$
0	1	1	0	1	
1	0	0	1	0	$Q=1$
1	0	1	1	0	
1	1	0	0	0	$Q=\bar{Q}$
1	1	1	0	0	

Truth table:

S	R	Q
0	0	Q_0 No change
0	1	0 Reset
1	0	1 Set
1	1	$Q = Q' = 0$ Invalid

SR Latch (NAND Gate)

Design:-



Characterise table:-

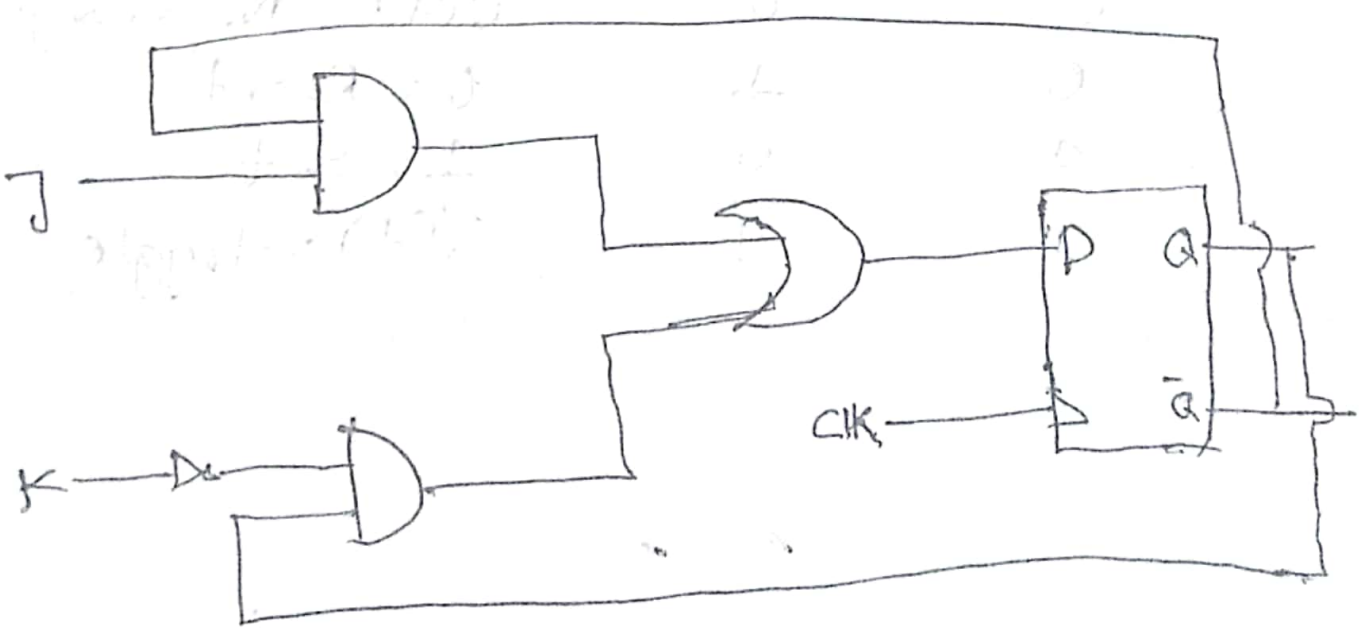
S	R	Q_0	Q	$\bar{Q}$	
0	0	0	1	1	
0	0	1	1	1	= Q = Q_0
0	1	0	1	0	
0	1	1	1	0	= Q = 1
1	0	0	0	1	
1	0	1	0	1	Q = 0
1	1	0	0	1	
1	1	1	1	0	Q = Q_0

Truth table:

S	R	Q
0	0	Q = Q' = 1
0	1	1 = Reset
1	0	0 = Set
1	1	Q = Q = No change

Jk Flip Flop:

Design



Block diagram:

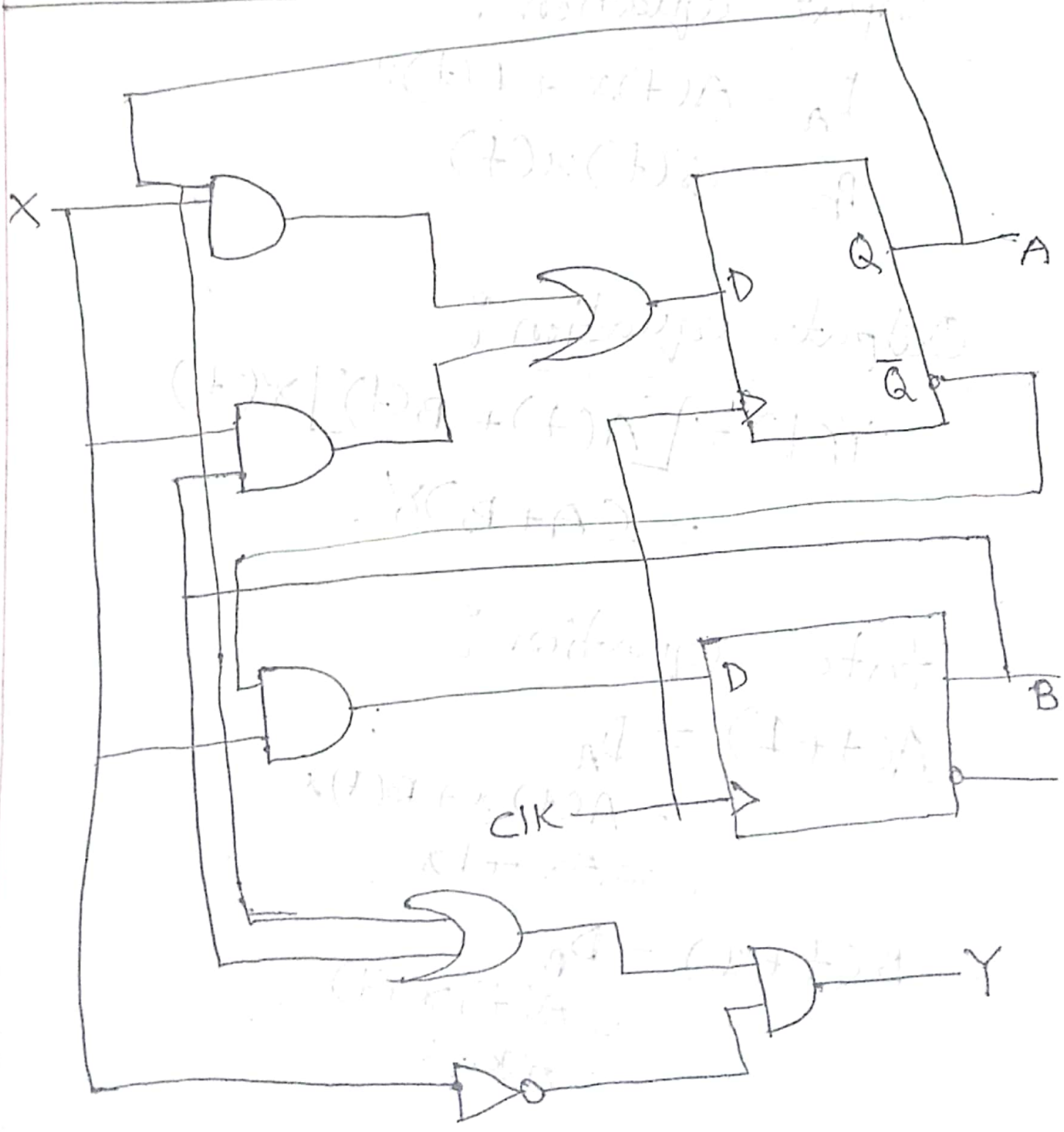
Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Truth table:

J	K	Q(t+1)
0	0	Q(t) = No change
0	1	0 = Reset
1	0	1 = Set
1	1	Q'(t) = toggle

Sequential Circuit

Analysis of clocked Sequential circuit the state



State equation :

Input equation :

$$D_A = A(t)x + B(t)x$$

$$D_B = A'(t)x(t)$$

Output equation :

$$Y(t) = [A(t) + B(t)]X(t)$$

$$= (A+B)X'$$

State equation :

$$A(t+1) = D_A$$

$$= A(t)x + B(t)x$$

$$= Ax + Bx$$

$$B(t+1) = D_B$$

$$= A'(t)x(t)$$

$$= A'x.$$

State Transition table

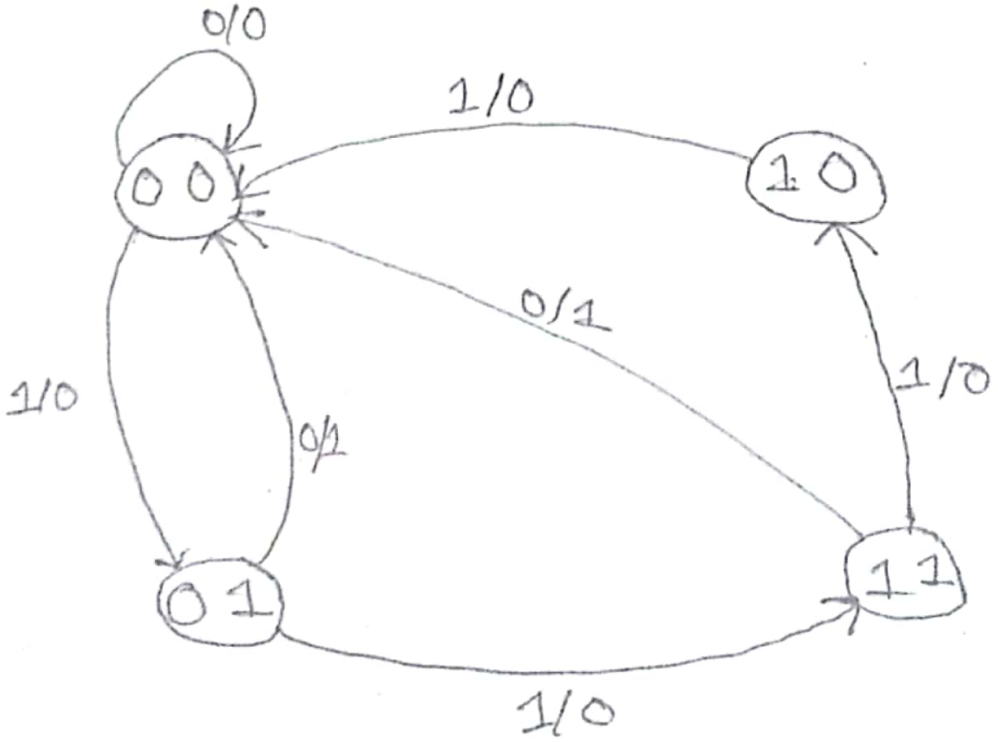
Present state		Input	Next state		Output
A(T)	B(T)	X	A(t+1)	B(t+1)	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

19202103390

P-9

Present State		Next State				Output	
		x=0		x=1			
A	B	A	B	A	B	x=0	x=1
0	0	0	0	0	1	0	0
0	1	0	0	1	1	1	0
1	0	0	0	1	0	1	0
1	1	0	0	1	0	1	0

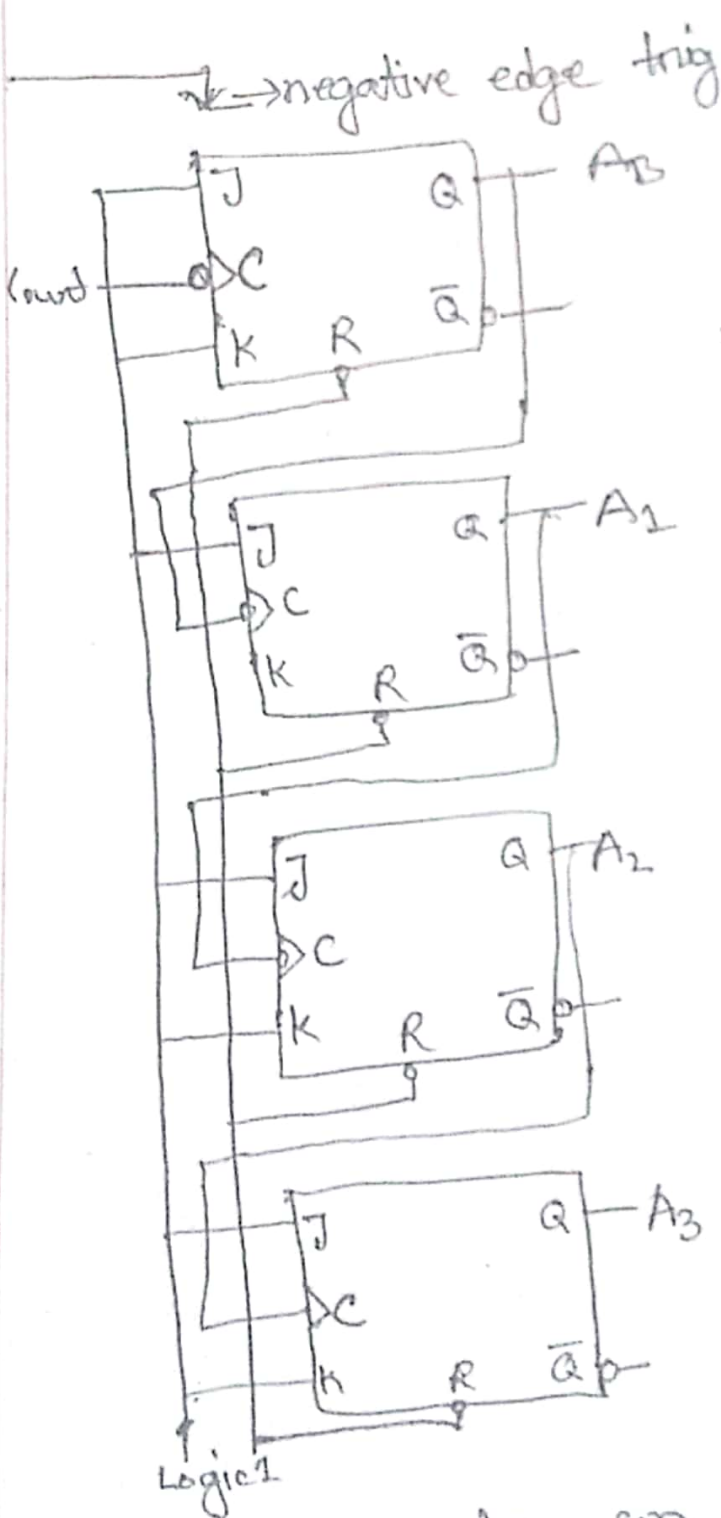
State diagram :



1920210339 0

P-10

Binary Ripple counter using JK Flipflop:



	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

4 bit ripple counter can count (0-15) = 16 decimal number