Effects of Inductor Current Ripple on the Performance of MPPT Using Boost Converter

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2021 International Conference on Technology and Policy in Energy and Electric Power (ICT-PEP) | 978-1-6654-1641-2/21/$31.00 ©2021 IEEE | DOI: 10.1109/ICT-PEP53949.2021.9600919

***Abstract*— With solar power and other renewables set to take over the market in the coming decades, maximum power point tracking (MPPT) will be essential to optimizing power output. One underserved topic of research is inductor current ripple's effect on MPPT algorithm performance. This study uses a boost converter topology to test the performance of constant duty cycle Perturb and Observe, Incremental Conductance and Constant Voltage PID algorithms. Inductor current ripple is controlled solely by changing inductance. This study concluded that all three algorithms were quite robust and affected very little over an inductor current ripple factor range of 20% to 40%. One novel finding was increased duty cycle oscillations when the MPPT update, and sample speed was faster than the boost converter response.**

Keywords—MPPT, boost converter, photovoltaics

I. INTRODUCTION

For most of its history, Photovoltaic (PV) energy was seen as a novelty for the environmentally concerned and was synonymous with conscious environmental thinking, that many companies used them as a form of virtue signaling. George Bush's lead energy economist, Ben Ho, commented on the state of PV in 2006, "At the time, I was looking at the numbers, and coal cost around five cents or four cents per kilowatt hour. Natural gas was also in that range. And solar was, like, a dollar per kilowatt hour" [1]. However, in the last decade, their popularity has grown for a different reason, government subsidies. To compete with nonrenewable energy sources, governments around the world offered subsidies to the PV industry to increase private sector investment in solar. The results have been dramatic. "The price of solar dropped by more than 90%, from $1 per kilowatt hour 15 years ago to 4 cents per kilowatt hour today." Lazard reported in [2] that the total cost of solar has dropped to 89% in the last decade.

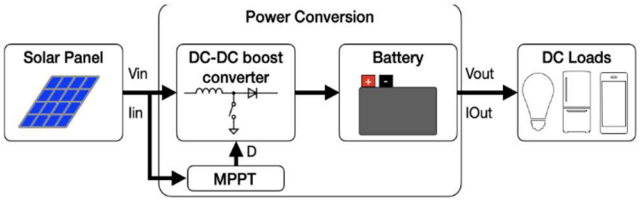

Fig. 1. Off-grid Photovoltaic System [6]

Solar energy technology has become efficient and cheaper than natural gas and coal. This fundamental shift in economics is a major driving force to solar. Tech companies with large energy needs are investing millions into solar to reduce their energy costs. Apple and Google data centers run completely on renewable energy, and Facebook has committed to 100% renewable energy by the end of 2020 [3-4]. In 2020, Blackstone invested $850 million dollars into Altus Power America, a Connecticut based solar energy company [5].

Much of PV technological development has been focusing on materials causing solar panels to become more than twice as efficient in the last decade [1]. However, other aspects of PV operation could also be explored to improve both PV performance and efficiency. One major component of a PV system that has attracted significant research interest is the power electronic interface. The hardware interface is required since PVs produce DC electricity while houses mostly operate with AC. Before DC to AC transformation is taking place, however, the output of PV must be conditioned to yield the most power from the solar panels. The circuitry to achieve this is commonly known as the maximum power point tracking (MPPT). These MPPTs utilize DC-DC converter to transform the voltage produced by the PVs. Many previous researches on the MPPTs focused on the algorithm to acquire the maximum power point and the DC-DC converter topology. One underserved topic of research which is the focus of this study is how inductor size in a DC-DC converter directly affects the performance of MPPT algorithms, and thus, the maximum output power of the system.

Fig. 1 illustrates a small off-grid PV diagram with three functional blocks: power generation (solar panel), power electronics block (Boost converter, MPPT, and battery), and DC loads [6-7]. Complex power electronic systems are needed to convert the electrical power generated in the first block to power loads in the third block. Electric power generated is almost never equal to the load power and needs voltage boosting to match the load voltage.

An example of a small off-grid system is a DC house system as reported in [8-16]. Families with a DC house will have access to electric stoves and lighting instead of burning biomass, reducing exposure to toxic combustion byproduct and smoke. Fig. 2 shows the simplified block diagram of the DC House system.

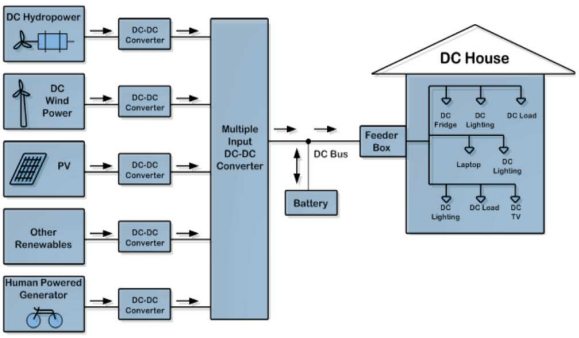

Fig. 2. Simplified diagram of the DC House project [16]

The boost converter is typically used in a PV MPPT system to increase the low voltage produced by PV. A boost converter works by storing energy in an inductor's magnetic field. This manifests as inductor current that increases output voltage. When the controller turns the switch on, the switch is a near zero impedance and voltage return path [17]. The boost converter can be operated in duty-cycle controlled impedance for MPPT. This is how the converter gets maximum power from the PV panel.

MPPT algorithms work on the assumption that PV panels have monotonic decreasing IV curves due to their internal resistances. For all operating conditions, there is a single maximum power point (MPP) where slope is zero. To the left of the MPP, the slope is positive, while to the right of MPP, the slope is negative. These characteristics are always true for every curve and are being used for two MPPT algorithms studied in this project [19].

Perturb and Observe (P&O) is one of the simplest MPPT algorithms used today. The algorithm compares output power at two different operating points and selects the maximum point, eventually reaching and maintaining an operation point at the MPP. The only downside of P&O is oscillation about the maximum power point. This is mainly due to the no condition for maintaining an operating point, and so the duty cycle may increase and decrease by one step continuously. A modified P&O algorithm addresses this limitation by adding a steady state hold position [20].

Incremental Conductance (IC) uses the slope of the voltage vs. power to find the maximum power point (MPP) where slope is zero. It calculates the change in voltage and change in current instead of just the change in output power. IC has three options for its operating point: maintain its voltage, increase its voltage, or decrease its voltage. If current remains constant, $\Delta I = 0$, power does not change and thus the panel is at the maximum power point [21]. The three IC states reduce oscillation about the maximum power point while maintaining the self-correcting tracking of P&O. The drawback is that three comparisons must be performed during MPP tracking compared to a single comparison with the P&O method [22]. Another important point is that the P&O and IC algorithms operate under the assumption that current and voltage outputs are relatively stable. In reality, the measurements have to be performed with current ripple due to the switching action in the boost converter [23].

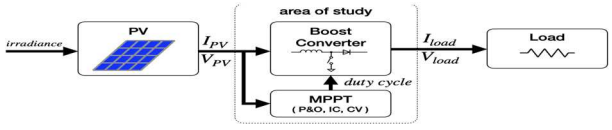

Fig. 3. MPPT Algorithm test setup diagram

The third MPPT system tracks the PV panel to a constant voltage provided by the panel manufacturer, usually after experimental testing. Likely this MPP will be maintained by a PID control over the converter's duty cycle [24].

All three algorithms are prevalent in industry and will be used in this study. P&O is chosen for its low overhead and prevalence. IC is similar to P&O, but it has less oscillation with a third operating condition, maintaining MPP. Constant voltage will serve as a baseline of pure tracking accuracy.

II. Requirements

Fig. 3 depicts the diagram of the proposed MPPT test system. To produce a time-varying power source from our PV panel, the irradiance is varied with a series of step inputs. This produces a change in the MPP for the system to track. A boost converter and MPPT controller will test tracking for three different algorithms. The load will be a resistor that can dissipate any load from the boost converter, properly sized to dissipate any power output from the system. Tables I and II summarize the design requirements and project specifications, respectively.

TABLE I. Design Requirements

Requirement	Value	Justification
Boost Switch Frequency	100kHz	Above nominal hearing threshold of 20kHz. Fast enough for good efficiency.
Duty Cycle Time Step	100ns	Time step is 1% of cycle period, providing good resolution and easy whole number calculations.
Simulation Time Step	100ns	Needs to match or be smaller the smallest time scale of the simulation, duty cycle. Easy to graph and calculate results on even ns time steps.
MPPT Algorithms	P&O IC CV	Three industry prevelant algorithms that are simple and fast to run in simulation with some built in support for Simulink.

TABLE II. Project Specifications

Requirement	Value	Justification
MPPT Power Accuracy	% of MPP	Quantifies ho well an MPPT algorithm tracks a MPP in steady state condition
Rise time	ns	Quantifies how quickly an MPPT algorithm can change to a new MPP steady state condition
Settling time	ns	Quantifies how quickly an MPPT algorithm settles to a new MPP steady state condition
Percent Overshoot	% of step size	Quantifies how large the overshoot power loss if the MPP changes steady state condition

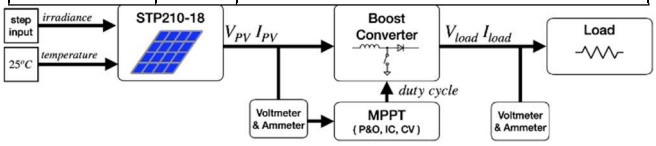

Fig. 4. MPPT Simulation Block Diagram

III. Design and Modeling

The final block diagram of our system is shown in Fig. 4. It has four distinct design sections: Photovoltaic (PV) panels, load, boost converter, and Maximum Power Point Tracker (MPPT). The order is relevant because each section has design parameters that set restrictions on subsystems downstream.

Much of the design and validation process follows the flowchart in [27] to design a MPPT system based on MPP resistance. There are several options outlined for more advanced topologies, but we chose a fixed Ro boost-converter system. The main consideration for the PV subsystem involves design overhead and how much time is needed to develop and validate the system.

We selected the Suntech Power STP210-18. The choice was mainly based on the solar panels that are currently being used for the DC House project. This panel operates at a maximum power output of 210W, which ranges from about 4A to 8A in our target region of study. There are two more parts to PV subsystem, irradiance, and temperature. Irradiance changes are far more common and sporadic than temperature changes which tend to be cyclical and slow to change. Hence, the irradiance will be varied and will be set at constant 25ºC room temperature. This is because in practice, irradiance is more likely to cause large changes in the MPP throughout the day. A change in maximum power point is simulated using a step input to irradiance. The irradiance upper bound is 1000W/m^2 which represents nominal maximum irradiance on a clear day. The lower bound was selected as 500W/m^2. This range provides a range of MPP from 209.9W at maximum irradiance to 108.1W at half power irradiance.

The load is the first subsystem with design restrictions due to panel selection and power output range. Using the method in [27], the first step is calculating the Rboost range between 1000W/m^2 and 500W/m^2.

$$R_{boost\_1}@\ 1000\frac{W}{m^2} = \frac{V_{mpp\_1}}{I_{mpp\_1}} = \frac{26.4V}{7.95A} = 3.321\Omega \quad (1)$$

$$R_{boost\_2}@\ 500\frac{W}{m^2} = \frac{V_{mpp\_2}}{I_{mpp\_2}} = \frac{27.005V}{3.996A} = 6.769\Omega \quad (2)$$

We then substituted for output voltage as a function of the input voltage and duty cycle, then solve for duty cycle. This leaves us an equation that successfully relates Rboost and Ro using duty cycle. We then chose 18Ω as our output resistance, and the expected duty cycle ranges from 0.387 to 0.57, which lies within the duty cycle limits between 0.15 and 0.85 with additional margin to spare.

Fig. 5 is the boost-converter topology used in our study. The minimum inductor operating in Continuous Conduction Mode maintains positive inductor current throughout its operation. The input voltage is the same as the PV MPP voltage, Vmpp. Inductor current ripple can be replaced by the MPP current, Impp and current ripple factor, γ. Current ripple factor is the ratio of peak-to-peak ripple to average current. Using ohm's law, we substituted MPP voltage and current with boost resistance. The resulting minimum inductor size is about 130µH. The actual inductance needed to achieve a 20% ΔIL will likely be higher but should have a similar magnitude.

The MPPT subsystem has two main sections, the MPPT block and the PWM generator as depicted in Fig. 6. The inputs to the system are current and voltage measurements from the PV panel. These two variables are fed into the MPPT block where one of three algorithms run: Perturb and Observe, Incremental Conductance, or Constant Voltage.

Fig. 7 is the final MPPT Simulink model used in this study. While the simulation runs, several measurements are logged for analysis via the oscilloscope blocks. For power measurements we log PV panel current, voltage, power, inductor current, output current, voltage, power. For non-power measurements we log irradiance and duty cycle.

IV. Test Results

Fig. 8 plots the inductor current for the three algorithms at the critical inductance. As you can see, the envelope of the system is smaller for the constant duty cycle system due to the reduced oscillation about the setpoint of 0.375. The γ_{IL} improves to 20.7% compared to 30.2% for a PO system. This test shows that a constant step size MPPT system will have a higher γ_{IL} than the expected value due to duty cycle oscillation for a PO system. The same test at critical inductance was run to determine if this trend was consistent for IC. The result also showed that PO and IC were virtually identical in performance. At critical inductance, IC had a γ_{IL} of 30.2% and a γ_{IL} of 20.4% under IC's constant duty cycle average of 0.375.

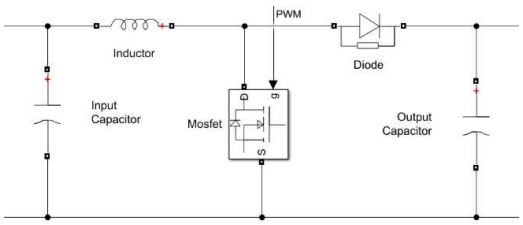

Fig. 5. Boost converter circuit model

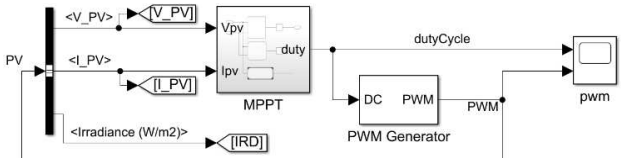

Fig. 6. MPPT subsystem.

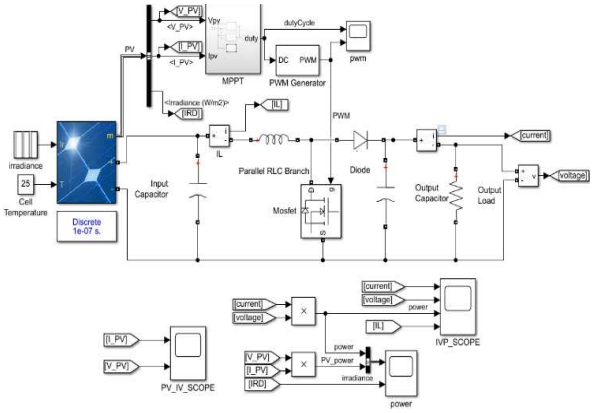

Fig. 7. Final PV-MPPT Simulink Model

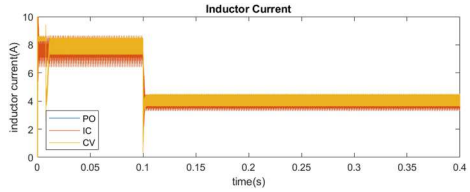

Fig. 8. PO, IC, and CV Inductor Current at L = 131µH

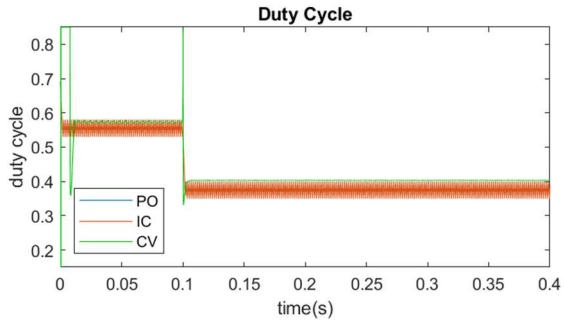

Fig. 9. PO, IC, and CV Duty Cycle at L = 131µH.

CV algorithm was much closer to ideal in duty cycle as shown in Fig. 9. This system was tuned to reduce the steady state oscillation, rise time, and fall time. The advantage of this CV-PID system is variable duty cycle step resolution compared to a standard PO or IC algorithm. The changes in duty cycle are calculated using PID so the duty cycle can be much smaller than 1% in steady state condition and much larger than 1% during transient response.

All three algorithms showed that γ_{IL} was larger than expected for a calculated critical inductance. This meant for our study we needed to iterate simulations of different inductor size until we achieve the desired γ_{IL} in 5% increment step from 20% to 40%. We expected PO and IC to have similar inductances that were moderately larger and CV to have slightly larger inductances compared to calculated critical inductance based on our initial simulations. Table III shows the resulting inductor sizes obtained through iterations.

Initial irradiance step down tests show positive correlation for average output power as γ_{IL} increased for both PO and IC. Typical best practice tells us to minimize γIL by increasing inductance until it becomes too large for its form factor or too expensive, but this may not be the case for our circumstances. Specifically, this may not be the case for MPPT systems of fixed duty cycle step size, PO and IC. The CV system had almost the exact same output power regardless of γ_{IL}.

The output power standard deviation trends slightly upward for all three algorithms as depicted in Fig. 10. This makes sense intuitively as we would expect larger deviation from the average as the inductor current input to the system increased in deviation as well. There is a significant different in the output power envelope for PO and IC compared to CV. Smaller inductor current ripple factor results in a larger power envelope in steady state for PO and IC, while it is relatively constant in CV. This difference gives us insight as to why average power increases as inductor current ripple increases.

Plotting average duty cycle versus γ_{IL} confirms that CV had the most accurate average duty cycle, leading to highest average output power. In contrasts, PO and IC average duty cycles appear to be between 3-4% lower than the more ideal CV algorithm. We know inaccurate average duty cycle is the problem, but we still need to root source the cause of this suboptimal performance. This can be partially answered by looking at the standard deviation and steady state envelope of duty cycle as shown in Fig. 11. The constant voltage system has almost no deviation and less than 1% envelope for duty cycle. PO and IC on the other hand will never have less than a 1% envelope due to their constant step size but it should be close to 1%. To gain more insight we plot all three algorithms duty cycle for visual inspection.

The first insight gained looking at the graph is that PO and IC duty cycles appear to oscillate periodically as depicted in Fig. 12. This points to a sampling frequency or transient response time issue. The second insight is that PO and IC do track duty cycle to the same value of 0.4 as CV, but the duty cycles oscillate on the lower end.

It should be noted that PO and IC perform identically. This makes sense due to the simulation parameters. IC was implemented in its most basic form, which resulted in identical duty cycle step changes as PO unless the current power measurement was equal to the previous power measurement. In the IC block, there is no reduction in precision during power comparison so it will almost never be exactly the same due to boost converter switching. This effectively eliminates the option to maintain duty cycle and causes identical step changes to PO. The identical overall performance can be attributed to the tests being run in simulation. With the same duty cycle controls the simulation will run the exact same way.

TABLE III. INDUCTOR SIZE IN μH FOR γ_{IL} AT 500W/M^2 IRRADIANCE

γ_{IL}	40%	35%	30%	25%	20%
Critical Inductance	65.5	74.8	87.3	104.7	130.9
PO	83.6	104.4	132.2	200.0	400.0
IC	83.6	103.3	132.2	200.0	400.0
CV	73.0	82.5	96.4	117.2	146.4

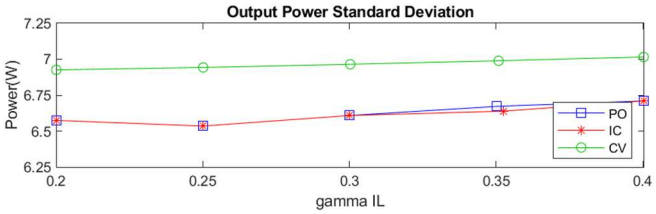

Fig. 10. PO, IC, and CV Output Power Standard Deviation and Range vs. γ_{IL}.

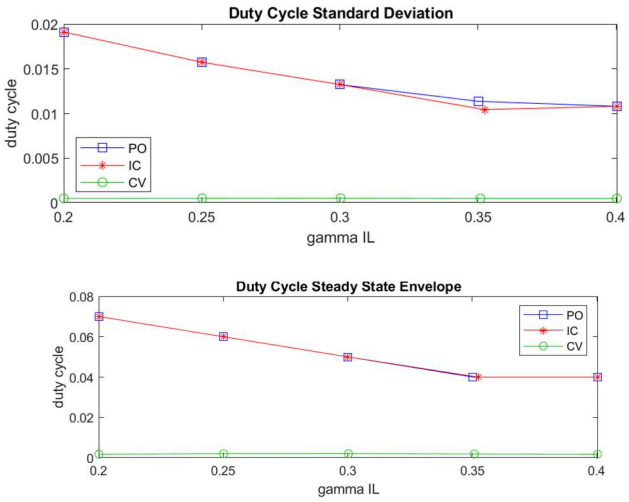

Fig. 11. PO, IC, and CV Duty Cycle Standard Deviation and Range vs γ_{IL}.

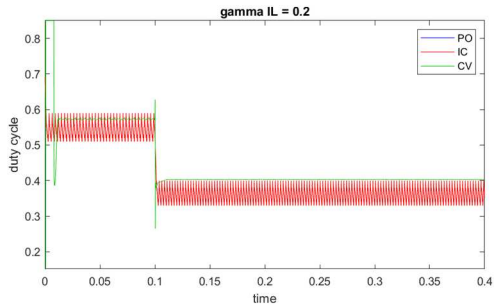

Fig. 12. PO, IC, and CV Duty Cycle vs Time for γ_{IL}.

Upon further inspection, CV also has a periodic oscillation as shown in Fig. 13. PO and IC oscillate every 24 cycles at 417 Hz and the CV oscillates every 18 samples at 555 Hz at 20% γ_{IL}. The general shape appears to be a triangular waveform with asymmetric slopes. PO and IC appear to rise monotonically towards a 0.4 duty cycle, then fall slower to its lower bound of 0.36. CV does the opposite with a slower rise to maximum with a much steeper and shorter fall.

The same duty cycle trends appear at 40% γ_{IL}, but oscillation frequencies get much shorter as shown in Fig. 14. PO and IC oscillate every 13 cycles at 770Hz, and CV oscillates every 11 cycles at 909Hz. The shortening of the oscillation cycle appears to be the reason PO and IC perform better at larger γ_{IL}. The envelope of the duty cycle is smaller, reducing the duty cycle envelope. This trend was consistent across all simulations. Larger γ_{IL} were achieved with smaller inductances and the periodic nature point to a transient response and sampling time conflict.

We simulated the model with the slowest transient response system of 20% γ_{IL}. With the new sampling time of 300µs, the duty cycle oscillation has been minimized but still persisting for PO and IC. The oscillation could potentially be reduced to 1% through additional blocks to the algorithms, such as an averaging filter or reduced precision for power comparisons. Fig. 15 shows that further reduction in the duty cycle may not improve performance at all. The 2% duty cycle oscillation does not show any negative effects on the average output power or its envelope. PO and IC seem to operate on par with the CV system at less than 0.1% duty cycle envelope, which is essentially constant. Results from 1000W/m^2 is listed on Table V.

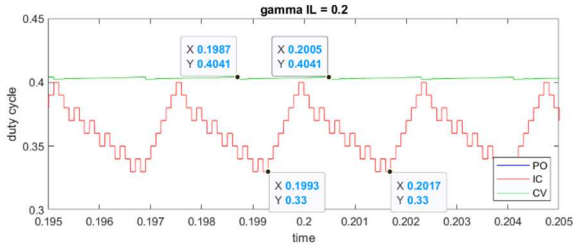

Fig. 13. PO, IC, and CV Duty Cycle Oscillations for γ_{IL} = 0.2.

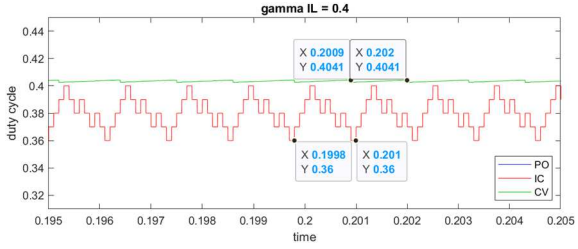

Fig. 14. PO, IC, and CV Duty Cycle Oscillations for γ_{IL} = 0.4.

TABLE IV. DUTY CYCLE ENVELOPE RESPONSE TO SAMPLING TIME AT 500W/M^2 IRRADIANCE

Ts	100 µs	150 µs	200 µs	300 µs	1 ms	10 ms
PO, L = 86.3 µH	4%	2%	2%	2%	2%	2%
IC, L = 86.3 µH	4%	2%	2%	2%	2%	2%
PO, L = 400 µH	7%	4%	3%	2%	2%	2%
IC, L = 400 µH	7%	4%	3%	2%	2%	2%

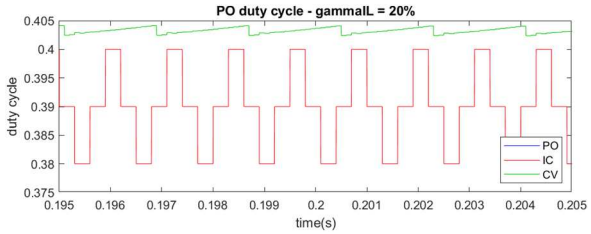

Fig. 15. PO, IC, and CV Duty Cycle Oscillations for γIL = 0.2, Ts = 300µs.

TABLE V. INDUCTOR SIZE IN μH FOR γ_{IL} AT 1000W/M^2 IRRADIANCE

γ_{IL}	40%	35%	30%	25%	20%
Critical Inductance	47.4	54.1	63.1	75.8	94.7
PO (t_s = 300us)	60.4	69.3	81.6	100.5	130.9
IC (t_s = 300us)	60.4	69.3	81.6	100.5	130.9
CV	55.6	63.9	74.6	89.1	112.5

The most prominent transient response for the 1000W/m^2 to 500W/m2 irradiance step was rise time for all three algorithms. As shown in Fig. 16, they follow the same trend, decreasing as γ_{IL} increased. This is due to the smaller inductors used to get a larger current ripple envelope providing a faster transient response than larger inductors. CV rise time is slightly lower as they used smaller inductances.

Settling time and overshoot did not have distinct trends, as depicted in Figs. 17 and 18. Values were within 1% and 10% respectively for the entire range of γ_{IL} tested. CV settling times were slightly faster than PO and IC due to smaller inductances, but the trend is flipped for overshoot. This was expected as the overshoot was a design tradeoff during PID tuning as the integrative coefficient was increased to duty cycle oscillation.

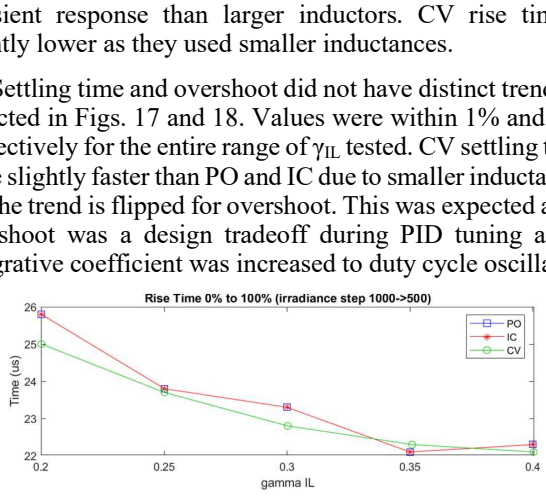

Fig. 16. PO, IC, and CV Rise Time vs γ_{IL} 500W/m^2 Irradiance Step Down.

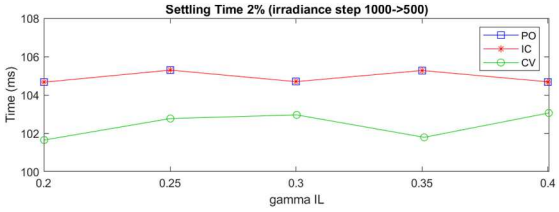

Fig. 17. PO, IC, CV Settling Times vs. γ_{IL} 500W/m^2 Irradiance Step Down.

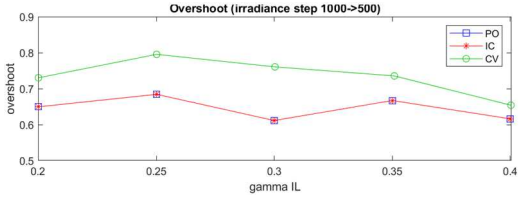

Fig. 18. PO, IC, and CV Overshoot vs. γ_{IL} 500W/m^2 Irradiance Step Down.

V. Conclusion

This paper presents results of the study to investigate the direct effects on output power, duty cycle, rise time, settling time, and fall time for three algorithms: Perturb and Observe, Incremental Conductance, and Constant Voltage.

Simulation results indicate that even without any prefiltering or modifications, all three algorithms are very robust to inductor current ripple in steady state conditions. Average output power changed less than 1% over a range of 20% to 40% γ_{IL}. Some small differences were observed in output power envelope and standard deviation, but these are attributed to the boost converter itself. Despite the different inductor current ripple, all three algorithms output virtually the same duty cycle as the average, standard deviation, and envelope barely changed. For power step down transitions, rise time increased with inductor size as expected, but settling time and overshoot were similar for all γ_{IL}. CV had slightly more overshoot as a tradeoff for slightly faster rise time.

Another finding was the importance of sampling and update speed of the constant step size MPPT algorithms relative to the system response time. The initial sampling period of 100µs was faster than the system response. This leads to the duty cycle stepping in a direction based on the system's response to the previous duty cycle. When the sampling period was increased to allow the system to respond and duty cycle to change based on its previous cycle's effect, the duty cycle oscillation was minimized from 7% to 2%. Results further indicated that a basic PO and IC algorithm of constant step size can tolerate a 2% duty cycle oscillation with virtually no negative effects. It also demonstrates there is a diminishing return on sampling speed without introducing additional blocks like an averaging filter.

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