Design of digital integrated systems: optimization of a 16 bit Brent-Kung adder

Arnout Devos

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1 Schematic and optimisation

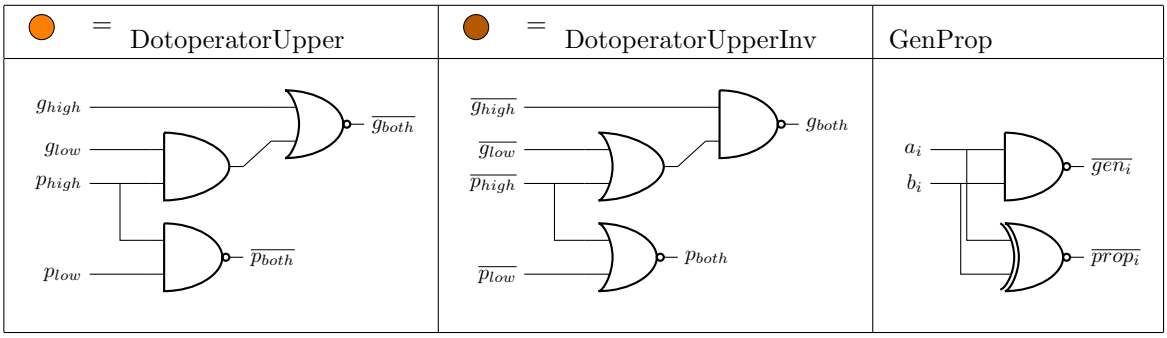
1.1 Optimisation

When trying to minimize the critical delay, first one needs to look at the critical path. The signal on this path needs to travel through a lot of gates (which also drive other gates) which is the determining factor of timing of the adder. Therefore this critical path is the main focus of the timing optimization[1].

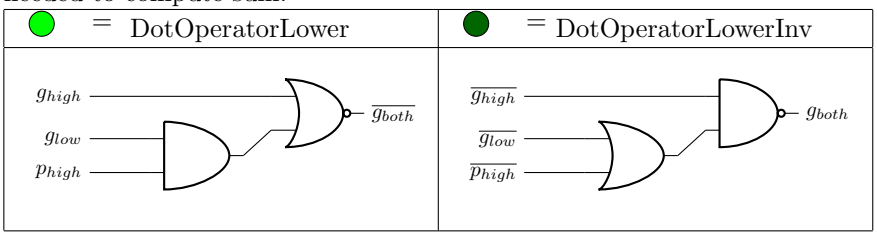
When meeting the delay requirements, energy can be optimized. This can be done by decreasing the supply voltage or appropriate sizing of the transistors. In fact upsizing can yield a total reduction in energy (dynamic switching energy) when lowering the supply voltage, taking into account the delay specification.

1.2 Achitectural optimization

- Gate level
  - Moving towards inverted inner stages to remove most inverters. Add inverters where needed to make result correct. An XNOR gate is added to generate $\overline{prop_i}$ in the GenProp block.

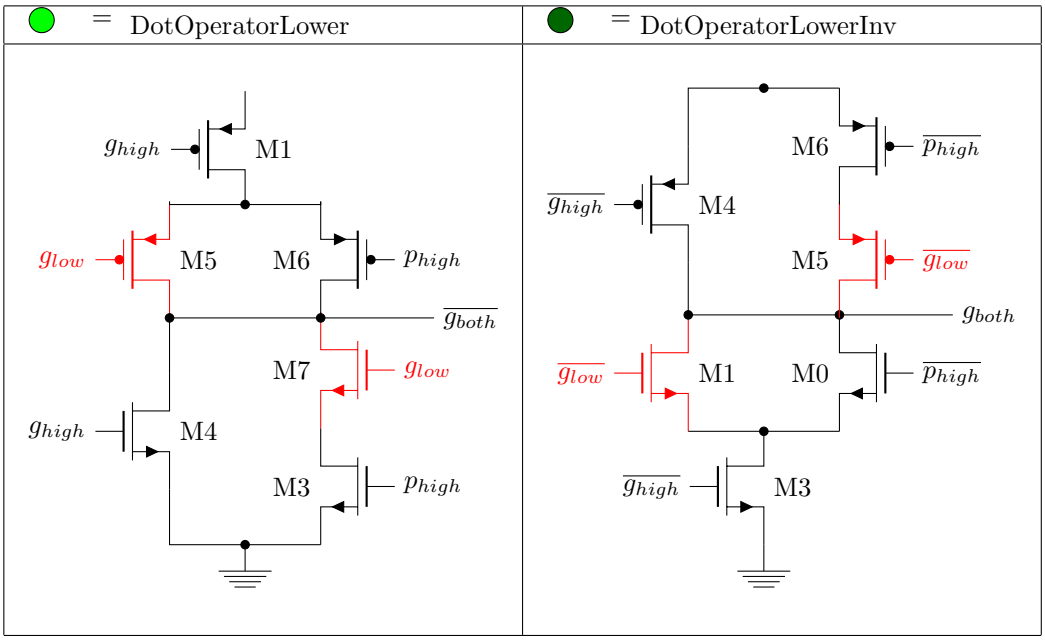


  - Remove propagate signals (inverted and non-inverted) from lower dotoperators since only g_i is needed to compute sum.



[1] Only the critical path going from a_0b_0 to s_{15} is optimized keeping the GenerateOverview.m script in mind. The optimization for minimal energy, given all sum outputs are below 650ps delay, is not considered here. In this implementation only the provided transistors are used, so no low-V_T or other technologies.

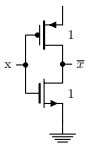
- Transistor level
  - Attach critical path Generate signal to TOR which is closest to ouptut. Because then, less capacitance has to be charged and signal can therefore propagate faster to the next gate.



  - Use passgate logic XOR (genprop and sums) to minimize switching energy. However still use a regular XOR on critical path for speed.
  - Since the critical path starts at the XNOR gate with $prop_1$, the wiring to the dotoperator will be done in such a way that $prop_1$ is connected to the transistors closest to the output.
- Structural level
  - Use minimal inverters (see section 1.3) to correct for the optimization of the critical path. This means that certain non-critical paths will need to be converted to their inverted counterpart again, because a minimal inverter has been used to minimally load the critical path.

1.3 Sizing

- Decrease sizing of all transistors loading the critical path to minimal sizing for both pMOS and nMOS to minimize energy consumption.
  - In case the critical path is loaded with more than 2 transistors on the non-critical path, minimal inverters are inserted as 'inverting buffers': relative size 1 pMOS & size 1 nMOS to load the preceding gate (on the critical path) with as little capacitance as possible.



- Scale sizing on critical path for optimal energy and delay.
  - Since minimal energy is the goal, a more than exponential sizing approach will yield the best results.
  - Make transistors connecting the critical path transistor to V_{DD} or *ground* arbitrarily big to provide a very good conducting path in case of a critical change. Remark that the increased capacitance which comes with this increase in width doesn't influence the timing since the intermediate node has already settled to the 'correct' value when the critical signal arrives.

1.4 Task

All in all you should have about two pages of explication (including the header).

2 Results

Please fill in table 1. Additional columns may be added, but provide at least one column with the data for the point with delay 650 ps.

2.1 Schematic

Figure 1: Schematic of the optimised adder

Delay	650 ps
Supply	0.883 V
Switching Energy	80 fJ
DC power	1.31 nW

Table 1: Final performance of the circuit