Design of Digital Integrated Systems: exercise session 2,3,4

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October 7, 2015

1 Introduction

The purpose of the next two and a half exercise sessions is to optimise a Brent-Kung adder. We will optimise a 16-bit adder to make things interesting, but not too difficult. At the end of these exercise sessions, you will have to hand in a report based on a template we will provide. The professor will ask you a question on the exam based on this report.

2 Starting point

To help you get started, we provide you with a standard textbook implementation of the adder. In appendix A, you can find a schematic representation of the adder. Download the zip-folder for this exercise session from Toledo.

Copy the files "Adder16b.m", "Adder16b_BrentKungStandard.m2s" and "Adder16b.vec" to the correct folders of last session. This is your starting point. Do not alter the "Adder16b.m" or "Adder16b.vec" in any significant way, as we will use those exact files to check your design. In the m2s-file, you should only change the adder subcircuit so that everyone has the same test environment. All output signals will be loaded with the equivalent of 16 minimal inverters and the input is driven by a minimal buffer, which are all not included in the delay and power calculations.

3 Goal

The goal of the optimisation is to present an adder that uses as little energy as possible while having a **maximum delay of 650 ps**. You can change the supply voltage (max 1V), the transistor sizes, the architecture and even the transistor architecture of the gates. Changing the core topology is not allowed, keep it to a Brent-Kung adder.

Hints:

- Start by looking for the critical path, see how you can reduce the number of gates.
- Are there gates you could get rid of?
- In a last step, try to size the gates.

4 Report

The final result of these exercise sessions is a report of a few pages. You could consider this a sort of "datasheet" for the adder you designed. Show how you have optimised the adder and why the techniques you used work. Add a schematic of the adder, indicating the size of the transistors. You can either do this in TikZ/LaTeX or Visio or by hand (as long as the drawing is sufficiently clear). You should indicate the delay, active power, standby power etc. for your adder, in function of the power supply. Plot the energy-delay trade-off and indicate the minimum EDP you can achieve.

To give you a hand in this process, we provided a template for the standard Brent-Kung. Obviously we can't describe the techniques we used to optimise it, as it isn't optimised. Make sure you add your optimisations in the document. The template can be found in the "doc" folder as a LaTeX file, with the figures in "doc/figures". The code that was used to generate the figures and compile the pdf can be found in "GenerateOverview.m" in the main folder.

A Schematic Brent-Kung adder