Design of digital integrated systems: optimisation of a 16 bit Brent-Kung adder

Your name here

November 25, 2015

1 Schematic and optimisation

1.1 Optimisation

On this page you describe the optimisations you have used

- Architectural
  - We changed this gate
    - like this
    - and like this
    - and like this
  - The main effects are
    - this
    - and this
- Sizing
  - we increased the size of
    - this transistor
    - and this transistor
    - etc.

All in all you should have about two pages of explication (including the header).

2 Results

Please fill in table 1. Additional columns may be added, but provide at least one column with the data for the point with delay 650 ps.

Delay	650 ps
Supply	x.xx V
Switching Energy	xxx fJ
DC power	x.xx nW

Table 1: Final performance of the circuit

2.1 Schematic

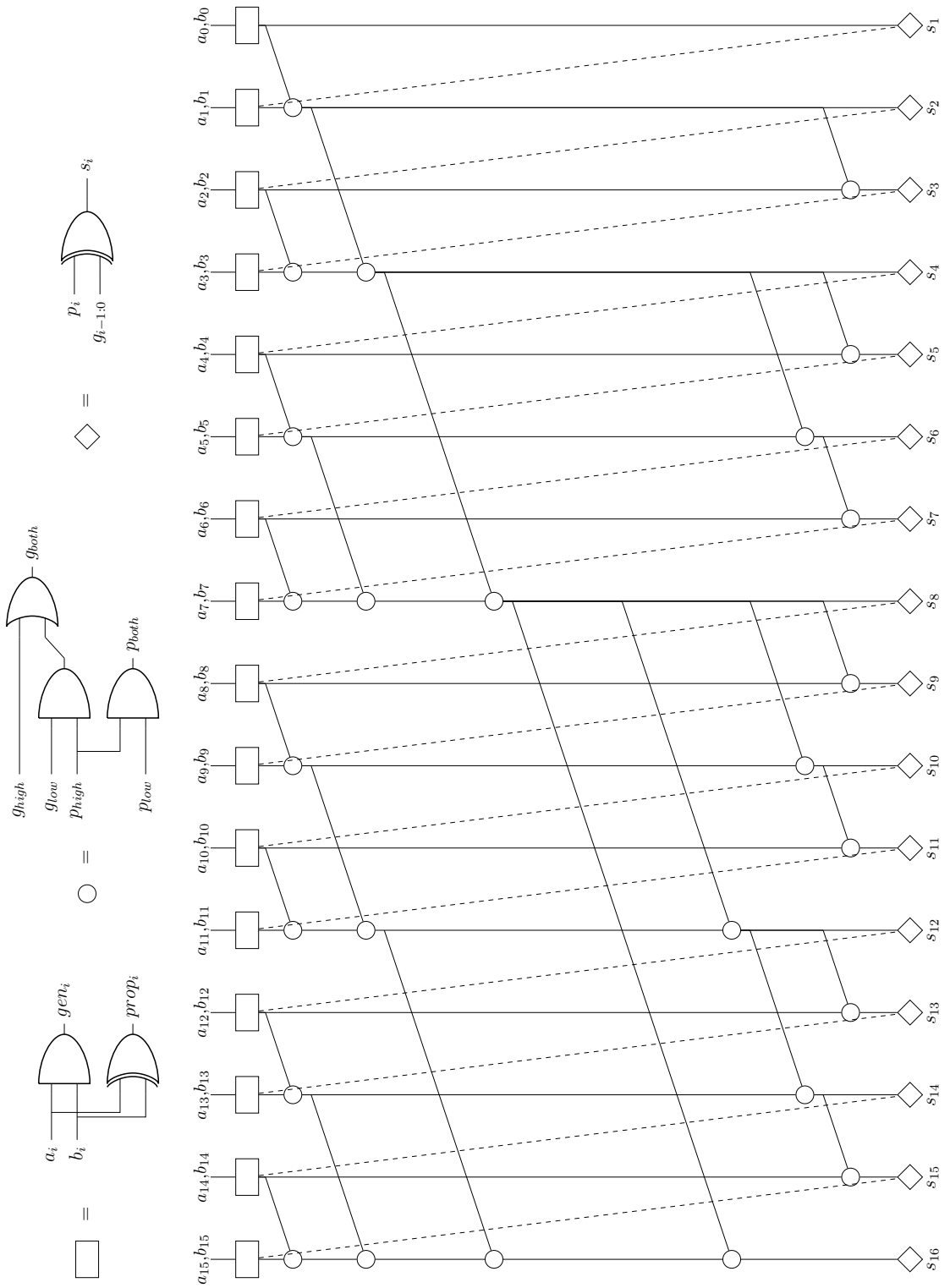

Figure 1: Schematic of the optimised adder