**HARDWARE TESTING**  Soldered all the components to the student boards, Loading the model on the FPGA, taking in used a socket for the transceiver to be pluggable. account timing constraints for the transceiver. Adjusting parameters in the model to get proper Simple testing with multimeter and sender/receiver and lossless transmission. testing with oscilloscope and simple program. Adjusting code and blocks if necessary, e.g. extra We found a little bug due to datasheet incorectness slow clock signal in sender for transceiver signal. and fixed it with two little wires on each student pcb. 90% 50% **XILINX**® Converted all our custom build logic to system Sending and receiving generator synthesizable logic. messages through GUI We made sure everything worked as in cooperation with USB before with new simulations. interface. Simplifies high level testing 90% 05 INTEGRATION & EXTRA Clear contract with Brain about what and how data will be sent. Bus implementation will be ready soon. 20% 03 **KU LEUVEN** 

> Jona Beysens Arnout Devos

**H2 Team RF** Andreas Van Barel