# Photosensitivity of silicon based junctionless field effect transistors: a simulation study

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***Abstract*—This paper reports on the simulated photosensitivity of double gate junctionless field effect transistors. The region of interest for illumination is in deep depletion where the device is most sensitive. N-type devices demonstrate up to six decades of $I_{on}/I_{off}$ current both for big (500) and small (20nm) silicon thicknesses with appropriate sizing and biasing.**

***Keywords*—Junctionless, double gate, illumination, photosensitivity, depletion.**

## I. Introduction

With the downscaling of silicon CMOS technology the conventional MOSFET suffers from problems known as short channel effects. These effects arise when the source and drain are brought closer and closer together making the channel shorter. This also put constraints on fabrication, since the drain, source and channel are regions with different doping concentrations. As a result of the technology downscaling a new device is ready to function properly: the junctionless transistor (JLT) is a multigate device without PN nor $P^+P$ or $N^+N$ junctions [1]. The channel of a JLT is highly doped as to achieve good ohmic contact and low on resistance. Since the current channel is formed in the bulk of the device, the impact of surface interactions such as surface roughness scattering is negligible [2].

JLT devices are also of interest in photodetector applications since they show good sensitivity and low dark current when biased in the OFF state [3]. A device which features a uniformily doped channel but imitates bipolar transistor working by gate control of carrier concentration instead of permanent doping, has been proposed in [3].

## II. Inner working

In order to observe a change in current due to illumination the dark current needs to be low like in a PN junction. This state is reached when the device is biased in the OFF state. For a donor doped channel this means applying a negative gate voltage. In this biasing condition, majority carriers are depleted from the channel and inversion layers of minority carriers appear near the gate oxides. This distribution of carriers is similar to a MOSFET working in inversion, however the drain and source doping are equal to that of the majority carriers making it impossible for the minority carriers near the gate oxides to move.

The photoelectric effect in JLT results in rise of electric conductivity (photoconductance), whereas in PN junctions it results in appearance of electromotive force (photovoltaic effect). Since the device is symmetrical with respect to the direction of the channel, a drain source bias needs to be applied in order to create an electric field which guides the carriers both in the ON and OFF state. When the channel is illuminated, the photo-generated minority carriers easily travel towards the contacts in response to the high electric field. However, the photo-generated majority carriers are trapped inside the potential barrier induced by the gates. In order to comply with charge neutrality the barrier is reduced due to the illumination. This lower potential barrier creates a way for the trapped majority carriers to diffuse. On top of that it makes it easier for charges to flow. The JLT is now pushed towards the ON state while the gates remain biased for a non-illuminated OFF state as can be seen in Figure 1.

Figure 1 is made using TCAD simulations where the OFF state is reached by applying a gate voltage of -2V whereas the ON state is reached by applying a gate voltage of 0V, all this under a Vds bias of 1V.

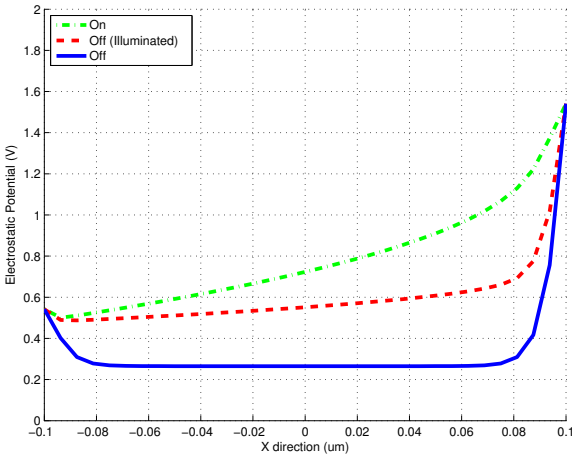


Fig. 1. Comparison of Electrostatic Potential distribution in the center of the channel on a JLT with 15nm Si thickness, 200nm Gate length, $V_{DS} = 1V$ and Nd = 2 $10^{19}$.

## III. Implementation & Simulation results

Contrary to the device in [3] in this manuscript a typical double gate JLT structure is used which allows for easy fabrication and exploits the advanced CMOS technology.

We consider a junctionless DG MOSFET which consists of an n-type doped channel ($L_G$ = 200nm) as shown in Figure 2.

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Here $L_G$ and $t_{ox}$ are the gate length and gate oxide thickness, $t_{Si}$ and $N_D$ are the silicon thickness and the donor density in the channel.

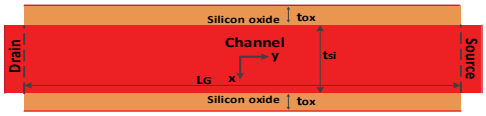


Fig. 2. JLT Architecture

Two orders of device sizes are implemented for simulation. Firstly the small size JLTs are studied in order to see what happens when current state of the art JLTs are illuminated. Then a bigger device of 500nm silicon thickness will be studied to achieve higher currents such that the device can be used in practical photodetector applications.

Current-voltage characteristics for $t_{Si} = 15nm$ for various doping concentrations can be found in Figure 3. Comparing the OFF state without illumination and the OFF state with illumination a difference of $10^4$ in current can be observed. However the currents are rather low since the device its dimensions are small. When illuminating with the power of the sun, being $1mW/cm^2$ instead of the $1\mu W/cm^2$ used here, a difference of $10^6$ in current can be observed which is a promising result. Therefore the current-voltage characteristics of a bigger device

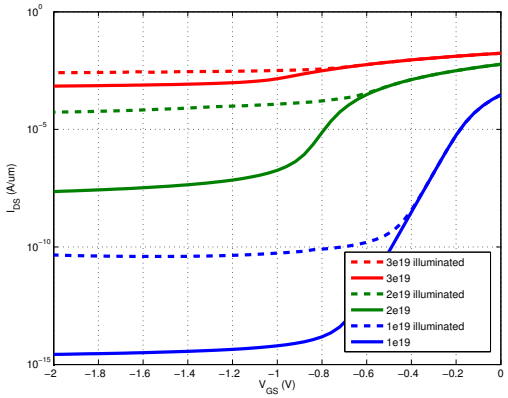


Fig. 3. Current-Voltage characteristic of a JLT with $15nm$ Si thickness, $200nm$ Gate length, $V_{DS} = 1V$ and $1\mu W/cm^2$ illumination

with $t_{Si} = 500nm$ and $L_G = 2\mu m$ are shown in Figure 4. As expected the 500nm semiconductor thickness JLT exhibits the same sort of characteristics as the smaller devices as can be seen in. Now however the absolute current will be higher and detectable for the use in photodetector applications.

## IV. Conclusion

This work showed that a junctionless transistor indeed exhibits photosensitive behavior when using appropriate sizing and doping concentrations. A trade-off needs to be made between the doping concentration (which affects resistance) and silicon thickness (which affects the current). According

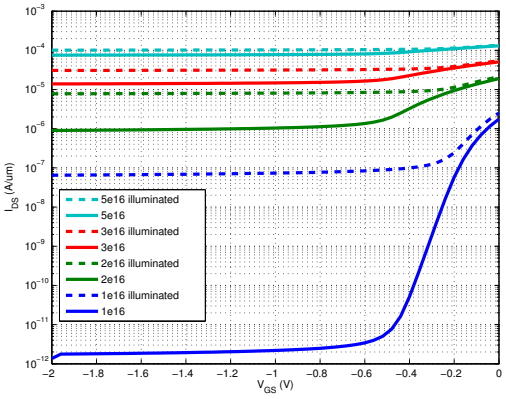


Fig. 4. Current-Voltage characteristic of a JLT with $500nm$ Si thickness, $2\mu m$ Gate length, $V_{DS} = 1V$ and $1\mu W/cm^2$ illumination

to simulations with illumination, when finetuning the two trade-off parameters, a current ratio of $3.10^4$ together with a reasonably high absolute current can be observed which is large enough for photodetector applications.

Further research could be conducted around the comparison of the photosensitivity of a Junctionless Double Gate MOSFET and a regular (junction) MOSFET. Another important point of research would be to investigate wether the change of current when illuminated is originating only from the illumination excited electron-hole pairs or is also due to other factors coming indirectly related to this illumination. In this work only silicon was used as semiconductor. However using other materials such as GaAs or Ge could improve the device's photosensitivity performance.

## References

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