Chapter 4
Design of the Automatic Voltage Regulator

AVRs are primarily used to regulate the output voltage of synchronous generators. In this chapter we will cover the tuning of exciters as recommended by the IEEE committee for excitation system models [16, 17]. The exciter tuning is in line with the recommended IEEE committee practice report in [18]. Although recent literature has confirmed that these models provide good agreement with detailed models [19], new models continue to be introduced for specialised situations [20]. Advanced control methods have appeared in the literature [21, 22] but it appears that the tuning based on classical control ideas has plenty of applications [23, 24]. The IEEE committee report [25] has some essential classical control ideas based on an interesting paper, which discusses the estimation of closed-loop poles from open-loop poles and frequency response [26]. AVRs are also known to enhance the transient stability of synchronous generators and some of the easy to follow classical papers on this subject are: [3, 27–29].

4.1 Synchronous Machine Model for AVR Tuning

For the initial AVR design synchronous generator is modelled as a first order system. Subsequent to this design the performance of this AVR is evaluated for the machine connected to the grid. The first order model is justified by looking at the SMIB system in Eqs. (3.96)–(3.98). For unloaded generator, i.e., the generator stator current is zero, E'_q is equal to the terminal voltage and thus Eq. (3.98) describes the dynamics between the field and terminal voltages. Most of the exicter design is done for unloaded generator. Setting $I_d = 0$ in (3.98), we get the following transfer function for the synchronous machine:

$$\frac{\Delta V_t(s)}{\Delta E_{\text{fd}}(s)} = \frac{1}{1 + sT'_{d0}} \tag{4.1}$$

H. R. Pota, *The Essentials of Power System Dynamics and Control*,
https://doi.org/10.1007/978-981-10-8914-5_4

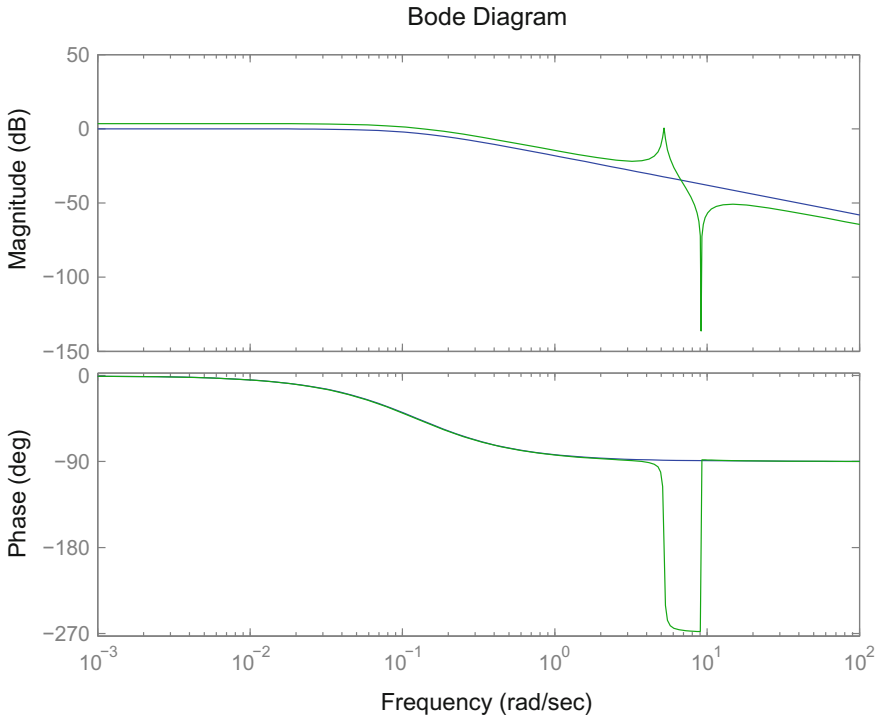

Fig. 4.1 Synchronous machine—frequency response $\frac{\Delta V_t(s)}{\Delta V_{\text{ref}}(s)}$

Although unloaded machine model is used for AVR tuning, it proves to be quite robust even when the machine is loaded. Figure 4.1 shows frequency responses of an unloaded generator and the same generator loaded at 0.9 pu. A few points need to be carefully observed about the two frequency responses in Fig. 4.1.

1. At low frequencies the exact plot has a higher gain than the approximate plot. This means that the steady-state error in practice will be lower than the designed value.
2. At higher frequencies the exact plot has a lower gain than the approximate plot. This means that the system will have higher gain margin than the designed value.
3. The biggest difference between the two plots is for a complex pole-zero pair. It can be seen that the phase and magnitude contribution due to the pair appears only near the electromechanical frequency of oscillation. A good AVR compensation method should not alter the frequency response in the range of this complex pole-zero pair. This also enables an independent design of the excitation system and the power system stabiliser.

AVR Models

IEEE recommended practice for excitation system models covers four DC commutator exciters, eight alternator-supplied rectifier exciters, and seven static excitation systems [16]. In what follows we will look at tuning the parameters of one exciter from each of the three groups. To understand the fundamentals of exciter tuning it is sufficient to look at a simple exciter model and tune its gain to meet performance specifications. Once it is understood how the gain for a simple AVR can be tuned the rest will follow rather easily.

A good understanding of the tuning process is achieved by considering a first order AVR model

$$\frac{K_A}{1 + sT_A}$$

where for practical systems K_A ranges between 200 and 500 and T_A is about 10 ms.

4.2 AVR Performance Requirements

The terminal voltage of a syncrhonous generator has to be maintained at a certain level. Due to the varying load conditions, and the resulting change in voltage drop across the stator reactance, the terminal voltage varies. Feedback control is one easy way to make sure that the terminal voltage is at a set value regardless of the changing load conditions. The correction needs to be made as quickly as possible, i.e., it must be a fast acting feedback controller. From Sect. 3.3.6 we know that to obtain a fast response, the open-loop bandwidth has to be large and to ensure a small steady-state error we know from Eq. (3.87) that the DC gain of the transfer function has to be large.

Formal performance specifications for AVR performance are given in IEEE guide [18] and a committee report [25]. The material covered here will enable the tuning of AVR parameters in most cases to satisfy the requirements in [18] and [25]. As the implemented AVRs are nonlinear, some fine tuning or empirical adjustments may be needed for practical systems.

4.2.1 AVR Tuning—K_A and Phase-Margin

The main issues involved with the design of an AVR can be illustrated using a simple example from [24]. The block diagram for this example is shown in Fig. 4.2 with $T_A = 0.04$ and $T'_{d0} = 1$.

The immediate problem is the selection of gain K_A such that it has a fast rise-time and small steady-state error. A block diagram of an AVR and a generator is shown in Fig. 4.3. In the block diagram the disturbance term $\Delta d(s)$ represents the weakening

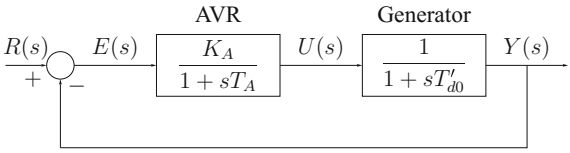

Fig. 4.2 AVR tuning block diagram

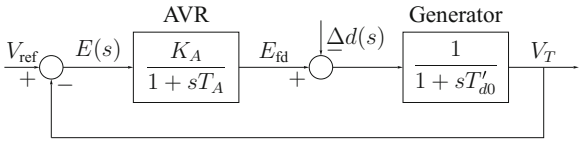

Fig. 4.3 AVR tuning—steady-state error

of the flux due to armature reaction, etc. In other words, $\Delta d(s)$, models the effect of all the disturbances which change the terminal voltage. Typically: $T_A = 0.05$, $T'_{do} = 5$, $K_A = 50$; with these values and for a unit step change in reference voltage and disturbance $\Delta d(s)$,

$$e_{ss} = \lim_{s\to 0} s\left(\frac{1}{s}\frac{(1+sT_A)(1+sT'_{do})}{(1+sT_A)(1+sT'_{do})+K_A} + \frac{1}{s}\frac{(1+sT_A)}{(1+sT_A)(1+sT'_{do})+K_A}\right) = \frac{2}{1+K_A} = 3.92\%$$

Steady-state error of this magnitude is not acceptable and a way is needed to increase the low frequency gain. Next we see what happens when K_A is increased.

For the closed-loop system in Fig. 4.2, the frequency and step response are plotted in Figs. 4.4 and 4.5 for gains: $K_A = \{1, 10, 20, 50\}$. The phase-margins corresponding to these four gains are: 180°, 75.6°, 59.8°, and 40.5°, respectively. From the previous analysis we can expect that higher values of K_A result in faster response and lower values of phase-margin result in response with low damping. This can be seen in the time responses in Fig. 4.5.

It can be seen that higher gain results in lower steady-state error and faster response. But higher gains also mean oscillations. It is important to realise that there is a trade-off between the exciter gain and the closed-loop system damping. At times it is possible to find a value of K_A that meets both the steady-state error and speed of response requirements. In most cases a constant gain AVR is not suitable for obtaining a satisfactory transient and steady-state response. A lag block can be used to provide the desired steady-state response and acceptable transients. For achieving a damped and fast response with small steady-state error the controller can be augmented with a lag block. Next we look at how to tune the parameters of the lag block to meet AVR performance specifications.

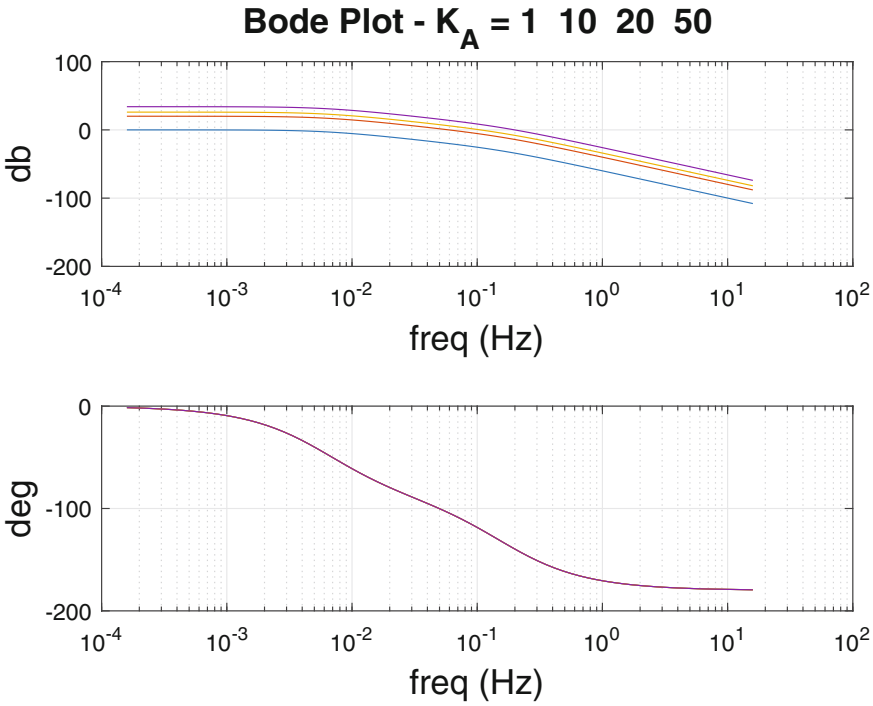

Fig. 4.4 Bode plot

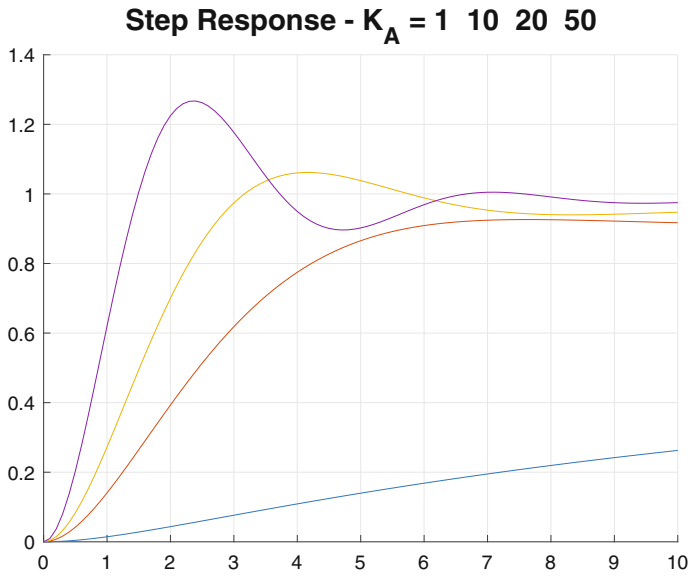

Fig. 4.5 Step response

4.2.2 AVR Tuning—Lag Block

A lag block is used to reduce gain at higher frequencies without reducing the DC gain and that's why it is also known as transient gain reduction block. In the example we have considered above, let us say that we need the steady-state error to be less than 0.5%. A gain $K_A = 500$ will give us a steady-state error of 0.4%. This choice of K_A gives a phase-margin of 25.4° and the cross-over frequency is 42.5 rad s^{-1}. We know that a phase-margin less than 60° is likely to lead to an oscillatory system. To increase the phase-margin at the expense of reducing the bandwidth or the response time one easy way is to use a lag block,

$$\frac{1 + sT_C}{1 + sT_B}, \quad T_B > T_C$$

Block diagram of the closed-loop system with a lag block is shown in Fig. 4.6.

The next design issue is the selection of time constants T_B and T_C. For a 0.25 s rise-time we need the open-loop bandwidth to be approximately 10 rad s^{-1}, i.e., the magnitude of the open-loop gain at 10 rad s^{-1} should be 1. The open-loop gain without the lag block is approximately 20 dB at 10 rad s^{-1} thus we need to choose T_B and T_C such that they result in the pole and zero one decade apart to reduce the gain by 20dB at higher frequencies. To provide a good phase-margin the net phase contribution due to the lag block near the cross-over frequency should be approximately zero. With this, we can choose $T_B = 10$ and a decade below $T_C = 1$. The frequency response of the open-loop system with these parameter values is shown in Fig. 4.7. The step-response of the closed-loop system with and without the lag block is shown in Fig. 4.8. From the figure it is clear that the lag compensator provides damping without affecting the steady-state error.

4.2.3 AVR Tuning—Rate-Feedback

There are many AVRs in practice which use a rate feedback block shown in Fig. 4.9. The system shown in Fig. 4.9 includes a rotating exciter modelled as a first-order block. There are two feedback loops in the system. The first feedback loop has the rate feedback block $\frac{sK_F}{1+sT_F}$ in the feedback path. In this design problem, appropriate values of T_F and K_F need to be chosen where all the other parameters are specified.

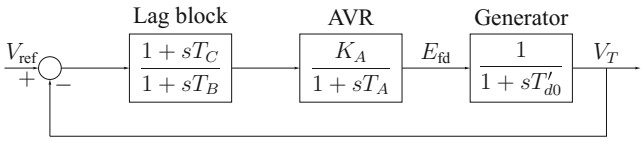

Fig. 4.6 AVR tuning lag compensator

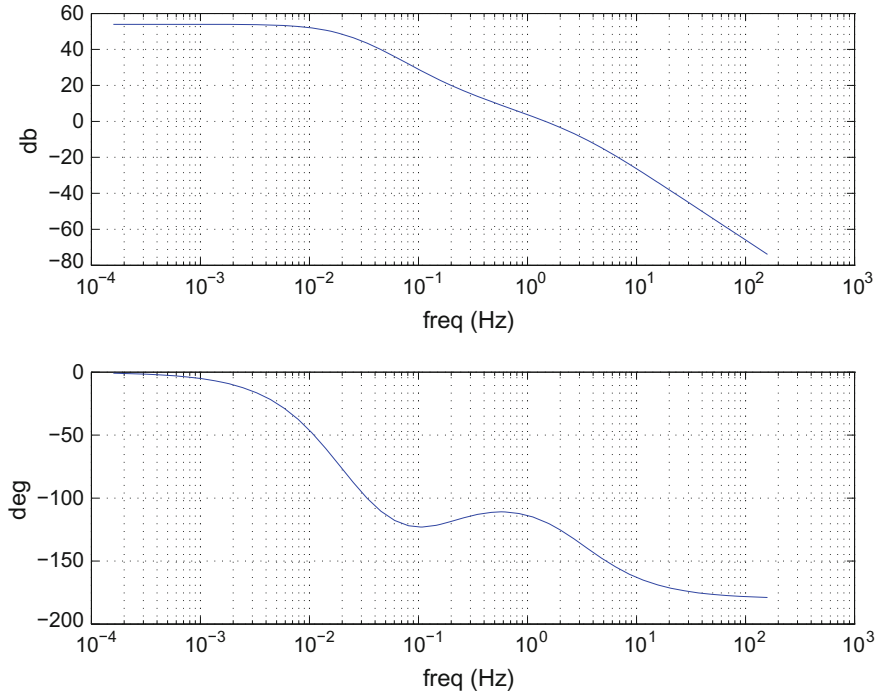

Fig. 4.7 Bode plot with compensator

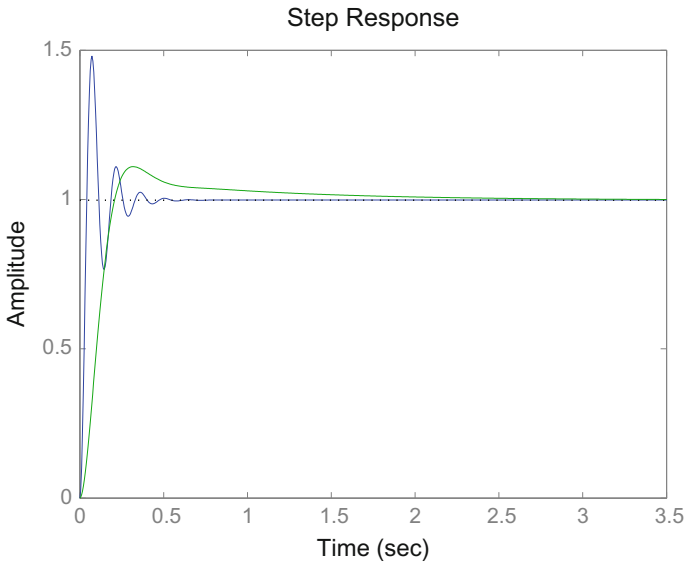

Fig. 4.8 Step-response with and without lag compensator

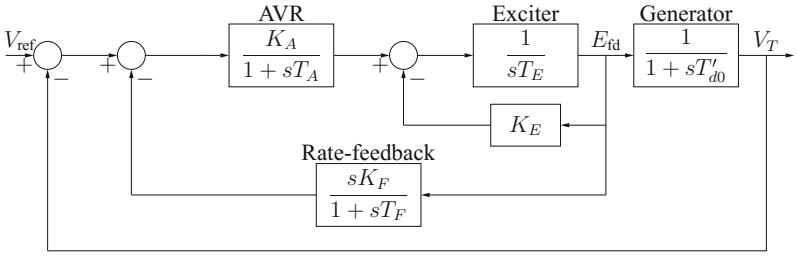

Fig. 4.9 AVR tuning rate-feedback compensator

The design objective is to have a fast response time and a small steady-state error to a step input. Typical parameters are: $K_A = 120$, $T_A = 0.15$, $T_E = 0.5$, $K_E = 1.0$, $T'_{d0} = 5$; in most designs $T_F \approx 10T_A$.

The purpose of the inner loop with rate feedback is to provide high DC gain and reduce high frequency gain to provide stability to the closed-loop system. To see how the inner loop with rate feedback provides this capability let us consider a feedback system with transfer function g in the forward path and h in the feedback path with the closed-loop transfer function $gh_{\text{cl}} = \frac{g}{1+gh}$. Approximate frequency response of the closed-loop will be the same as that of g when $|gh| << 1$ and $\frac{1}{h}$ when $|gh| >> 1$.

The cascade of the exciter and AVR blocks, with transfer function $g = \frac{K_A}{(1+sT_A)(K_E+sT_E)}$, provides a high DC gain of $\frac{K_A}{K_E}$; the first break point is at $\frac{K_E}{T_E}$ rad s^{-1} and the second break point is at $\frac{1}{T_A}$ rad s^{-1}. The rate feedback block, $h = \frac{sK_F}{1+sT_F}$, has a DC gain of $-\infty$, a low frequency reponse of 20 dB/decade, and a break point at $\frac{1}{T_F}$ rad s^{-1}. Since we have $\frac{K_A}{K_E} < \frac{1}{T_F} < \frac{1}{T_A}$, the closed-loop magnitude response for the inner loop is: DC gain of $\frac{K_A}{K_E}$, then -20 dB/decade from $\frac{K_E}{T_E}$ rad s^{-1}, flat from $\frac{1}{T_F}$ rad s^{-1}, and again -20 dB/decade from $\frac{1}{T_A}$ rad s^{-1}. The gain in the flat part is $\frac{T_F}{K_F}$. The frequency response for the inner loop is shown in Fig. 4.10 where the flat section can be clearly seen.

In this design, it is aimed that the open-loop crossover frequency for the entire loop in Fig. 4.9 is in the flat section of the inner loop gain. It is a common practice to have the crossover frequency as the geometric mean of the two end-points of the flat section.

The following steps give the design process.

1. If K_A is not already specified, choose it to satisfy the steady-state error specifications.
2. $T_F \approx 10T_A$
3. Choose $\omega_c = \sqrt{\frac{1}{T_F}\frac{1}{T_A}}$
4. Find the gain which needs to be applied to the generator transfer function such that the crossover is at ω_c. This extra gain $K_{\omega_c} = |1 + \jmath\omega_c T'_{d0}|$.
5. Set $K_F = K_{\omega_c} T_F$

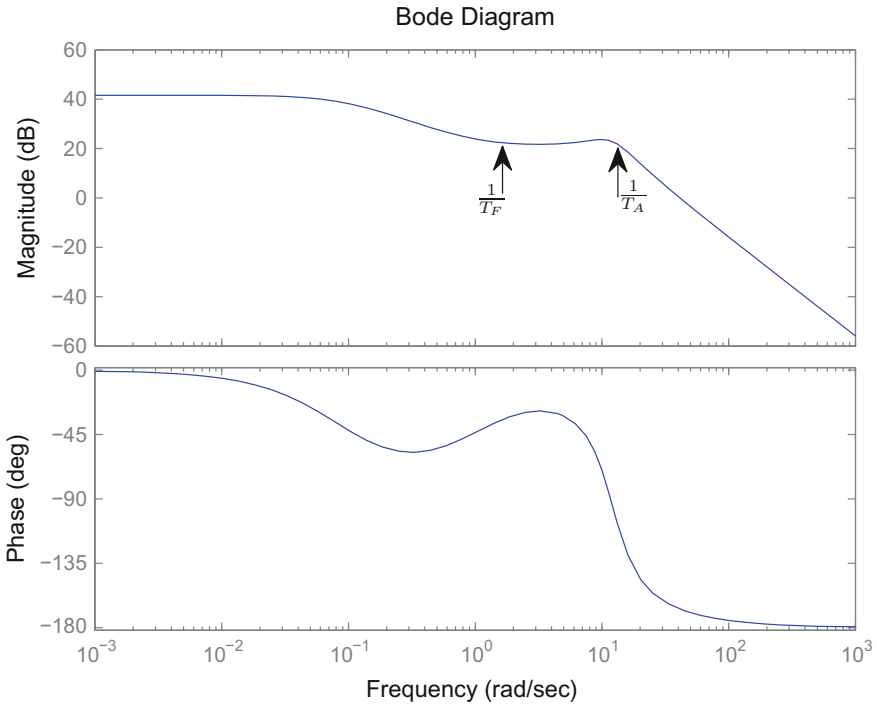

Fig. 4.10 Rate feedback—inner-loop frequency response

Following the above steps we get for the parameters given above $T_F = 1$, and $K_F = 0.0772$. The open-loop frequency response for the entire loop is shown in Fig. 4.11 and the closed-loop step response is shown in Fig. 4.12. From the figures it is clear that the design specifications are met.

4.2.4 AVR Tuning—PID Design

The steady-state error due to a step input with a PID controller is zero. For this reason majority of AVRs have a PID block as a part of the AVR structure. The main design objective with a PID control is to get a fast response with good damping. Fast and a well-damped response is achieved with large open-loop bandwidth and a large phase margin.

Here we illustrate the design of a PID controller using the example of a very popular AVR known as IEEE AC7B compensator shown in Figs. 4.13 and 4.14.

Let us say that the desired open-loop gain crossover frequency is ω_c, which is between 1 and 10 rad s^{-1}, and the desired phase margin is ϕ_d, which is between 60° and 90°.

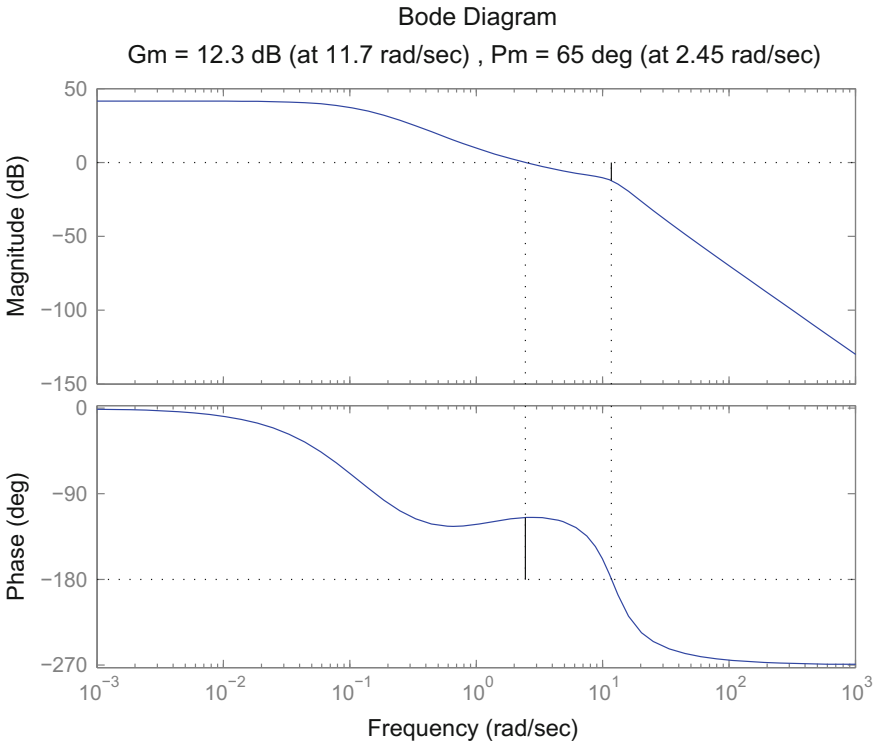

Fig. 4.11 Rate feedback—open-loop frequency response

In the design the following assumptions are made:

1. F_{ex} is unity.
2. In per unit system $I_{\text{fd}} = V_T$.
3. The correction for exciter saturation $V_x = 0$.
4. Either use the PID block $C_R(s)$ or the rate-feedback block ($K_{F3} \neq 0$).
5. $K_P V_T$ is unity.
6. Compensator voltage, $V_C = V_T$, in Fig. 4.13.

Exercise: Redraw the block diagrams in Figs. 4.13 and 4.14 with the above simplifying assumptions. (Hint: the outputs of the shaded boxes in Fig. 4.13 are either 0 or 1.)

The transfer function between X and E_{fd} in Fig. 4.14 is:

$$G_{XE_{\text{fd}}}(s) = \frac{\frac{C_A(s)}{sT_E+K_E}}{1+\frac{K_{F1}C_A(s)}{sT_E+K_E}} \tag{4.2}$$

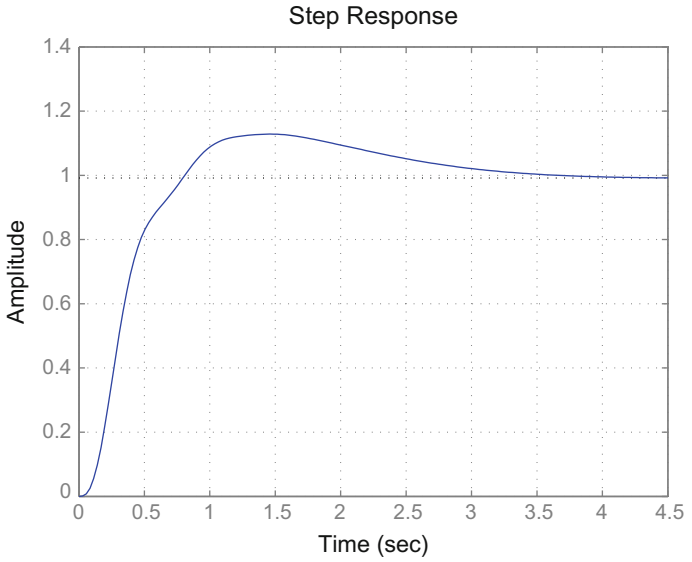

Fig. 4.12 Rate feedback—closed-loop step response

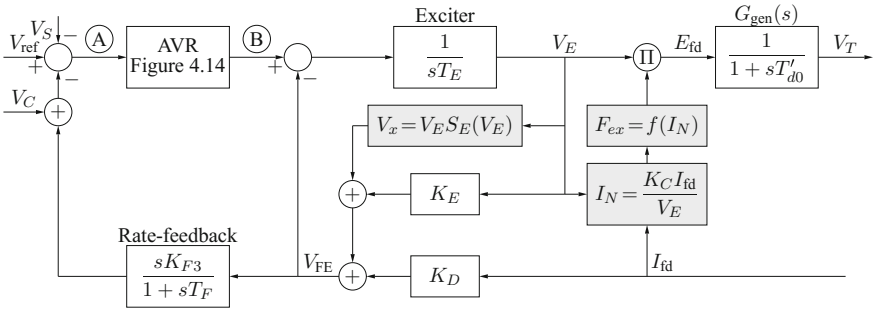

Fig. 4.13 AVR tuning IEEE AC7B compensator—block 1

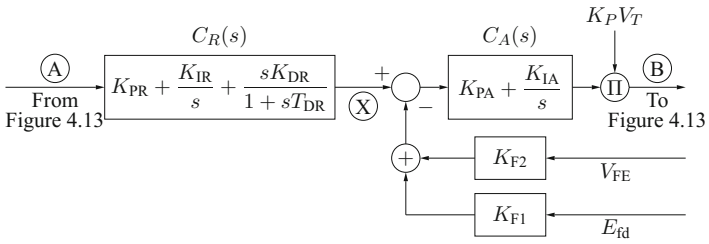

Fig. 4.14 AVR tuning IEEE AC7B compensator—block 2

where the feedback from the K_D block is ignored. Input $K_P V_T$ to the multiplier block in Fig. 4.14 is to account for the main supply to the exciter, which is from the generator terminals. In exciter tuning $K_P V_T$ can be considered as unity.

The first step in the design process is to design for the inner loop. The steps are:

1. Choose the inner loop crossover $\omega_{c_i} = 2\omega_c$.
2. Choose the location of the zero of the PI controller a decade below the crossover frequency, i.e., $\frac{K_{\text{IA}}}{K_{\text{PA}}} = \frac{\omega_{c_i}}{10}$.
3. Choose K_{PA} such that the inner loop crossover frequency is at ω_{c_i}.

The second stage in the design process is to choose controller $C_R(s)$ to achieve the overall bandwidth ω_c and the phase margin ϕ_d. First note that the inner loop transfer function is:

$$G_{\text{in}} = \frac{G_{xE_{\text{fd}}}(s)}{1 + G_{xE_{\text{fd}}}(s) K_D G_{\text{gen}}(s)} \tag{4.3}$$

The open-loop gain then is (with $K_{F3} = 0$):

$$G_{\text{ol}} = C_R(s) G_{\text{in}} \tag{4.4}$$

The controller $C_R(s)$ is written as $C_R(s) = K_x C_{\text{lag}}(s) C_{\text{lead}}(s)$ and

$$C_{\text{lag}}(s) = \frac{\frac{\beta}{\omega_c} s + 1}{s} \text{ and } C_{\text{lead}}(s) = \frac{\frac{s}{\omega_z} + 1}{\frac{s}{\omega_p} + 1} \tag{4.5}$$

The following steps can be used to choose the gains for the PID controller $C_R(s)$.

1. Select $\beta = 10$.
2. Find out the phase margin ϕ with $C_{\text{lag}}(s) G_{\text{in}}$.
3. The extra phase lead ϕ_l needed to achieve the desired phase margin is $\phi_d - \phi$.
4. Choose ω_z, ω_p, and K_x according to Sect. 3.3.7.
5. Equating the co-efficeints of $C_R(s)$ and $K_x C_{\text{lag}}(s)$, we can obtain

$$T_{\text{DR}} = \frac{1}{\omega_p}; \; K_{\text{IR}} = K_x; \; K_{\text{DR}} = \frac{\beta K_{\text{IR}}}{\omega_z \omega_p} - K_{\text{PR}} T_{\text{DR}}; \; K_{\text{PR}} = \left(\frac{\beta}{\omega_c} + \frac{1}{\omega_z} \right) K_{\text{IR}} - K_{\text{IR}} T_{\text{DR}}.$$

Let us look at a system with the following parameters: $K_{F1} = 0.212$, $K_{F2} = 0.0$, $K_{F3} = 0.0$, $T_E = 0.36$, $K_E = 1.0$, $K_C = 0.30$, $K_D = 1.04$, $T_R = 0.01$, $T'_{d0} = 8.9$, $K_E = 1$, $K_D = 0.6$. The controller parameters for $\omega_c = 5\,\text{rad}\,\text{s}^{-1}$ and $\phi_d = 65\%$ are: $K_{\text{PA}} = 17.5366$, $K_{\text{IA}} = 17.5366$, $T_{\text{DR}} = 0.1803$, $K_{\text{PR}} = 11.0192$, $K_{\text{IR}} = 5.3972$, $K_{\text{DR}} = 0.4091$. The open-loop frequency response and the closed-loop step response is shown in Figs. 4.15 and 4.16.

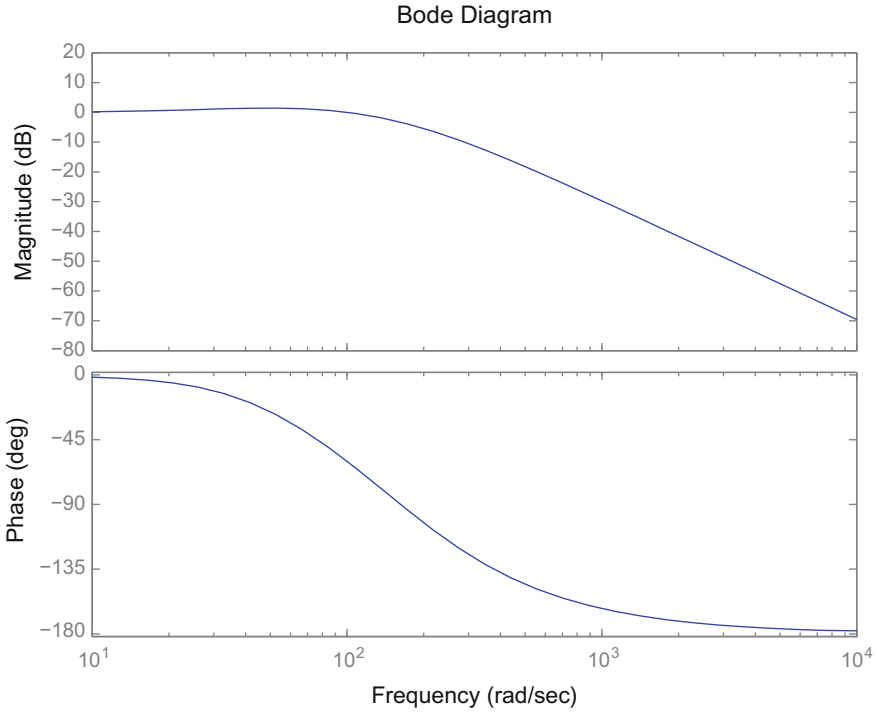

Fig. 4.15 Lead-lag compensator

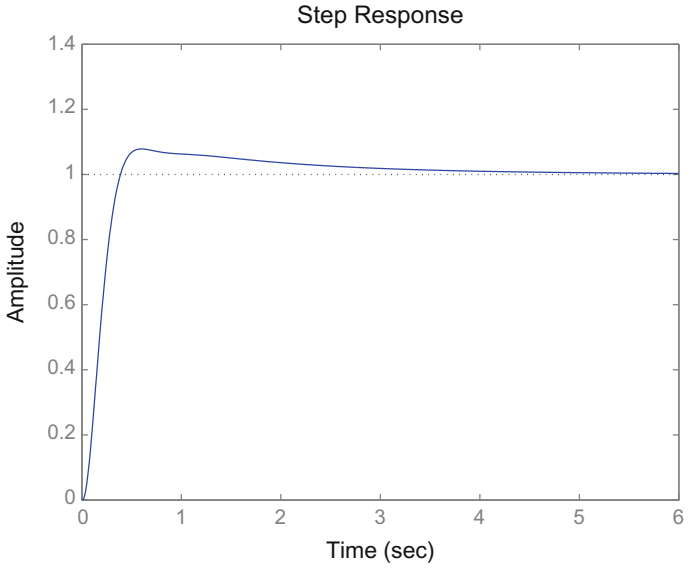

Fig. 4.16 Lead-lag compensator

4.3 AVR Models

All AVRs fall in one of the follwing three categories:

1. DC generator directly connected to the synchronous generator field.
2. AC generator connected to the synchronous generator field via a solid-state rectifier.
3. Solid-state rectifiers supplied from the synchronous terminal voltage and connected to the synchronous generator field.

In the following we look at some of the common features of the exciters so that we can model them appropriately for AVR tuning.

4.3.1 Rotating Exciters

Rotating exciters can be either AC or DC generators. In the literature AC generators are also known as brushless machines [30, 31]. DC generators and alternators still exist as exciters in old generators, but static exciters are becoming common for new generators.

In all rotating exciters there is a field coil and its electrical properties form the most important part of the exciter model. The field voltage supplied to the synchronous generator, E_{fd}, the output of the exciters, is proportional to the total flux linkages, λ in the exciter field coil. For rotating generators we can take it that the generated voltage $E_{\text{fd}} = k_f \omega_{\text{ex}} \lambda$, where ω_{ex} is the exciter angular velocity which can be considered constant, λ are the total flux linkages in the exciter field coil, and k_f is a proportionality constant. Further let $k_\lambda = k_f \omega_{\text{ex}}$, and so we can write $E_{\text{fd}} = k_\lambda \lambda$. Let us first look at the relationship between λ and the applied voltage to the exciter field coil.

4.3.2 Current-Flux Relationship in Coils with Saturation

The modelling of the saturation term can be done in many different ways but the important point to keep in mind is that including the effect of saturation is to include an extra term as shown in Fig. 4.17. Instead of using the exponential function to model saturation, e.g., in Fig. 2.38, some simulations use a quadratic relationship, e.g.,

$$S_e(E_{\text{fd}}) = \frac{B\,(E_{\text{fd}} - A)^2}{E_{\text{fd}}}. \tag{4.6}$$

In general, we are able to write a relationship between exciter field current and synchronous machine field voltage E_{fd} as, $i = E_{\text{fd}}\,(K_E + S_e(E_{\text{fd}}))$.

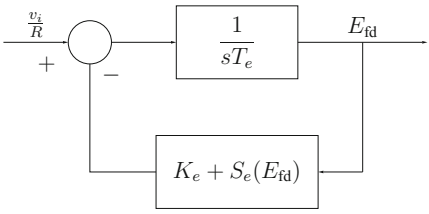

Fig. 4.17 Rotating exciter block diagram

For the exciter field circuit shown in Fig. 2.38, we write

$$\begin{aligned} v_i &= Ri + \frac{d\lambda}{dt} \\ v_i &= RE_{\text{fd}}\left(K_E + S_e(E_{\text{fd}})\right) + \frac{1}{k_\lambda}\frac{dE_{\text{fd}}}{dt} \end{aligned} \tag{4.7}$$

So with $T_e = \frac{1}{Rk_\lambda}$, $K_e = K_E$, we obtain the block diagram in Fig. 4.17 to represent the model in (4.7).

The block diagram in Fig. 4.17 is used to represent field coil in both DC and AC exciters, with suitable adjustments in the parameters T_e and K_e. In excitation systems with only solid-state components, there is a saturable core reactance which is used to control the input to the rectifier and this can be also modelled using the block diagram in Fig. 4.17. Thus this block is a common feature of almost all excitation systems.

4.4 Practical Exciters

In this section we look at two of the popular exciters and see how we can use the methods detailed in this chapter to tune the parameters of these two exciters. These two popular exciters are: an AC machine exciter IEEE AC1A and a solid-state exciter IEEE ST2A. The block diagrams of these two exciters are shown in Figs. 4.19 and 4.20. Let us look at the components in these block diagrams with a view to make assumptions about their dynamics in the AVR tuning process.

4.4.1 AC Exciter

The block diagram for a synchronous machine in Fig. 2.21, with damper windings neglected, can be used to represent a brushless AC exciter as shown in Fig. 4.18. The exciter supplies an inductive load so the terminal voltage, which is the main generator's field voltage E_{fd}, is proportional to E'_q. The block $K_E + S(E'_{\text{fd}})$ in Fig. 4.18 represents the gain adjustment and the extra exciter field current needed due to sat-

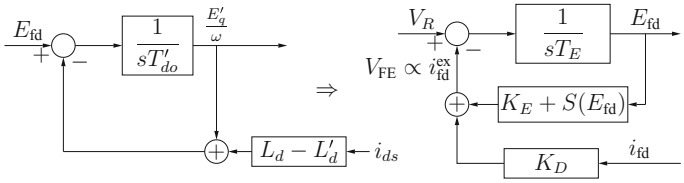

Fig. 4.18 Brushless exciter block diagram

uration. In most cases $K_D = L_d - L'_d$. The input to the integrator block $\frac{1}{sT_E}$ is $\dot{\lambda}^{\text{ex}}_{\text{fd}} = V_R - r^{\text{ex}}_{\text{fd}} i^{\text{ex}}_{\text{fd}}$, where the superscript 'ex' is used for exciter quantities. This means that the quantity being subtracted from V_R in Fig. 4.18 is proportional to the exciter field current. In many exciter control schemes the exciter field current is fedback through a rate block for a faster exciter response.

4.4.2 Rectifier Equivalent Representation

The voltage drop in the rectifier is modelled using the block $f(I_N)$ in Figs. 4.19 and 4.20, which is defined as follows:

$$f(I_N) = \begin{cases} 1 - 0.577 I_N, & I_N < 0.433 \\ \sqrt{0.75 - I_N^2}, & 0.433 < I_N < 0.75 \\ 1.732(1 - I_N), & 0.75 < I_N < 1.0 \\ 0, & I_N > 1. \end{cases} \tag{4.8}$$

The effect of the voltage drop due to the commutating inductance in the system is modelled as a voltage drop as a function of the load current. It can be written as:

$$E_{\text{fd}} = E^0_{\text{fd}} - X_{\text{comm}} I_{\text{fd}} \Rightarrow \frac{E_{\text{fd}}}{E^0_{\text{fd}}} = 1 - \frac{X_{\text{comm}} I_{\text{fd}}}{E^0_{\text{fd}}}$$

where X_{comm} is the effective commutating reactance and the formula in (4.8) models this term. The multiplication block in Fig. 4.19 models this as a gain term due to the rectification process. The block $V_E = |K_P V_T + \jmath K_I I_T|$ in Fig. 4.20 is to compensate voltage drop between the terminal voltage and some other point at which the AVR is designed to regulate the voltage.

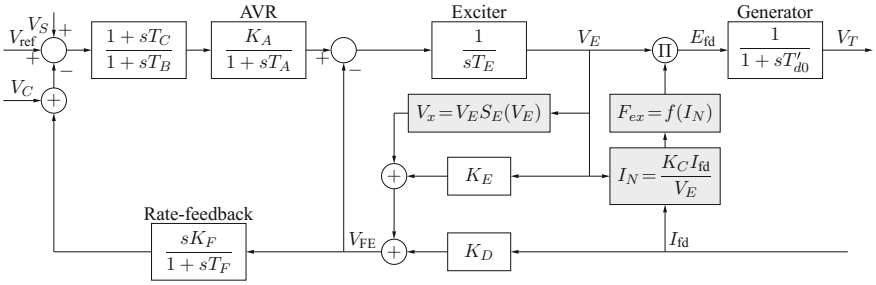

Fig. 4.19 AVR tuning IEEE AC1A compensator

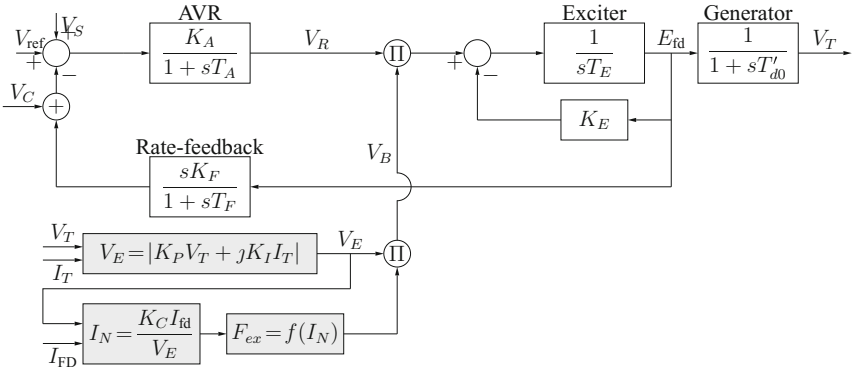

Fig. 4.20 AVR tuning IEEE ST2A compensator

4.4.3 Compensating Voltage V_C and VAR Droop

Details about the compensating voltage V_C in Figs. 4.13, 4.19, and 4.20 are given in [16]. This term is needed to provide a droop for reactive power sharing amongst generators. For a fast exciter without the V_C term,

$$E_{\text{fd}} = K_A\,(V_{\text{ref}} - V_T) \text{ and } Q \approx \frac{E_{\text{fd}} - V_T}{X_s}$$
$$V_T = \frac{K_A V_{\text{ref}}}{1+K_A} - \frac{X_s Q}{1+K_A} \tag{4.9}$$

From (4.9) one can see that for large K_A, the terminal voltage and reactive power output Q are very weakly coupled and regulating V_T will not properly regulate Q. A compensating voltage

$$V_C = |\bar{V}_T + (R_C + \jmath X_C)\,\bar{I}_T|$$

can help with this. The terminal current $I_T = I_P - \jmath I_Q$, where I_P is the current in phase with the terminal voltage V_T. From this one can write for change only in reactive component as,

$$V_T = \frac{K_A V_{\text{ref}}}{1 + K_A} - \frac{(X_s + K_A X_c) I_Q}{1 + K_A} \tag{4.10}$$

where X_c can be selected to provide a reactive power droop or load compensation or several of the other things as suggested in [16]. Voltage V_S in Figs. 4.13, 4.19, and 4.20 is a stablising voltage term (normally the output of a PSS) which can be considered to be zero for AVR tuning.

4.4.4 Assumptions for AVR Tuning

It can be seen that the compensation for loading and rectifier voltage drop is applied as a product term. For the purposes of AVR tuning these values can be assumed to be 1pu and thus removed from the representation for the purposes of design. The block diagrams in Figs. 4.19 and 4.20 are generally simplified with the result that the resulting block diagram takes the form of the block diagram (without the shaded boxes) with either a constant-gain or a lag, or a rate-feedback, or a PID controller. It can be seen that once the product terminals are removed from the block diagrams in Figs. 4.19 and 4.20, it is straightforward to use them to tune AVR parameters.