

COMP22111: Processor Microarchitecture

Stump assembler mnemonics

Listed are the instructions that can be interpreted by the Stump assembler.

Data operations

Stump has 6 different data operations that can be Type 1 or Type 2. An instruction mnemonic appended with S will update the condition code register.

Type 1

```

ADD{S}  <dest>, <srcA>, <srcB> {, shift}
      - dest := (Shifted)srcA + srcB

ADC{S}  <dest>, <srcA>, <srcB> {, shift}
      - dest := (Shifted)srcA + srcB + 1

SUB{S}  <dest>, <srcA>, <srcB> {, shift}
      - dest := (Shifted)srcA - srcB

SBC{S}  <dest>, <RsrcA>, <srcB> {, shift}
      - dest := (Shifted)srcA - srcB - 1 +  $\bar{C}$ 

AND{S}  <dest>, <RsrcA>, <srcB> {, shift}
      - dest := (Shifted)srcA AND srcB

OR{S}   <dest>, <RsrcA>, <srcB> {, shift}
      - dest := (Shifted)srcA OR srcB
  
```

where {, shift} indicates where a shift operation ASR, ROR, or RRC can be appended.

Type 2

```

ADD{S}  <dest>, <srcA>, #<imme>
      - dest := srcA + #<imme>

ADC{S}  <dest>, <srcA>, #<imme>
      - dest := srcA + #<imme> + 1

SUB{S}  <dest>, <srcA>, #<imme>
      - dest := srcA - #<imme>

SBC{S}  <dest>, <srcA>, #<imme>
      - dest := RsrcA - #<imme> + 1 +  $\bar{C}$ 

AND{S}  <dest>, <srcA>, #<imme>
      - dest := srcA AND #<imme>

OR{S}   <dest>, <srcA>, #<imme>
  
```

- $dest := srcA \text{ OR } \#<imme>$

Data pseudo-operations

The following instructions are pseudo instructions that the compiler translates into instructions using the basic Stump instruction set.

- MOV{S} <dest>, <srcB> {, shift}
 - Implemented as ADD{S} <dest>, R0, <srcB> {, shift}

- CMP <srcA>, <srcB> {, shift}
 - Implemented as SUBS R0, <srcA>, <srcB> {, shift}

- TST <srcA>, <srcB> {, shift}
 - Implemented as ANDS R0, <srcA>, <srcB> {, shift}

- MOV{S} <dest>, #<expr>
 - Implemented as ADD{S} <dest>, R0, #<imme>

- CMP <srcA>, #<expr>
 - Implemented as SUBS R0, <srcA>, #<imme>

- TST <srcA>, #<expr>
 - Implemented as ANDS R0, <srcA>, #<imme>

- NOP
 - Possibly implemented as ADD R0, R0, R0

- NEG{S} <dest>, <srcB>
 - Implemented as SUB{S} <dest>, R0, <srcB>

Memory transfers

- LD $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle]$
 - $\text{dest} := \text{mem}[\langle\text{srcA}\rangle]$

- ST $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle]$
 - $\text{mem}[\langle\text{srcA}\rangle] := \text{dest}$

- LD $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle, \#<\text{imme}>]$
 - $\text{dest} := \text{mem}[\langle\text{srcA}\rangle + \#<\text{imme}>]$
 - $<\text{imme}>$ can be a label in which case the address of the label is used (truncated to 5 bits!)

- ST $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle, \#<\text{imme}>]$
 - $\text{mem}[\langle\text{srcA}\rangle + \#<\text{imme}>] := \text{dest}$
 - $<\text{imme}>$ can be a label in which case the address of the label is used (truncated to 5 bits!)

- LD $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle, \langle\text{srcB}\rangle]$
 - $\text{dest} := \text{mem}[\langle\text{srcA}\rangle + \langle\text{srcB}\rangle]$

- ST $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle, \langle\text{srcB}\rangle]$
 - $\text{mem}[\langle\text{srcA}\rangle + \langle\text{srcB}\rangle] := \text{dest}$

- LD $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle, \langle\text{srcB}\rangle, \text{shift}]$
 - $\text{dest} := \text{mem}[(\text{shifted})\langle\text{srcA}\rangle + \langle\text{srcB}\rangle]$

- ST $\langle\text{dest}\rangle, [\langle\text{srcA}\rangle, \langle\text{srcB}\rangle, \text{shift}]$
 - $\text{mem}[(\text{shifted})\langle\text{srcA}\rangle + \langle\text{srcB}\rangle] := \text{dest}$

- LD $\langle\text{dest}\rangle, [\text{R7}, \text{label}]$
 LD $\langle\text{dest}\rangle, \text{label}$
 - perform the same operation, offset from PC

- ST $\langle\text{dest}\rangle, [\text{R7}, \text{label}]$
 ST $\langle\text{dest}\rangle, \text{label}$
 - perform the same operation, offset from PC

Control transfer

```

bal    label      ; Always
b     label      ; Always (alternative)
bra   label      ; Always (alternative)
bnv   label      ; Never (uninteresting)
bhi   label      ; HIgher
bls   label      ; Lower or Same
bcc   label      ; Carry Clear
bcs   label      ; Carry Set
bne   label      ; Not Equal
beq   label      ; EQual
bvc   label      ; oVerflow Clear
bvs   label      ; oVerflow Set
bpl   label      ; PLus (positive)
bmi   label      ; MInus (negative)
bge   label      ; Greater or Equal
blt   label      ; Less Than
bgt   label      ; Greater Than
ble   label      ; Less or Equal

```

If the branch condition satisfied then

```
PC := label
```

Compiler Pre-directives

```

label  EQU  <expr>      ; Set label
ORG   <expr>      ; Origin of next sequence
DEFW  <expr> {, <expr> -}
DATA  <expr> {, <expr> -}

```

Note: DEFW and DATA are the same and allow memory to be reserved for data pointed at by a label, i.e.

```
Pointer  DEFW 0
```

EQU can be used to improve code readability by allowing labels to be used to represent data in the code. As EQU is a pre-compiler directive and will result in the label being substituted with the data value at compile time.