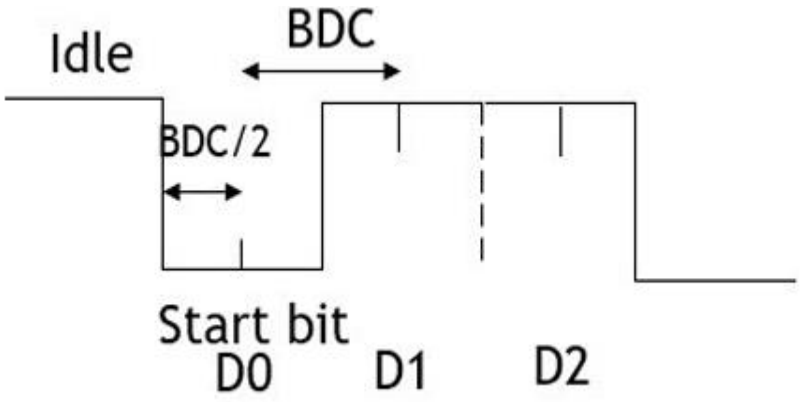
FSM description

- **Idle State:** It will be in this state when reset. It will remain in this state until start bit is not 0.
- **Synchronization State:** wait_counter_enable is high. It will wait in this state until wc is not equal to BDC/2.
- **Receive State:** It will transition from synchronization state to receive state when wc=BDC/2.



Bit_duration_count(BDC)=fclk/Baud Rate

Bit_duration_count(BDC) is the number of cycles required to sample one bit corresponding to the clock of the receiver.
Wait_counter_reset is high.
Bit_counter_enable is high.
Ld_sr (loading the shift register) is high.

- **Check State**: Checking whether bit_index is one or not.
  Shift_right is high
- **R_wait state**: Wait until BDC-1
  Wait_counter_enable is high.
- **Done state**: Data bits is received and write enable is high so data is written into the FIFO.
  Rx_done is high. This signal acts as write enable for fifo.
  Ld_rx is high means loading the received data out from shift register and storing in the fifo.
- **D_wait**: wait in this state until the next start bit comes.