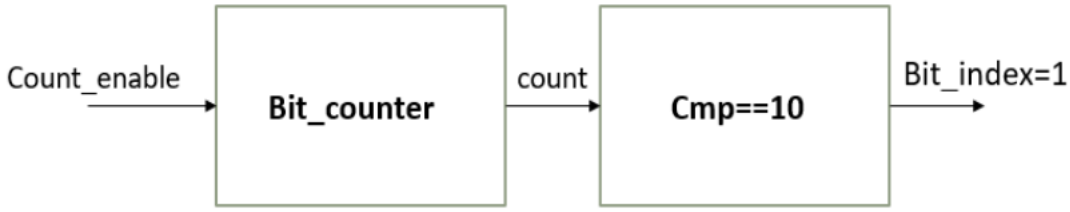
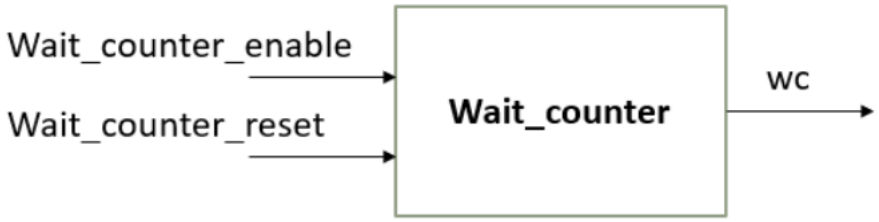
.Datapath Components

- **Bit_counter**



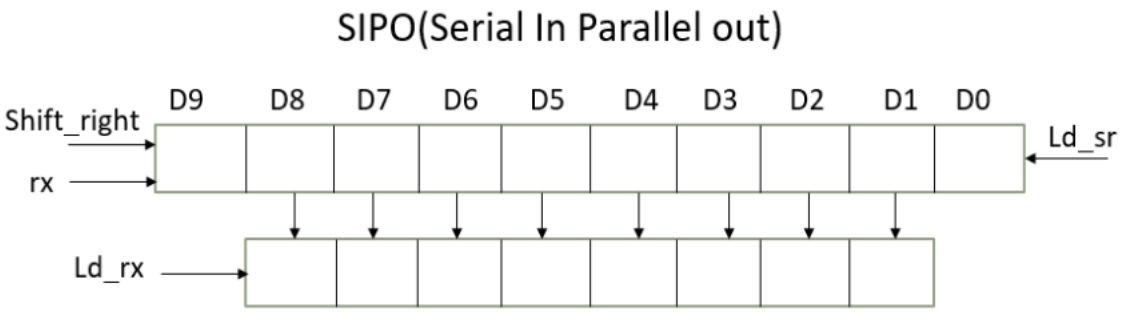
Bit_counter is used to count the number of bits received by the receiver i.e start bit(1 bit)+data bit(8bits)+stop bit(1 bit)=10. If the number of bits is 10 then bit_index is 1 and it means data has been successfully received by the receiver.

- **Wait_counter**



Wait_counter is used to count the number of cycles to sample one bit corresponding to the clock of the receiver

- **SIPO(Serial In Parallel Out)**

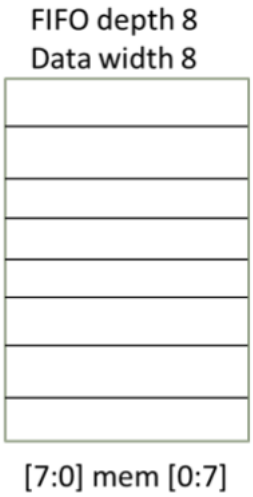


Shift Register is used to store and shift the start bit, data bits and stop bit. When bit_index is high i.e all bits have been received then load the received.Data (ld_rx) is high and 8 bit data bits will be loaded out.

NOTE: The LSB bit is shifted in shift register first then other bits follow.

D0:start bit D1-D8:data bits D9:stop bit

- **FIFO(First In First Out)**



It is required to store the 8 bit data bits sequentially when it has been successfully loaded out of the shift register.