Arpit Sakhreliya

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Education

University of Maryland, College Park, MD — **Aug '24 - May '26 (Expected)**

MEng- Electrical and Computer Engineering — GPA: 3.3/4

Relevant Coursework: Computer Architecture | Compilers and Optimization | FPGA & ASIC Design | CMOS VLSI Design | System Theory.

Gujarat Technological University (GTU), Ahmedabad, India — **Oct '18 - Jul '22**

BE- Electrical Engineering — GPA: 8.5/10

Relevant Coursework: Digital Logic & Microprocessors | Embedded Systems | Computer Networks | Signal Processing | Control Systems.

Work Experience

Teaching Assistant | Computer Organization for Embedded Systems — **Jan '25 - Present**

- Led weekly discussions for 15 students, clarifying MIPS/RISC assembly, ISA design, and microarchitecture concepts.
- Evaluated assignments and mentored four semester-long projects, strengthening student proficiency in embedded systems design.

Embedded Software Engineer | Prayosha Food Services Pvt. Ltd, India — **Apr' 24 - Jun' 24**

- Developed ESP32 firmware integrating Quectel GSM module via UART, enabling stable 4G connectivity for remote devices.
- Designed a binary parsing library for secure UART-based firmware updates, reducing update failure rates by 40%.
- Implemented custom partitioning & rollback mechanisms with ESP-IDF & FreeRTOS, enhancing OTA update reliability by 10%.

Junior Research Fellow | SysIDEA Robotics Lab | IIT Gandhinagar, India — **May '22 - Apr '24**

- Devised a STM32-based control unit and drivetrain for the shoulder joint of the humanoid robot, featuring sensor-less torque estimation and MATLAB interface integration with CAN2.0b.
- Applied Kalman filtering and Recursive Least Squares for motor parameter identification, reducing joint control errors by 25%.
- Developed FPGA-based accelerator (NI-RIO) for dynamic system equation solving & MPC, improving computation speed by 3x.

Projects

FPGA-Based Custom ALU Implementation for Real-Time Signal Processing — Aug '24 - Oct '24

- Designed a 16-bit floating-point ALU on Nexys 4 DDR FPGA using FSMD architecture in Verilog, optimized for fused multiply-add (FMA) units, Kalman filtering, FFT, and matrix multiplication for real-time DSP tasks.
- Formulated a custom instruction set for the ALU accelerator, reducing latency by more than 20% for signal processing.
- Interfaced ATmega328 via UART, enabling low-latency computation offloading to FPGA for real-time robotics applications.

Cache Simulation and Performance Analysis — Oct '24 - Dec '24

- Programmed a trace-driven cache simulator in C, supporting configurable cache size (64B–16MB), block size (16B–16KB), and associativity (1–16 way) with write-back/write-allocate policies.
- Integrated MESI snoopy protocol for multi-core cache coherence and implemented LRU replacement for set-associative caches, monitoring miss rates, replacements, and demand fetches.
- Analyzed SPEC CPU2017 traces to optimize cache configurations, reducing miss rates and access latency.
- leveraged CACTI to evaluate dynamic energy consumption, leakage power, and AMAT for enhanced energy efficiency.

Out-of-Order RISC-V Pipeline Simulator (Tomasulo Algorithm) — Aug '24 - Oct '24

- Developed a cycle-accurate, out-of-order RISC-V processor simulator (RV32I-F ISA) implementing Tomasulo's Algorithm for register renaming, dynamic scheduling, and in-order commit.
- Constructed a seven-stage pipeline with multi-cycle functional units and writeback, resolving structural, data, and control hazards.
- Engineered instruction queue, reorder buffer (ROB), and memory conflict queue for load/store dependency handling and validated performance using benchmark assembly programs.

Honors And Awards

- **May '23:** Acknowledged in *"Event-Driven Intermittent Control"* journal paper for IMU data acquisition system. (Link)
- **Jul '22:** Nidhi Prayas grant of **$8,500** for developing an Analog-Adaptive embedded drive for actuators.
- **Jan '21:** DIC Grant of **$900** for the Adaptive Surface Irrigation System, funded by MHRD.
- **Aug '21:** Robotics team member, ranked 9th in ABU Robocon International competition, Jimo, China.
- **Oct '20:** SSIP Grant of **$1,150** for the Intelligent IoT Pumping System project, funded by the Gujarat Government.

Skills

Programming Languages: C, C++, Verilog, Python, Assembly.
Software/Tools: Vivado, Cadence, Linux, Altium, Keil, STM32CubeIDE, MATLAB, Multisim, LabVIEW, ThingWorx, Kepware.
Libraries & protocols: OpenCV, PyTorch, Pandas, NumPy, RS-485, Ethercat, MQTT, C-make, SPI, I2C, UART, CAN, TCP, UDP.