Arpit Sakhreliya

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Education

MEng. Electrical and Computer Engineering, University of Maryland, College Park **August 2024-Exp. May 2026**
Courses: Computer Architecture | CMOS VLSI Design | Advanced Embedded System Design | Compilers and Optimization GPA: 3.3/4

BE Electrical Engineering, Gujarat Technological University, Ahmedabad, India **October 2018-July 2022**
Courses: Analog and Digital Logic | Semiconductor Devices and Technology | Signal Processing | Embedded Systems GPA: 8.5/10

Professional Summary

VLSI engineer and computer architect with hands-on experience in RTL design, FPGA-based verification, ASIC design synthesis, static timing analysis, and power optimization. Proficient in Verilog/SystemVerilog, UVM, and Cadence tools. Developed FPGA-based floating-point ALU and out-of-order RISC-V pipelines at the cycle-accurate level. Secured multiple competitive research grants and served as a teaching assistant for computer organization and microarchitecture fundamentals. Eager to contribute to innovative projects and advance silicon technology.

Skills

HDL & Design: Verilog, VHDL, RTL design, synthesis, timing and waveform analysis, and UVM methodology.
Programming & Modeling: C/C++, Python, Assembly, FSM/FSMD, Microarchitecture Simulation, Power Analysis & Optimization.
Platforms & Tools: Vivado, Spectre, Cadence, CACTI, Synopsys Design Compiler, Linux, Matlab & Simulink, LTspice, LabVIEW.
Interfaces & Protocols: AXI, AHB, APB, UART, SPI, I2C, TCP/IP, CAN, RS-485, JTAG, Ethernet.

Work Experience

Teaching Assistant | Computer Organization for Embedded Systems | UMD **January 2025-June 2025**
- Instructed 20 students in weekly sessions covering MIPS, datapaths, cache coherence, pipelining, and microarchitecture concepts.
- Mentored and evaluated four semester-long student projects on topics including custom instruction encoding, data paths, and cache.

Embedded Software Engineer | Prayosha Food Services Pvt. Ltd., India **April 2024-June 2024**
- Devised UART-based ESP32 (Xtensa SoC) firmware to interface with Quectel EC25, enabling 4G telemetry for remote devices.
- Designed a lightweight binary parsing cpp library for secure UART-based firmware updates, reducing update failure rates by 40%.
- Implemented custom partitioning & rollback mechanisms with ESP-IDF & FreeRTOS, enhancing OTA update reliability by 10%.

Junior Research Fellow | SysIDEA Robotics Lab | IIT Gandhinagar, India **October 2021-April 2024**
- Designed and implemented pipelined control logic in **NI-LabVIEW** for a multi-rate real-time BLDC actuator system on **SB-RIO FPGA**, achieving 30 kHz inner current and 5 kHz outer position loops with synchronized sensor feedback and actuator.
- Created fixed-point datapaths for Kalman filter, disturbance observer, and cost-optimization algorithms on SB-RIO, achieving sub-microsecond latency and meeting 40 MHz timing closure through pipelined time-critical datapath optimization.
- Developed a **20 kHz real-time IMU acquisition system** over **TCP/IP** using **STM32 and lwIP**, enabling low-latency data capture for human balance research; **acknowledged** in a peer-reviewed journal paper, *"Event-Driven Intermittent Control"* (Link).

Projects

Multiply-Accumulate (MAC) Unit Design | Cadence Virtuoso @ 14nm | Spectre **January 2025-May 2025**
- Devised a MAC unit for neural network acceleration, comprising a 6-bit unsigned Dadda multiplier and 10-bit Kogge-Stone adder; incorporated a 19-bit synchronous register file with D flip-flops to enable pipelined accumulation and high-throughput computation.
- Modeled a 14 nm CMOS transistor-level schematic in Cadence Virtuoso, applying pass-transistor logic, sizing, and logical effort modeling to minimize critical-path delay, reduce dynamic power, and optimize area while balancing drive strength across stages.
- Performed transient and corner simulations using Cadence Spectre to validate timing and power; achieved worst-case delay of 899 ps at 3 V and dynamic power of 0.648 mW, timing closure and functional correctness for ASIC tape-out readiness.

FPGA-Based Custom ALU & Systolic-Array Edge Accelerator | Xilinx Vivado **August 2024-October 2024**
- Constructed a 16-bit floating-point ALU on Nexys 4 DDR FPGA using FSMD architecture in Verilog, optimized for fused multiply-add (FMA) units, Kalman filtering, FFT, and 4x4 systolic array multiplier for low-latency edge ML classifications.
- Formulated a custom instruction set for the FPGA accelerator, reducing latency from 5 ms to around 3.8 ms for signal processing.
- Unified FPGA-based accelerator with STM32 over UART, offloading compute-intensive tasks with sub-10 ms round-trip latency.

Out-of-Order RISC-V Pipeline Simulator (Tomasulo Algorithm) **August 2024-October 2024**
- Simulated a cycle-accurate out-of-order processor simulator for the RV32I-F ISA using Tomasulo's Algorithm, incorporating register renaming, dynamic instruction scheduling, out-of-order issues, and in-order commit across a seven-stage pipeline.
- Engineered a centralized instruction queue (IQ), reorder buffer (ROB), and memory conflict queue (CQ) with address-based disambiguation to enforce store-load ordering, manage data/control hazards, and optimize instruction throughput within the pipeline.
- Integrated multi-cycle functional units and a shared writeback port for efficient resource utilization; validated simulation accuracy and performance using custom benchmark programs and trace-matching techniques to ensure execution correctness.

Cache Simulation and Performance Analysis (MESI coherence protocol, CACTI) **August 2024-October 2024**
- Engineered a trace-driven cache simulator in C, optimizing cache configurations (size, associativity, block size) and analyzing performance on SPEC CPU2017 benchmarks (MCF, NAMD, XZ) using metrics such as hit rates, miss penalties, and cache latency.
- Integrated MESI snoopy cache coherence protocol across multiple cores, enabling efficient state transitions, invalidations, and coherence tracking. Applied LRU replacement policy for set-associative caches and tracked miss rates and demand fetches.
- Characterized cache architectures with CACTI, evaluating dynamic energy, leakage power, access latency, cache associativity, and average memory access time (AMAT); conducted energy-delay product analysis to balance energy efficiency and performance.