EXPERIMENT No. 01

A. Aim: To analyze and design a resistive network.

B. Apparatus Used: 1. CRO, DC Power supply, breadboard.
2. Resistor R1, R2, R3, R4, (….KΩ), Potentiometer VR (….KΩ),

C. Theory: In electronics we deal with electrons and electricity produced by the movement of electrons from one point to another between two different voltage sources, so by controlling these electrons, we can control voltage and current at any node among the circuit. The resistor is an essential component that uses for this purpose. It's opposes the flow of charge across it and with the help of *Ohm's law* value of output current can be calculated easily. By connecting two or more resistances in series, voltage can be reduced in the desired value.

Study a Resistor:-

Resistors are usually classified according to the following three properties.

i. Composition (e.g. carbon granule, carbon film, wire wound etc.)
ii. Power rating (e.g. 1/8 W, 1/4 W etc.)
iii. Tolerance (e.g. No Color-20 %,Silver-10%,Gold-5%,Brown-1%,Red-2% etc.)

Each resistor has two main characteristics:

1. Its resistance value in ohms
2. Its power dissipating capacity in watts

Power ratings are obtained from the manufacturer's specification sheet. Tolerance is usually indicated on the resistor itself along with the value of the resistance. The value and the tolerance, unless printed on the resistor, are decoded by the printed colored bands. The 1st and 2nd band gives the significant digits and the 3rd band gives the number of zeros to the right of the two significant digits. The ten colors denoting the 0-9 are the following black (0),brown (1), red (2), orange (3), yellow (4), green (5), blue (6), violet (7), grey (8), white (9). The 4th band indicates the tolerance. A golden band indicates the tolerance of 5% and a silver band indicates a tolerance of 10% absence of the 4th band implies a tolerance of 20% a brown band indicates 1% tolerance.

Definitions:-

Component: **-** A device with two or more terminals into which, or out of which, charge may flow.

Node: **-** A point at which terminals of more than two components are joined. A conductor with a substantially zero resistance is considered to be a node for the purpose of analysis.

Branch: **-** The component which joins two nodes.

Mesh: **-** A group of branches within a network joined so as to form a complete loop.

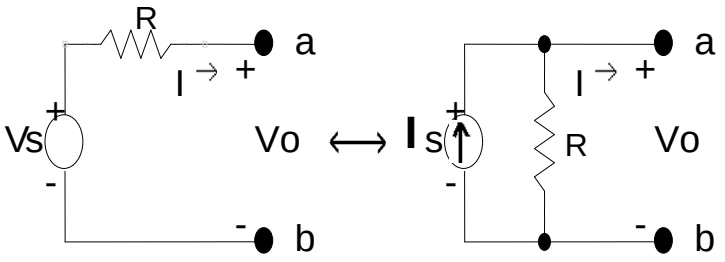
Circuit: **-** An electronic circuit is composed of individual electronic components, such as resistors, transistors, capacitors, inductors and diodes, connected by conductive wires or traces through which electric current can flow. The combination of components and wires allows various simple and complex operations to be performed: signals can be amplified, computations can be performed, and data can be moved from one place to another.

Equivalent circuits: **-** An equivalent circuit refers to a theoretical circuit that retains all of the electrical characteristics of a given circuit. Often, an equivalent circuit is sought that simplifies calculations, and more broadly, that is a simplest form of a more complex circuit in order to aid analysis.

Source transformation: - A generator with internal impedance (i.e. non-ideal generator) can be represented as an ideal voltage generator or an ideal current generator plus the impedance. These two forms are equivalent and the transformation is given below. If the two networks are equivalent with respect to terminals ab (Figure 1.0), then V and I must be identical for both networks. Thus,

$$V_S = I_S R \text{ or } I_S = \frac{V_S}{R}$$

Figure 1.0



- ***Norton's theorem*** states that any two-terminal network can be reduced to an ideal current generator and parallel impedance.
- ***Thevenin's theorem*** states that any two-terminal network can be reduced to an ideal voltage generator plus series impedance.

Figure 1.1

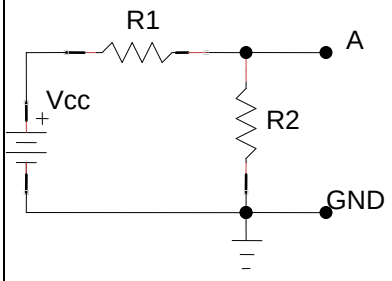


Figure 1.2

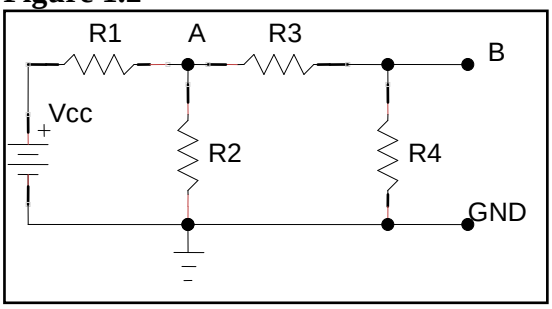


Figure 1.3

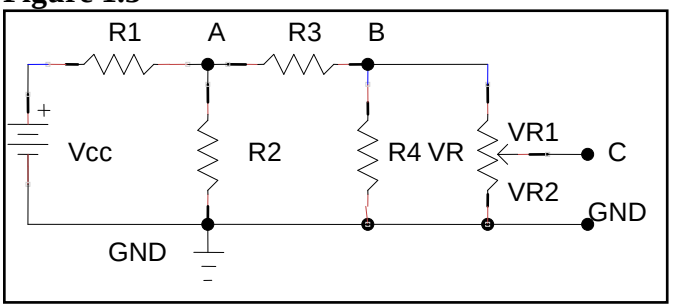


Figure 1.1: Calculate and measure the value of voltage between A and GND.
Figure 1.2: Calculate and also measure the value of the voltage at B.
Figure 1.3: Given a potentiometer as shown in the circuit diagram, measure its value to get the (select any voltage at its capability) and find the values of VR1 and VR2.
$\mathbf{V_C}$ = +.....**V**.
(Take these readings for an AC 12 V_{RMS} also.)

D. Procedure: ***Exercise 1:-*** Connect two resistors (R1 & R2) back to back on a breadboard and + 12 Volt across R1 and R2, connect the CRO probe for voltage measurement.

Exercise 2:- Connect R3 and R4 as given in figure 1.2, connect the CRO probe as required for voltage measurement.

Exercise 3:- Connect POT (Potentiometer/Variable resistor, VR) as given in Figure 1.3 and rotate the shaft to adjust the resistance of POT to obtain predetermined voltage.

E. Observation*: (Include your own Table relevant to the Experiment)*

For DC Voltage:-

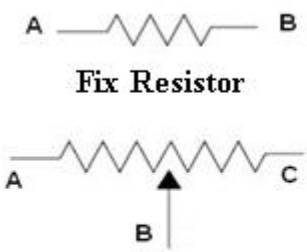
Independent Variable (Unit)	Value variable (Unit)
V_A	
V_B	
V_C	
VR1 (Variable Resisor1)	
VR2 (Variable Resisor2)	

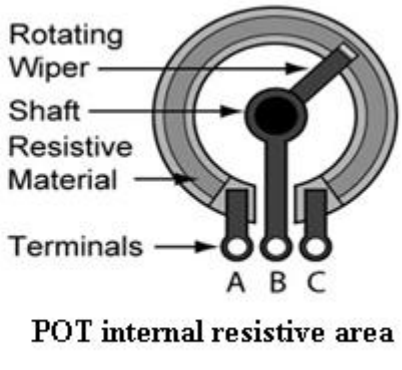
For AC Voltage:-

Independent Variable (Unit)	Value variable (Unit)
V_A	
V_B	
V_C	
VR1	
VR2	

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)





G. Conclusions: *This practical practice helps us to understand:*

- Making of a circuit with circuit elements.
- Ohm's law, Norton and Thevenin's theorem.
- Source transformation.
- Voltage and current measurement with CRO.

Precautions:

1. Always connect Vcc to positive rail and GND to the negative rail in the breadboard.
2. Do not short positive and negative terminal each other.

3. The observation should be taken properly.
4. Do not try to sabotage the equipment by pressing or rotating unknown buttons.

Approved By: Prepared By:

(HOD ECE) (Lab Instructor)

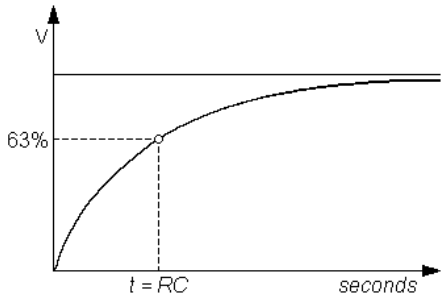
EXPERIMENT No. 02

A. Aim: To analyze and study the time response of RC and RL circuits.

B. Apparatus Used: 1. CRO, DC Power Supply, function generator, breadboard. Resistor 10KΩ (1), Capacitor 0.01µF (1), Inductor 1mH (1).

C. Theory: If a sinusoidal voltage is applied to a capacitor, of value C, through a resistance of value R, the voltage across the capacitor rises slowly. The time constant is defined as the time it will take to charge to 63.21% of the final voltage value.

Graph between voltage and the charging time.



Formula for time constant (T= RC) This value is derived from the mathematical constant *e*, specifically $1 - e^{-1}$, more specifically as voltage to charge the capacitor versus time

Charging , $\mathbf{V_C (t) = V (1- e^{- t / \tau})}$, = 0.63**V**

Discharging , $\mathbf{V_C (t) = V (e^{- t / \tau})}$, = 0.37**V**

V_C (t) = Voltage across the capacitor, V = Supply voltage.

After a period equivalent to 4 time constants, (4T) the capacitor in this RC charging circuit is virtually fully charged and the voltage across the capacitor is now approx 99% of its maximum value, 0.99Vs. The time period taken for the capacitor to reach this 4T point is known as the *Transient Period:*. After a time of 5T the capacitor is now fully charged and the voltage across the capacitor, (VC) is equal to the supply voltage, (Vs). As the capacitor is fully charged no more current flows in the circuit. The time period after this 5T point is known as the *Steady State Period*.

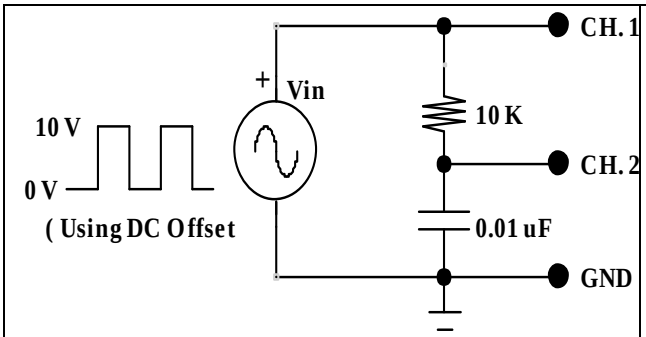


Figure 1.1: Integrator circuit

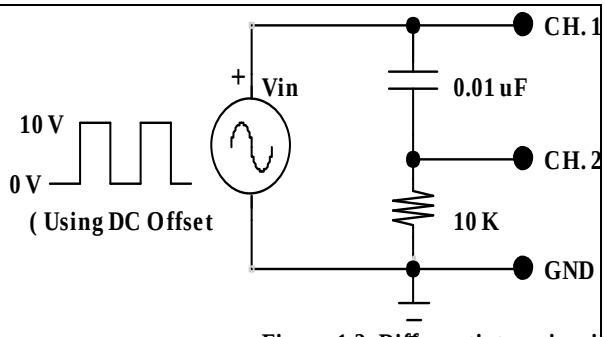


Figure 1.2: Differentiater circuit

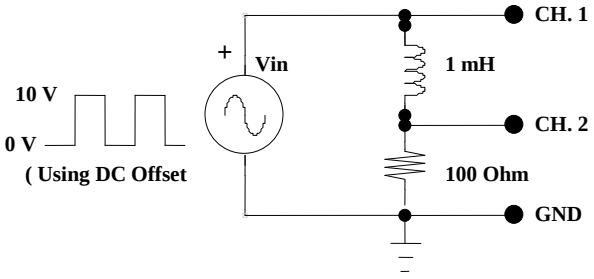


Figure 1.3: Series RL circuit

D. Procedure:

Exercise 1:- *STEP RESPONSE OF AN INTEGRATOR CIRCUIT:-*

Wire the circuit of figure 1.1. Connect the output of the function generator (FG) to the RC circuit and also the CH-1 input of the CRO. Choose a square wave signal. Adjust the amplitude control of the FG to obtain a waveform of 10V peak to peak (0-10). Connect the output of the RC circuit to the CH-2 input of the CRO (in DC Mode).

(i) Step response when T/2<<5τ; Choose the waveform frequency (f) to be 40 KHz. Observe and sketch V_i and V_o w.r.t. time. Note down the salient features of V_o.

Choose any two convenient points on the rising or falling part of V_o and measure the corresponding voltages and the time interval. Calculated (τ =RC) and compare the results with the values used.

(ii) Step response when $T/2 = 5\tau$. Choose f = 1 KHz. Adjust the input signal frequency slightly, if necessary, to satisfy $T/2 = 5\tau$. Observe and sketch V_i and V_o.

(iii) Step response when $T/2 >> 5\tau$: Choose f = 500Hz. Observe and sketch V_i and V_o.

Exercise 2:-*STEP RESPONSE OF A RC DIFFERENTIATOR CIRCUIT:*

Wire the circuit of fig.2. As in the case of RC integrator, Obtain step response of the RC circuit for the following three cases. Sketch V_i and V_o of each case.

1. Step response when $T/2 << 5\tau$.

2. Step response when $T/2 = 5\tau$.

3. Step response when $T/2 >> 5\tau$.

4. Increase the input signal frequency beyond 40 KHz and note the minimum frequency at which the linear tilt (drop) seen in the *Vo* waveform is negligible.

In case of charging V_{in} = Initial voltage at the start of charging, V_F = Supply voltage (p-p).

In case of discharging ; V_{in} = Initial voltage at the start of discharging, , V_F = 0.

Exercise 3:-*STEP RESPONSE OF RL CIRCUITS: (τ = –):*

Wire the RL circuit of Fig. 3. Keep the amplitude control of the FG as in the previous cases. Observe the step response when T/2<<5τ. The inductor given to you has nominal values of 1mH. Adjust the frequency of the input signal in such a way that the maximum V_o *and* amplitude is well below its steady-state value. Choose any two convenient points on the rising and falling parts of V_o and calculate it. Note down the signal frequency.

$$I_c(t) = I_{in} + (I_F - I_{in})$$

E. Observation: *(Include your own Table relevant to the Experiment)*

For Integrator circuit :-

Input Frequency (Hz)	Value of **"τ"**
40 KHz (Square wave, 0-10 Volt)	
1 KHz (Square wave, 0-10 Volt)	
500Hz (Square wave, 0-10 Volt)	

For Differentiator circuit :-

Input Frequency (Hz)	Value of **"τ"**
40 KHz (Square wave, 0-10 Volt)	
1 KHz (Square wave, 0-10 Volt)	
500Hz (Square wave, 0-10 Volt)	

For RL circuit:-

Input Frequency (Hz)	Value of **"τ"**
40 KHz (Square wave, 0-10 Volt)	
1 KHz (Square wave, 0-10 Volt)	
500Hz (Square wave, 0-10 Volt)	

(Adjust input voltage after connecting FG to RL circuit)

F. Analysis of Results:- *(Include sample calculations/Display/plot/typical graph)*

○ Also draw the input and output frequency at each frequency division with indicating t1, t2 and v1, v2 on the observation sheet.

G. Conclusions: *This practical practice helps us to understand:*

○ Making of a circuit with circuit elements.
○ Behavior of a signal passing through an RC circuit.
○ Time constant and its usefulness.
○ Voltage and current measurement with CRO.

Precautions:

1. Always connect Vcc to positive rail and GND to the negative rail in the breadboard.
2. Do not short positive and negative terminal each other.
3. The observation should be taken properly.
4. If possible draw the waveform on plain paper/ rough notebook with time and voltages.

Approved By: Prepared By:

(HOD ECE) (Lab Instructor)

EXPERIMENT No. : 03

A. Aim: To analyze and study the frequency response of RC and RL circuit.

B. Apparatus Used: 1. CRO, DC Power Supply, Function Generator, Breadboard.
2. Resistor 10KΩ (1), Capacitor 0.01μF (1), Inductor 1mH (1)

C. Theory: RC and RL circuits are often used in electronics circuits to achieve frequency selection. For example RC and RL filters that are commonly used to pass a certain band of frequencies and to stop (attenuate) another band of frequencies. For applications such as the above, frequency responses are important. The aim of this experiment is to study the frequency response characteristics of some of the commonly used RC and RL circuits. For this purpose sinusoidal signals are applied to the inputs of these circuits and their output responses are observed and then compared with theory.

Figure 3.1: RC Low Pass Circuit:-

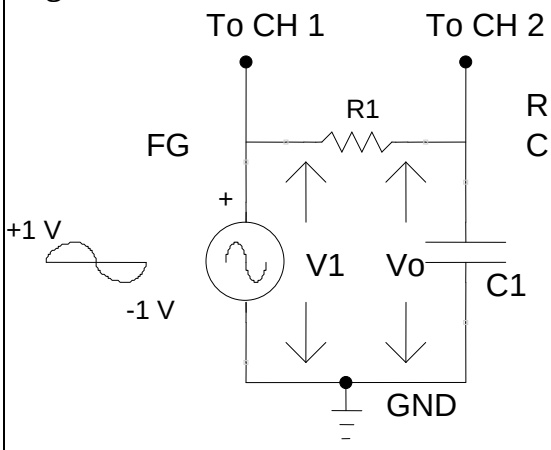


Figure 3.2: RC Low Pass Circuit:-

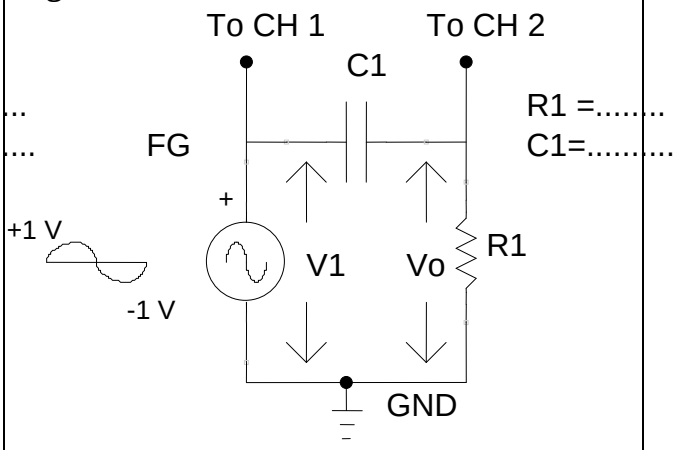


Figure 3.3: RL Low Pass Circuit:-

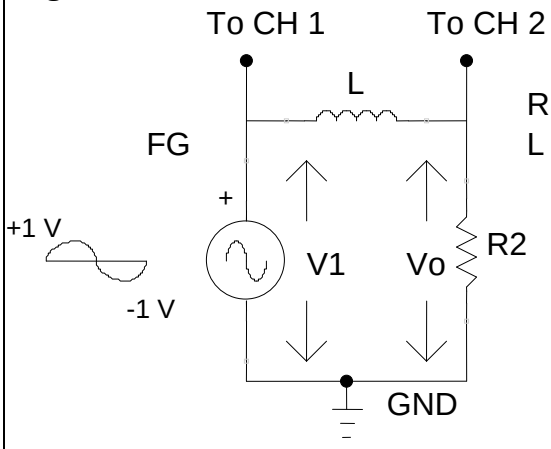
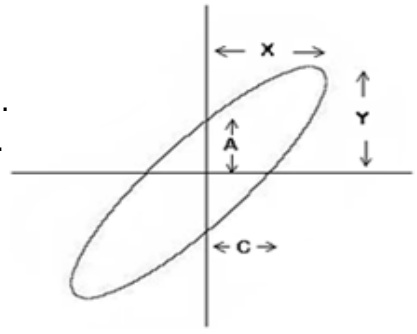


Figure 3.4: Phase measurement.



A = Ysinφ
C= Xsinφ

(Lissajous pattern)

If input is a sine wave, then the output also is a sine wave, but with a different amplitude and phase shift. Gain and output amplitude may be calculated with the following formulas,

The gain of an RC circuit is = ——— **,**

Magnitude of output waveform =——— and

Phase shift = - arctan —— **.**

D. Procedure: ***Exercise 1:-*** *Frequency Response of RC Circuits:* Wire the RC low pass circuit of figure 3.1. Set up the function generator to produce a sine wave of amplitude of 2 V peak to peak (-1 V to +1 V). Connect V_1 to CH. 1 and V_O to CH. 2 of the CRO.

For several frequencies from about 100 Hz to 40 KHz, measure the gain — (take more reading around the -3db points), for each of these frequencies. Plot the frequency response G *(f)* = $20log\left(—\right)$ versus *f* on a semi log graph paper. Measure the -3db frequency f_c. Calculate F_C =—— using the given R and C values. Compare this $\boldsymbol{f_c}$ with the measured value.

Exercise 2:- Lissajous pattern:- Display the X-Y points of the two waveforms $\boldsymbol{V_i}$ **(t)** and $\boldsymbol{V_o}$ **(t)**. Keep the sensitivities of both CH1 and CH2 of the CRO to be the same. Ensure that when CH. 1 and CH. 2 are put to GND. The X-Y plot appears as a dot exactly at the center of the CRO (origin).

Vary the frequency of the sine wave supplied and observe the shape of the Lissajous pattern. A sample Lissajous pattern is shown in figure1.2. Measure the X coordinates C and X (and Y).

Coordinate A and Y, as a cross check for three frequencies $<<f_c$, $f = f_c$ and $f>>f_c$.
Calculate ' j ' from the relationship C = X sin j, and a = Y sin j. Comment on the changes in the shape of the ellipse observed on the CRO.
Exercise 3: RC High pass network: - Wire the RC high pass of figure1.3. Repeat exercise **(1)** and **(2)**. Use the same 10KΩ and 0.01 μF.

Exercise 3:- *Frequency Response of RL circuits:-* Wire the RL low pass circuit of figure 1.4. Repeat exercise (1) and (2).

A. E. Observation*: (Include your own Table relevant to the Experiment)*
RC Low pass filter

Frequency	V_I	V_O	Gain	Gain(dB)
1. 100 Hz				
….				
15. 40 KHz				

RC High pass filter

Frequency	V_I	V_O	Gain	Gain(db)
1.100 Hz				
….				
15. 40 KHz				

RL Low pass filter

Frequency	V_I	V_O	Gain	Gain(db)
1. 100 Hz				
….				
15. 40 KHz				

(Divide this frequency range to create the best graph and take more reading at about cut off point)

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

G. Conclusions: *This practical practice helps us to understand:*

- Relation between frequency and impedance of a RC and RL circuit.
- Measuring of phase difference with the help of CRO and Lissajous pattern.
- Low pass and high pass circuit working.

Precautions:

1. Use separate zero voltage label for both channels if visualized both channel at the same time.
2. Take more reading at the nearer of the cutoff frequency.
3. At the time of creating Lissajous pattern Volts/Div of both channels of CRO should be equal.
4. Reduce the CRO intensity if the dot is much brighter, to avoid damage of the screen

Approved By: Prepared By:

(HOD ECE) (Lab Instructor)

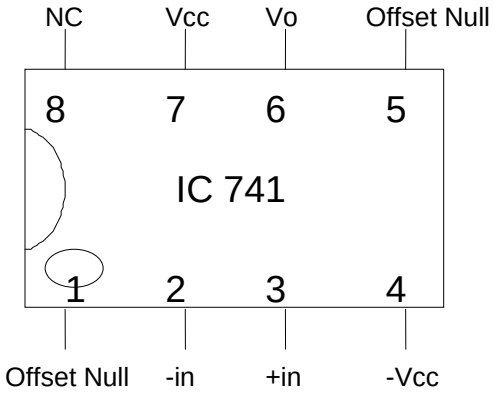
EXPERIMENT No. : 04

A. Aim: To design and analyzing of an inverting and non- inverting mode amplifier using operation amplifier.

B. Apparatus Used: 1. CRO, Function generator, breadboard, DC Power supply.
2. IC Op-Amp (1), resistor R1 (1), resistor R2(1),

C. Theory: An operational amplifier (operational amplifier) is a DC coupled high gain electronic voltage amplifier with a differential input and, usually a single ended output. In this configuration, an op-amp produces an output potential (relative to circuit ground) that is typically hundreds of thousands of times larger than the potential difference between its input terminals.

Figure 4.0:



Pin configuration of Op Amp 741

Pin no. 1:- To adjust offset Null.
Pin no. 2:- Inverting input.
Pin no. 3:- Non inverting input.
Pin no. 4:- Negative supply (-12Vcc) pin.
Pin no. 5:- To adjust offset Null.
Pin no. 6:- Output terminal.
Pin no. 7:- Positive supply (+12Vcc) pin.
Pin no. 8:- Not connected.

Figure 4.1: Inverting mode amplifier (Low pass Amplifier

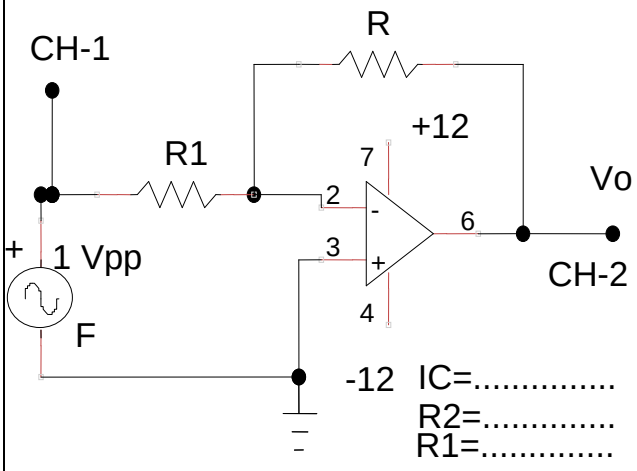
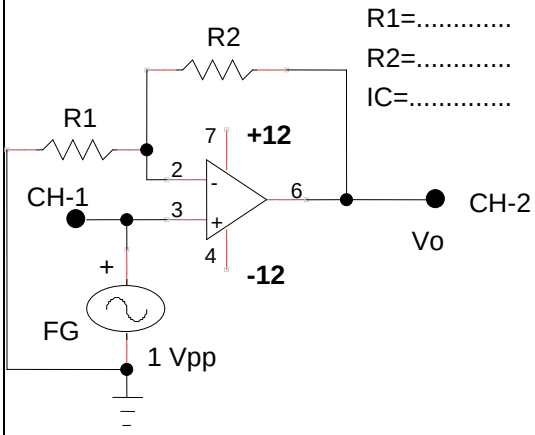


Figure 4.2: Non inverting mode amplifier (Low pass Amplifier



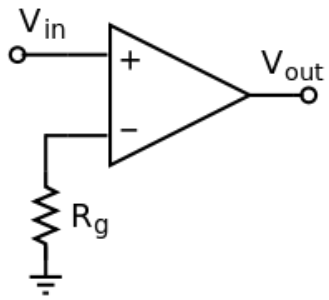
IC 741 used: - The IC 741 series are general purpose operational amplifiers.

Supply Voltage- (**LM741A**) ±22V, (**LM741**) ±22V, (**LM741C**) ±18V

Power Dissipation- (**LM741A**) 500 mW, (**LM741**) 500 mW, (**LM741C**) 500 mW

Input Voltage- (**LM741A**) ±15V, (**LM741**) ±15V, (**LM741C**) ±15V

Operating Tem.-- (**LM741A**) −55°C to +125°C , (**LM741**) −55°C to +125°C, (**LM741C**) 0°C to +70°C.



An op-amp without negative feedback

(a comparator)

Operation:-The amplifier's differential inputs consist of a non-inverting input (+ve) with voltage positive voltage and an inverting input (–ve) with negative voltage; ideally the op-amp amplifies only the difference in voltage between the two, which is called the *differential input voltage*. The output voltage of the op-amp $\mathbf{V_{out}}$ is given by the equation:

$$V_{\text{out}} = A_{\text{OL}}(V_+ - V_-)$$

Where A_{OL} is the open loop gain of the amplifier (the term "open-loop" refers to the absence of a feedback loop from the output to the input).

D. Procedure: ***For Inverting Mode: -***

Exercise 1:- Connect an inverting mode amplifier configuration for a gain of 10 as shown in figure1.1. Apply a sinusoidal input of amplitude 1 V (peak-to-peak),

Exercise 2:- Vary the frequency of the input signal from 5 KHz to 100 KHz.

Exercise 3:- Observe the lowest and the highest input signal frequency for which gain remains constant.

Exercise 4:- Take two readings of output voltage, one at the lowest and the other at the highest frequency for which gain remains constant.

Exercise 5:- Near the highest frequency, vary the frequency in adding of 2 KHz, 5 KHz, and 10 KHz, etc. In further readings and note down the output voltage and measure – 3db frequency.

Exercise 6:- Plot the frequency response and calculate the bandwidth. i.e. Bandwidth = F_H - F_L

For Non- inverting Mode:-

Exercise 1:- Design a non- inverting mode amplifier configuration for gain of 2 as shown in figure 1.2.

Exercise 2:- Repeat the steps, as mentioned above. The frequency in this case needs to be varied from 5 KHz to 500 KHz.

E. Observation*: - For Inverting Mode: -*

S.No.	Input frequency	Output voltage	Gain	Gain in dB
1				
…..				
10				

For Non inverting Mode: -

S.No.	Input frequency	Output voltage	Gain	Gain in dB
1				
…..				
10				

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

G. Conclusions: *This practical practice helps us to understand:*

- Working of an operation amplifier IC 741.
- Inverting and non inverting mode of operation amplifier.
- Negative feedback in operational amplifier.
- DC biasing to IC 741.

Precautions:

1. Measure the function generator voltage on CRO by fixing V/D at 0.2 V/D.
2. Connect +12Vcc at pin no. 7 and -12Vcc at pin no. 4, in IC741.
3. Connections should be done properly and observation should be taken properly.

Approved By: Prepared By:

(HOD ECE) (Lab Instructor)

EXPERIMENT No. : 05

A. Aim: To analyze and design adder and scalar circuit using Op Amp(IC 741).

B. Apparatus Used: 1. CRO, Function Generator, Breadboard,
2. Resistor 1KΩ (7), 10 1KΩ (3), Jumper wire.

C. Theory: ***Summing Amplifier:*** **-** The adder can be obtained by using either non-inverting mode or differential amplifier. Here the inverting mode is used. So the inputs are applied through resistors to the inverting terminal and non-inverting terminal is grounded. This is called "virtual ground", i.e. the voltage at that terminal is zero. The gain of this summing amplifier is 1, any scale factor can be used for the inputs by selecting proper external resistors.

The above given summing circuits function can be verified by examining the expression for the output voltage Vo which is obtained for applying KCL at node X.

$\mathbf{I_a + I_b + I_c = I_b + I_F}$

Since R_{in} and A (Open-loop Gain) of the Op Amp are ideally infinity, so $I_b = 0$. Therefore,

—

If $R_f = R_{in}$ than we get, $\mathbf{V_o = -(V_a + V_b + V_c)}$.

Figure 5.1: Circuit diagram for summing amplifier

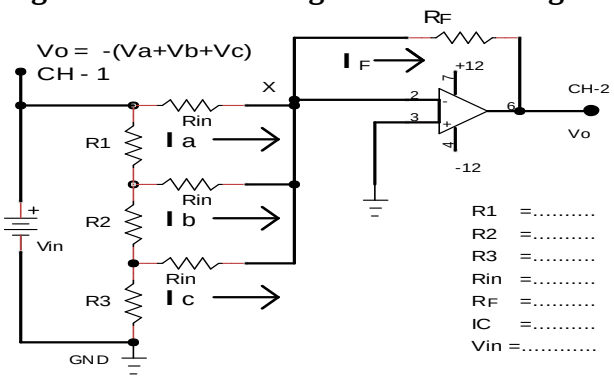
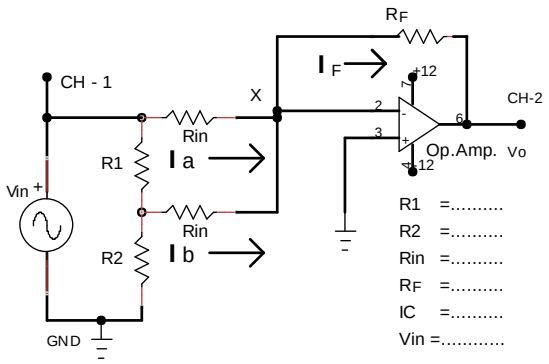


Figure 5.2: Scaling Amplifier:-



A **Scaling Amplifier** can be made if the individual input resistors are "NOT" equal. Then the equation would have to be modified to:

— —

This allows the output voltage to be easily calculated if more input resistors are connected to the amplifiers inverting input terminal. The input impedance of each individual channel is the value of their respective input resistors, i.e, R_a, R_b, R_c … etc.

D. Procedure:-

Summing amplifier

Exercise 1:- Connect the circuit as shown in the circuit diagram.

Exercise2:- Apply a sinusoidal input voltage of 2V DC/ 2 V_{p-p} amplitude and 1 KHz frequency. Note down the output voltage from the CRO for each circuit.

Exercise 3:- Compare the observed output voltage with the theoretical values.

Scaling amplifier

Exercise 1:- Connect the circuit as shown in the circuit diagram.

Exercise 2:- Apply sinusoidal input voltage of 2 V peak to peak amplitude at 1 KHz frequency. Note down the output voltage from the CRO for each circuit.

Exercise 3:- Compare the observed output voltage with the theoretical one.

E. Observation*: (Include your own Table relevant to the Experiment)*

Independent Variable(Unit)	Dependent variable(Unit)

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

G. Conclusions: *This practical practice helps us to understand:*

○ How to addition and scaling of DC & DC, DC & AC, AC & AC.

Precautions:

1. The Voltage may be applied from different sources.
2. Feedback resistor should be connected between pin 2 and 6.
3. Connect proper polarity of voltage to the IC.

Approved By: Prepared By:

(HOD ECE) (Lab Instructor)

EXPERIMENT No. : 06

A. Aim:- To analyze and design a band pass circuit.

B. Apparatus Used:-

1. CRO, Function Generator, Breadboard, DC power supply.
2. Op Amp IC (1 or 2), Resistor R1, R2, R3, R4, R5, R6 and capacitor C1, C2,

C. Theory:- A band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range.

Band pass is an adjective that describes a type of filter or filtering process; it is to be distinguished from pass band, which refers to the actual portion of affected spectrum. Hence, one might say "A dual band pass filter has two pass bands." A *band pass signal* is a signal containing a band of frequencies not adjacent to zero frequency, such as a signal that comes out of a band pass filter.

An ideal band pass filter would have a completely flat pass band (e.g. with no gain/attenuation throughout) and would completely attenuate all frequencies outside the pass band. Additionally, the transition out of the pass band would be instantaneous in frequency. In practice, no band pass filter is ideal. The filter does not attenuate all frequencies outside the desired frequency range completely; in particular, there is a region just outside the intended pass band where frequencies are attenuated, but not rejected.

There are basically two types of band pass filters viz. wide band pass filter and narrow band pass filters. Unfortunately, there is no set dividing line between the two. However, a band pass filter is defined as a wide band pass if its figure of merit or quality factor Q is less than 10 while the band pass filter with Q>10 are called narrow band pass filter. Thus Q is a measure of selectivity, meaning the higher the value of Q the more selective is the filter, or the narrower is the bandwidth (BW) The relation between Q, 3 dB bandwidth, and the center frequency f_C is given above figure 6.3.

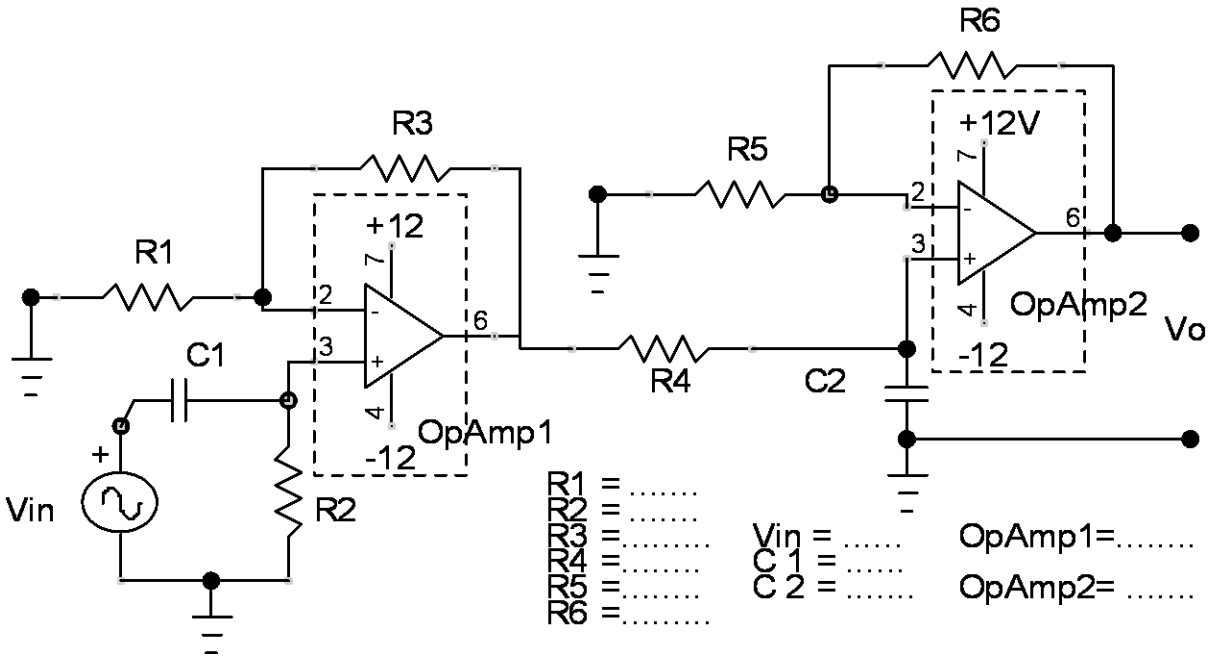
Q Factor:-

A band-pass filter can be characterized by its Q factor. The Q factor is the inverse of the fraction of bandwidth. A high Q filter will have a narrow pass band and a low Q filter will have a wide pass band. These are respectively referred to as narrow-band and wideband filters.

1. Design of first order high pass filter with given value of R_1 = 10K and C_1 = 0.047μ*F*. Find the value of F_L (-3db frequency) using the formula ——— Since a pass band gain of 4 is required, the gain of each section is 2, let $R_F = R_{in}$ =10 K, find the value of the gain using the formula = — .

2. Design of first order low pass filter with the given value of R_2 = 10 K and C_2 = 0.001uF, find the value of F_H (-3db frequency using the formula = ——— .

Figure 6.1:- Band Pass Filter:-



D. Procedure:-

Exercise 1:- 1. Connect the circuit as given in figure 6.1.

Exercise 2:- Apply sinusoidal signal of one volt peak to peak amplitude of 500 Hz and vary the frequency and observe the frequency range for which you get a constant output voltage. Take two readings of output voltage at the two extreme ends of the frequency for which the gain remains constant. Now vary the frequency in period (as instructed in Lab.) on both sides of this corner frequency and note down the output voltages an measure – 3db frequency on both sides.

Exercise 3:- Find gain, gain in dB and plot the frequency response on a semi log graph paper.

Exercise 4:- Find bandwidth and value of **Q** using the formula.

E. Observation*:*

S. No.	Input frequency, voltage	Output voltage	Gain	Gain in dB
1.				
2.				
3.				
4.				
5.				
…..				

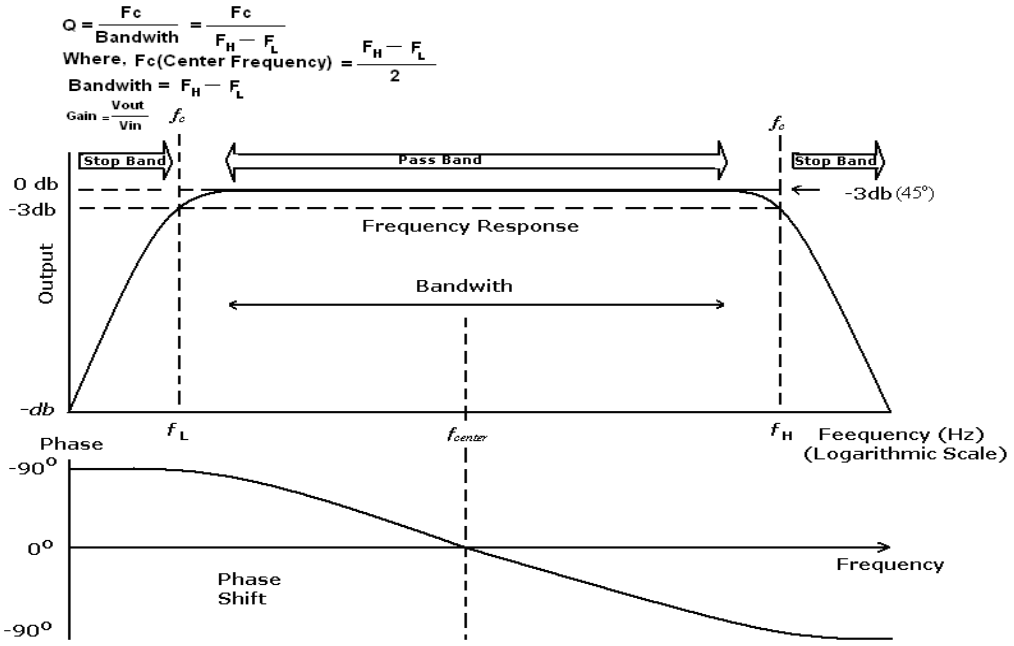
15.				

(Take more readings around cut off frequency to create a linear graph)

F. Analysis of Results:

(Include sample calculations/Display/plot/typical graph)

Figure 6.3



G. Conclusions: *This practice helps us to understand:*

○ Gain bandwidth product.
○ Center frequency, cutoff frequency (3 dB).
○ Use of two IC 741 in a circuit.

Precautions:

1. Check the connections before switching on the kit.
2. Connections should be done properly.
3. The Observation should be taken properly.
4. Take smaller frequency division at cutoff frequency.

Approved By: Prepared By:

(HOD ECE) (Lab Instructor)

EXPERIMENT No. :- 07

A. Aim: - To study and analyze the basic logic gate and universal gate.

B. Apparatus Used:-

1. CRO, Breadboard, DC Power Supply.
2. Logic gates IC (7400, 7402, 7404, 7408, 7432, and 7486)

C. Theory: - The voltage in a digital circuit is allowed to be in only one of two sates HIGH and LOW.
HIGH is taken to mean logical (1) or logical TRUE.
LOW is taken to mean logical (0) or logical FALSE.

***In The TTL logic family*:-**

Any voltage in the range 2 to 5.0 V is HIGH.
Any voltage in the 0 to 0.8 V is LOW.
Any voltage outside this range is undefined, and therefore illegal, except briefly during transitions. The flow of digital signals is controlled by transistors which function as switches with just two states, OPEN and CLOSED. The state of a switch is controlled by a digital signal. The switch remains closed so long as a logical (1) signal is applied. A logical (0) control signal keeps it open.
Logic signals interact by means of gates. The three fundamental gates AND, OR, and NOT are named after the three fundamental operations logic that they carry out, the function of each gate is defined by its TRUTH TABLE, which specifies the output state for each possible combination of input states. The physical basis for the truth tables can be understood in terms of two switches. If the switches are in series, you get the "AND" function. Parallel switches perform the "OR" operation. When several gates are combined to perform a complex logical operation, elegance and economy persuade one to use as possible.

Figure7.1:- X-OR Gate from basic logic gates:-

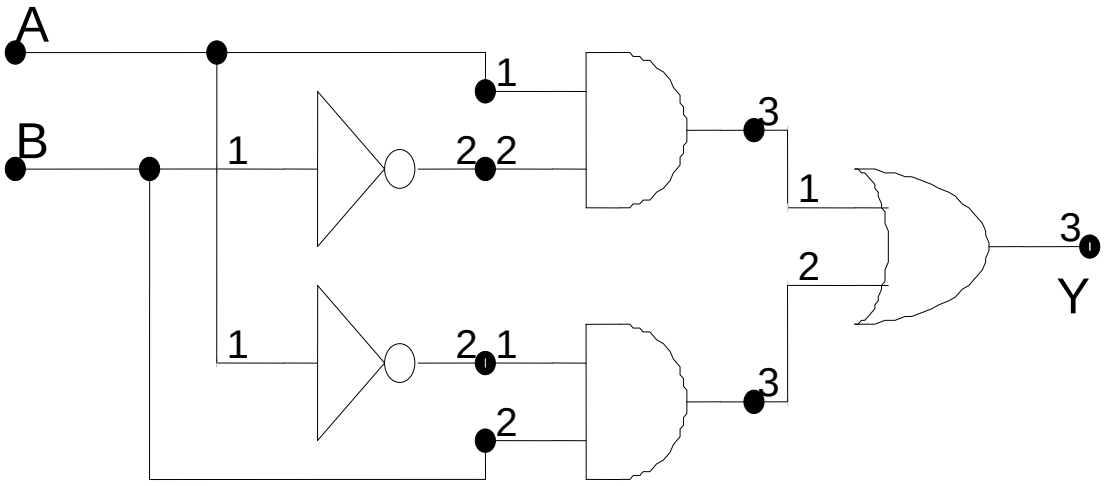
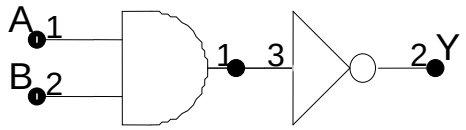


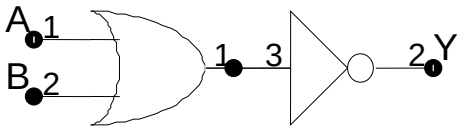
Figure7.2:- Universal Gate using basic logic gates:-

NAND Gate from basic logic Gates



AND Gate Not Gate

NOR Gate from basic Logic Gate



OR gate Not Gate

D. Procedure:-

Exercise 1:- *NAND/ NOR* (universal gate) *gates using basic logic gates:* There are four logic gates in an IC7408 (Quad 2-input AND Gates) and IC7432 (Quad 2-input OR Gates) and six logic gates in IC7404 (Hex Inverting Gates), insert its pins to the essential place.

Exercise 2:- Connect pin 3 of IC 7408/IC 7432 to pin 1 of IC 7404 and pin 2 is for output, Now give input as voltage (2.8 - 5 V) or ground (zero Volt) to pin 1, 2 of AND.

Exercise 3:- Verify the truth table of AND, OR, NOT, NOR, NAND Gates.

E. Observation*:* verify the truth table (Input variables as input form)

NOT Gate (IC 7404)

Input (A)	Output ( )

AND Gate (IC 7408)

A	B	Y

OR Gate (IC 7432)

A	B	Y

AND Gate (IC 7408)

A	B	Y

NAND Gate (IC 7400)

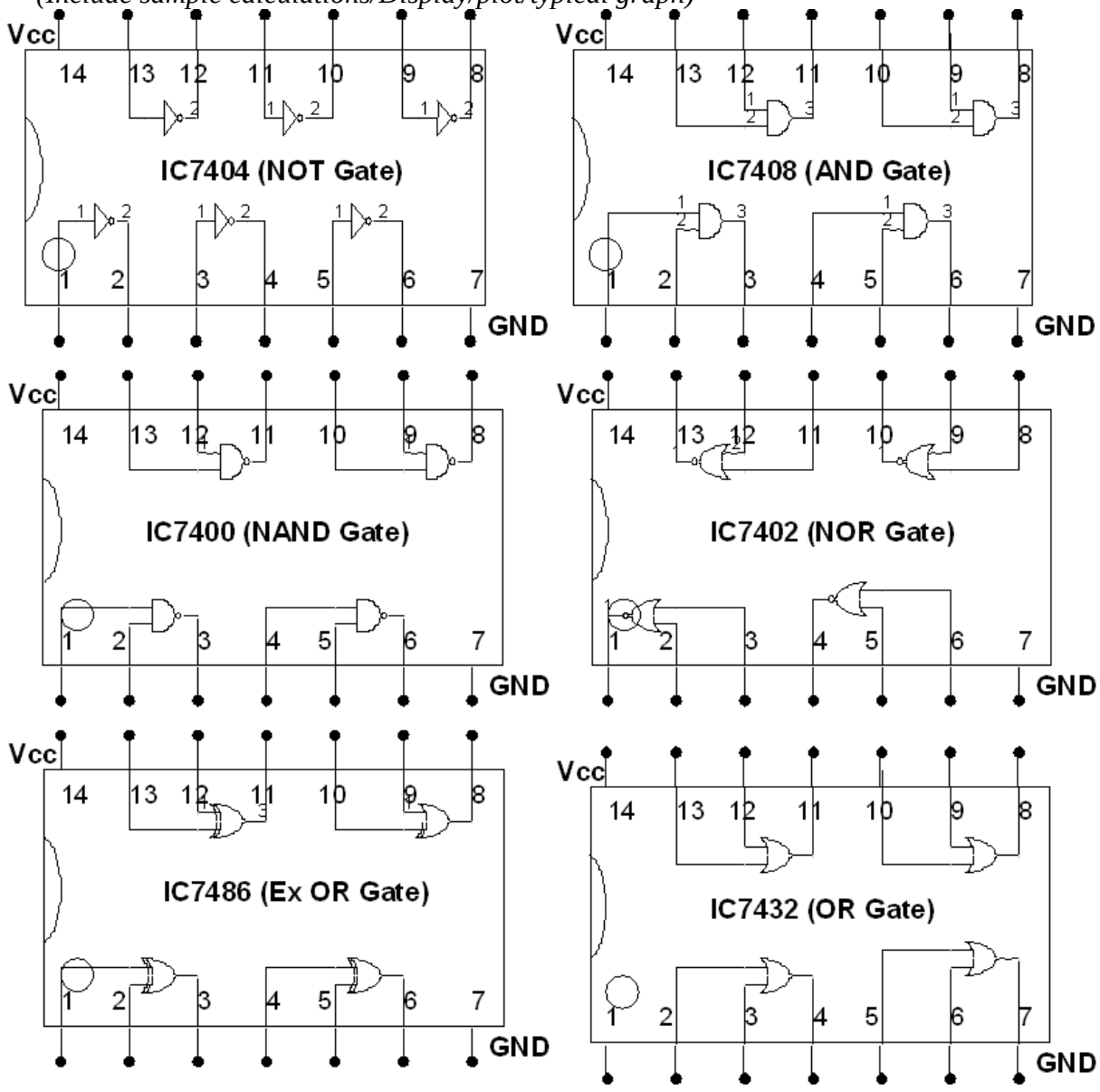
A	B	Y

NOR Gate (IC 7402)

A	B	Y

F. Analysis of Results:-

(Include sample calculations/Display/plot/typical graph)



(IC 7404,7408,7432,7400.7402,7486 are Quad 2 input ICs.)

Figure 7.3: Pin configuration of logic gates

G. Conclusions:- *This practical practice helps us to understand:*

○ Concept of digital input and output become clear.

○ Functioning of various digital IC.

Precautions:-

1. Check the connections before switching on the kit.
2. Connections should be done properly.
3. Do not connect more than +5 volt Vcc in TTL IC.

Approved By:

(HOD ECE)

Prepared By:

(Lab Instructor)

EXPERIMENT No. : 08

A. Aim: - To analyze and design, digital circuits used for performing basic arithmetic operations, addition and subtraction.

B. Apparatus Used: - 1. CRO, Function Generator, Breadboard, DC power supply.
2. IC 4011 (3), Jumper wires.

C. Theory: *Binary Adder:* -Adder plays an important role in digital circuits, especially, of course, in computers as digital circuits are typically binary adders, Multidigit binary values are added 1 bit position at a time each position produces a sum digit and a carry output (C_{out}) into the next bit position.

***Half Adder:* -** The addition table for two binary digits is shown in Table 1. This table shows that the sum and carry produced by the addition of 2 bits. Note that the sum is The Exclusive- OR function, and carry is simply the AND function. Since the previous bit position can produce carry, the adder really reads three inputs, the 2 bits to be added, plus carry from previous bit position. An adder without the carry input C_{in} is referred to is a half adder. An Adder that provides for the carry input is termed a Full Adder. Shown in table 2 is the truth table for a Full Adder.

***Full Adder:* -** This type of adder is a little more difficult to implement than a half-adder. The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as CIN. When full adder logic is designed we will be able to string eight of them together to create a byte-wide adder and cascade the carry bit from one adder to the next.
The output carry is designated as COUT and the normal output is designated as S. Take a look at the truth-table.
From the truth-table, the full adder logic can be implemented. We can see that the output S is an EX-OR between the input A and the half-adder SUM output with B and C_{IN} inputs. We must also note that the C_{OUT} will only be true if any of the two inputs out of the three are HIGH.

Half subtractor: - The half subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, A (minuend) and B (subtrahend)

and two outputs D_I (difference) and B_O (borrow). An important point worth mentioning is that the half subtractor diagram aside implements (b-a) and not (a-b) as borrow is calculated from the equation,

D_I (difference)=A. ,
Truth table is given in table 3.

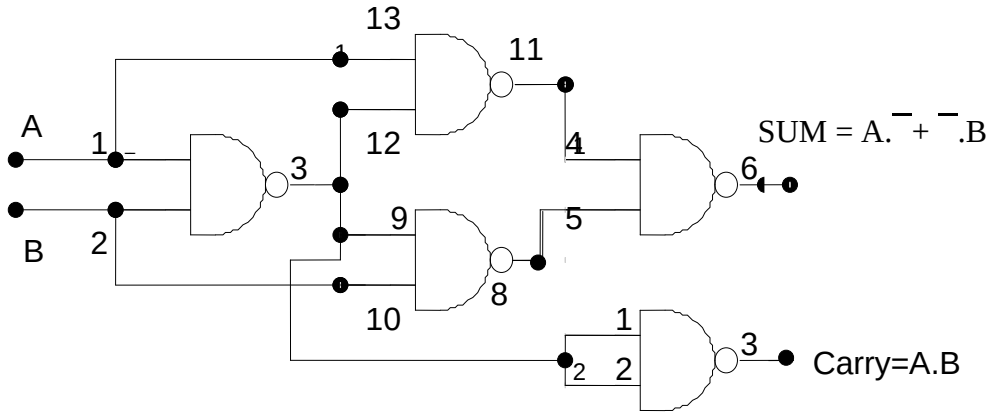


Figure 8.1: Half Adder using NAND gate

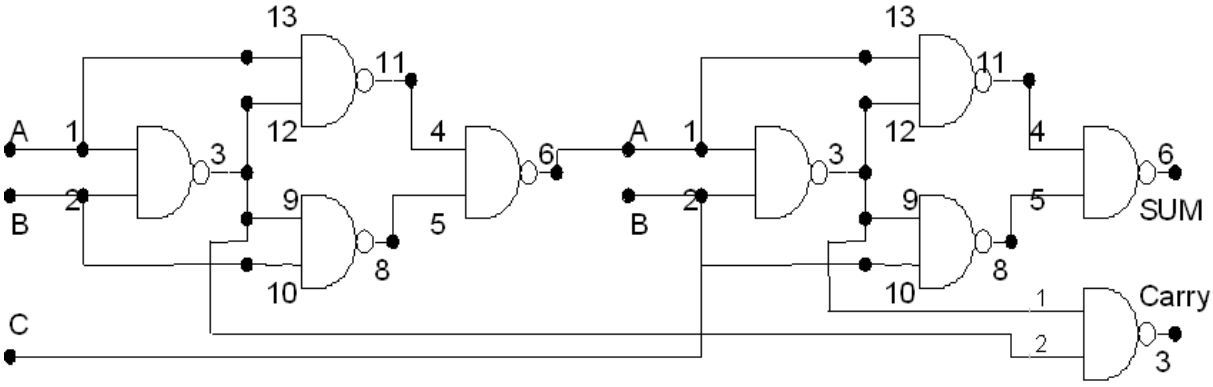


Figure 8.2: Full Adder using NAND gate.

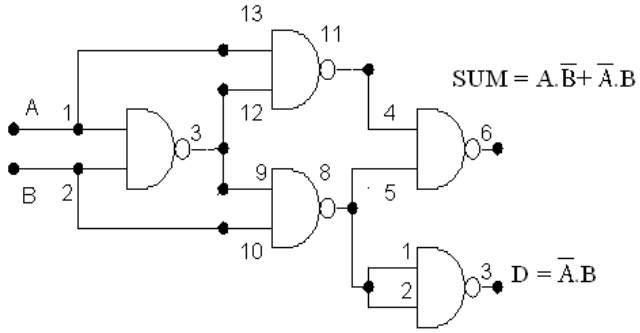
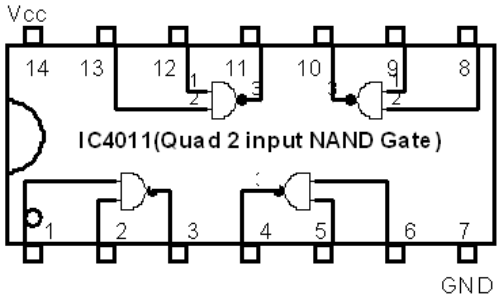


Figure 8.3: Half Adder using NAND gate.

Figure 8.4: IC4011 pin configuration.



D. Procedure: ***Exercise 1:-*** Connect whole circuit on Breadboard and Vcc and GND.

Exercise 2:- For logic 1 input connects particular pin to + 5 V and for logic 0 connects to ground with the help of jumper wire.

Exercise 3:-Enable AC/DC mode of CRO and adjust trace at zero voltage.

Exercise 4:-Now Change input variable (voltage) and note down the output (voltage). All exercises are common for HA, FA and HC.

E. Observation: (Include sample calculations/Display/plot/typical graph)

Half Adder

Table 1

A	B	Summ	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Subtractor

Table 2

A	B	Diff.	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Table 3

A	B	C_{IN}	S	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

F. Analysis of Results: (Include sample calculations/Display/plot/typical graph)

G. Conclusions: This practical practice helps us to understand:

- Working with CMOS IC 4011.
- Binary adder and subtractor.

Precautions:

1. Check the connections before switching on the power supply.
2. Connections should be done properly.
3. The observation should be taken properly.

Approved By:

(HOD ECE)

Prepared By:

(Lab Instructor)

EXPERIMENT No. : 09

A. Aim: To analyze and design a Sequential Circuits (Flip Flops and latches).

B. Apparatus Used: 1. CRO, Function Generator, Breadboard.
2. IC 4027 (1), 7408 (1), 7432 (1), 7404 (1) and jumper wire.

C. Theory: *In digital_circuit theory*, ***sequential logic*** is a type of logic circuit whose output depends not only on the present value of its input signals but on the past history of its inputs. This is in contrast to combinational logic, whose output is a function of only the present input. That is, sequential logic has state (memory) while combinational logic does not. Or, in other words, sequential logic is combinational logic with memory. Sequential logic is used to construct finite state machines, a basic building block in all digital circuitry, as well as memory circuits and other devices. Virtually all circuits in practical digital devices are a mixture of combinational and sequential logic.

In electronics, a ***flip-flop or latch*** is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting pulses, and for synchronizing variably-timed input signals to some reference timing signal.

Digital sequential logic circuits are divided into synchronous and asynchronous types

Synchronous sequential logic: - Nearly all sequential logic today is clocked or synchronous logic. In a synchronous circuit, an electronic oscillator called a clock (or clock generator) generates a sequence of repetitive pulses called the clock signal which is distributed to all the memory elements in the circuit. The basic memory element in sequential logic is the flip-flop.

Asynchronous sequential logic: - Asynchronous sequential logic is not synchronized by a clock signal; the outputs of the circuit change directly in response to changes in inputs. The advantage of asynchronous logic is that it can be faster than synchronous logic, because the circuit doesn't have to wait for a clock signal to process inputs. The speed of the device is potentially limited only by the propagation delays of the logic gates used.

Clocked J-K flip flop:

We are not supposed to make both inputs of the RS latch (or the RS flip flop) active at the same time, because it makes the Q and Q' outputs the same value, and this is logically incorrect. The Q' outputs should always be the inverse of the Q output. It would be useful to have a flip – flop that does something new and useful when both inputs are active, and This section describes the first attempt at designing a useful JK flip-flop.

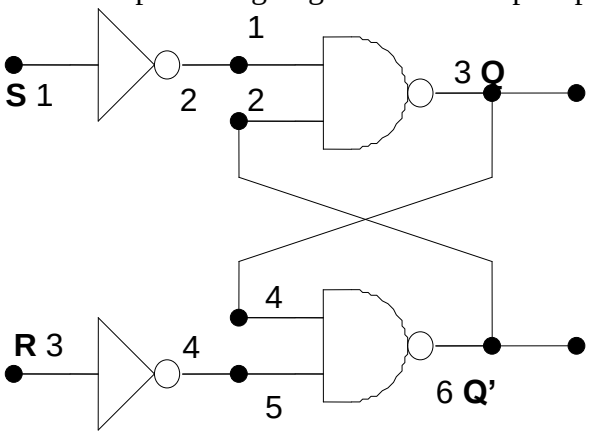


Figure 9.1: NAND Latch

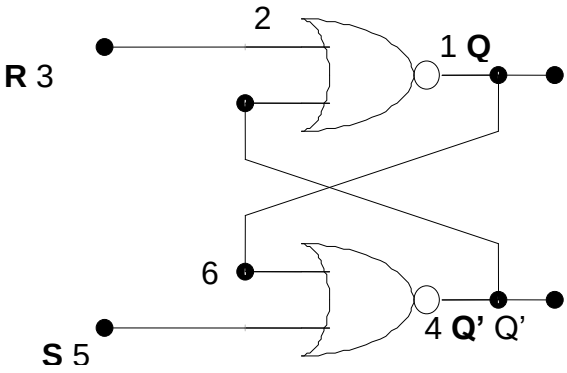


Figure 9.2: NOR Latch

Figure 9.3: IC 4027(Dual JK flip flop) pin configuration.

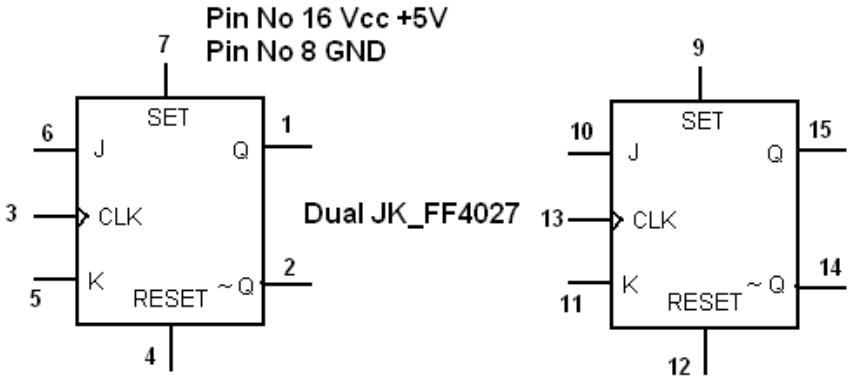


Figure 9.3

►The IC 4027 is a edge triggered dual JK flip-flop. Data is accepted when CP is LOW, and transferred to the output on the positive-going edge of the clock.

►5 V, 10 V, and 15 V parametric ratings at pin no.16.

►VSS at pin no.8 connect to GND.

D. Procedure: ***Exercise 1:-*** In figure 9.1 and 9.2 connect the circuit as given, change the input variables and take output in voltage form.

Exercise 2:- *In Clocked j-k flip flop, IC 4027 have two flip flops in an IC so select any one. Pin configuration is given in figure 9.3.*

Exercise 3:- *Because the output state is transient and 4027 edge triggered, so continuous clock is not possible. Use a jumper to connect Vcc and GND to form a clock pulse.*

E. Observation: *(Include your own Table relevant to the Experiment)*

Truth Table: ***NAND Latch/NOR Latch:-***

R*(Voltage)*	**S***(Voltage)*	**Q***(Voltage)*	**Q'***(Voltage)*

Truth Table: ***Clocked J-K flip flop:-***

CLK	J (Voltage)	K (Voltage)	S (Voltage)	R(Voltage)	Q(Voltage)	(Voltage)
	0	0				
	0	1				
	1	0				
	1	1				
X	X	X				
X	X	X				
X	X	X				

F. Analysis of Results:-

(Include sample calculations/Display/plot/typical graph)

G. Conclusions:-*This practical practice helps us to understand:-*

- Use of IC 4027.
- Memory element and array.
- Clocked J-K flip flop and latches.

Precautions:

1. Check the connections before switching on the DC supply.
2. Connections should be done properly.
3. The observation should be taken properly.

Approved By: Prepared By:-

(HOD ECE) (Lab Instructor)