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Network-on-Chip

Sunil Kumar

The course will enable you to:

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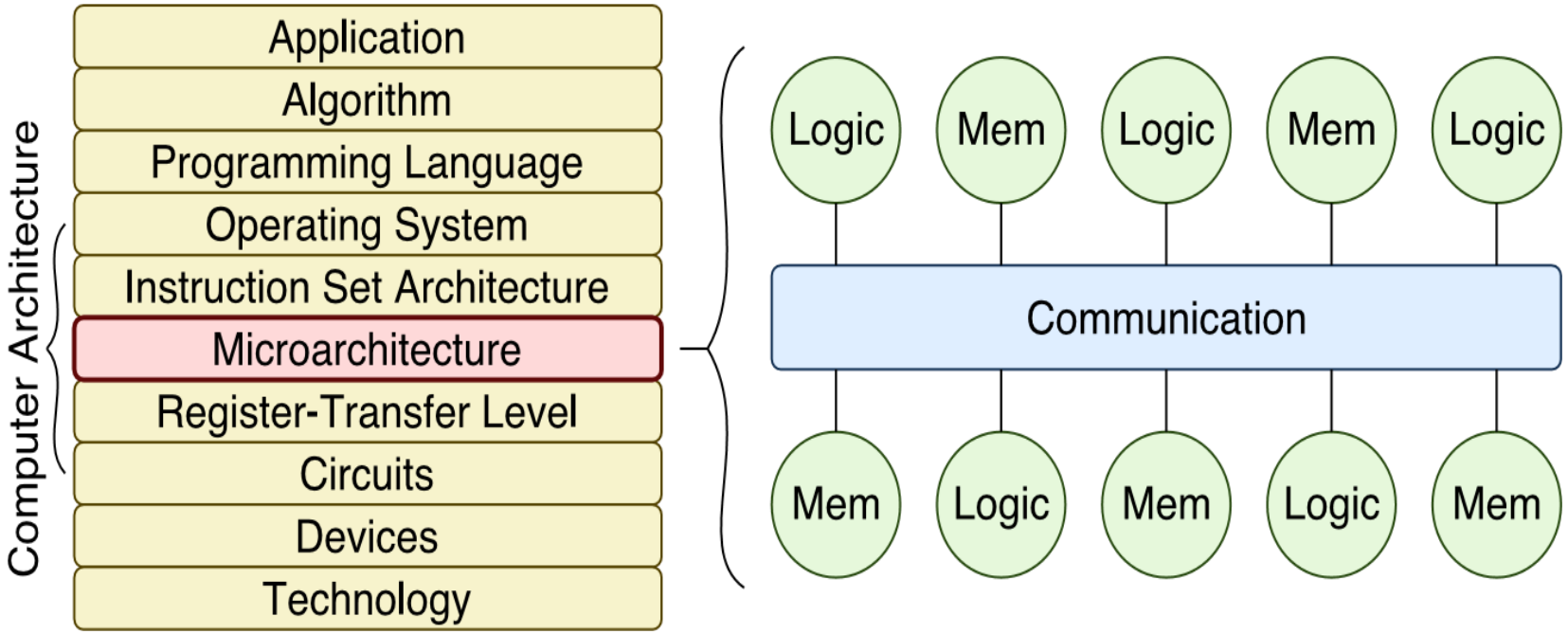
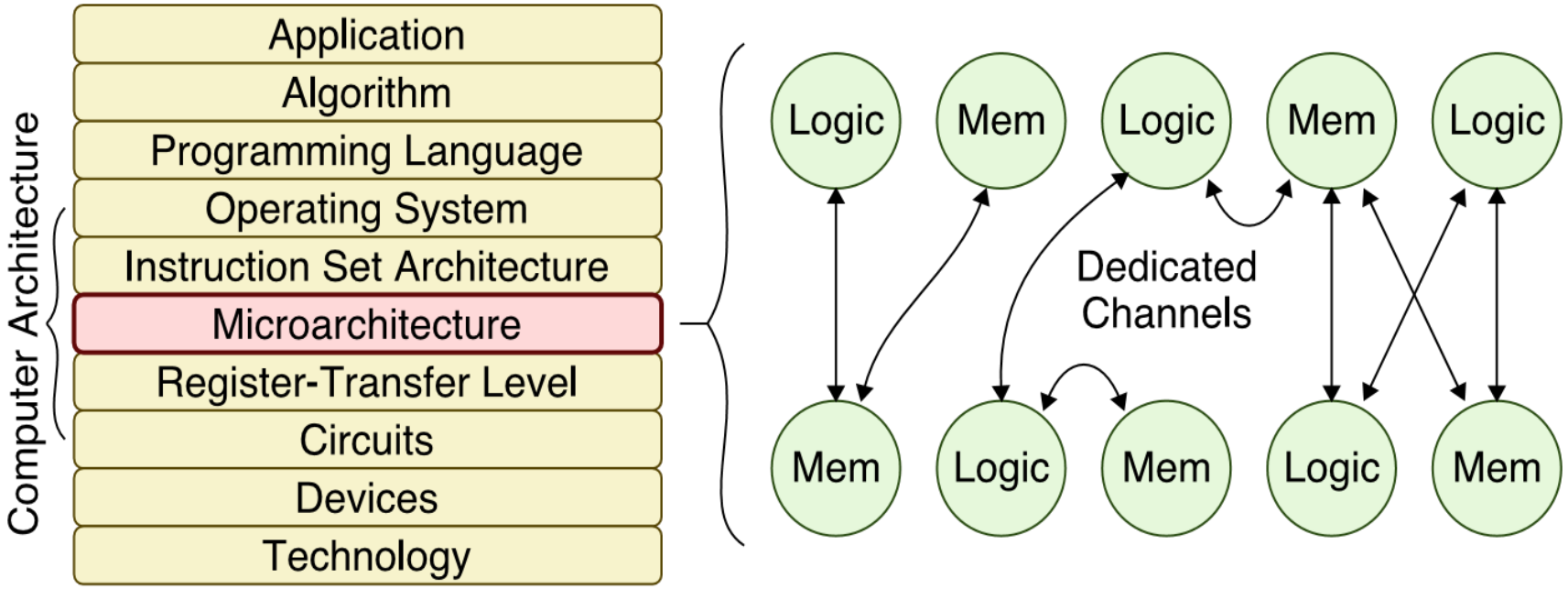
- Understand the basic principles of Network-on-Chip.
- Understand the various techniques of NoC topologies.
- Understand the switching, flow control, routing techniques and router microarchitecture.
- Carry out experiments, analyze results and to make necessary conclusions using NoC simulator.

Introduction



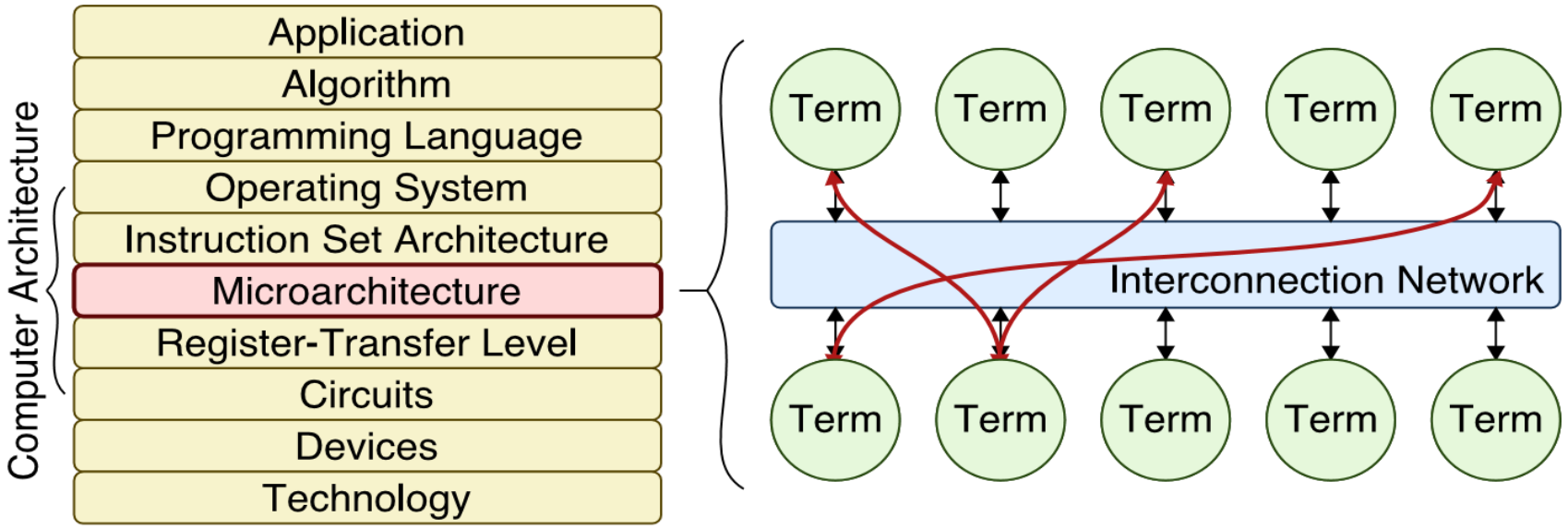
Introduction



Application: Ideally wants low-latency, high-bandwidth, dedicated channels between logic and memory

Technology: Dedicated channels too expensive in terms of area and power

Introduction

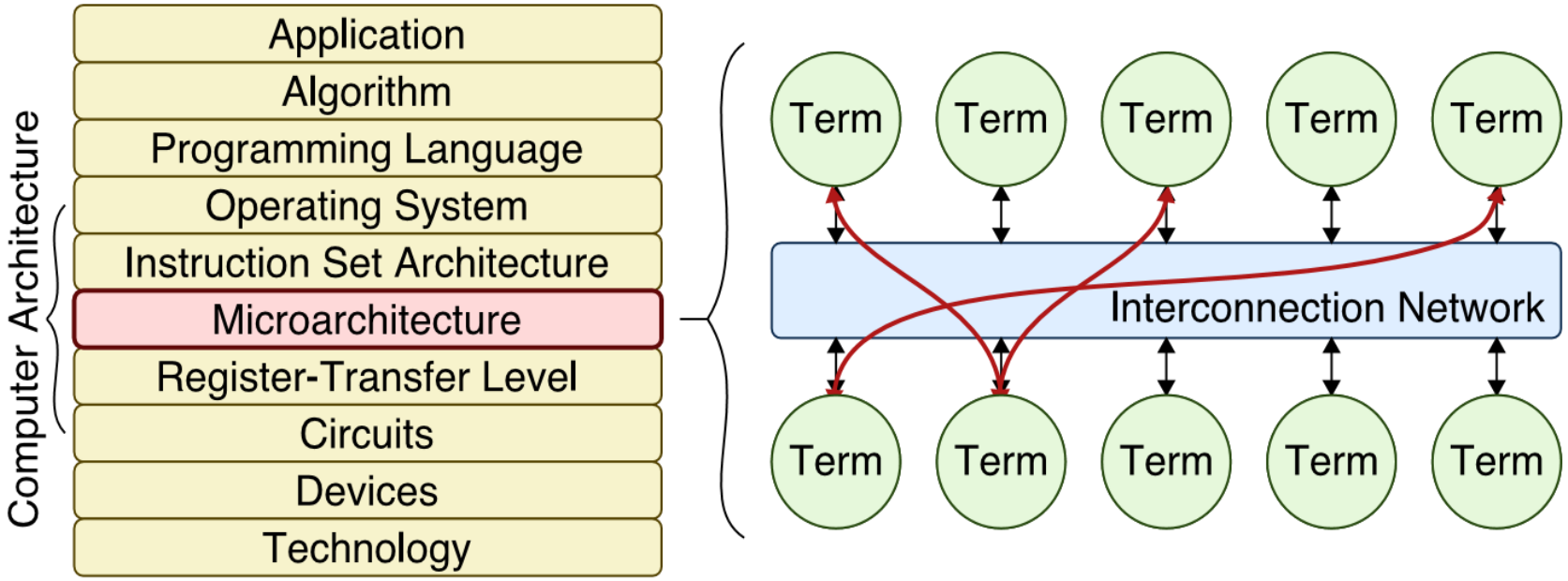


An Interconnection Network is a programmable system that transports data between terminals

Technology: Interconnection network helps efficiently utilize scare resources such as area and power

Application: Managing interconnection network can be critical to achieving good performance

Introduction



One Theme for Course:
Interplay between application requirements, technology constraints, and interconnection networks

Interconnection Networks: Introduction

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- How to connect individual devices together into a community of communicating devices?
- Device:
  - Component within a computer
  - Single computer
  - System of computers
- Types of elements:
  - end nodes (device + interface)
  - Links
  - interconnection network
- Internetworking: interconnection of multiple networks

Interconnect network

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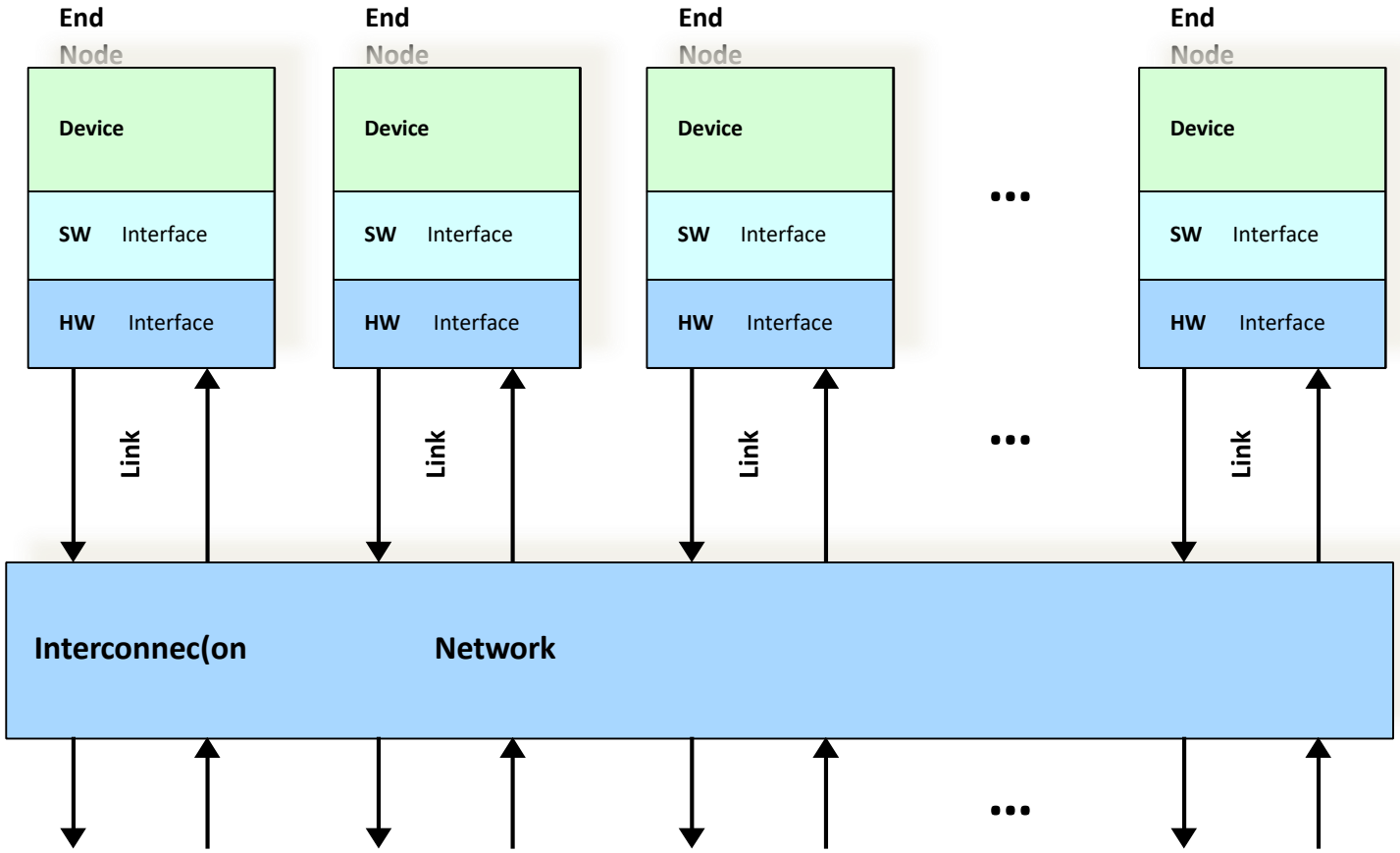

Interconnection Network Domains

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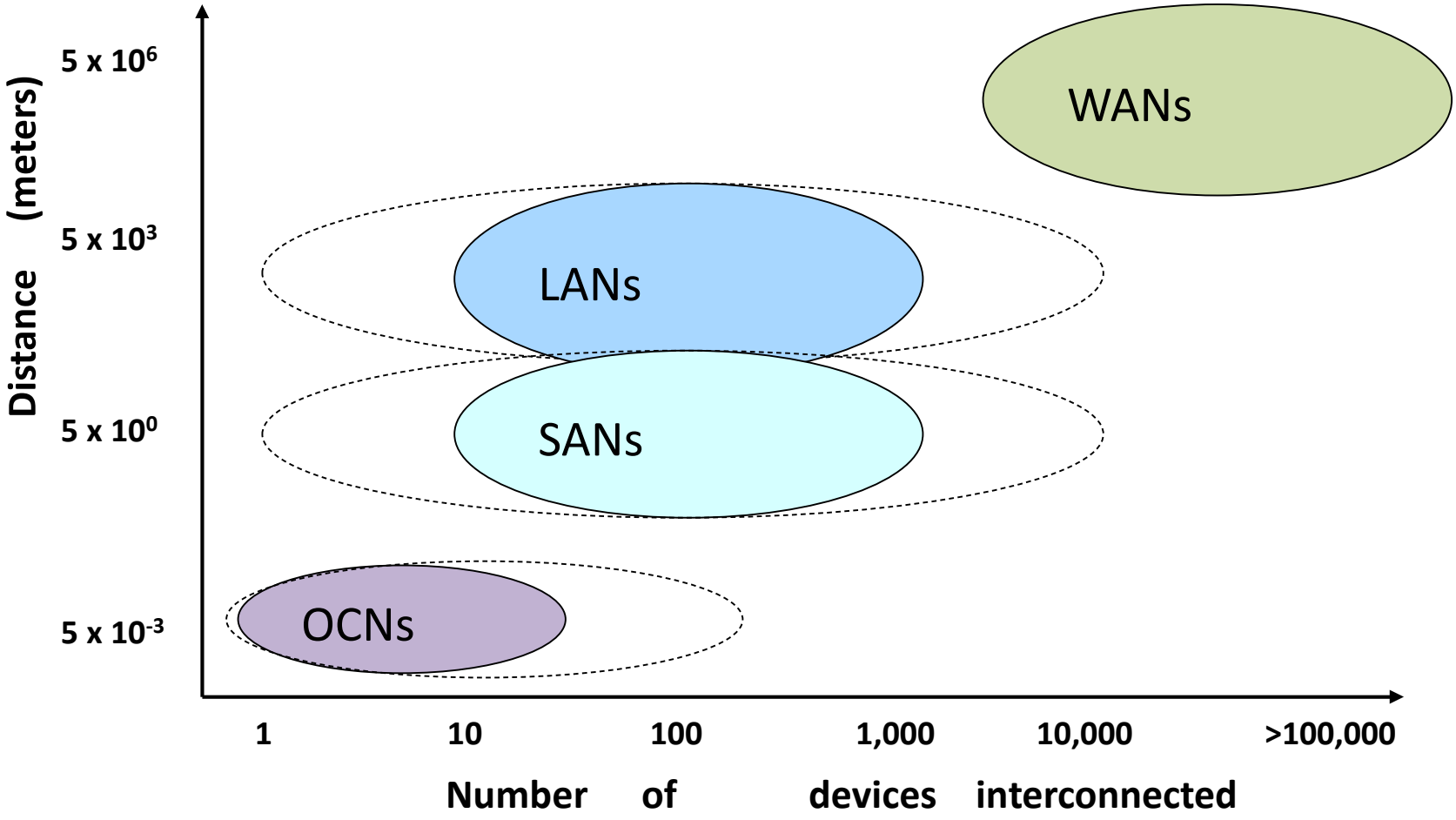

Interconnection Network

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- Key Design Principles
  - Transfer maximum amount of information (high bandwidth) within the least amount of time (low latency) so as to not bottleneck the system
  - Efficiently utilize shared but scarce resources (buffers, links, logic) to reduce area and power.

NoC and Off-Chip Networks

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- **NoC**
  - Sensitive to cost:
    - area and power
  - Wires are relatively cheap
  - Latency is critical
  - Traffic is known a-priori
  - Design time specialization
  - Custom NoCs are possible
- **Off-Chip Networks**
  - Cost is in the links
  - Latency is tolerable
  - Traffic/applications unknown
  - Changes at runtime
  - Adherence to networking standards

Why Study NoC?

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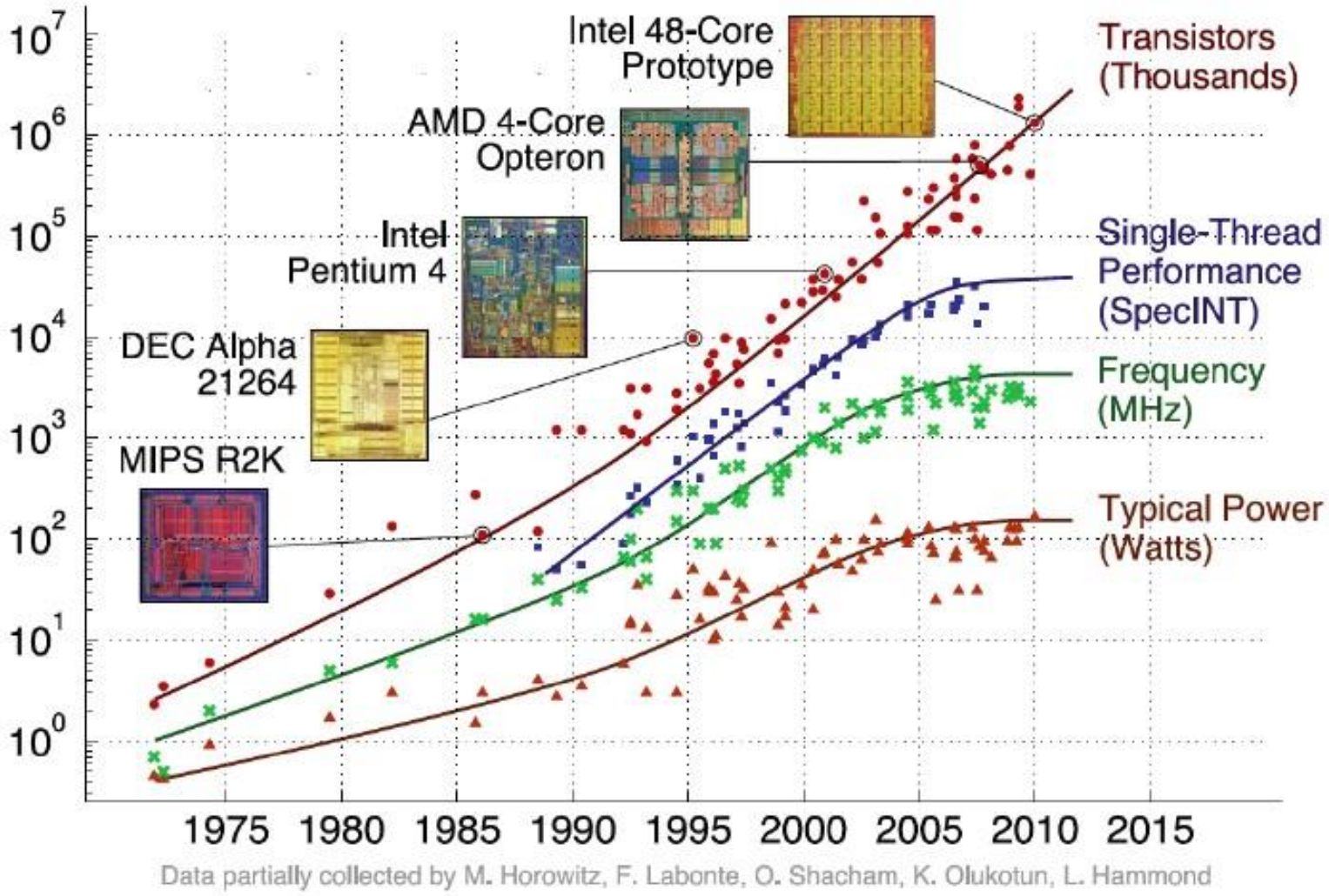

Why Study NoC?

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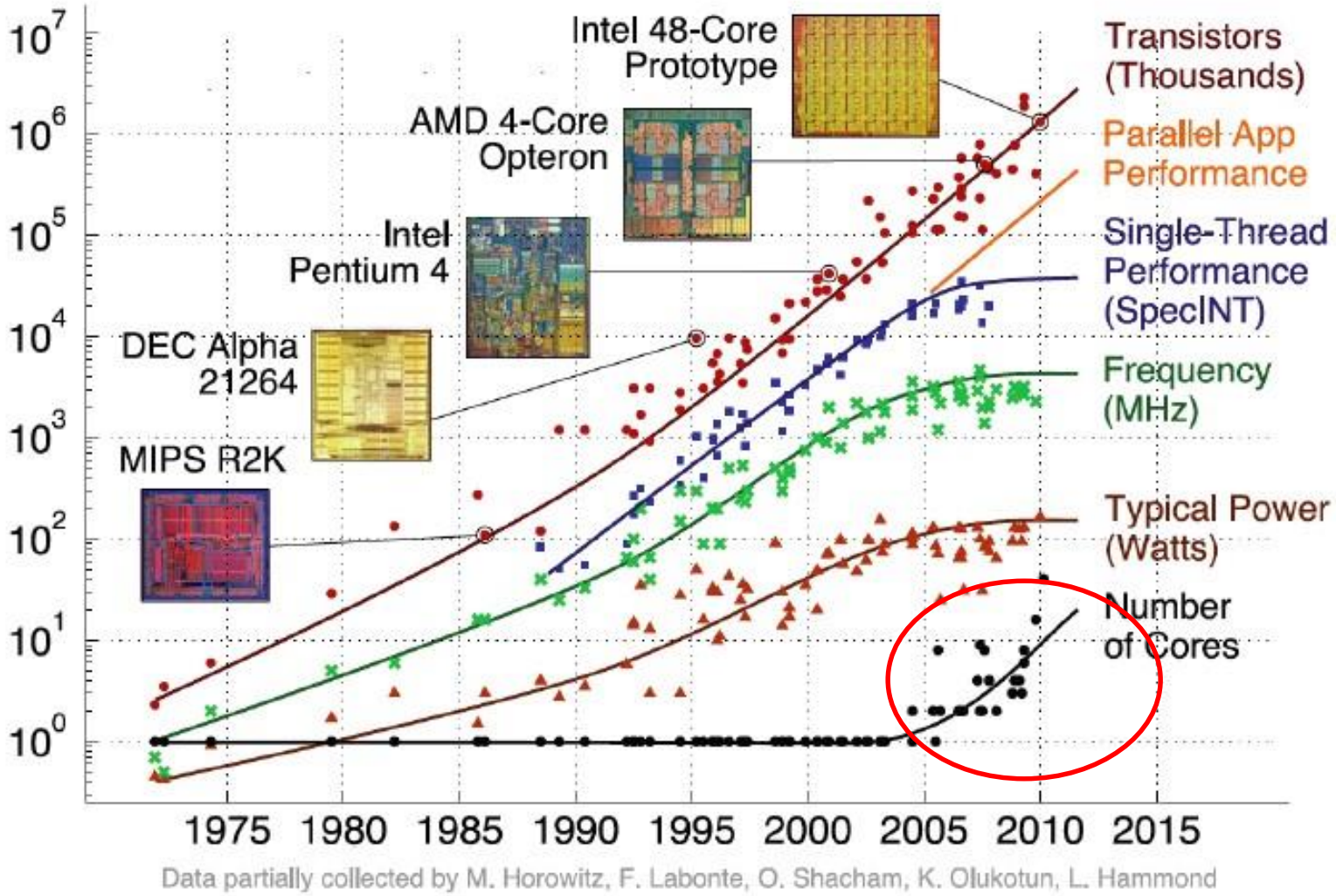

Examples of Multicore and Manycore Processors

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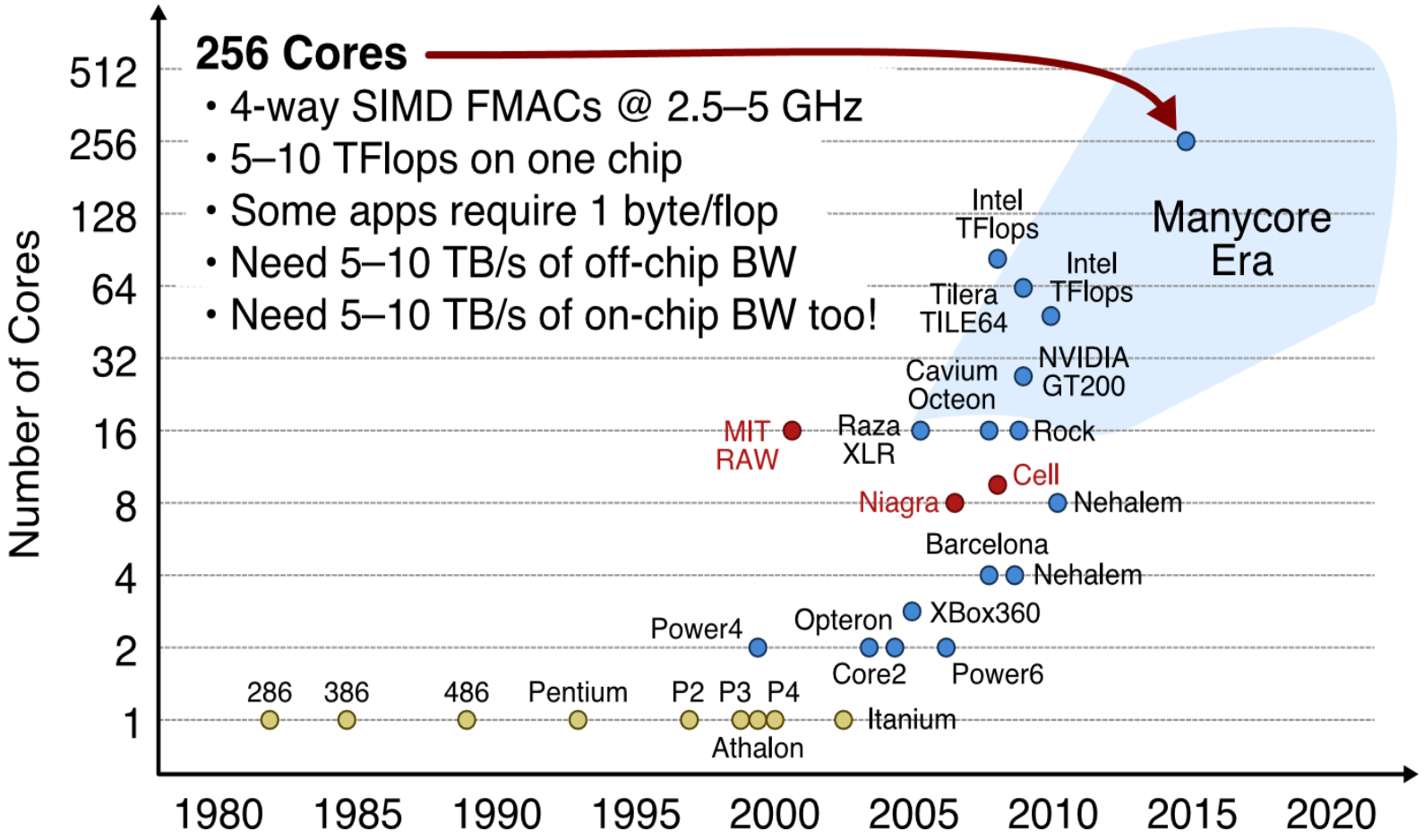
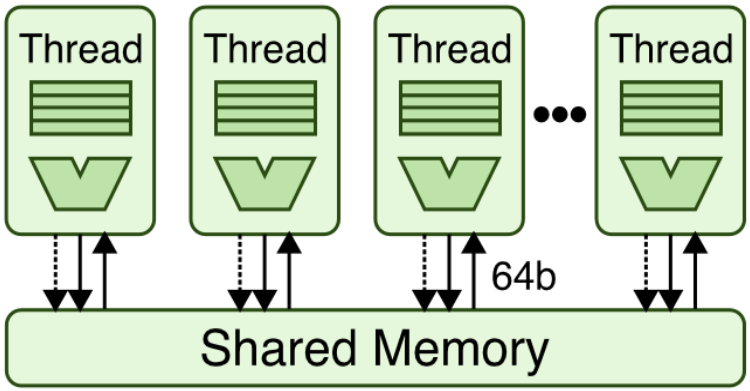
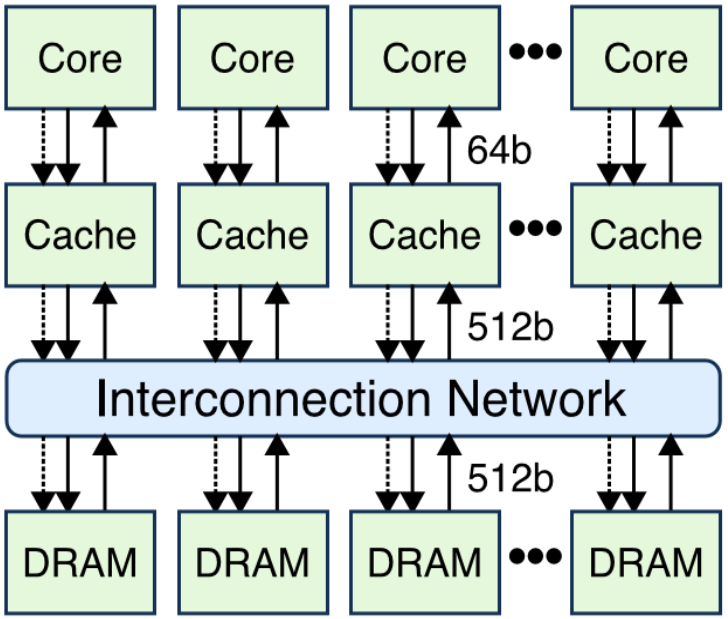


Irregular Threaded Application Running on Processor-to-Memory Network





Application Requirements

Message Size	512b
Average Bandwidth	400 MB/s
Peak Bandwidth	8 GB/s
Latency	Minimum
Traffic Pattern	Arbitrary

What network design meets these requirements within the technology constraints and with the least a ea, power, and lowest latency?

Streaming Application Running on Processor-to-Processor Network

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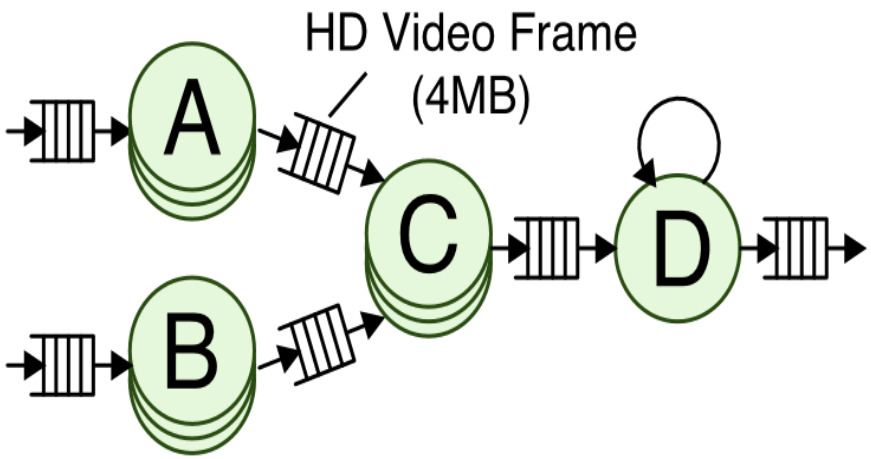

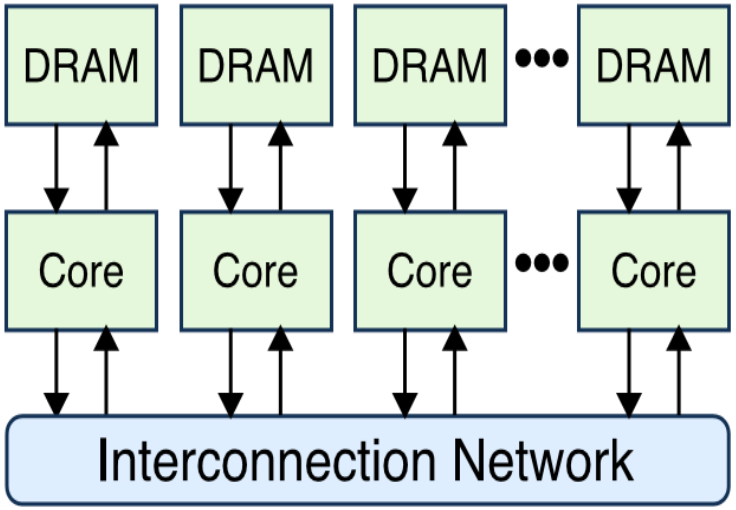

Application Requirements

Message Size	4MB
Average Bandwidth	120 MB/s
Peak Bandwidth	120 MB/s
Latency	Tolerant
Traffic Pattern	Streaming

What network design meets these requirements within the technology constraints and with the least area, power, and maximum bandwidth?

Goal: Flexible Networks Capable of Running Many Different Kinds of Applications

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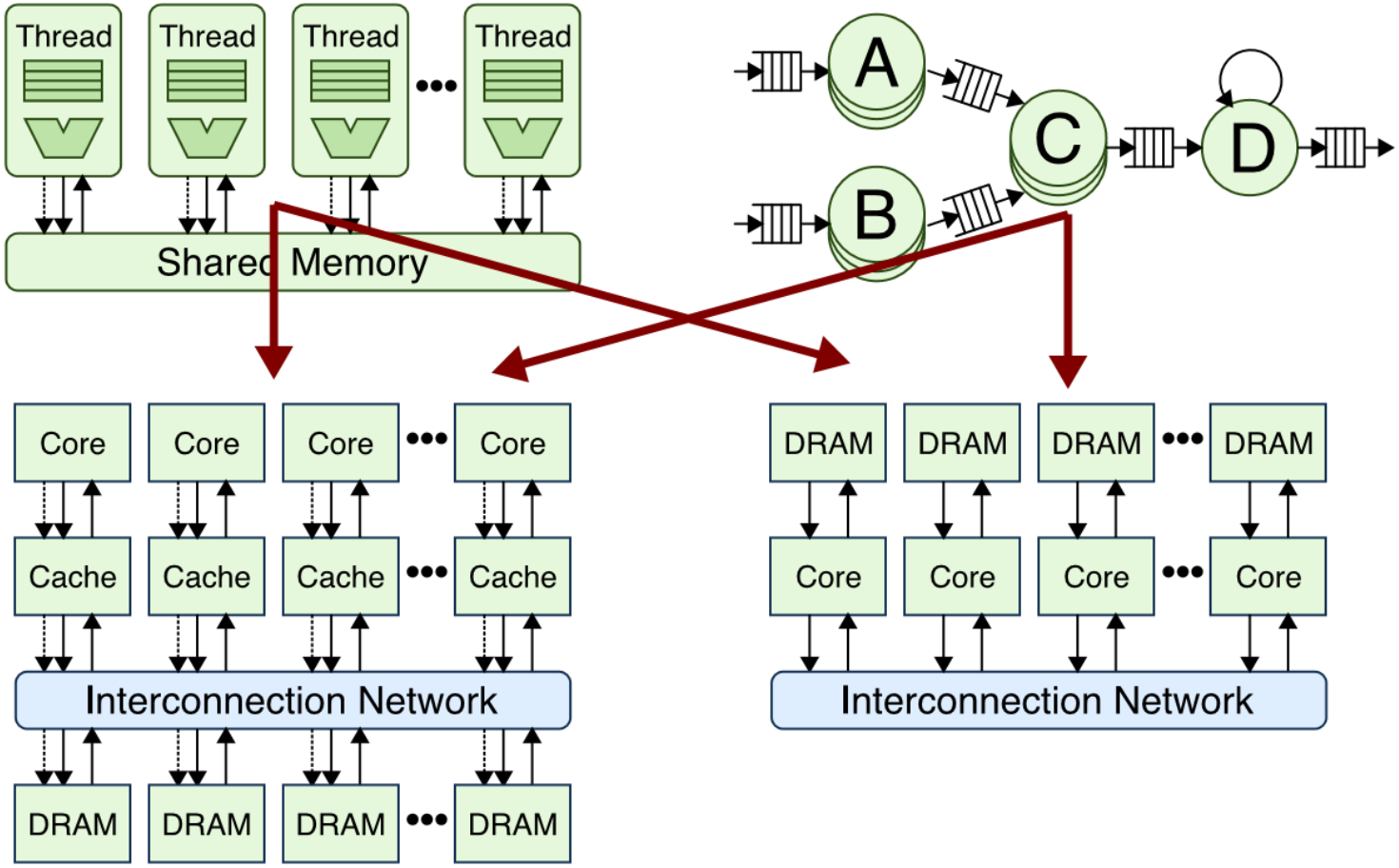

Interconnection Network Basics

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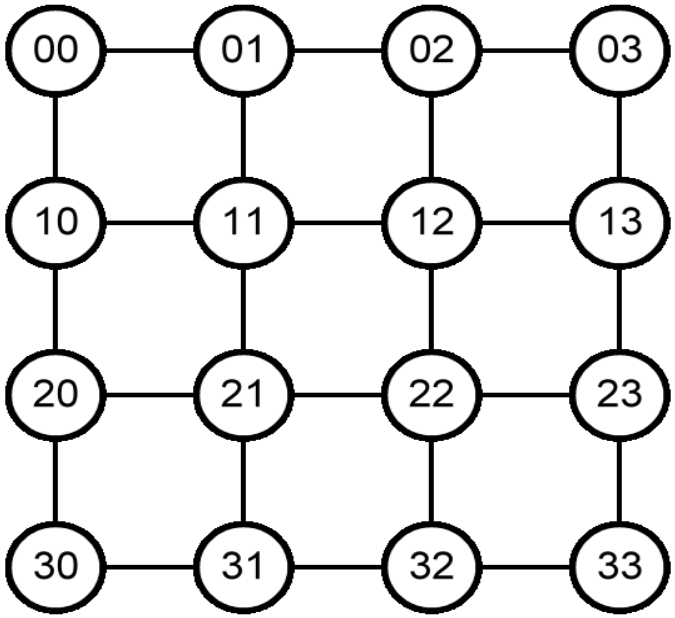
- Topology
  - Arrangement of Nodes and Channels
- Routing
  - Determining Path Between Terminals
- Flow Control
  - Managing Allocation of Resources
- Router Microarchitecture

Topology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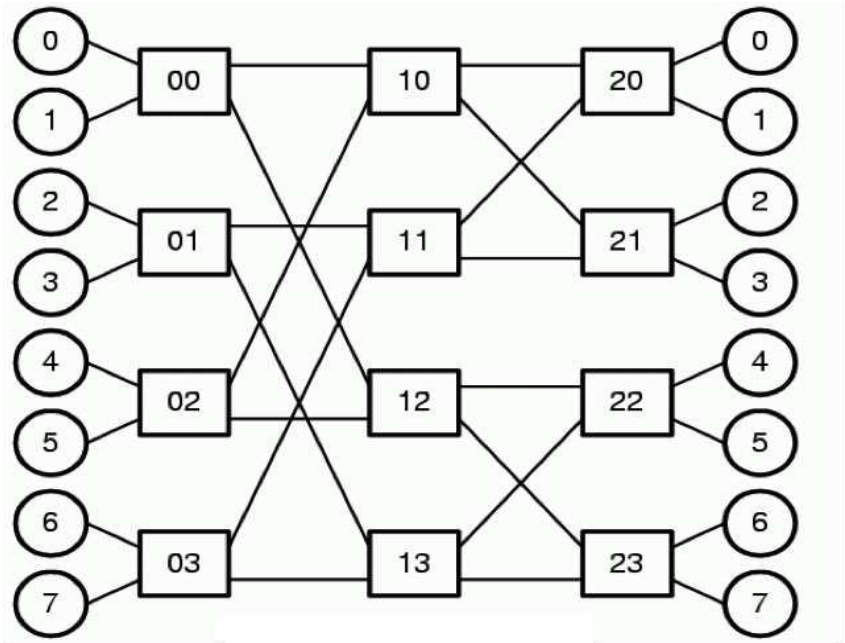
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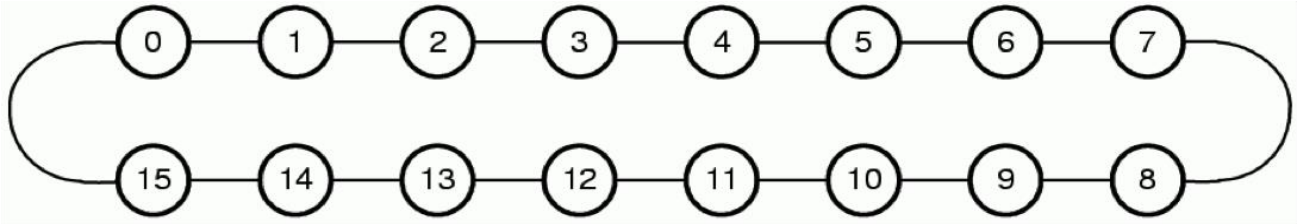
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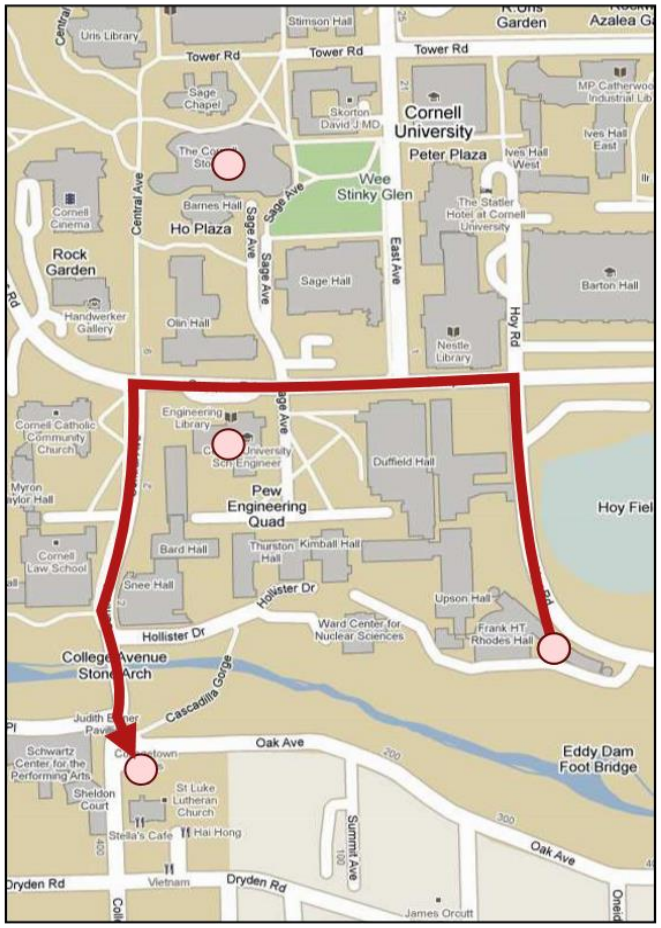
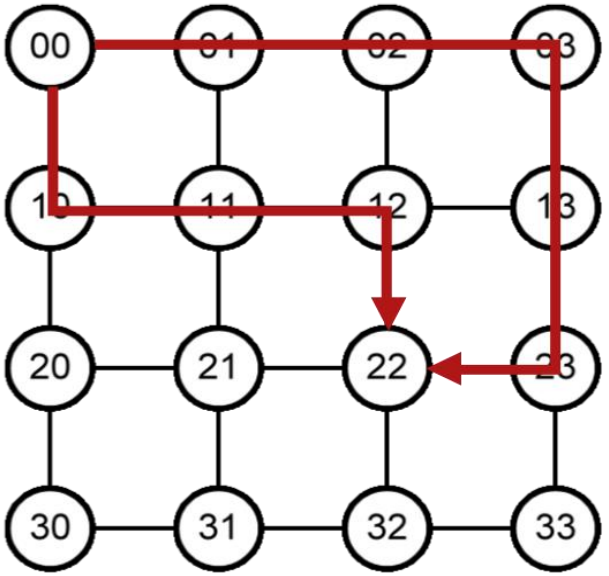
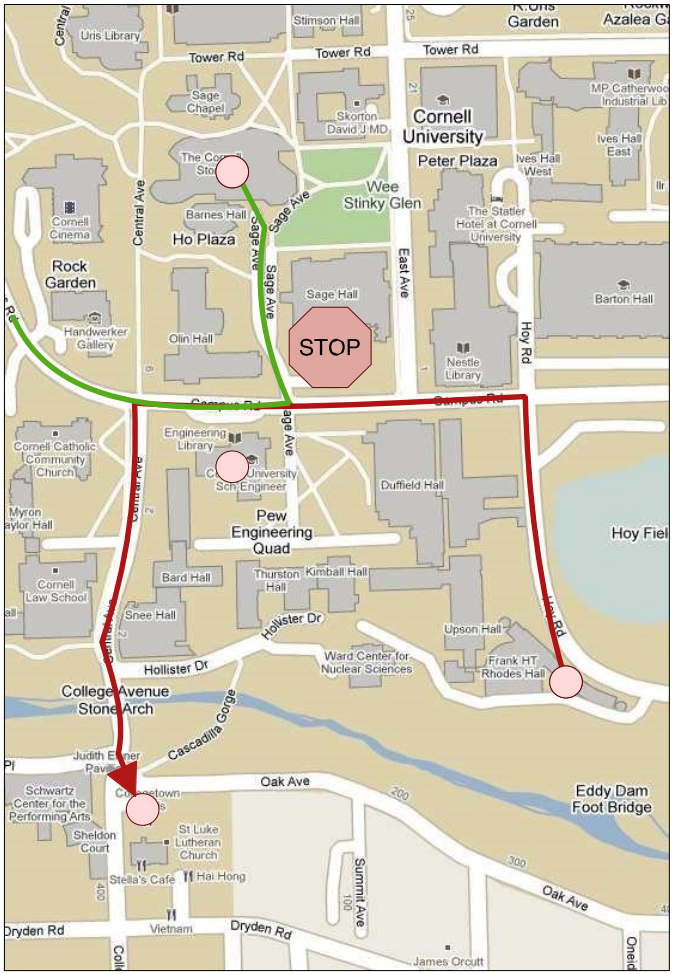
Routing

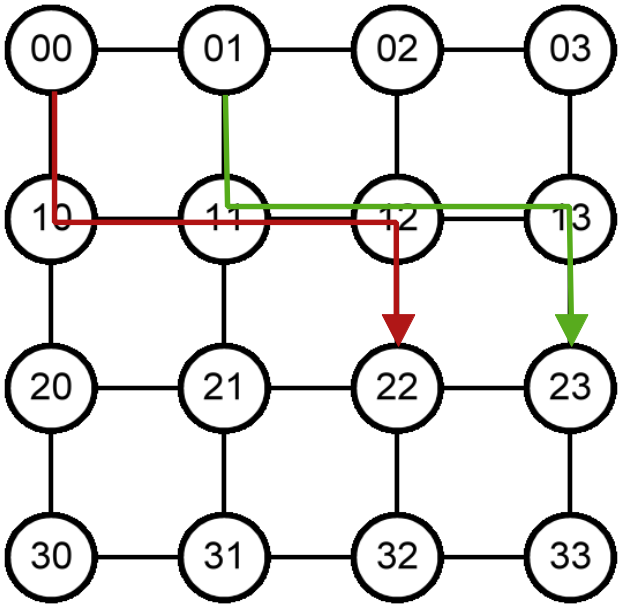


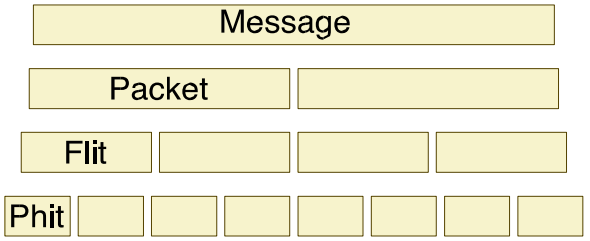


Minmal Routing vs. Non-Minimal Routing
Oblivious vs. Adaptive Routing
Deterministics vs. Randomized Routing

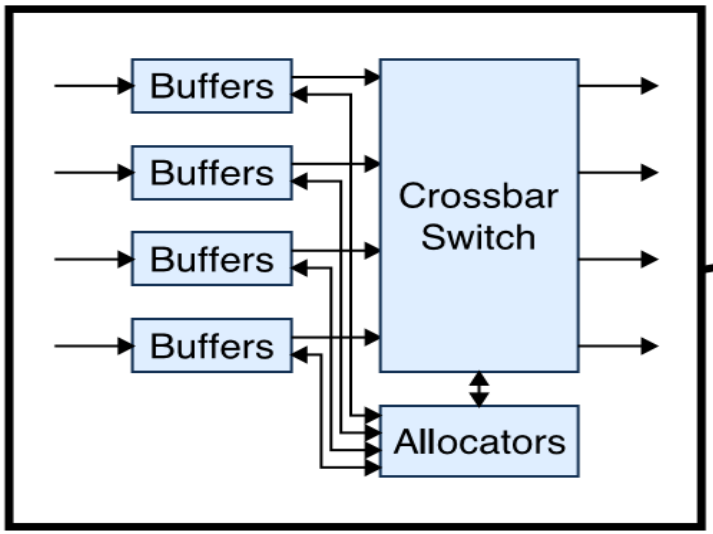
Flow Control

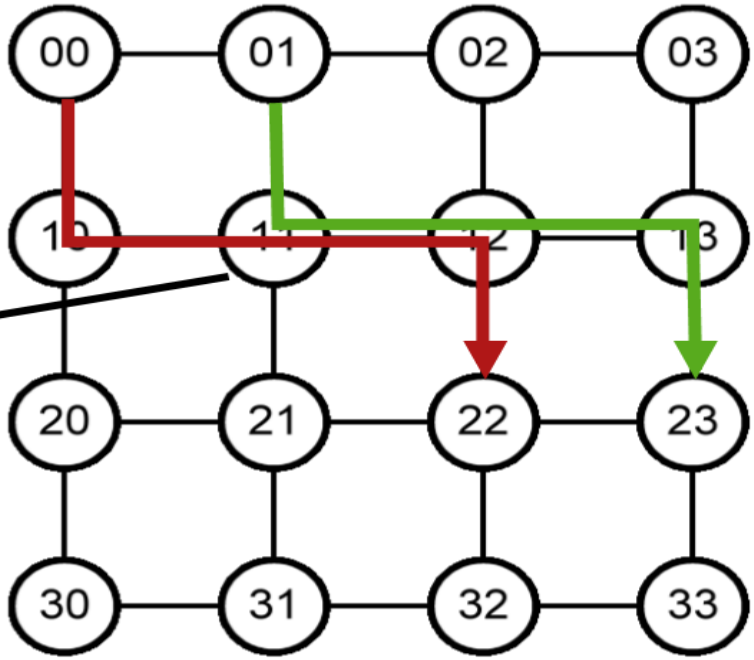


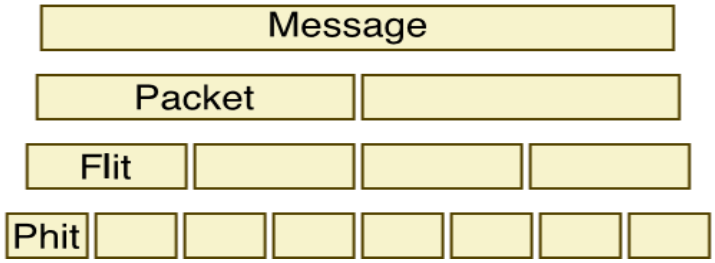




Router Architecture

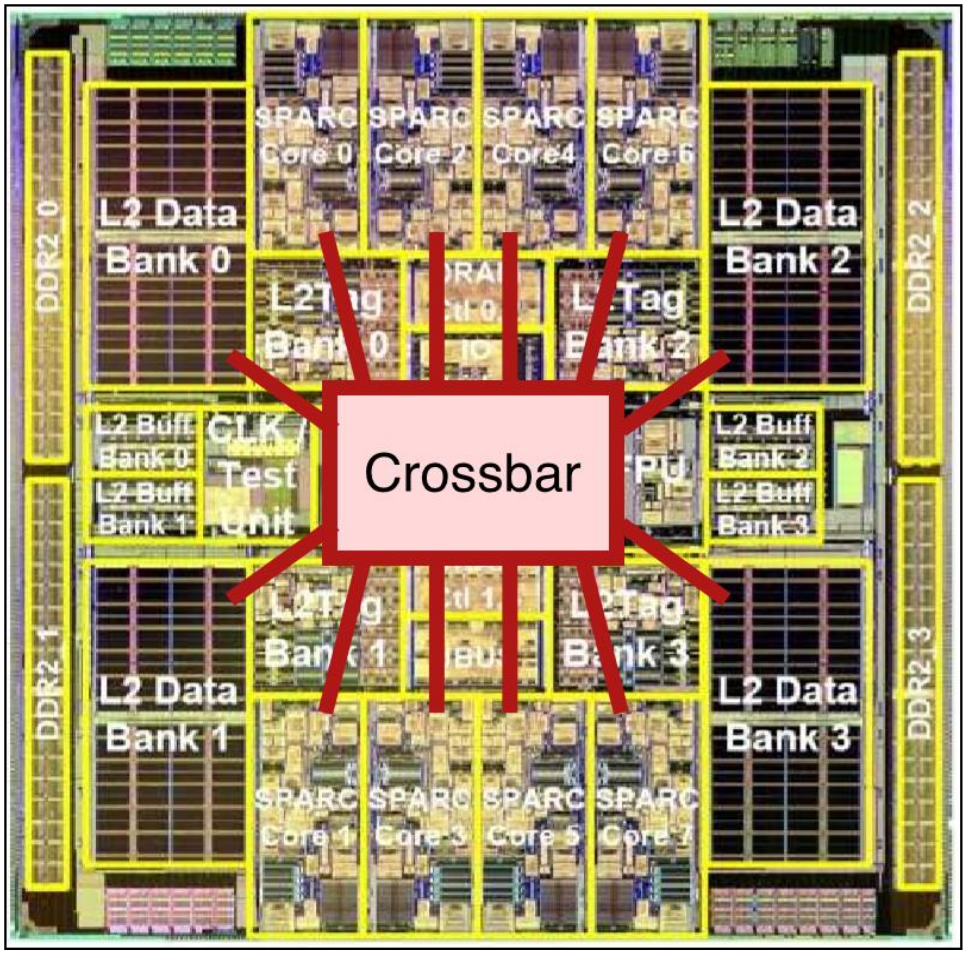






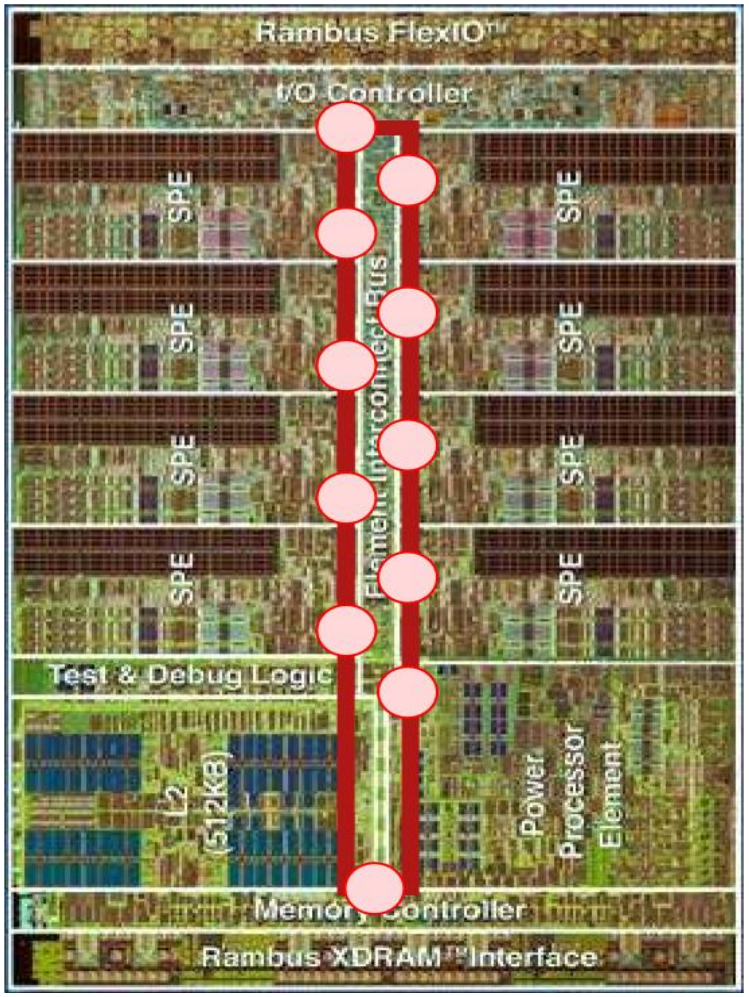
Example Architectures

Sun Niagara Processor



- 8 multithreaded processors
- Single-stage crossbar connecting 8 cores to 4 L2 cache banks
- "200 GB/s" total bisection BW

IBM Cell Processor



- 1 general-purpose processor
- 8 processors specialized for data-parallelism
- 4 uni-directional rings
- Each ring is 128b wide at 1.6 GHz
- Network Bisection BW = 25.6 GB/s
- Total Bisection = 102.4 GB/s

MIT Raw Processor

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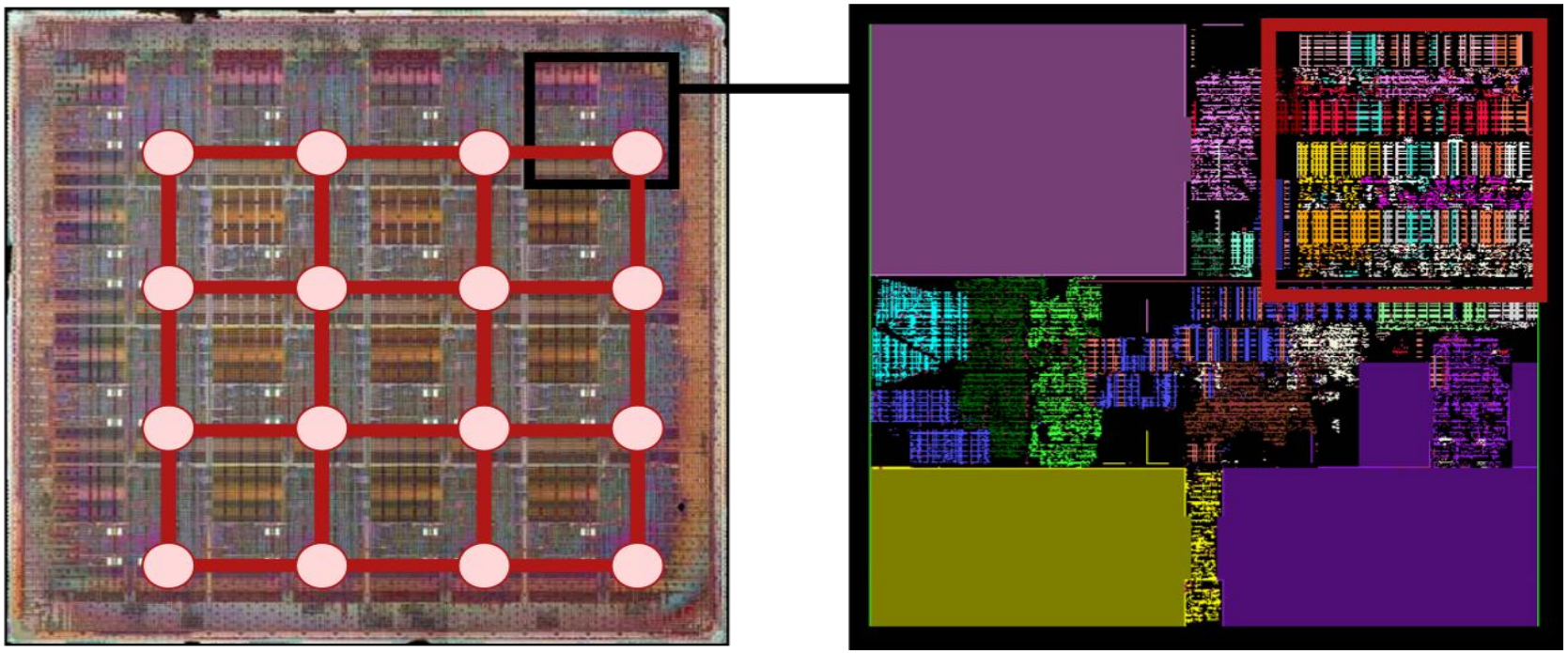

- 16 simple RISC cores
- Two dynamically routed mesh networks (32b/channel)
- Two statically routed mesh networks for message passing (32b/channel)
- Bisection bandwidth per network is 8*32b at 400 MHz 12.8 = 12.8 GB/s
- Total bisection bandwidth is 51.2 GB/s
- Network consumes 20-30% of total chip power

Tilera Tile100

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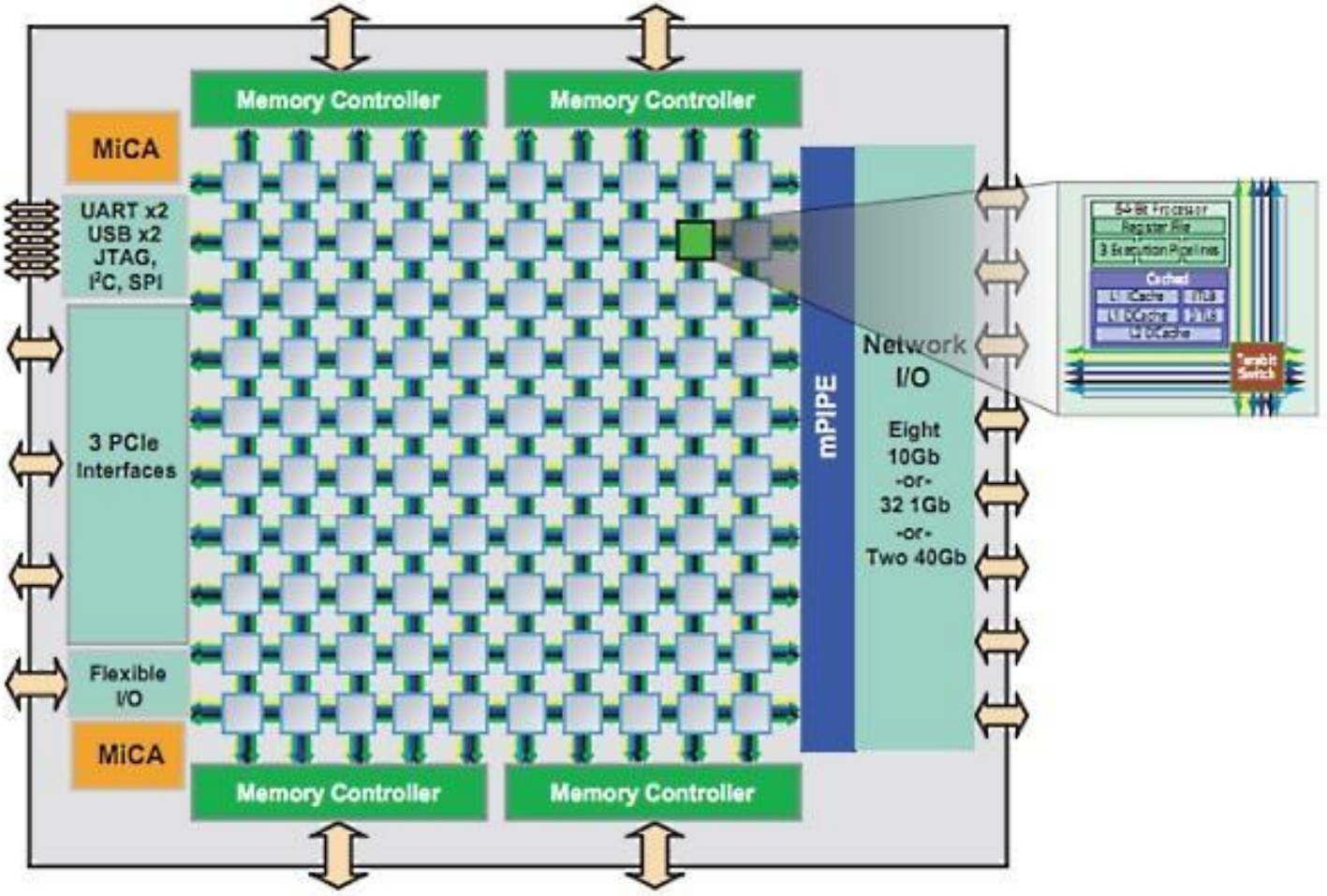

Any Question?