root
: Root

board
: SimpleBoard

memory
: ChanneledMemory

mem_ctrl
: MemCtrl

port

cache_hierarchy
: L1L2Hierarchy

membus
: SystemXBar

mem_side_ports

cpu_side_ports

l2_cache
: Cache

mem_side

cpu_side

processor
: SimpleProcessor

cores
: SimpleCore

core
: RiscvO3CPU

dcache_port

icache_port

l2_bus
: L2XBar

mem_side_ports

cpu_side_ports

l1_dcaches
: Cache

mem_side

cpu_side

l1_icaches
: Cache

mem_side

cpu_side