Lab workshop on FPGA Architecture and programming using Verilog

fpga0722

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Verilog code:

```
`timescale 1ns / 1ps
module miniproject(
 input clk,
 //input i0,input i1,input i2,input i3,
 //output reg[3:0] y,
 output reg[3:0] Y
 //output [1:0] count
 );
//MUX4to1:
 wire [1:0] count;
 //wire dat;
 wire [3:0] y;
 c_counter_binary_2 your_instance_name (
 .CLK(clk), // input wire CLK
 .Q(count) // output wire [1 : 0] Q
);
assign dat=count[1] ? (count[0] ? i3 : i2) : (count[0] ? i1 : i0);
//D Latch:
decoder_2x4 decoder (count, dat, y);
always@(*)
if(clk)
Y<=y;
```

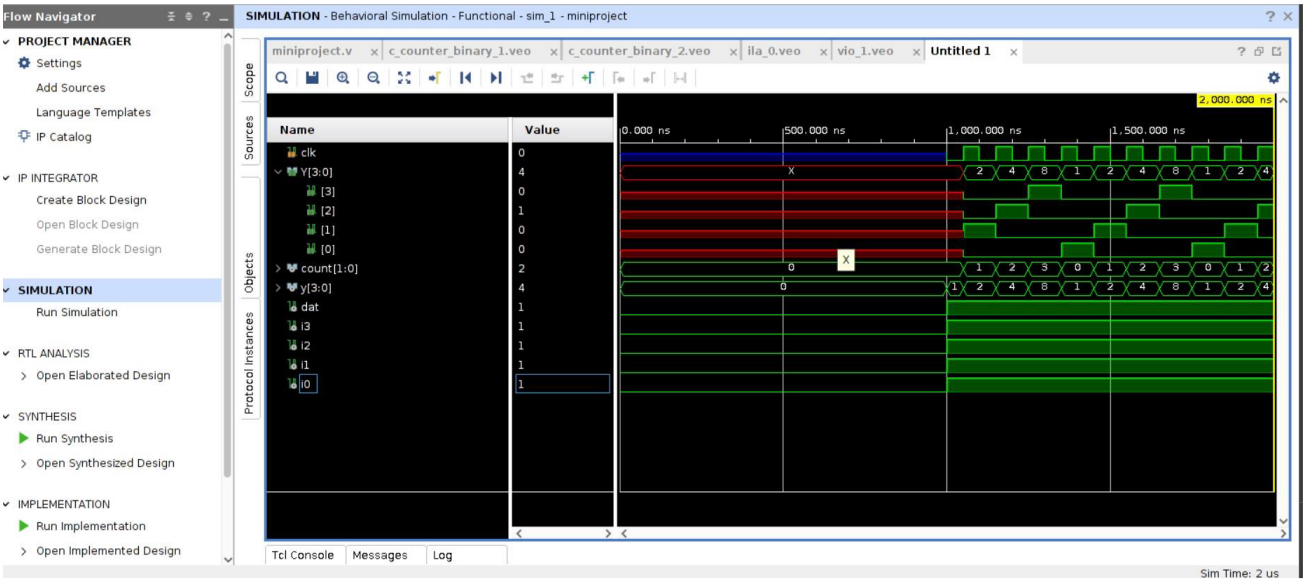
```
ila_0 your_result (
.clk(clk), // input wire clk
.probe0(Y) // input wire [3:0] probe0
);
vio_1 your_input_name (
 .clk(clk), // input wire clk
 .probe_out0({i3,i2,i1,i0}) // output wire [3 : 0] probe_out0
);
endmodule
```

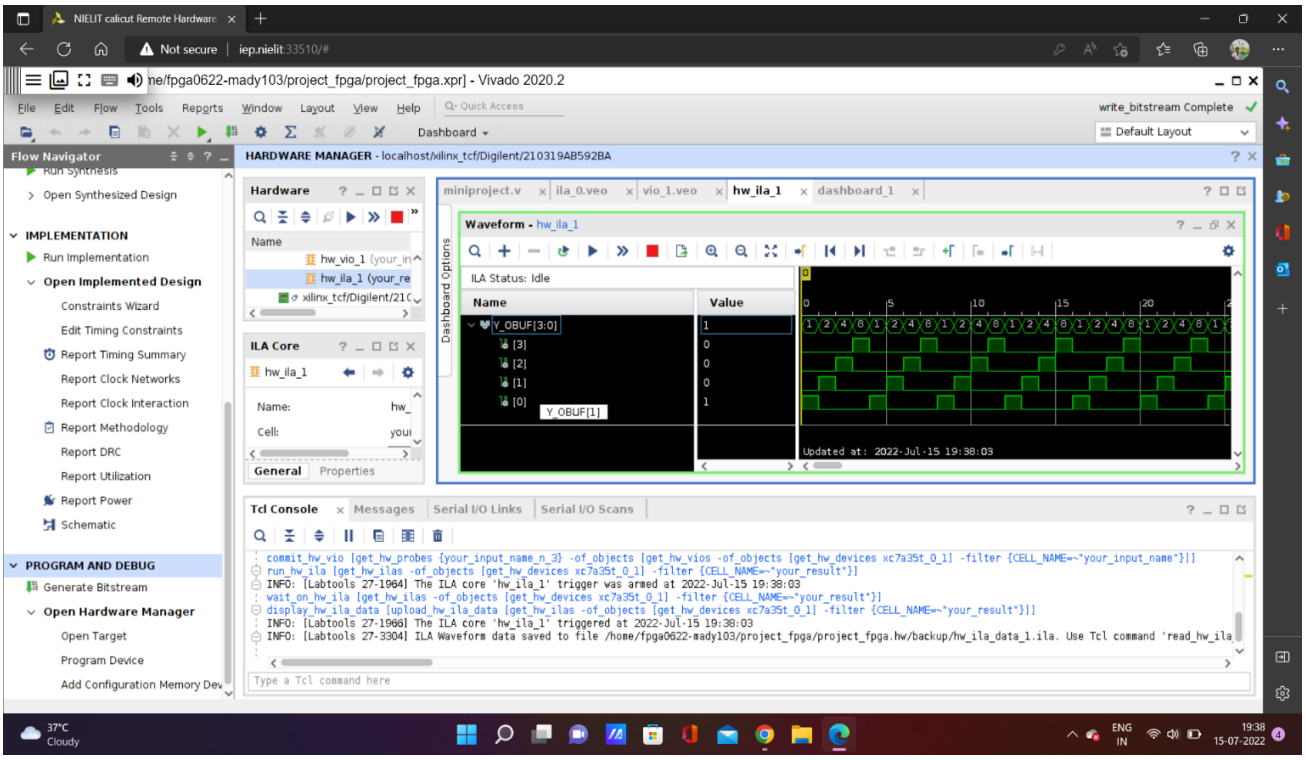
//2x4Decoder:

```
module decoder_2x4(
input [1:0] in,
input en,
output reg [3:0] out
);
always@(*)
if(en)
case(in)
0:out = 1;
1:out = 2;
2:out = 4;
3:out = 8;
default: out = 0;
endcase
else
out = 0;
```

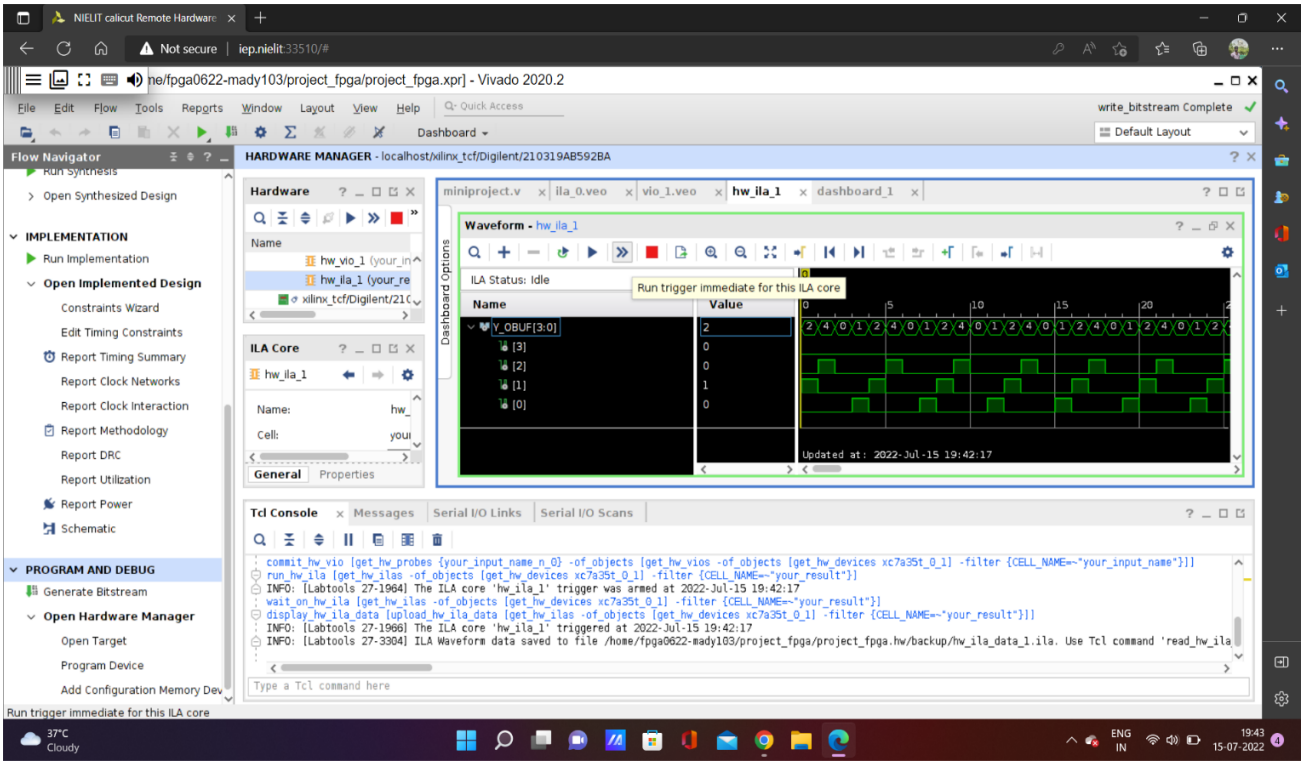
endmodule

Waveforms

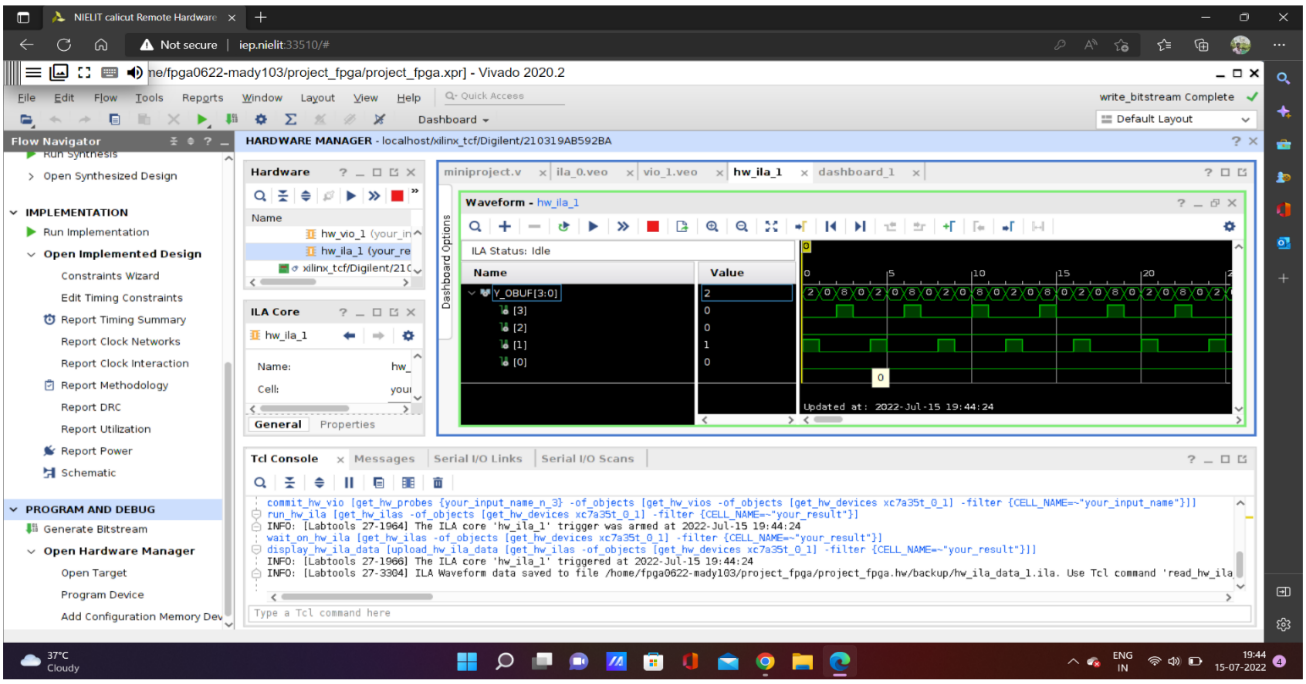




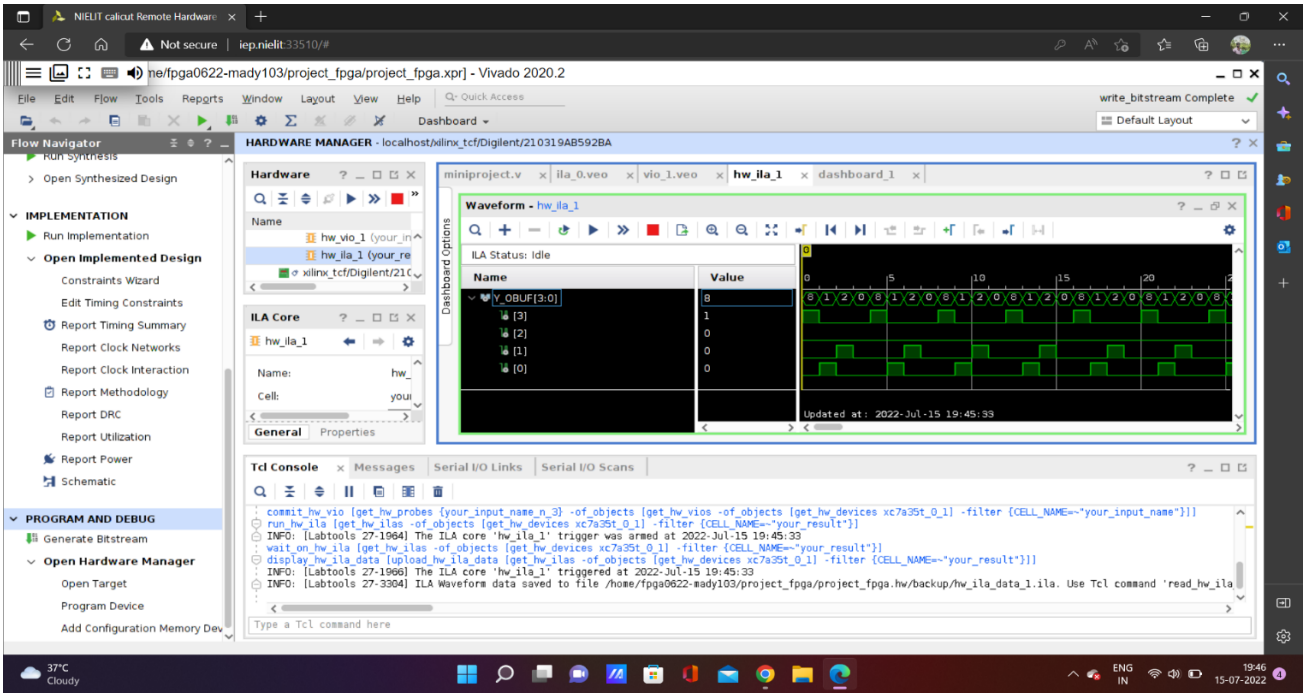
When the input is 4’b0110:



When the input is 4’b1010:



When the input is 4’b1011:


NIELIT calicut Remote Hardware
Not secure | iep.nielit:33510/#
ne/fpga0622-mady103/project_fpga/project_fpga.xpr] - Vivado 2020.2
File Edit Flow Tools Reports Window Layout View Help
write_bitstream Complete
Default Layout
Dashboard
Flow Navigator
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
Add Configuration Memory Dev
HARDWARE MANAGER - localhost/xilinx_tcf/Digilent/210319AB592BA
Hardware
Name
hw_vio_1 (your_in
hw_ila_1 (your_re
xilinx_tcf/Digilent/21
ILA Core
hw_ila_1
Name:
Cell:
General
Properties
Dashboard Options
miniproject.v
ila_0.veo
vio_1.veo
hw_ila_1
dashboard_1
Waveform - hw_ila_1
ILA Status: Idle
Name
Value
Y_OBUF[3:0]
[3]
[2]
[1]
[0]
8
1
0
0
0
Updated at: 2022-Jul-15 19:45:33
Tcl Console
Messages
Serial I/O Links
Serial I/O Scans
commit_hw_vio [get_hw_probes {your_input_name_n_3} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7a35t_0_1] -filter {CELL_NAME=~"your_input_name"}]]
run_hw_ila [get_hw_ilas -of_objects [get_hw_devices xc7a35t_0_1] -filter {CELL_NAME=~"your_result"}]
INFO: [Labtools 27-1964] The ILA core 'hw_ila_1' trigger was armed at 2022-Jul-15 19:45:33
wait_on_hw_ila [get_hw_ilas -of_objects [get_hw_devices xc7a35t_0_1] -filter {CELL_NAME=~"your_result"}]
display_hw_ila_data [upload_hw_ila_data [get_hw_ilas -of_objects [get_hw_devices xc7a35t_0_1] -filter {CELL_NAME=~"your_result"}]]
INFO: [Labtools 27-1966] The ILA core 'hw_ila_1' triggered at 2022-Jul-15 19:45:33
INFO: [Labtools 27-3304] ILA Waveform data saved to file /home/fpga0622-mady103/project_fpga/project_fpga.hw/backup/hw_ila_data_1.ila. Use Tcl command 'read_hw_ila
Type a Tcl command here
37°C
Cloudy
ENG
IN
19:46
15-07-2022