**Design Project Date of Submission: April 04, 2017**

# Table of Content

1. **Introduction…………………………………………………………………………………**
2. **Objective……………………………………………………………………………………..**
3. **Requirements………………………………………………………………………………**
4. **Design Procedure…………………………………………………………………………**
5. **Calculations………………………………………………………………………………….**
6. **Final Design………………………………………………………………………………….**
7. **Simulated Results…………………………………………………….....................**
8. **Conclusion and Remarks ……………………………………………………………..**
9. **References……………………………………………………………………………………**
10. **Appendix………………………………………………………………………………………**

**(1)Introduction:**

A transistor is a semiconductor device. It can be used an Amplifier or as a switch. Transistors are the basic elements in integrated circuits. The major types of transistor are: BJT, MOSFET, UJT etc. In this design project we are working with only BJTs.

**Transistor has three basic configurations: [2]**

**1)** Common Emitter Configuration – has both Current and Voltage gain

**2)** Common Collector Configuration- has Voltage gain but no Current Gain

**3)** Common Collector Configuration- has Current gain but no Voltage Gain

**Bipolar Transistors have the ability to operator within three different regions: [2]**

**1)** Active Region- transistor operates as an amplifier

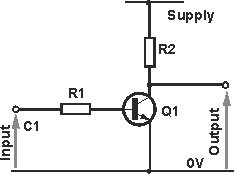
**2)** Saturation mode- transistor is fully – ON operating as a switch

**3)** Cut-off mode- the transistor is fully- OFF operating as a switch

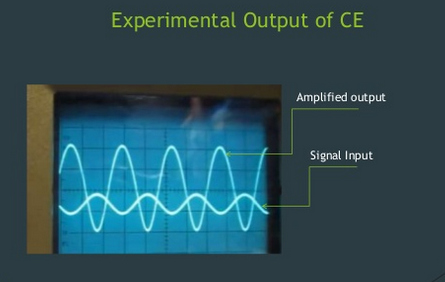
**COMMON EMITTER AMPLIFIER:** In a common emitter, input is applied to the base, output is taken across the collector and the emitter is grounded **[2].**

**Features [2]:**

1. Moderate /high input impedance
2. Moderate output impedance
3. High voltage gain
4. High current gain
5. Output is inverted



**Figure 1: CE Amplifier circuit [3]**

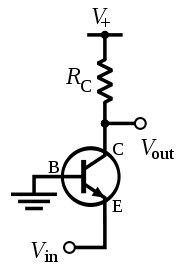


**Figure 2 : shows the signal input and the amplified output [2]**

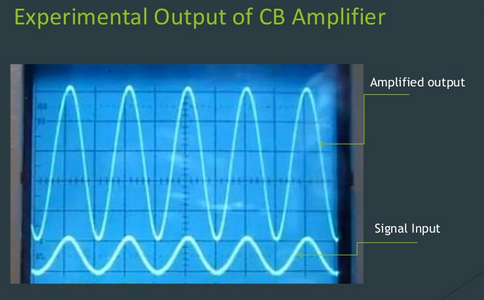
**COMMON BASE AMPLIFIER:** In a common base, input is applied to the emitter, output is taken across the collector and the base is grounded **[2].**

**Features [2]:**

1. low input impedance
2. Moderate/high output impedance
3. High voltage gain
4. Unity current gain
5. Non-inverting amplifier



**Figure 3 the common base amplifier circuit [3]**

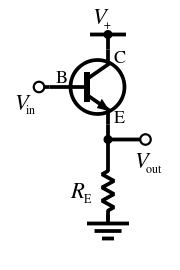


**Figure 4 shows the signal input and the amplified output [2]**

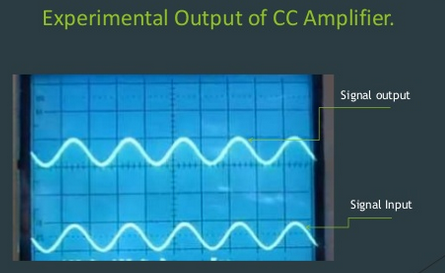
**COMMON COLLECTOR AMPLIFIER:** In a common collector, input is applied to the base, output is taken across the emitter and the collector is grounded [2].

**Features:**

1. Moderate/high input impedance
2. low output impedance
3. low(unity) voltage gain
4. High current gain



**Figure 5: common collector amplifier circuit [3]**



**Figure 6 shows the signal input and the amplified output [2]**

**(2) Objective:** The objective of this design project was to understand how the multistage amplifiers work and can be implemented in different ways to meet the given requirements.

**(3) Requirements**

1.

2. Frequency= 20Hz – 20 KHz

3. Power Supply = 15V

4. Output Resistance = (no larger than 15KΩ)

5. Input Resistance = (no less than 200 kΩ)

6. Quiescent current from power supply= (no larger than 2mA)

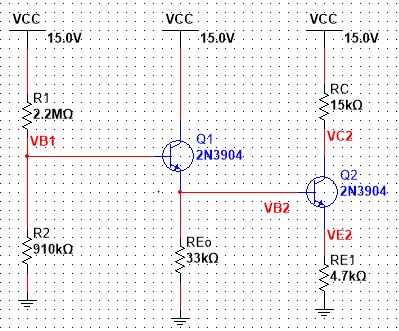
7. Maximum no-load output signal = 8V

**(4) Design Procedure:** Amplifiers are cascaded according to their features to get different desired outputs which is otherwise not possible by a single stage amplifier. In this design project we are looking forward to a multistage design circuit which will have a relatively high input and output impedance of 500KΩ and 15k. Therefore a CC Amplifier followed by a CE Amplifier was used to meet the requirement. The CC voltage gain in the first stage is unity so we can easily get the 50V/V gain from CE amplifier in the second stage without being bothered about the voltage gain contribution by the first stage (CC). Here the CC amplifier provides the high input resistance instead of the CE Amplifier. CC amplifier has a low output resistance so we can only rely on the second stage CE amplifier for the output resistance as CC does not contribute much to it.

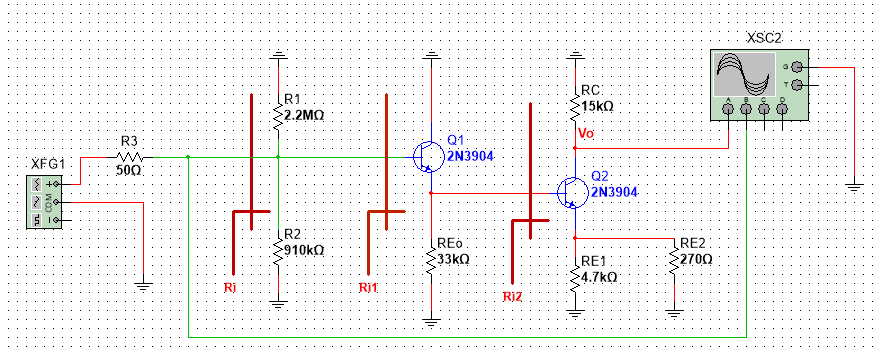
First the R0 which is equal to RC was set to 15K. Then the node voltages and branch currents for second stage Q2 (CE amplifier) was calculated. V E2 was set to 3VBE while doing the calculations. The collector current for Q1 was found by multiplying an arbitrary value with the base current of Q2. The reason for these assumptions are explained below in the calculations. Then the quiescent node voltages and branch currents of both stages were used to calculate the resistor values.

The capacitor values does not have any effect, it is used for the AC coupling and to make sure the DC values are not disturbed while we do the AC analysis.

**(5) Calculations**



**Figure 7: DC analysis replacing the capacitors with open circuit and all AC powers turned off**



**Figure 8: AC analysis circuit with capacitors short circuited and all DC voltages grounded**

* For a good swing (input Signal, ac).

Signal Swing is the difference of maximum output voltage and minimum output voltage. The goal is to get a symmetrical output signal swing for a convenient analysis. Thus the voltage was found out using the average value of VCC and VE to get a suitable output voltage swing.

According to the requirements the output resistance should be no larger than 15kΩ, therefore the is assumed to be 15kΩ.



**Calculating the branch currents:**

Therefore,  **=**

For current stability we take that

All types of transistor amplifiers operate using AC signal inputs which alternate between a positive value and a negative value so some way of “pre-setting” the amplifier circuit to operate between these two maximum or peak values is required [1]. This is achieved using a process known as **Biasing [1]**. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal [1].

To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected [1]. This is in fact the DC operating point of the amplifier and its position may be established at any point along the load line by a suitable biasing arrangement [1]. The best possible position for this Q-point is as close to the center position of the load line as reasonably possible, thereby producing a Class A type amplifier operation, i.e. .

Thus since our we want our to be around, therefore we need to choose in a way that our is around 7.5. Taking this into account was set to which is. Now our value is 6.6V is very close to 7.5V so our purpose is served and now we can expect a stable current.

**According to Requirement**

**Assuming:**

* 50 = =

1+ 16.8 =

* **kΩ**

We know

* Let assume

Q1

**Explanation is given in the Appendix in Figure 9: [4]**

* **mA**

=5.95 + (101×0.240)

=30.2KΩ [CE Amplifier]

=100/3.36 + (101×15.76) =1622.42KΩ

We assume and

Let

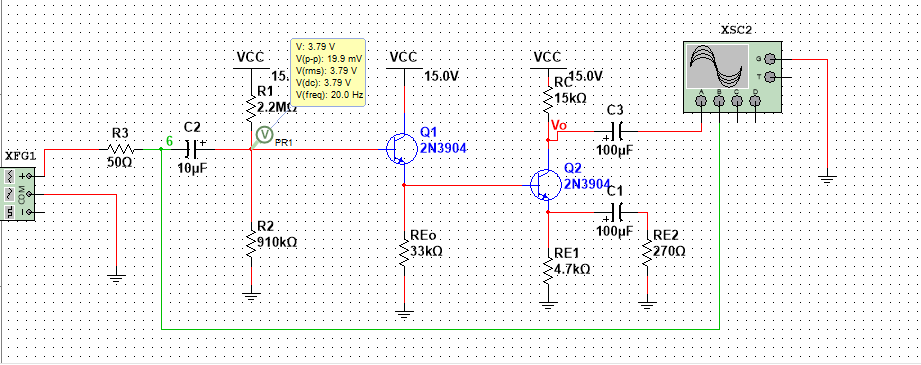
5001622.42

Now,

Voltage Division:

Solving the equations simultaneously we get

**(6) Final Design**

****

**Figure 10: Design Circuit, CC Amplifier cascaded with the CE Amplifier**

Resistors present in the lab kit close to the above calculated values were used to do the circuit:

* **kΩ**

**All the Requirements were met!**

**1.**

**2. Frequency= 20Hz – 20 KHz**

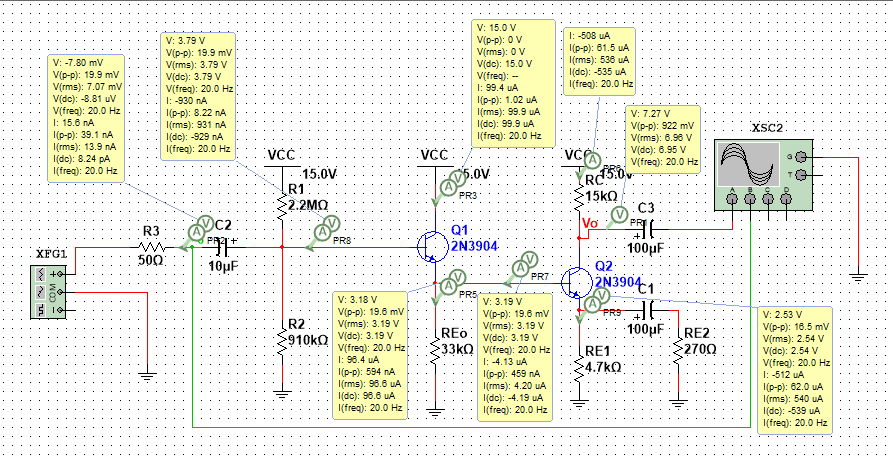
**3. Power Supply = 15V**

**4. Output Resistance = 15KΩ (no larger than 15KΩ)**

**5. Input Resistance = 500KΩ (no less than 200 kΩ)**

**6. Quiescent current from power supply= 8.24pA (no larger than 2mA)**

**7. Maximum no-load output signal = 8V**



**Figure 11: Design Circuit with simulated node voltages and branch currents**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| Calculated values | 15 | 3.50 | 2.80 | 0.084 | 0.000840 | 0.08484 |
| Simulated Values(with the resistors from the lab kit) | 15 | 3.79 | 3.19 | 0.099 | 0.000930 | 0.09660 |
| Percentage error | 0% | 7.65% | 12.2% | 15.1% | 9.68% | 12.2% |

**Table 1: Comparing the node voltages and branch currents between calculated and simulated results**

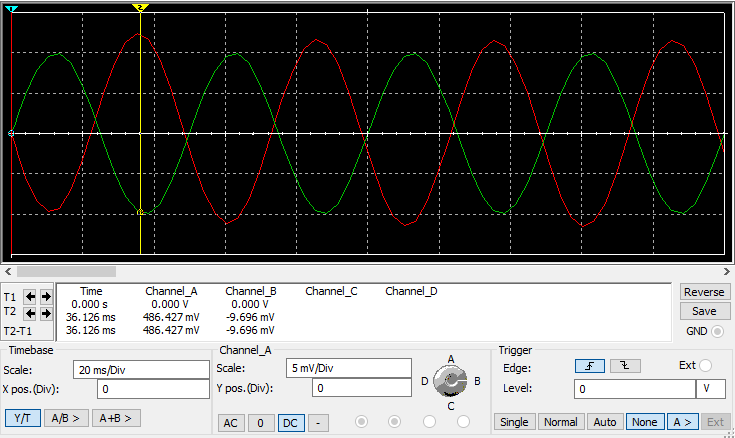
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |
| Calculated values | 8.70 | 2.80 | 2.10 | 0.420 | 0.0042 | 0.424 |
| Simulated Values | 6.95 | 3.19 | 2.54 | 0.535 | 0.0042 | 0.540 |
| Percentage error | 25.2% | 12.2% | 17.3% | 21.5% | 0% | 21.4% |

**Table 1: Comparing the node voltages and branch currents between calculated and simulated results**

|  |
| --- |
| (Close to our assumption of 500KΩ) **[Error=1.6%]**  **[Error=0.3%]**  (In the required range of 50(**[Error=7.9%]** |

**Table 3: Calculations from Figure 11 Simulation**

**Table 1** and **Table 2** shows the percentage error of the quiescent node voltages and branch currents. **Table 3** shows the error of the, Ro and Av0. The percentage error as calculated is quite insignificant. The clear reason for this was that the calculated resistors values were not exactly used during the simulation as they there were not provided in the lab kit. Thus to make sure we can carry out this experiment in the lab, close values of resistors provided were used. The gain is almost the same and in the range of 50( as the difference in the resistance values were really small and can be ignored.

**(7) Simulation Results**

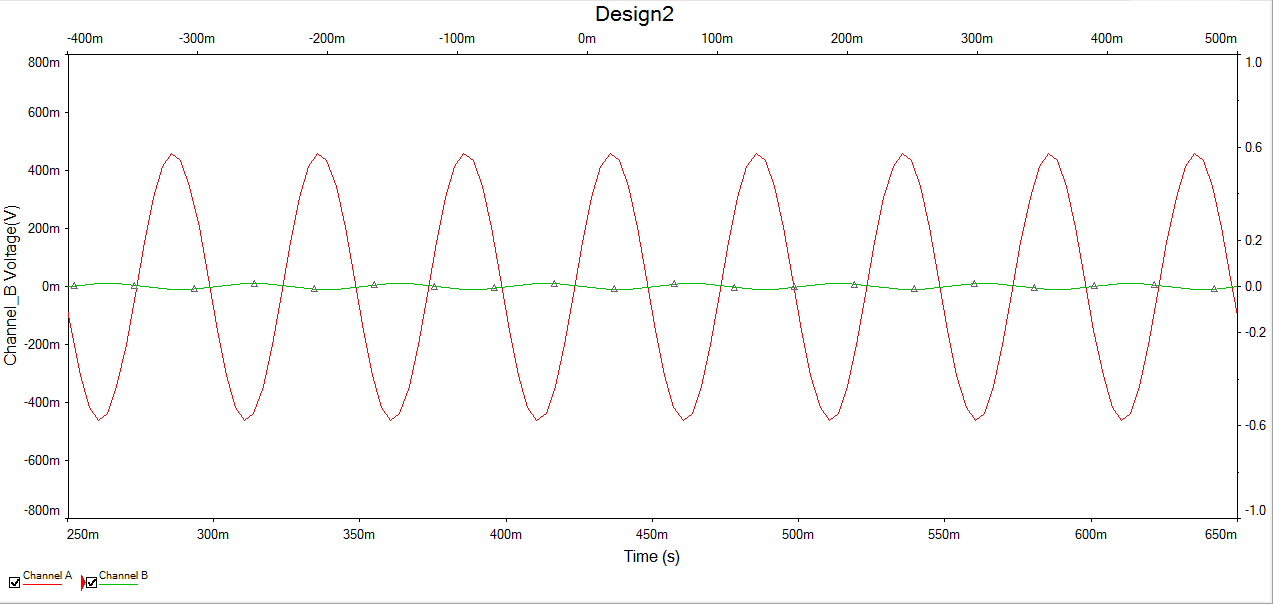
**Graph 1(a) 20Hz with 20mV pk-pk**

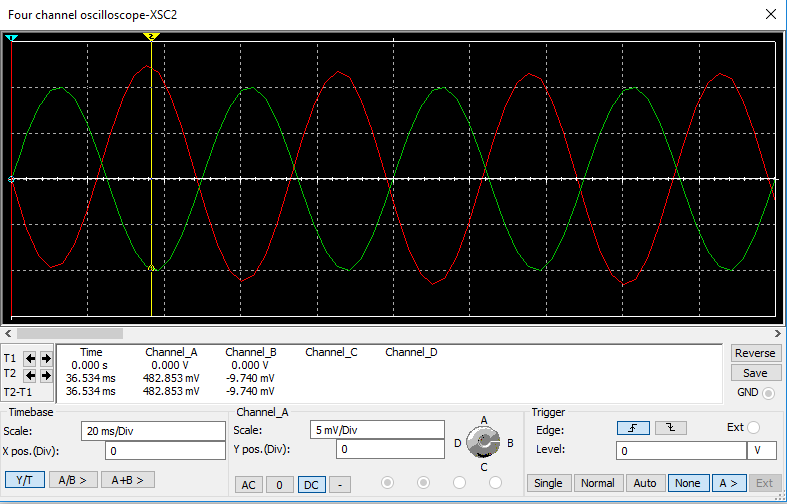
**From the above graph for 20Hz frequency**

Channel A =

Channel B=

(This is good because it is between the required ranges of that is

**Graph 1(b) 20Hz with 20mV pk-pk**



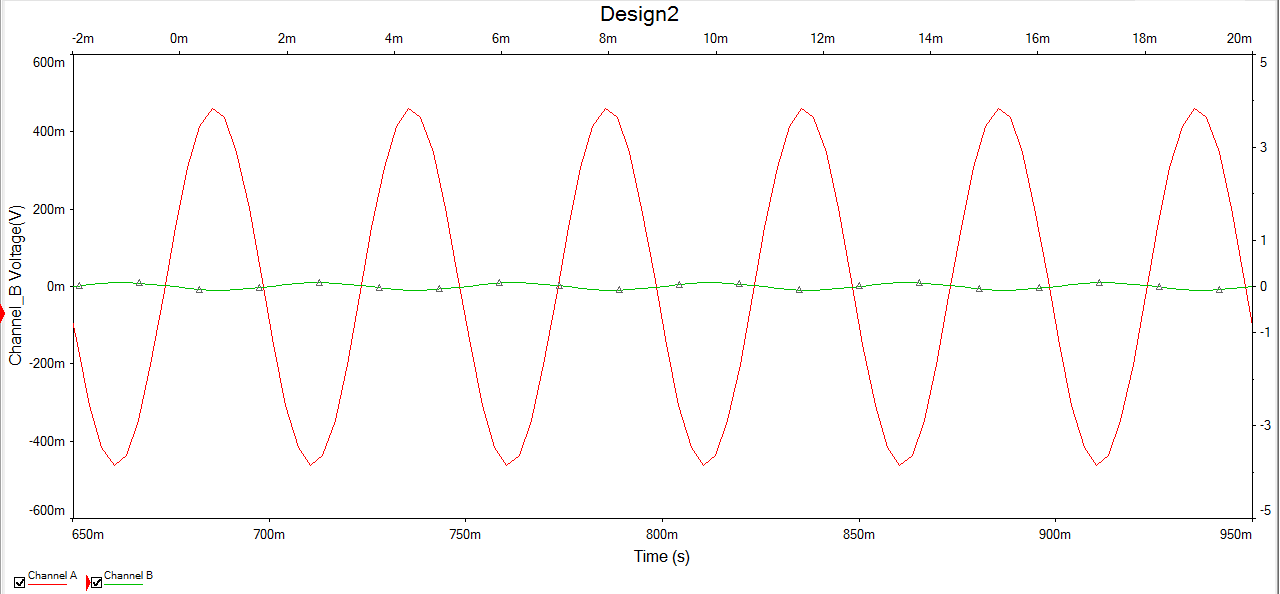
**Graph 2(a) 20 kHz with 20mV**

**From the above graph for 20 kHz frequency**

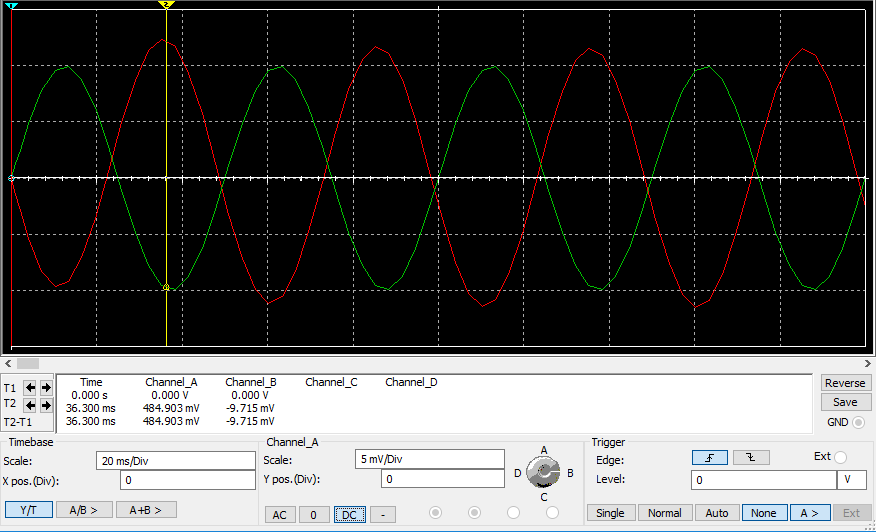
Channel A =

Channel B=

(This is good because it is between the required range of that is



**Graph 2(b) 20 kHz with 20mV**

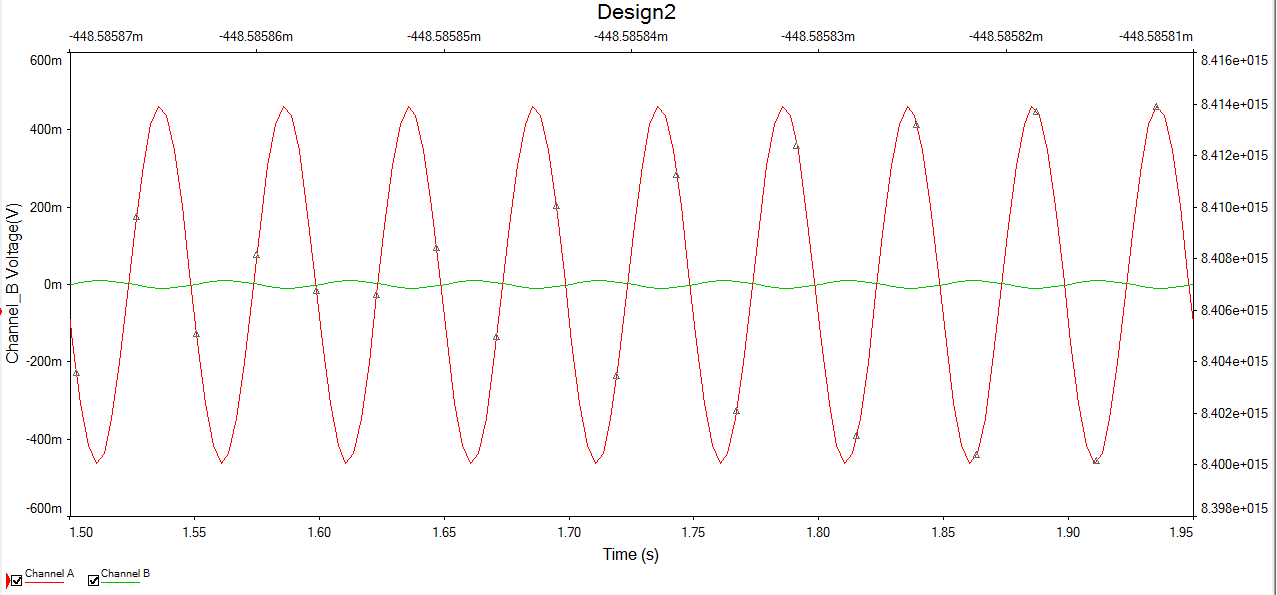
**Graph 3(a): 1 kHz with 20mV**

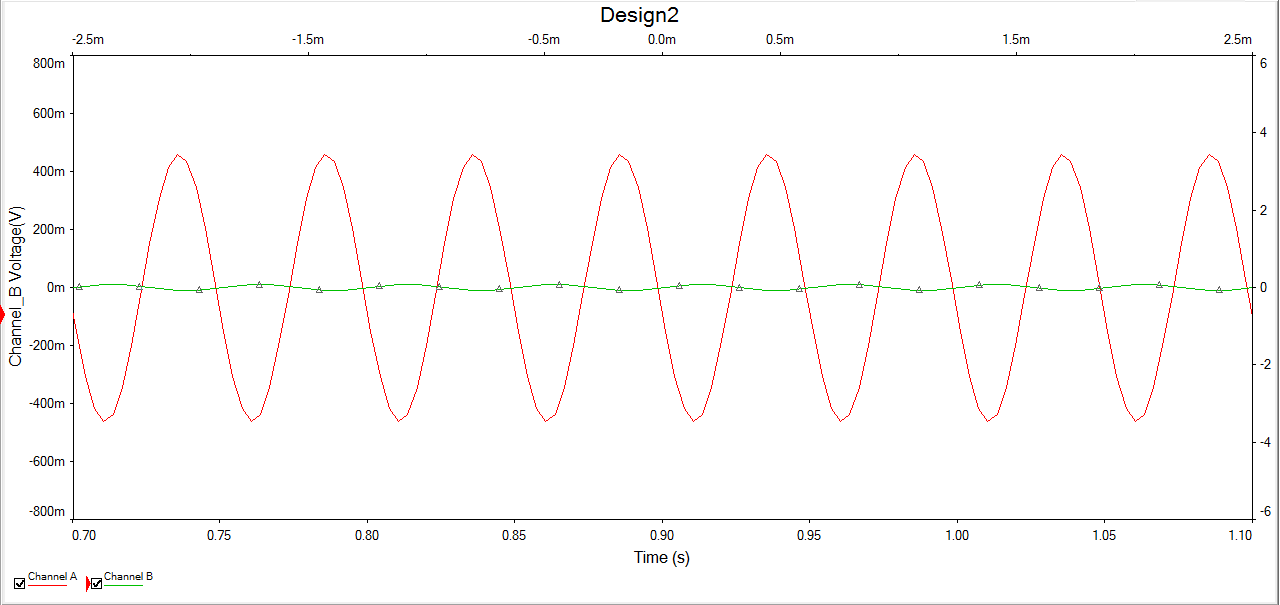
**From the Graph 3(a)**

Channel A =

Channel B=

* ( this is good because it is between the required range of that is

**Graph 3(b) 1 kHz with 20mV**



**Graph 4: 8V pk-pk output voltage swing**

**(8) Conclusions and Remarks:**

**The Stimulated results satisfies all the assumptions and requirements given**.

**Graph 1**: **Graph 1(a)** and **Graph1 (b)** shows the simulation of output voltage VO and input voltage VI at **20 Hz with 20mV pk-pk voltage**. The graph shows a sinusoidal shape for both input and output voltage. In graph1 (b) the peak-peak output voltage has a much higher amplitude compared to the input peak-peak voltage. This can be confirmed looking at the Channel A (output signal) and Channel B (input signal) values in Graph1 (a) and the calculations below. The output signal is about 486.427 V and the input signal is about 9.696V which says that the output signal is amplified by a gain of.

**Graph 2**: **Graph 2 (a)** and **Graph 2 (b)** shows the simulation of output voltage VO and input voltage VI at **20 KHz with 20mV pk-pk voltage**. The graph shows a sinusoidal shape for both input and output voltage like in Graph 1. In Graph 2 (a) it shows that the voltage gain is around **49.5 V/V**. The percentage error in voltage gain at **20Hz and 20 kHz** is

This shows that the voltage gain remains same between the frequency range of **20Hz and 20 KHz** as the percentage error is clearly negligible.

**Graph 3: In Graph 3 (a),** circuit was simulated at a frequency of **1 KHz with 20mV pk-pk voltage**. The voltage gain calculated was around. The gain is inside the required range.

**Graph 4: In graph 4** simulation, a large enough input signal was applied around **12V pk-pk voltage** to get an output voltage swing of **8V peak-peak in magnitude**.

**(9) References**

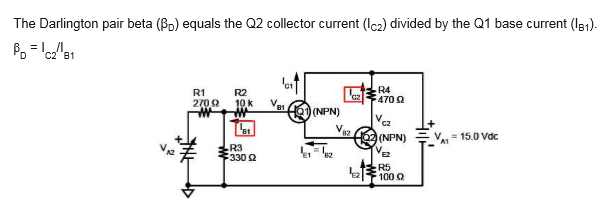
**[1]** Common Emitter Amplifier and Transistor Amplifiers. (2017, January 16). Retrieved April 04, 2017, from http://www.electronics-tutorials.ws/amplifier/amp\_2.html

**[2]** Bharath405 Follow. (2015, April 07). CE, CB, CC AMPLIFIERS. Retrieved April 04, 2017, from <https://www.slideshare.net/bharath405/mini-project-presentation-46723110>

**[3]** Common Emitter Amplifier Design. (n.d.). Retrieved April 04, 2017, from <http://www.radio-electronics.com/info/circuits/transistor/common-emitter-amplifier-design.php>

**[4]** www1.labvolt.com/publications/Exercises/91566-p0\_6-1.pdf

**(10) Appendix**



**Figure 9: [4]**