

## **Chapter 2**

### **The Sourcebox Unit**

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The Sourcebox unit described in this chapter contains all the circuitry common to virtually all the TV games described in this book. It is the interface unit that stands between the game itself and the TV receiver. The Sourcebox unit, for instance, generates all the sync and blanking signals that synchronize both the TV raster and the game operations. Unless this system is built and made to operate properly, the experimenter cannot hope to make any real progress in his or her understanding of anything else that follows.

This chapter describes the theory of operation, shows complete circuit detail, and provides some practical hints on construction. The opening section of Chapter 2 gives the experimenter an opportunity to test the system.

The block diagram in Fig. 2-1 shows the basic circuits contained in the Sourcebox unit. The purpose of each block might be self-evident to anyone who has made a thorough study of the material in Chapter 1. The following sections of this chapter, however, describe the purpose and theory of each block in some detail. The construction hints are inserted at appropriate places in the discussion, rather than at the end of the chapter.

#### **SOURCEBOX ORGANIZATION**

The Sourcebox unit is organized into 10 basic circuits as described here:

1. *Power supply*—The power supply provides DC voltage levels to all of the circuits in the Sourcebox unit as well as

plug-in game modules and the so-called tinkerboxes (breadboard units intended for self-learning experiments and game design). With the notable exception of the +1.5-V supply voltage for the rf modulator, the power supply gets its power from a standard 120-VAC, 60-Hz source.

2. *7-MHz oscillator*—This is the master clock oscillator for the entire TV game system. For best results, this should be a crystal-controlled, 14-MHz oscillator, followed by a toggling flip-flop that both divides the crystal frequency by two and assures a clean, 7-MHz HCLK waveform.
3. *Horizontal-count source*—The horizontal-count source generates a 9-bit binary counting code that divides the game screen into 455 equal horizontal segments. Each horizontal scan line on the screen is thus divided into 455 discrete sections, each of which is capable of rendering one bit of horizontal video information.

The nine binary-counting outputs are labeled 1H, 2H, 4H, 8H, and so on through 256H, with 1H being the least-significant (highest-frequency) output and 256H being the most-significant output bit.

The horizontal-count source also generates an HRST (Horizontal ReSeT) pulse that is used for clocking the vertical-count source and synchronizing the operation of some game circuits. An inverted version of this positive-going HRST pulse, designated  $\overline{\text{HRST}}$ , is used for generating horizontal-sync pulses.

4. *Horizontal sync and blanking generator*—The inverted HRST pulse from the horizontal-count source is converted to horizontal sync and blanking pulses in this part of the Sourcebox unit. The horizontal-sync pulse (HSYNC) ultimately triggers the TV's horizontal retrace operation. The horizontal-blanking pulse (HBLANK) is likewise used for blanking horizontal retrace on the TV screen and for certain kinds of control operations for the video games.
5. *Vertical-count source*—The vertical-count circuit is almost identical to its horizontal counterpart. It generates a 9-bit binary count that divides the receiver's raster into 262 vertical segments, or lines. In a manner of speaking, this circuit provides information regarding the position of the TV's beam in the vertical sense.

Like the horizontal-count source, the nine outputs are labeled 1V through 256V, with 1V being the least-

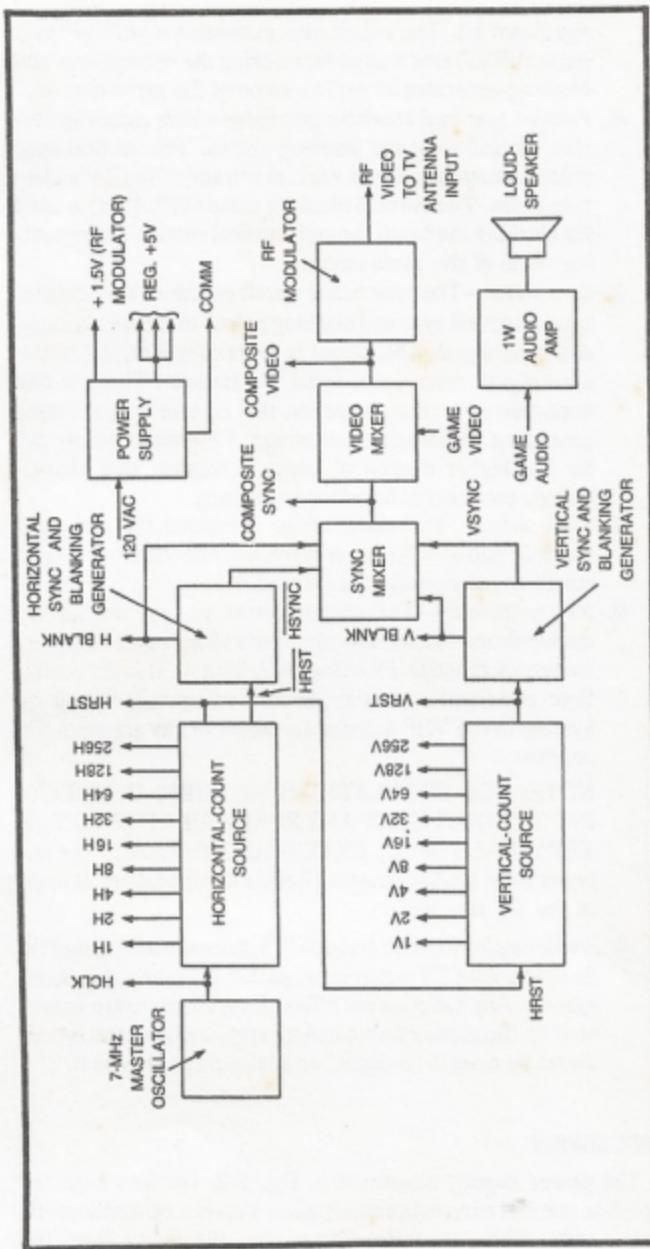


Fig. 2-1. Block diagram of the Sourcebox unit.

significant bit. The circuit also generates a vertical-reset pulse (VRST) that is used for clocking the vertical sync and blanking generator as well as some of the game circuits.

6. *Vertical sync and blanking generator*—This circuit generates vertical sync and blanking pulses. The vertical-sync pulse ultimately initiates vertical retrace of the TV's electron beam. The vertical-blanking pulse (VBLANK) is used for blanking the beam through vertical retrace and operating some of the game circuits.
  7. *Sync mixer*—The sync mixer circuit combines the horizontal and vertical sync and blanking pulses to create a composite sync signal. This signal is practically identical to the sync signals from commercial TV stations. There is one important exception, however; this system does not have provisions for interlaced scanning. Few video games call for the higher degree of image resolution that characterizes commercial interlaced scanning.
  8. *Video mixer*—The video mixer combines the sync and blanking pulses with game video information to provide a complete, composite video signal.
  9. *RF modulator*—The rf modulator is responsible for amplitude modulating the composite video signal with an rf frequency tuned to TV channels 2, 3, or 4. This part of the Sourcebox unit makes it possible to connect the game system to the VHF antenna terminals of any standard TV receiver.
- NOTE: FCC REGULATIONS PROHIBIT CONNECTING THE OUTPUT OF ANY RF MODULATOR TO THE TERMINALS OF AN EXTERNAL ANTENNA. The antenna must be disconnected before the modulator is fixed to the TV receiver.
10. *Audio amplifier*—The audio for TV games is not carried via the composite TV signal through the receiver's own audio system. Any audio special effects for a TV game are generated by the game system and merely amplified and reproduced by a small loudspeaker in the Sourcebox unit.

## POWER SUPPLY

The power supply, illustrated in Fig. 2-2, services both the Sourcebox unit and external game circuits. This is a conventional IC power supply, taking its main power from the utility lines and

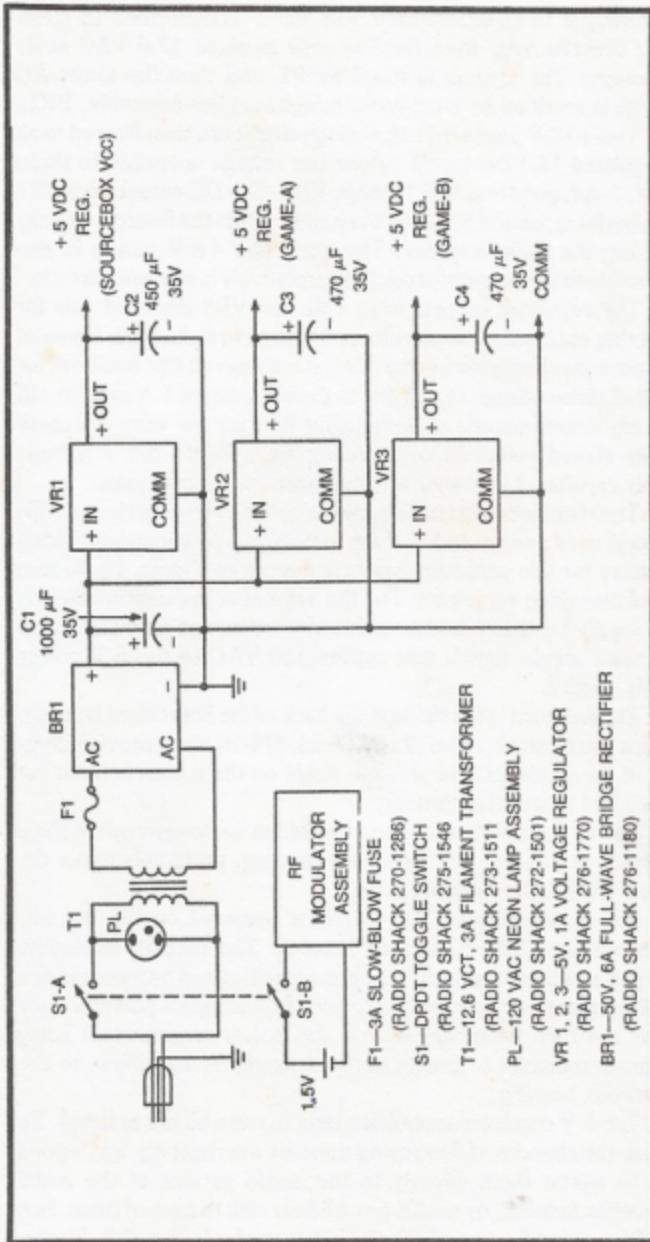


Fig. 2-2. Power supply schematic diagram.

converting it to an unregulated +18 VDC. Transformer T1 steps down the 120 VAC from the line cord to about 12.6 VAC at its secondary. The system is fused by F1, and then the lower AC voltage is rectified by a full-wave bridge rectifier assembly, BR1.

The +18-V peaks from the bridge circuit are then filtered to an unregulated 18 VDC by C1 before the voltage is applied to three +5-V, 1-A regulators, VR1 through VR3. The DC output from VR1 supplies its regulated 5-V level to circuits within the Sourcebox unit, including the audio amplifier. This particular +5-V source is also accessible to the outside for operating relatively low-power circuits.

The regulated outputs from VR2 and VR3 are used only for powering external game circuits and design breadboards. Some of the more involved video games described later in this book call for using all three voltage regulators to their maximum 1-A capacity. In fact any experimenter contemplating designs for very elaborate games should count on constructing an outboard 5-V regulated supply capable of providing an additional one or two amps.

The rf modulator assembly, described in more detail later in this chapter, uses a separate 1.5-V AA battery as a power supply. Using a battery for this particular application ensures a clean, ripple-free modulated video waveform. For the sake of convenience, the battery supply for the rf modulator is switched on and off by means of the same toggle switch that applies 120 VAC to the 5-V power supply section.

The line cord is fed through the back of the Sourcebox housing, using a plastic strain relief (Radio Shack 278-1636) to prevent abrasion of the insulation and possible strain on the connections to the switch and power transformer.

Power switch S1 should be mounted at some convenient place on the front panel of the Sourcebox housing, preferably under the neon POWER ON indicator lamp.

Power transformer T1 should be mounted on the bottom, inside surface of the Sourcebox housing. The rectifier assembly, fuse and fuse holder, and all four filter capacitors can be mounted to a small perfboard or custom PC board. This compact power supply board can then be mounted near the power transformer, using insulated standoffs to prevent any short-circuit conditions to the Sourcebox housing.

The 5-V regulator assemblies tend to run a bit hot at times. To reduce the chances of destroying them by overheating, it is a good idea to mount them directly to the inside surface of the metal Sourcebox housing, or to affix a small heat sink to each of them. See the dimensions for one of the three heat sinks in Fig. 2-3. Similar

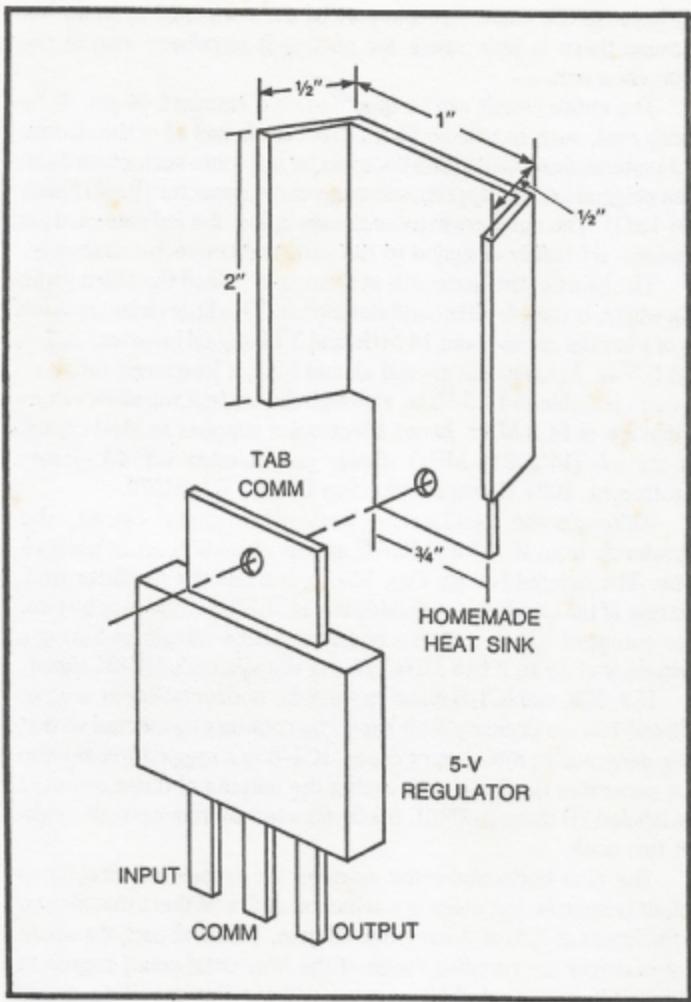


Fig. 2-3. Recommended heat sink for the voltage regulators.

heat sinks are available commercially, but it is rather easy to cut and bend custom versions from standard 1/16-in. aluminum stock.

#### HORIZONTAL SOURCE BOARD

Figure 2-4 is a complete schematic diagram for the circuit that generates all the horizontal counting, sync, blanking, and reset pulses. This particular circuit board also holds the audio amplifier IC,

not because the audio signal is part of the horizontal system, but because there is little space for putting it anywhere else in the Sourcebox unit.

The entire circuit can be mounted on a standard 44-pin, 4- by 4-inch card, such as a Radio Shack 276-153. In fact all of the circuits and systems described in this book can be built onto such a board and then plugged into the appropriate edge-card connector (Radio Shack 276-1551). The numbers in parentheses in Fig. 2-4 indicate card pin numbers arbitrarily assigned to the card-and-connector assembly.

The heart of the horizontal system, and indeed the video game as a whole, is the 14-MHz oscillator circuit. This little circuit is made up of a crystal cut to about 14 MHz and TTL digital inverters IC7-A and IC7-B. Actually the crystal should have a frequency rating as close as possible to 14.3 MHz, although the system will allow values within 2% of 14.3 MHz. James Electronics supplies an ideal crystal for the job (14.31818 MHz). Order part number CY14A, James Electronics, 1021 Howard Ave., San Carlos, CA 94070.

Although the oscillator is basically a digital circuit, the waveforms from IC7-A and IC7-C appear sinusoidal on an oscilloscope. The toggled J-K flip-flop, IC1-A, isolates the oscillator from the rest of the circuitry and divides the 14.3-MHz frequency by two. The output of IC1-A is thus a quasi-sinusoidal waveform having a frequency close to 7.015 MHz. This is the system's HCLK signal.

IC2, IC3, and IC1-B make up the 9-bit horizontal-count source. IC2 and IC3 are ordinary 4-bit binary up counters connected so that they generate an 8-bit binary count. IC1-B is a toggled J-K flip-flop that generates the 9th bit. Note that the outputs of these counters are labeled 1H through 256H, the labels used so frequently throughout this book.

The nine horizontal-count sources are connected directly to output terminals, but there is a selection of five of them that also go to the inputs of IC4, an 8-input NAND gate. This is all part of a circuit that restricts the counting range of the horizontal-count source to 455 HCLK pulses. A 9-bit counter without this resetting circuit would count 511 states.

The resetting circuitry senses a count of 454 at IC4, generating a negative-going pulse at the D input of IC5A. IC5A is an edge-triggered D flip-flop which sets its Q output to the D-input logic level whenever its CLK input shows a positive-going edge. IC5-A is clocked by HCLK in this case; and as long as the horizontal-count source is generating numbers less than 454, the Q output of IC5-A remains at a logic-1 level. The complemented output from  $\overline{Q}$  is at logic 0 at the same time.

One HCLK pulse after the count reaches 454, however, IC5-A loads its Q output with a logic-0 level and the  $\bar{Q}$  output takes on a logic-1 level. This condition immediately clears all nine bits from the horizontal-count source to zero, thus restarting the 455-step operation all over again.

The signal from the Q output of IC5-A is thus a negative-going pulse that lasts for one HCLK pulse interval and occurs at the very beginning of each horizontal-count cycle. A positive-going version of that same pulse, HRST, is directed to IC2, IC3, and the plug assembly leading to the outside world.

The circuit build around the four 2-input NAND gates of IC6 are responsible for generating the horizontal blanking (HBLANK) and inverted horizontal sync (HSYNC) pulses. IC6-B and IC6-C make up what is commonly known as a  $\bar{R}-\bar{S}$  flip-flop. Whenever the negative-going HRST pulse is directed to the pin-10 input of IC6-C, the output of that same IC is set to a logic-1 level. The device remains in that state while the horizontal-count source is cleared and restarted. The moment the count reaches 80, as determined by the 16H and 64H inputs to IC6-A, this flip-flop circuit is reset so that the pin-8 output of IC6-C returns to logic 0. This point then remains at logic 0 until another HRST pulse occurs.

The real significance of the output of IC6-C is that it generates the system's HBLANK pulse, a positive pulse that begins as the horizontal-count circuit is reset to zero and ends 80 HCLK pulses later. Ultimately the beam on the TV screen will be blanked off through this 80-pulse, horizontal blanking interval.

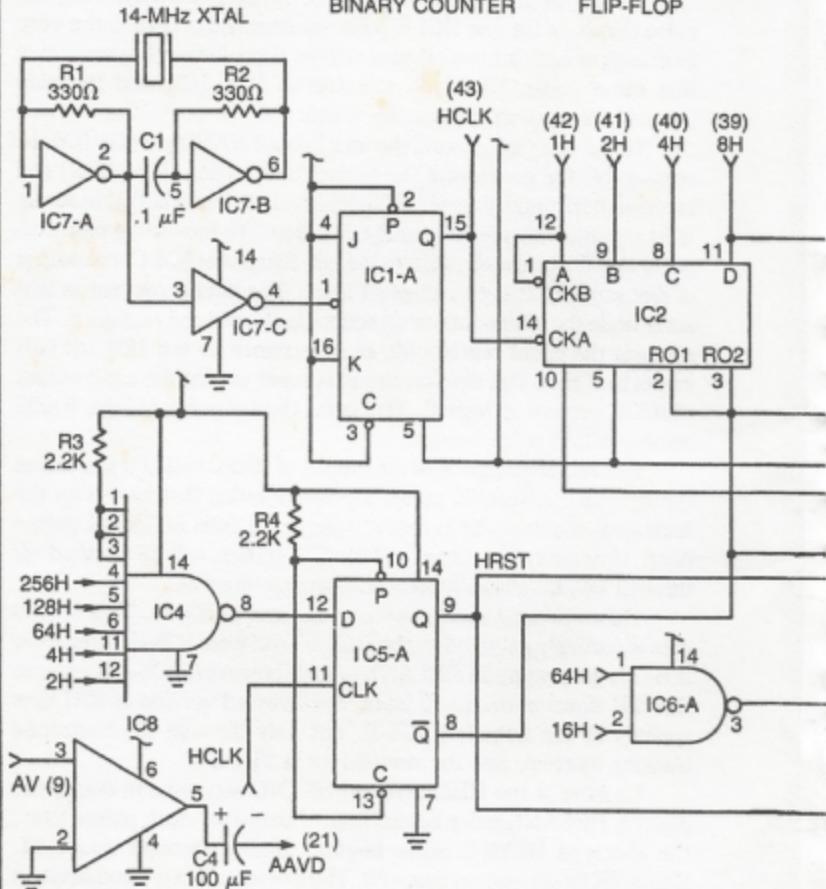
The horizontal sync pulse is generated at IC6-D. This NAND gate is normally gated off by the logic-0 level from IC6-C. Whenever IC6-C is generating an HBLANK signal, however, IC6-D is open to the 32H signal at its pin-12 input. An inverted version of 32H thus appears at the output of IC6-D, but only through the horizontal blanking interval. See the waveforms in Fig. 2-5.

Looking at the HBLANK and HSYNC sequence in detail, the positive HBLANK pulse begins first. Thirty-two clock pulses later, the inverted HSYNC pulse begins, lasting through count 64. HBLANK finally ends at count 80. The overall effect is a combination of horizontal blanking and sync pulses that work very much like their counterparts in a commercial TV broadcast signal.

The only purpose of audio amplifier IC8 is to amplify any special-effects sounds and match the circuit to an 8-ohm loudspeaker. Since audio special effects are not described until Chapter 10, the volume control and loudspeaker need not be connected at this time.

IC1—7476 DUAL  
J-K FLIP-FLOP  
IC2, 3—7493 4-BIT  
BINARY COUNTER

IC4—7430 8-INPUT  
NAND  
IC5—7474 DUAL-D  
FLIP-FLOP



IC6—7400 QUAD  
2-INPUT NAND  
IC7—7404 HEX  
INVERTER

IC8—LM386 AUDIO  
AMP

NOTES:

(1) NUMBERS IN PARENTHESSES  
INDICATE PLUG CONNECTION  
NUMBERS  
(2) =  $\frac{1}{2}$  COMM;  $\frac{1}{4}$  = 5V (34)  
256H

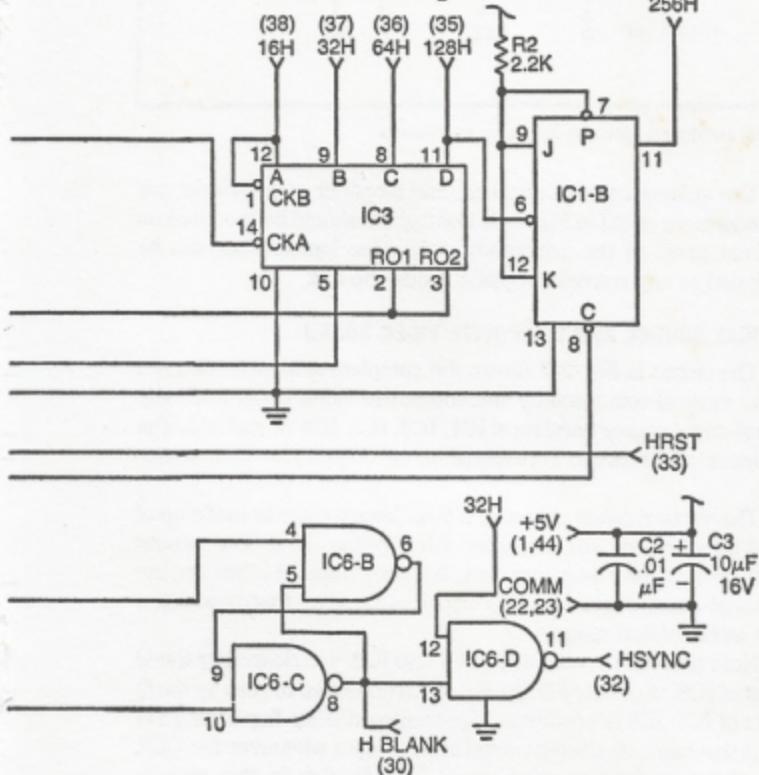


Fig. 2-4. Horizontal source board schematic diagram.

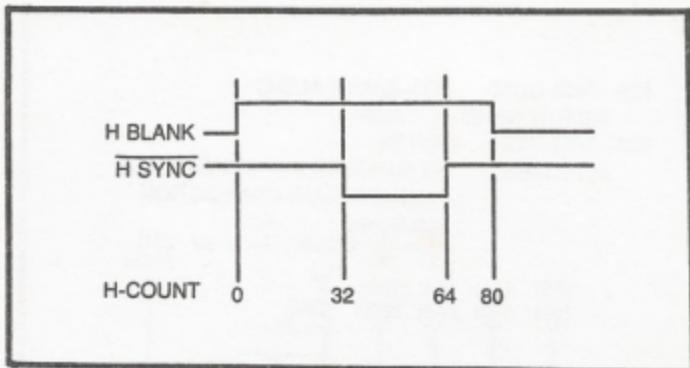


Fig. 2-5. Horizontal blanking and sync waveforms.

The volume control, speaker, and amplifier arrangement are shown in more detail in Fig. 2-6. Control R5 should be mounted on the front panel of the Sourcebox, while the loudspeaker can be positioned at any convenient place inside the box.

#### VERTICAL SOURCE AND COMPOSITE VIDEO BOARD

The circuit in Fig. 2-7 shows the complete schematic diagram for the vertical-count source and composite video generator. The vertical-count source consists of IC1, IC2, IC3, IC4-A, and IC5. The remainder of the circuit is responsible for composite video operations.

The vertical-count source is a 9-bit binary counter made up of two 4-bit counters and a toggled J-K flip-flop, IC3. The natural counting range for a 9-bit counter is between 0 and 511; but like the horizontal-count generator, this circuit is fixed so that it counts a much more limited range.

Note that the two counters, IC1 and IC2, are cleared by the  $\bar{Q}$  output of IC5, while the J-K flip-flop (IC3) is cleared to zero by the Q output of IC5. IC5 is a positive-edge triggered D flip-flop having a Q output that takes on the logic level of its D input whenever the CLK input shows a positive-going edge. The flip-flop in this case is clocked by HRST from the Horizontal Source board—at a frequency very close to 15,750 Hz.

NAND gate IC4-A keeps the D input to IC5 pulled up to logic 1 most of the time, so the repeated HRST pulses at the CLK input keep the Q output of IC5 fixed at logic 1 most of the time. There is a time, however, when the D input to IC5 is set to logic 0: when the 1V, 4V and 256V inputs to IC4-A show logic 1 at the same time. This

condition represents count 261 from the vertical-count source, and it is responsible for clearing the counters back to zero.

The vertical-count section thus generates 260 different patterns representing that many vertical lines on the screen.

The vertical-blanking and sync pulses are generated in a fashion almost identical to the corresponding horizontal section. One difference is that this circuit is built around a flip-flop triggered by positive-going, rather than negative-going, pulses.

The VBLANK generating flip-flop is composed of NOR gates IC6-A and IC6-B. The pin-4 output of IC6B is at logic 0 most of the time, rising to logic 1 only when a VRST (vertical reset) pulse occurs at the Q output of IC5. This pulse sets the pin-4 output of IC6-B to logic 1 and, as described earlier in this section, clears the vertical-count source to zero.

The VBLANK signal remains at this logic-1 level until the 16 V signal at the input of IC6-B goes to logic 1. This action returns the pin-4 output of IC6-B to zero and, in fact, forces it to remain at 0 until another VRST pulse occurs.

The VBLANK signal thus goes to logic 1 the instant the vertical counters are reset to zero, and it remains in that condition until the counters increment to count 16. VBLANK can then be described as a positive-going pulse that lasts 16 HRST pulses.

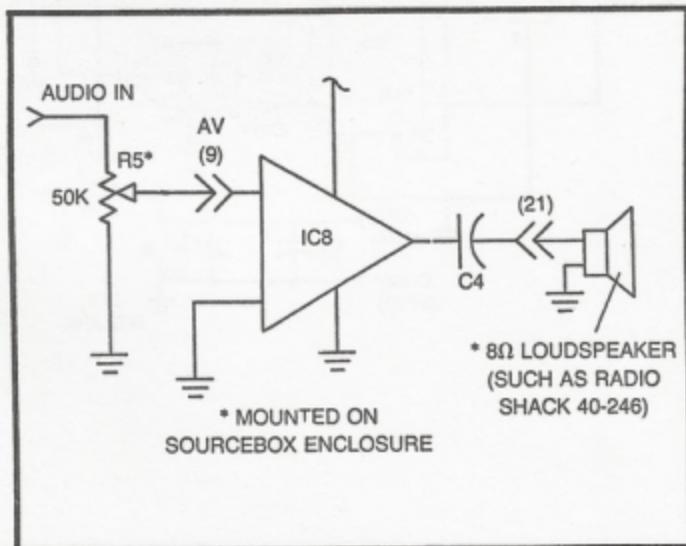
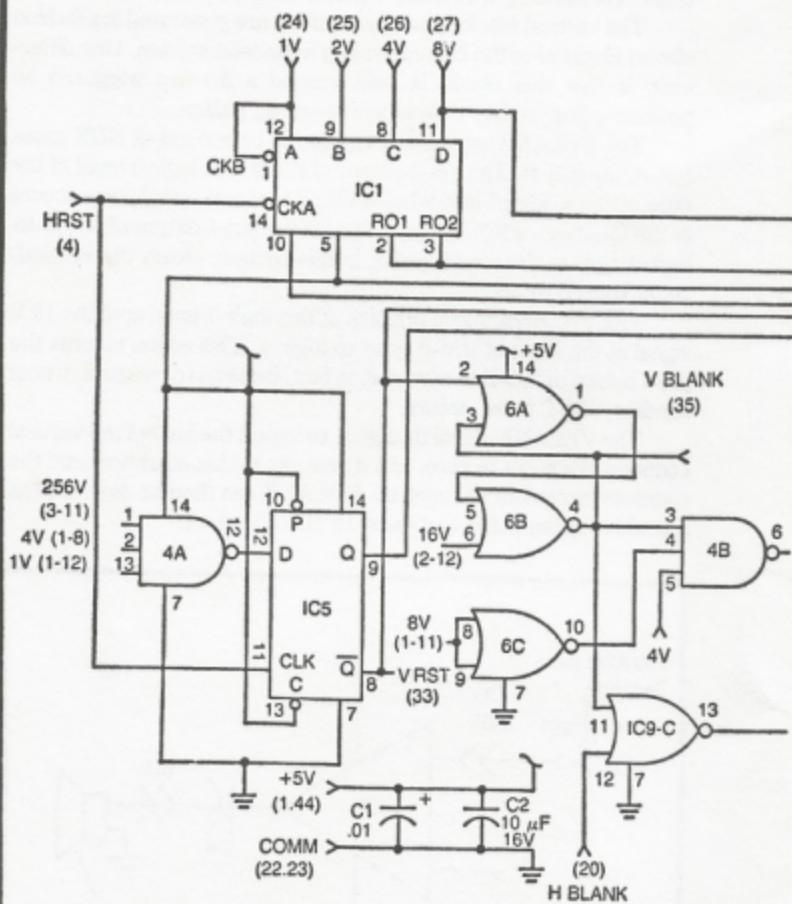


Fig. 2-6. The complete audio amplifier system.



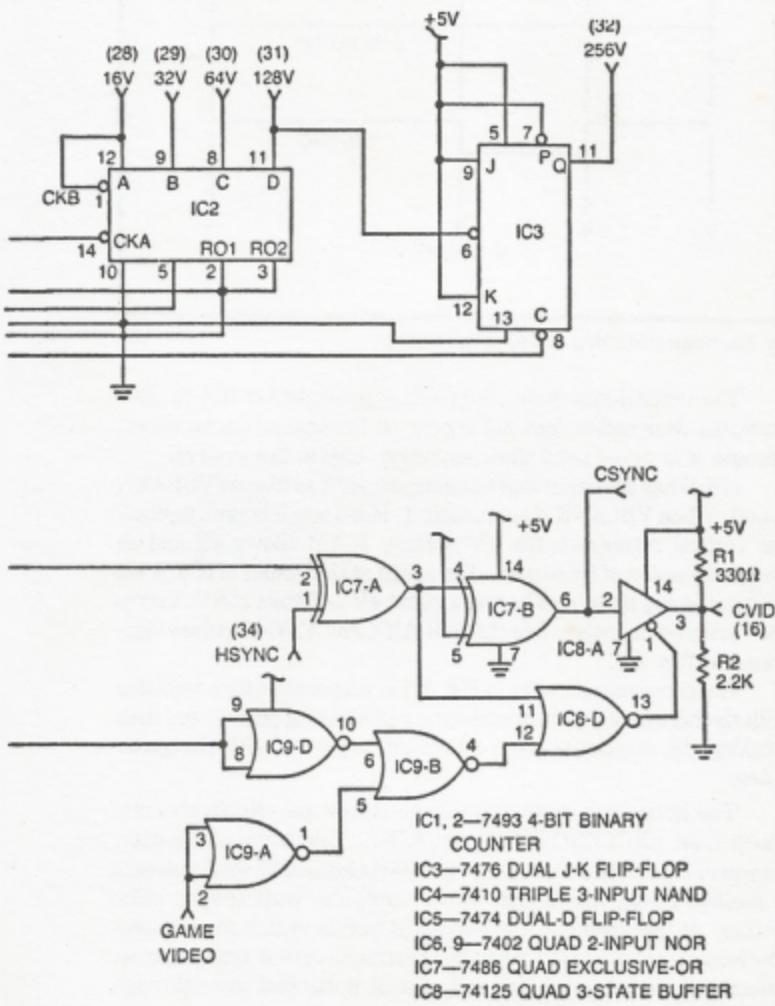


Fig. 2-7. Vertical source and composite video board schematic.

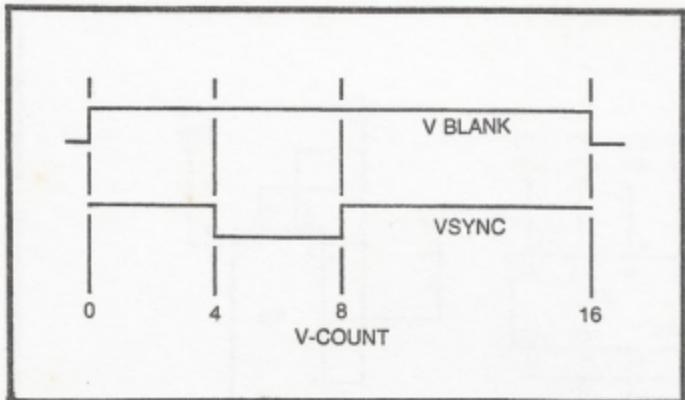


Fig. 2-8. Vertical blanking and sync waveforms.

The vertical-sync pulse, VSYNC, is generated at IC4-B. This particular designation does not appear on the schematic, however, because it is never used alone anywhere else in the system.

IC4-B has an output that remains at logic 1 as long as VBLANK is at 0. When VBLANK rises to logic 1, indicating it is time to blank the vertical retrace on the TV screen, IC4-B allows 4V and an inverted version of 8V to pass. The result at the output of IC4-B is a negative-going pulse that begins a count 4V and ends at 8V. This is the vertical-sync pulse. See the VBLANK and VSYNC pulses illustrated in Fig. 2-8.

The remaining circuitry in Fig. 2-7 is responsible for combining both the horizontal- and vertical-sync and blanking pulses, and then working the composite sync waveform together with the game video.

The horizontal- and vertical-sync pulses are effectively combined in the EXCLUSIVE-OR gate, IC7-A. The output of this gate, shown in Fig. 2-9(a), shows the 15,750-Hz horizontal sync pulses in a positive-going, active-high format until the vertical-sync pulse occurs. At that moment, the horizontal pulses switch to an active-low format, providing the effect of a serrated vertical-sync pulse, an effect that is necessary for maintaining horizontal sync through vertical sync and retrace.

IC7-B serves merely as an inverter for obtaining an inverted version of this composite sync signal.

The horizontal- and vertical-blanking pulses are ORed together in IC9-C and IC9-D, and then these combined signals are ORed with the game video in IC9-B. The output of IC9-B is thus a combination

of horizontal- and vertical-blanking pulses and any game video applied from external circuitry to IC9-A.

These two sets of waveforms—the composite sync from IC7-B and video and blanking pulses—are finally amplitude modulated at the 3-state buffer, IC8-A. A precise analysis of this operation is left to experimenters who have some experience with Boolean algebra. The overall effect, however, is shown in Fig. 2-9(b).

The composite video waveform in Fig. 2-9(b) clearly shows three distinct voltage levels. The highest voltage level, about +5V, is the domain of the blacker-than-black sync pulses. At the other extreme is the white-video information, at about 0V. Black-video information and the blanking pulses fall between these two extremes, occurring only when the 3-state buffer is put into its high-impedance state by the output of IC6-D.

The vertical-count and composite-video board in Fig. 2-7 can be assembled on the same kind of 44-pin edge card that the horizontal section is. Both boards should be situated in their respective edge-card connectors in the Sourcebox housing.

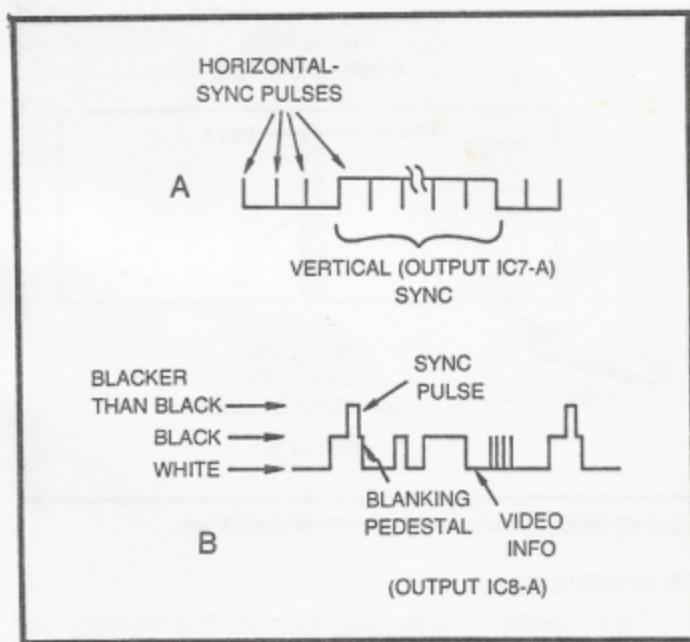


Fig. 2-9. Composite waveforms. (a) Composite sync. (b) Composite video to the modulator.

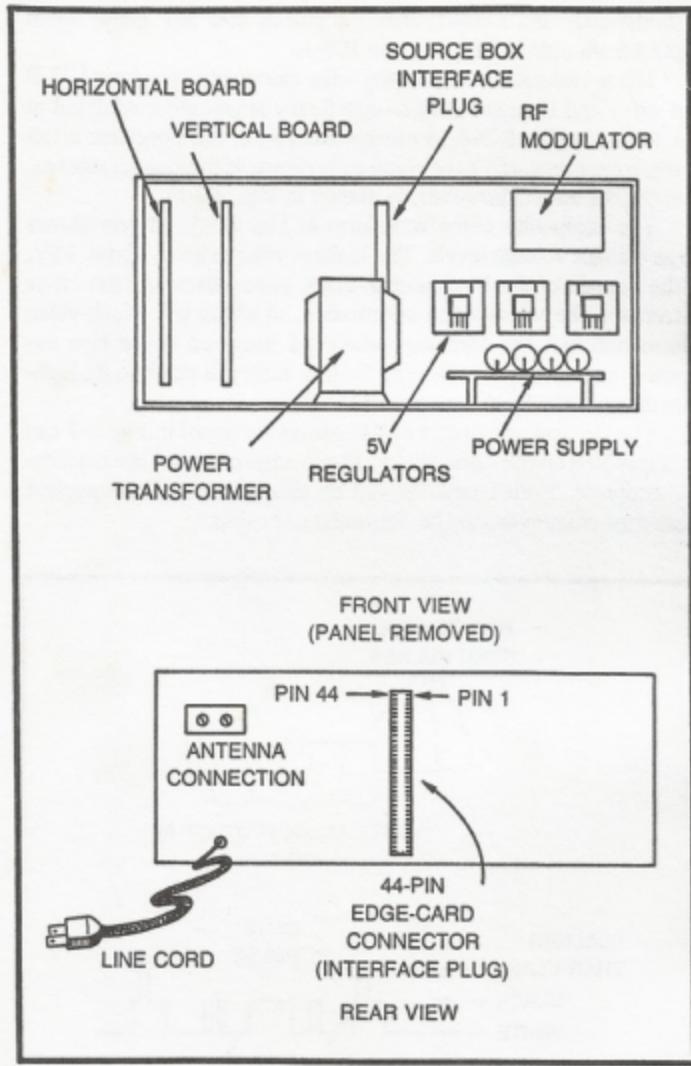


Fig. 2-10. Suggested cabinet layout for the Sourcebox unit.

### THE RF MODULATOR

The rf modulator is responsible for modulating the composite video (CVID) from the vertical/video board at a VHF frequency that can be selected on TV channels 2, 3, or 4. In a word, the whole idea

is to get all this video, sync, and blanking information into a conventional TV receiver.

It is possible to build VHF modulators from scratch, but considering the fact these little circuits are now commercially available for

PIN	FUNCTION	PIN	FUNCTION
1	+5 V-A	23	COMM
2	+5 V-B	24	1V
3	HBLANK	25	2V
4	HRST	26	4V
5	+5 V (SOURCEBOX)	27	8V
6	nc	28	16V
7	nc	29	32V
8	nc	30	64V
9	audio in	31	128V
10	nc	32	256V
11	nc	33	nc
12	COMP SYNC	34	256H
13	MOD IN	35	128H
14	CVID	36	64H
15	nc	37	32H
16	GAME VID IN	38	16H
17	nc	39	8H
18	nc	40	4H
19	VRST	41	2H
20	VBLANK	42	1H
21	nc	43	HCLK
22	COMM	44	+5 V-A

NOTE:

COMP SYNC = UNMODULATED COMPOSITE SYNC

MOD IN = rf MODULATOR INPUT

CVID = UNMODULATED COMPOSITE VIDEO

GAME VID IN = INPUT FROM ANY EXTERNAL GAME CIRCUIT

MOD IN AND CVID ARE NORMALLY SHORTED TOGETHER

Fig. 2-11. Listing of power supply terminals and signals that must be present at the interface plug.

about \$10, the job of building one from scratch is hardly worth the trouble.

Suitable modulators are now being used by microprocessor enthusiasts who want to interface their computer systems with a TV display. So the best source of modulators is the amateur computer shops now springing up all over the country. At the time of this writing, Radio Shack is planning to offer a suitable modulator in the near future. Although it is intended specifically for use with that company's microprocessor system, it would serve our purposes quite well.

Mount the modulator inside the Sourcebox unit, as far as possible from the master clock and crystal (to avoid possible rf interference between the two).

### SOME MECHANICAL CONSIDERATIONS

All of the Sourcebox circuitry fits quite nicely into Radio Shack's "compact" 5½-by 9- by 4½-inch cabinet (Radio Shack 270-281). See Fig. 2-10.

The two major circuit boards can be inserted into 44-pin edge-card connectors mounted vertically on the inside rear surface of the cabinet. The rf modulator is likewise mounted on that surface, using a 2-terminal, feedthrough TV antenna connector (Radio Shack 274-663). The power supply components are mounted inside the cabinet as described earlier in this chapter.

What has not been adequately described thus far is the means for getting access to the horizontal- and vertical-counting signals as well as any other system inputs and outputs that are vital to the operation of game systems. The most convenient way to interface the Sourcebox with the outside world is by means of another 44-pin edge-card connector that feeds through the back of the cabinet.

All of the connections between the Sourcebox and outside world are made through this connector. Its solder connections are inside the cabinet, connected to the appropriate signal sources as suggested in Fig. 2-11. Getting access to these signals from the outside world is thus a simple matter of plugging the appropriate 4-by 4-inch 44-pin PC card into the plug on the back of the cabinet.

No matter how you choose to arrange the circuitry for the Sourcebox unit, bear in mind that you must have convenient access to the supply voltages and signal connections listed in Fig. 2-11.