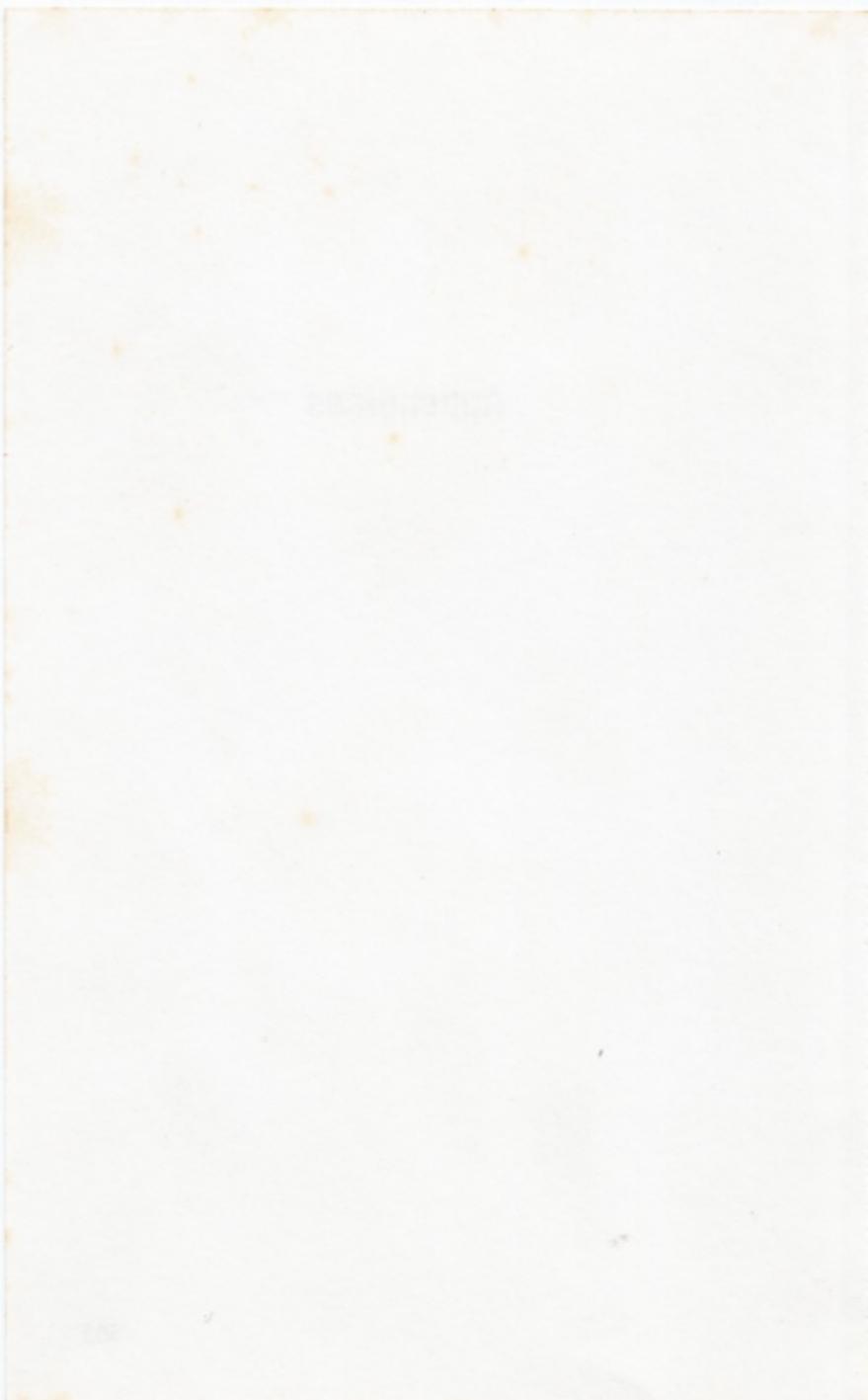


Appendices



Appendix I

This appendix is a complete listing of horizontal- and vertical-count binary outputs.

H- OR V-COUNT OUTPUTS

256 128 64 32 16 8 4 2 1

0	0	0	0	0	00000
					00001
					00010
					00011
					00100
					00101
					00110
					00111
					01000
					01001
					01010
					01011
					01100
					01101
					01110
					01111
					10000
					10001
					10010
					10011
					10100
					10101
					10110
					10111
					11000
					11001
					11010
					11011
					11100
					11101
					11110
0	0	0	0	0	11111

DECIMAL EQUIVALENT

0 ← H AND V BLANKING BEGIN

1

2

3

4 ← V SYNC BEGINS

5

6

7

8 ← V SYNC ENDS

9

10

11

12

13

14

15

16 ← V BLANKING ENDS

17

18

19

20

21

22

23

24

25

26

27

28

29

30

31

← H SYNC BEGINS

32

33

34

35

36

37

38

39

40

41

H SYNC

256 128 64 32 16 8 4 2 1

0	0	0	1	0 1 0 1 0
				0 1 0 1 1
				0 1 1 0 0
				0 1 1 0 1
				0 1 1 1 0
				0 1 1 1 1
				1 0 0 0 0
				1 0 0 0 1
				1 0 0 1 0
				1 0 0 1 1
				1 0 1 0 0
				1 0 1 0 1
				1 0 1 1 0
				1 0 1 1 1
				1 1 0 0 0
				1 1 0 0 1
				1 1 0 1 0
				1 1 0 1 1
				1 1 1 0 0
				1 1 1 0 1
				1 1 1 1 0
				1 1 1 1 1

42 ← H SYNC

43

44

45

46

47

48

49

50

51

52

53

54

55

56

57

58

59

60

61

62

63

0	0	1	0	0 0 0 0 0
				0 0 0 0 1
				0 0 0 1 0
				0 0 0 1 1
				0 0 1 0 0
				0 0 1 0 1
				0 0 1 1 0
				0 0 1 1 1
				0 1 0 0 0
				0 1 0 0 1
				0 1 0 1 0
				0 1 0 1 1
				0 1 1 0 0
				0 1 1 0 1
				0 1 1 1 0
				0 1 1 1 1
				1 0 0 0 0
				1 0 0 0 1
				1 0 0 1 0
				1 0 0 1 1
				1 0 1 0 0

64 ← H SYNC ENDS

65

66

67

68

69

70

71

72

73

74

75

76

77

78

79

80

81

82

83

84

H BLANKING
(CONT'D)

80 ← H BLANKING ENDS

256 128 64 32 16 8 4 2 1

0	0	1	0	10101	85
				10110	86
				10111	87
				11000	88
				11001	89
				11010	90
				11011	91
				11100	92
				11101	93
				11110	94
				11111	95
0	0	1	0	00000	96
				00001	97
				00010	98
				00011	99
				00100	100
				00101	101
				00110	102
				00111	103
				01000	104
				01001	105
				01010	106
				01011	107
				01100	108
				01101	109
				01110	110
				01111	111
				10000	112
				10001	113
				10010	114
				10011	115
				10100	116
				10101	117
				10110	118
				10111	119
				11000	120
				11001	121
				11010	122
				11011	123
				11100	124
				11101	125
				11110	126
0	0	1	1	11111	127

256 128 64 32 16 8 4 2 1							
0	1	0	0	0	0	00000	128
						00001	129
						00010	130
						00011	131
						00100	132
						00101	133
						00110	134
						00111	135
						01000	136
						01001	137
						01010	138
						01011	139
						01100	140
						01101	141
						01110	142
						01111	143
						10000	144
						10001	145
						10010	146
						10011	147
						10100	148
						10101	149
						10110	150
						10111	151
						11000	152
						11001	153
						11010	154
						11011	155
						11100	156
						11101	157
						11110	158
						01111	159
0	1	0	0	0	0		
0	1	0	1	0	0	00000	160
						00001	161
						00010	162
						00011	163
						00100	164
						00101	165
						00110	166
						00111	167
						01000	168
						01001	169
						01010	170
0	0	1	0	0	1		

256 128 64 32 16 8 4 2 1

0	0	1	0	0	1	0	1	1	171
				0	1	0	0	0	172
				0	1	0	1	0	173
				0	1	1	0	0	174
				0	1	1	1	1	175
				1	0	0	0	0	176
				1	0	0	1	1	177
				1	0	0	1	0	178
				1	0	1	1	1	179
				1	0	1	0	0	180
				1	0	1	0	1	181
				1	0	1	1	0	182
				1	0	1	1	1	183
				1	1	0	0	0	184
				1	1	0	0	1	185
				1	1	0	1	0	186
				1	1	0	1	1	187
				1	1	1	0	0	188
				1	1	1	0	1	189
				1	1	1	1	0	190
				0	0	0	0	0	191

0	1	1	0	0	0	0	0	0	192
				0	0	0	1	1	193
				0	0	0	1	0	194
				0	0	0	1	1	195
				0	0	1	0	0	196
				0	0	1	0	1	197
				0	0	1	1	0	198
				0	0	1	1	1	199
				0	1	0	0	0	200
				0	1	0	0	1	201
				0	1	0	1	0	202
				0	1	0	1	1	203
				0	1	1	0	0	204
				0	1	1	0	1	205
				0	1	1	1	0	206
				0	1	1	1	1	207
				1	0	0	0	0	208
				1	0	0	0	1	209
				1	0	0	1	0	210
				1	0	0	1	1	211
				1	0	1	0	0	212
				0	1	1	0	1	213

256 128 64 32 16 8 4 2 1

0	1	1	0	1	0	1	1	0	214
				1	0	1	1	1	215
				1	1	0	0	0	216
				1	1	0	0	1	217
				1	1	0	1	0	218
				1	1	0	1	1	219
				1	1	1	0	0	220
				1	1	1	0	1	221
				1	1	1	1	0	222
0	1	1	0	1	1	1	1	1	223

0	1	1	1	0	0	0	0	0	224
				0	0	0	1	0	225
				0	0	1	0	0	226
				0	0	1	1	1	227
				0	0	1	0	0	228
				0	0	1	0	1	229
				0	0	1	1	0	230
				0	0	1	1	1	231
				0	1	0	0	0	232
				0	1	0	0	1	233
				0	1	0	1	0	234
				0	1	0	1	1	235
				0	1	1	0	0	236
				0	1	1	0	1	237
				0	1	1	1	0	238
				0	1	1	1	1	239
				1	0	0	0	0	240
				1	0	0	0	1	241
				1	0	0	1	0	242
				1	0	0	1	1	243
				1	0	1	0	0	244
				1	0	1	0	1	245
				1	0	1	1	0	246
				1	0	1	1	1	247
				1	1	0	0	0	248
				1	1	0	0	1	249
				1	1	0	1	0	250
				1	1	0	1	1	251
				1	1	1	0	0	252
				1	1	1	0	1	253
				1	1	1	1	0	254
0	1	1	1	1	1	1	1	1	255

256 128 64 32 16 8 4 2 1

1	0	0	0	0	0 0 0 0 0	256
					0 0 0 0 1	257
					0 0 0 1 0	258
					0 0 0 1 1	259
					0 0 1 0 0	260
					0 0 1 0 1	261
					0 0 1 1 0	262
					0 0 1 1 1	263
					0 1 0 0 0	264
					0 1 0 0 1	265
					0 1 0 1 0	266
					0 1 0 1 1	267
					0 1 1 0 0	268
					0 1 1 0 1	269
					0 1 1 1 0	270
					0 1 1 1 1	271
					1 0 0 0 0	272
					1 0 0 0 1	273
					1 0 0 1 0	274
					1 0 0 1 1	275
					1 0 1 0 0	276
					1 0 1 0 1	277
					1 0 1 1 0	278
					1 0 1 1 1	279
					1 1 0 0 0	280
					1 1 0 0 1	281
					1 1 0 1 0	282
					1 1 0 1 1	283
					1 1 1 0 0	284
					1 1 1 0 1	285
					1 1 1 1 0	286
1	0	0	0	0	1 1 1 1 1	287
1	0	0	1	0	0 0 0 0 0	288
					0 0 0 0 1	289
					0 0 0 1 0	290
					0 0 0 1 1	291
					0 0 1 0 0	292
					0 0 1 0 1	293
					0 0 1 1 0	294
					0 0 1 1 1	295
					0 1 0 0 0	296
					0 1 0 0 1	297
					0 1 0 1 0	298
1	0	0	1	0	0 1 0 1 1	299

256 128 64 32 16 8 4 2 1

1	0	0	1	0	1	1	0	0	300
				0	1	1	0	1	301
				0	1	1	1	0	302
				0	1	1	1	1	303
				1	0	0	0	0	304
				1	0	0	0	1	305
				1	0	0	1	0	306
				1	0	0	1	1	307
				1	0	1	0	0	308
				1	0	1	0	1	309
				1	0	1	1	0	310
				1	0	1	1	1	311
				1	1	0	0	0	312
				1	1	0	0	1	313
				1	1	0	1	0	314
				1	1	0	1	1	315
				1	1	1	0	0	316
				1	1	1	0	1	317
				1	1	1	1	0	318
				1	1	1	1	1	319
1	0	0	1	1	1	1	1	1	

1	0	1	0	0	0	0	0	0	320
				0	0	0	1	0	321
				0	0	0	1	0	322
				0	0	0	1	1	323
				0	0	1	0	0	324
				0	0	1	0	1	325
				0	0	1	1	0	326
				0	0	1	1	1	327
				0	1	0	0	0	328
				0	1	0	0	1	329
				0	1	0	1	0	330
				0	1	0	1	1	331
				0	1	1	0	0	332
				0	1	1	0	1	333
				0	1	1	1	0	334
				0	1	1	1	1	335
				1	0	0	0	0	336
				1	0	0	0	1	337
				1	0	0	1	0	338
				1	0	0	1	1	339
				1	0	1	0	0	340
				1	0	1	0	1	341
				1	0	1	1	0	342
1	0	1	0	1	0	1	1	0	

256 128 64 32 16 8 4 2 1

1	0	1	0	1	0	1	1	1	1	343
					1	1	0	0	0	344
						1	1	0	1	345
							1	1	0	1
								1	1	1
									1	1
										347
										348
										349
										350
										351

1	0	1	1	0	0	0	0	0	0	352
					0	0	0	1	1	353
						0	0	1	0	354
							0	0	1	1
								0	1	0
									0	1
										355
										356
										357
										358
										359
										360
										361
										362
										363
										364
										365
										366
										367
										368
										369
										370
										371
										372
										373
										374
										375
										376
										377
										378
										379
										380
										381
										382
										383

256 128 64 32 16 8 4 2 1

1	1	0	0	0	0	0	0	0	384
					0	0	0	1	385
					0	0	1	0	386
					0	0	1	1	387
					0	0	1	0	388
					0	0	1	0	389
					0	0	1	0	390
					0	0	1	1	391
					0	1	0	0	392
					0	1	0	1	393
					0	1	0	1	394
					0	1	0	1	395
					0	1	1	0	396
					0	1	1	0	397
					0	1	1	1	398
					0	1	1	1	399
					1	0	0	0	400
					1	0	0	1	401
					1	0	0	1	402
					1	0	0	1	403
					1	0	1	0	404
					1	0	1	0	405
					1	0	1	1	406
					1	0	1	1	407
					1	1	0	0	408
					1	1	0	0	409
					1	1	0	1	410
					1	1	0	1	411
					1	1	1	0	412
					1	1	1	0	413
					1	1	1	0	414
					1	1	1	1	415

1	1	0	1	0	0	0	0	0	416
					0	0	0	1	417
					0	0	1	0	418
					0	0	1	1	419
					0	0	1	0	420
					0	0	1	0	421
					0	0	1	1	422
					0	0	1	1	423
					0	1	0	0	424
					0	1	0	0	425
					0	1	0	1	426

256 128 64 32 16 8 4 2 1

1	1	0	1	0 1 0 1 1	427
				0 1 1 0 0	428
				0 1 1 0 1	429
				0 1 1 1 0	430
				0 1 1 1 1	431
				1 0 0 0 0	432
				1 0 0 0 1	433
				1 0 0 1 0	434
				1 0 0 1 1	435
				1 0 1 0 0	436
				1 0 1 0 1	437
				1 0 1 1 0	438
				1 0 1 1 1	439
				1 1 0 0 0	440
				1 1 0 0 1	441
				1 1 0 1 0	442
				1 1 0 1 1	443
				1 1 1 0 0	444
				1 1 1 0 1	445
1	1	0	1	1 1 1 1 0	446
				1 1 1 1 1	447

1	1	1	0	0 0 0 0 0	448
				0 0 0 0 1	449
				0 0 0 1 0	450
				0 0 0 1 1	451
				0 0 1 0 0	452
				0 0 1 0 1	453
1	1	1	0	0 0 1 1 0	454

H BLANK BEGINS

Appendix II

Digital Integrated Circuits

7400	Quad 2-input NAND
7402	Quad 2-input NOR
7404	Hex inverter
7420	Dual 4-input NAND
7427	Triple 3-input NOR
7430	8-input NAND
7448*	BCD to 7-segment converter
7474*	Dual D flip-flop
7475*	Quad D latch
7476*	Dual JK flip-flop
7483*	4-bit binary full adder
7485	4-bit comparitor
7486	Quad EXCLUSIVE OR
7490*	Decade counter
7492*	± 6 counter
7493*	4-bit binary counter
74125	Quad 3-state buffer
74147	Decimal-to-BCD converter
74150	16:1 multiplexer
74151	8:1 multiplexer
74153	Dual 4:1 multiplexer
74154	4-line to 16-line decoder
74155	Dual 2-line to 4-line decoder
74157	Quad 2:1 multiplexer
74191*	Presetable binary up/down counter

*designates ICs detailed in this appendix

This appendix lists the digital ICs that are referenced within this book. Those marked with an asterisk (*) are detailed on subsequent pages.

7448* BCD to 7-Segment Converter

DESCRIPTION — The 9358/5448, 7448 and 9359/5449, 7449 are TTL, BCD to 7-Segment Decoders consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. The 9358/5448, 7448 offers active HIGH, open-collector outputs for current-sourcing applications to drive logic circuits or discrete, active components. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input for the 9358/5448, 7448. Four NAND gates and four input buffers provide BCD data and its complement and a buffer provides blanking input for the 9359/5449, 7449.

The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive other components. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs are shown in the truth tables.

The 9358/5448, 7448 circuit incorporates automatic leading and/or trailing edge zero-blanking control (\overline{RBI} and \overline{RBO}). Lamp test (\overline{LT}) of these types may be performed at any time when the $\overline{BI}/\overline{RBO}$ node is a HIGH level. They contain an overriding blanking input (\overline{BI}) which can be used to control the lamp intensity or to inhibit the outputs.

PIN NAMES

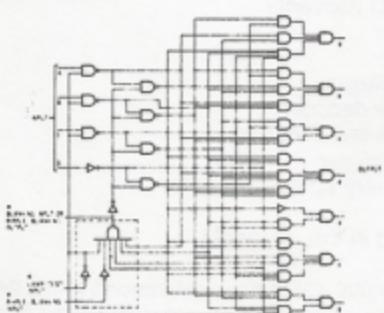
		LOADING
A, B, C, D	BCD Inputs	1 U.L.
\overline{RBI}	Ripple Blanking Input	1 U.L.
\overline{LT}	Lamp Test Input	1 U.L.
$\overline{BI}/\overline{RBO}$	Blanking Input or Ripple Blanking Output	2.6 U.L.
\overline{BI}	Blanking Input	5 U.L.
a to g	Outputs	1 U.L.
		6 U.L.

DIP (TOP VIEW)



Positive logic: See truth table

LOGIC DIAGRAM



* NOT INCLUDED WITH THE 9359/5449



NUMERICAL DESIGNATIONS - RESULTANT DISPLAYS*

TRUTH TABLE 9358/5448, 7448

DECIMAL OR FUNCTION	INPUTS								OUTPUTS					NOTE	
	EI	RBI	D	C	B	A	SWING	a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	M	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	H	L	L	H
4	H	X	L	H	H	L	H	L	H	M	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	M	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	H	H	H	H	H	H	H	M	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	H	M	L	L	H	H	
12	H	X	H	H	L	L	H	L	M	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	M	H	M	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BL	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	2
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

NOTES:

- (1) BI/RBO is wired-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking out (BI) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input (RBI) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X=Input may be HIGH or LOW.
- (2) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.
- (3) When ripple-blanking input (RBI) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output (RBO) goes to a LOW level (response condition).
- (4) When the blanking input/ripple-blanking output (BI/RBO) is open or held at a HIGH level, and a LOW level is applied to lamp-test input, all segment outputs go to a LOW level.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	+65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V _{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

7474* Dual D Flip-Flop

DESCRIPTION — The 9N74/5474, 7474 are edge triggered dual D type flip-flops with direct clear and preset inputs and both Q and \bar{Q} outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. They are designed for use in medium to high speed applications.

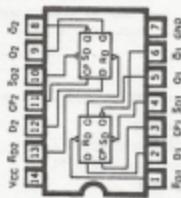
Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out and information present will not be transferred to the output. The 9N74/5474, 7474 have the same clocking characteristics as the 9N70/5470, 7470 gated (edge triggered) flip-flop circuits. They can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)

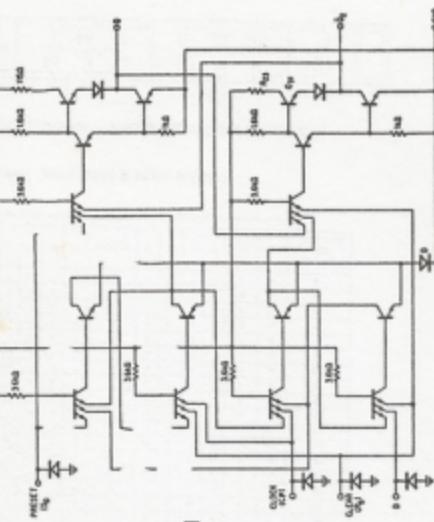


Positive logic:

LOW input to preset sets Q to HIGH level

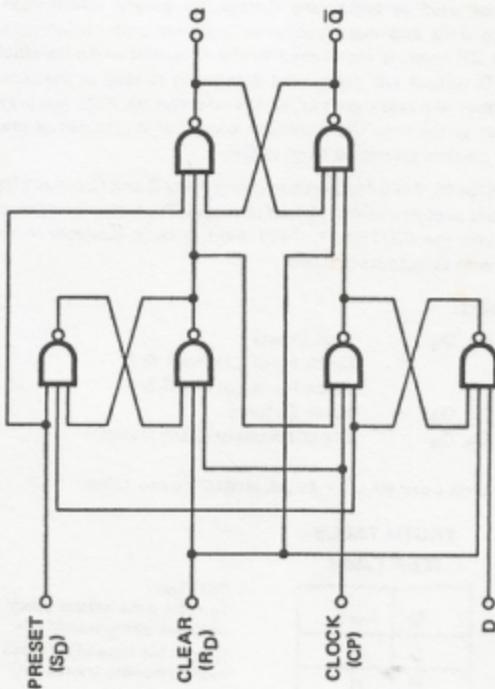
LOW input to clear sets Q to LOW level

Preset and clear are independent of clock



Component values shown are typical.

LOGIC DIAGRAM (EACH FLIP-FLOP)



TRUTH TABLE (Each Flip-Flop)

t _n		t _{n+1}	
INPUT	OUTPUT	OUTPUT	OUTPUT
D	Q	\bar{Q}	
L	L	H	H
H	H	L	L

NOTES:

t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse.

7475* Quad D Latch

DESCRIPTION — The TTL/MSI 9375/5475, 7475 and 9377/5477, 7477 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is HIGH and the Q output will follow the data input as long as the clock remains HIGH. When the clock goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go HIGH.

The 9375/5475, 7475 features complementary Q and \bar{Q} output from a 4-bit latch and is available in the 16-lead packages. For higher component density applications the 9377/5477, 7477 4-bit latch is available in the 14-lead package with \bar{Q} outputs omitted.

PIN NAMES

D ₁ , D ₂ , D ₃ , D ₄	Data Inputs
CP ₁₋₂	Clock Input Latches 1 & 2
CP ₃₋₄	Clock Input Latches 3 & 4
Q ₁ , Q ₂ , Q ₃ , Q ₄	Latch Outputs
\bar{Q}_1 , \bar{Q}_2 , \bar{Q}_3 , \bar{Q}_4	Complementary Latch Outputs

LOADING

2 U.L.
4 U.L.
4 U.L.
10 U.L.
10 U.L.

Note: 1 Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW

TRUTH TABLE

(Each Latch)

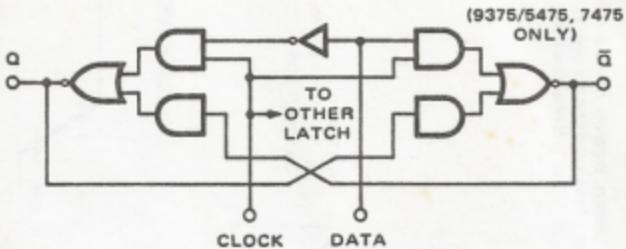
t _n	t _{n+1}
D	Q
H	H
L	L

NOTES:

t_n = bit time before clock negative-going transition.

t_{n+1} = bit time after clock negative-going transition.

**LOGIC DIAGRAM
(EACH LATCH)**



(9375/5475, 7475
ONLY)

DIP (TOP VIEW)



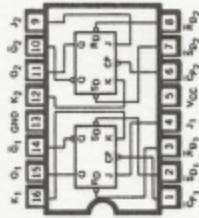
Positive logic: See truth table.
NC — No internal connection.

7476* Dual JK Flip-Flop

DESCRIPTION — The TTL/SSI 9N76/E476, 7476 is a Dual JK Master/Slave flip-flop with separate presets, separate clears and separate clocks. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: 1) Isolate slave from master. 2) Enter information from J and K inputs to master. 3) Disable J and K inputs. 4) Transfer information from master to slave.

LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



TRUTH TABLE

t_n		t_{n+1}	
J	K	Q	\bar{Q}_n
L	L	Q_n	\bar{Q}_n
L	H	L	H
H	L	H	L
H	H	H	H

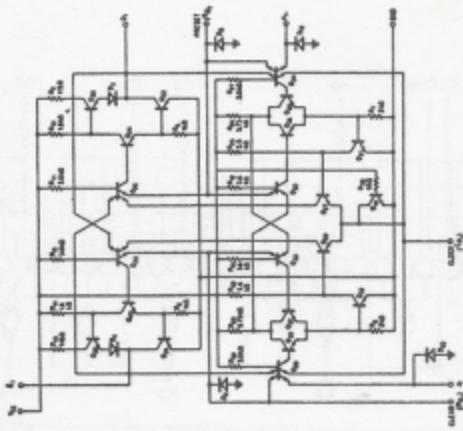
NOTES:
 t_n = Bit time before clock pulse.
 t_{n+1} = Bit time after clock pulse.

CLOCK WAVEFORM

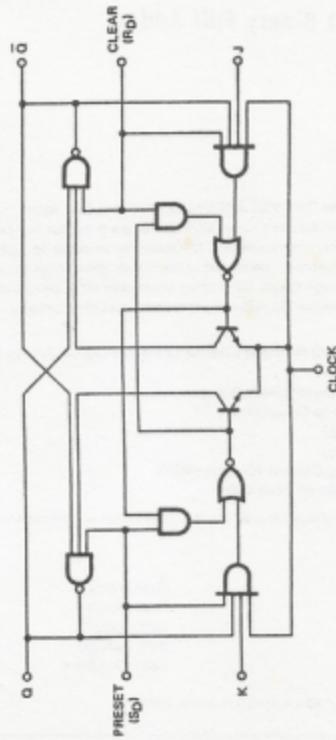


Positive logic:
 LOW input to preset sets Q to HIGH level
 LOW input to clear sets Q to LOW level
 Clear and preset are independent of clock

**SCHEMATIC DIAGRAM
(EACH FLIP-FLOP)**



LOGIC DIAGRAM
(EACH FLIP-FLOP)



Component values shown are typical.

7483* 4-Bit Binary Full Adder

DESCRIPTION — The TTL/MSI 9383/5483,7483 is a Full Adder which performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium to high speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilized high speed, high fan out TTL. The implementation of a single-inversion, high speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "lookahead" and carry-cascading circuits.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V _{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
*Input Voltage (dc)	-0.5 V to +5.5 V
*Input Current (dc)	-30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	-0.5 V to +V _{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

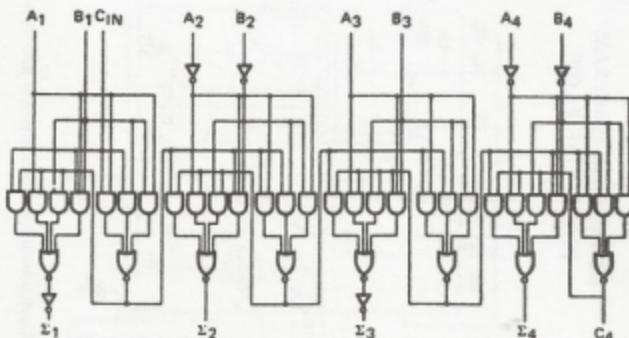
PIN NAMES

A ₁ ,B ₁ ,A ₃ ,B ₃	Data Inputs
A ₂ ,B ₂ ,A ₄ ,B ₄	Data Inputs
C _{IN}	Carry Input
$\Sigma_1,\Sigma_2,\Sigma_3,\Sigma_4$	Sum Outputs
C ₄	Carry Out Bit 4

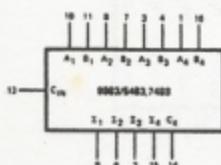
LOADING
4 U.L.
1 U.L.
4 U.L.
10 U.L.
5 U.L.

1 Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW

LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 5
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)

TRUTH TABLE (See Note 1)

INPUT	WHEN $C_{IN} = 0$								WHEN $C_{IN} = 1$							
	WHEN $C_2 = 0$				WHEN $C_2 = 1$				WHEN $C_2 = 0$				WHEN $C_2 = 1$			
	A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	C_4	Σ_1	Σ_2	C_2	C_4				
A_3	B_3	A_4	B_4	L	L	L	L	L	H	L	L	L	L	H	L	L
L	L	L	L	H	L	L	L	L	L	H	L	L	H	L	L	L
H	L	L	L	L	H	L	L	L	L	L	H	L	L	H	L	L
L	H	L	L	H	L	H	L	L	L	L	H	L	H	L	L	L
H	H	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	L	L	H	L	H	L	H	L	H	H	H	L	L	L
H	L	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H
L	H	H	L	H	H	H	H	L	L	L	L	L	L	H	L	H
H	H	L	H	L	H	H	L	L	H	H	H	L	H	L	H	H
L	L	H	H	H	H	H	H	L	H	H	L	H	L	H	H	H
H	L	H	H	H	H	H	H	L	H	H	L	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

NOTE:

1. Input conditions at A_1, A_2, B_1, B_2 and C_{IN} are used to determine outputs Σ_1 and Σ_2 , and the value of the internal carry C_2 . The values at C_2, A_3, B_3, A_4 , and B_4 , are then used to determine outputs Σ_3, Σ_4 and C_4 .

7490* Decade Counter

530

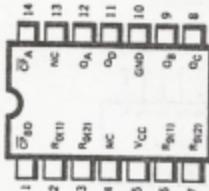
DESCRIPTION — The TTL/MSI 9390/5490, 7490 is a Decade Counter which consists of four dual rank, master slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Count inputs are inhibited, and all outputs are returned to logical zero or a binary coded decimal (BCD) count of 9 through gated direct reset lines. The output from flip-flop A is not internally connected to the succeeding stages, therefore the count may be separated into these independent count modes:

A. If used as a binary coded decimal decade counter, the \overline{CP}_{BD} input must be externally connected to the Q_A output. The \overline{CP}_A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count for nine's complement decimal application.

B. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the QD output must be externally connected to the \overline{CP}_A input. The input count is then applied at the \overline{CP}_{BD} input and a divide-by-ten square wave is obtained at output Q_A .

C. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The \overline{CP}_{BD} input is used to obtain binary divide-by-five operation at the Q_B , Q_C , and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

CONNECTION DIAGRAM
DIP (TOP VIEW)



LOADING	
1 U.L.	
1 U.L.	
2 U.L.	
4 U.L.	
10 U.L..	

Pin Names
R0
R9
 \overline{CP}_A
 \overline{CP}_{BD}
 Q_A , Q_B , Q_C , Q_D
Outputs

1 Unit Load (U.L.) = $40\mu A$ HIGH/1.6mA LOW.

TRUTH TABLES

RESET COUNT (Refer to Fig. 2)				OUTPUT			
COUNT	Q_0	Q_1	Q_2	Q_3	$R_{(1)}$	$R_{(2)}$	$R_{(3)}$
0	L	L	L	S	H	H	X
1	L	L	S	H	H	L	L,L,L
2	L	L	H	L	X	X	H
3	L	S	H	L	X	S	H,L,H
4	S	H	S	L	X	S	L
5	L	H	L	H	L	X	L
6	L	H	H	L	L	X	S
7	S	H	H	L	X	X	L
8	H	L	L	H	L	L	H

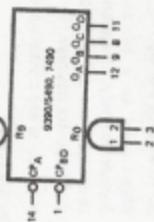
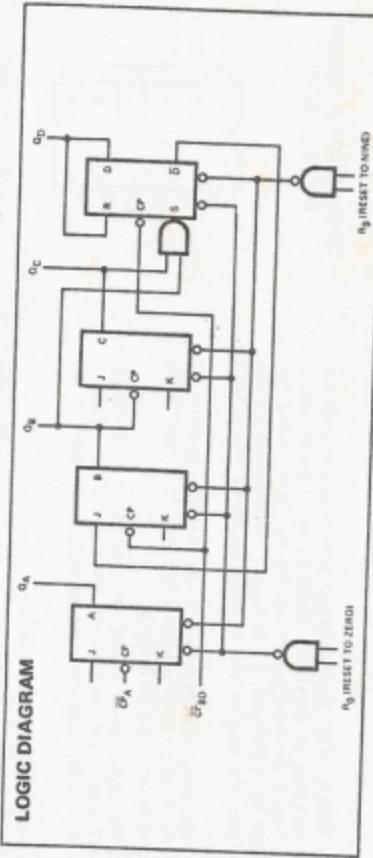
NOTES:

1. Output Q_A connected to input CP BD for BCD count.
2. X indicates that either a HIGH level or a LOW level may be present.

LOGIC SYMBOL



LOGIC DIAGRAM



V_{CC} = Pin 5
GND = Pin 10
NC = Pin 4, 13

R₀ INSET TO ZERO

7492* $\div 6$ Counter

532

DESCRIPTION — The TTL/MSI 9392/5492, 7492 is a 4-Bit Binary Counter consisting of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops, the counter may be operated in two independent modes:

- When used as a divide-by-twelve counter, output Q_A must be externally connected to input \overline{CP}_{BC} . The input count pulses are applied to input \overline{CP}_A . Simultaneous divisions of 2, 6 and 12 are performed at the Q_A , Q_C and Q_D outputs as shown in the truth table.
- When used as a divide-by-six counter, the input count pulses are applied to input \overline{CP}_{BC} . Simultaneously, frequency divisions of 3 and 6 are available at the Q_C and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES

R_0

\overline{CP}_A

\overline{CP}_{BC}

Q_A , Q_B , Q_C , Q_D

1 Unit Load (U.L.) = $40 \mu A$ HIGH/1.6 mA LOW

RESET-ZERO INPUTS

Clock Input

Count Outputs

LOADING

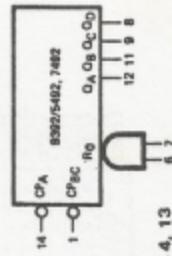
1 U.L.

2 U.L.

4 U.L.

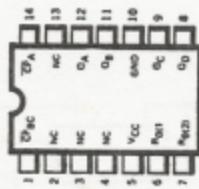
10 U.L.

LOGIC SYMBOL



$V_{CC} = \text{Pin } 5$
 $GND = \text{Pin } 10$
N.C. = Pins 2, 3, 4, 13
67

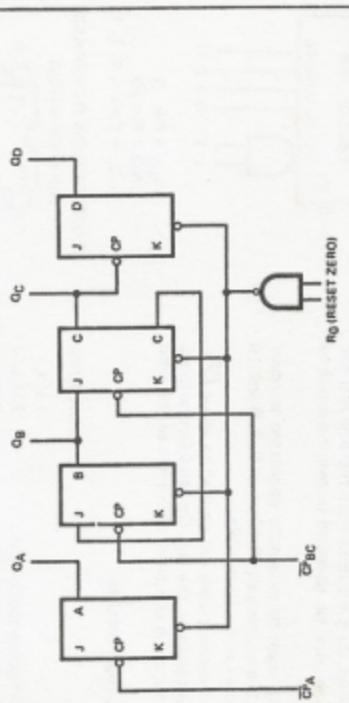
CONNECTION DIAGRAM
DIP (TOP VIEW)



TRUTH TABLE
(See Notes 1, 2 and 3)

COUNT	OUTPUT	Q_0	Q_1	Q_2	Q_3
0		L	L	L	L
1		L	L	L	H
2		L	L	H	L
3		L	L	H	H
4		L	H	L	L
5		L	H	L	H
6		H	L	L	L
7		H	L	L	H
8		H	L	H	L
9		H	L	H	H
10		H	H	L	L
11		H	H	L	H

LOGIC DIAGRAM



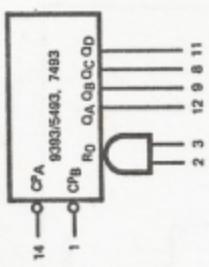
NOTES:

1. Output Q_A connected to input $\overline{C}B_C$.
2. To reset all outputs to LOW level both $R_Q(1)$ and $R_Q(2)$ inputs must be at HIGH level state.
3. Either (or both) reset inputs $R_Q(1)$ and $R_Q(2)$ must be at a LOW level to count.

7493* 4-Bit Binary Counter

534

LOGIC SYMBOL



DESCRIPTION — The TTL/MSI 9393/5493, 7493 is a 4-Bit Binary Counter consisting of four master/slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a LOW level. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

- When used as a 4-bit ripple-through counter, output Q_A must be externally connected to input \overline{CP}_B . The input count pulses are applied to input CP_A . Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_A , Q_B , Q_C , and Q_D outputs as shown in the truth table.
- When used as a 3-bit ripple-through counter, the input count pulses are applied to input \overline{CP}_B . Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_B , Q_C , and Q_D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with TTL and DTL logic families.

PIN NAMES

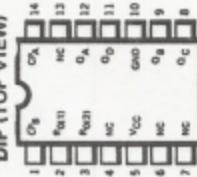
R_0
 \overline{CP}_A
 \overline{CP}_B
 Q_A , Q_B , Q_C , Q_D

LOADING

1 U.L.
2 U.L.
2 U.L.
10 U.L.

Reset-Zero Input
Clock (Active LOW going edge) Input
Clock (Active LOW going edge) Input
Outputs

CONNECTION DIAGRAMS

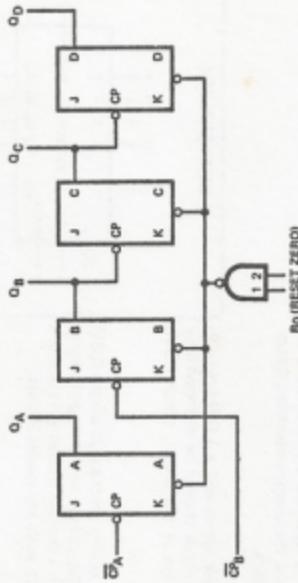


V_{CC} = Pin 5
GND = Pin 10
N.C. = Pins 4, 6, 7, 13

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	H	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

1 Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW

LOGIC DIAGRAM



NOTES:

1. Output Q_A connected to input \overline{CP}_B .
2. To reset all outputs to LOW level both R_{Q(1)} and R_{Q(2)} inputs must be at HIGH level state.
3. Either (or both) reset inputs R_{Q(1)} and R_{Q(2)} must be at a LOW level to count.

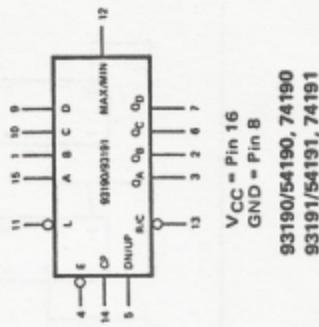
74191* Presettable Binary Up/Down Counter

DESCRIPTION - The 93190/54190, 74190 and 93191/54191, 74191 are Synchronous Up/Down Counters with enable control presetting facility, single line up/down control, cascading for multi-decade operation and buffered inputs. The 93190/54190, 74190 is a BCD counter, while the 93191/54191, 74191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when input conditions are met. This mode of operation will eliminate the output counting spikes which are normally associated with asynchronous (ripple clock) counters.

A HIGH at the enable input inhibits counting. A LOW at the enable input and a LOW-to-HIGH clock transition triggers the four master/slave flip-flops. The enable input should be changed only when the clock is HIGH. The down/up input determines the direction of the count. When LOW, the count goes up; when HIGH, the count goes down.

These counters are fully programmable. The outputs may be preset to any state by placing a LOW on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8
93190/54190, 74190
93191/54191, 74191

Two outputs have been made available to perform the cascading function. ripple clock and maximum/minimum count. The latter output produces a HIGH level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a LOW level output pulse equal in width to the LOW level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish lookahead for high speed operation.

Power dissipation is typically 325 mW for either the decade or binary version. Maximum input clock frequency is typically 25 MHz and is guaranteed to be at least 20 MHz.

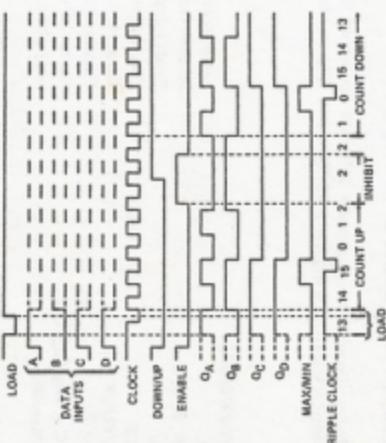
PIN NAMES

- L
- A, B, C, D
- E
- CP
- DN/UP
- R/C
- QA, QB, QC, QD
- Max./Min.

LOADING

- Load Input 1 U.L.
- Parallel Input 1 U.L.
- Enable Input 3 U.L.
- Clock Input 1 U.L.
- Down/Up Input 1 U.L.
- Ripple Clock Output 10 U.L.
- Parallel Output 10 U.L.
- Max./Min. Output 10 U.L.

1 Unit Load (U.L.) = $40 \mu\text{A}$ HIGH/ 1.6 mA LOW



The following sequence is illustrated:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen

BINARY COUNTER 93191/54191, 74191

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