Design of a Direct-Mapped Cache Memory

Structure of Computer Systems

1 Design Specification

Consider a processor connected to a byte-addressable main memory. The address bus is 16-bit wide. Design a direct-mapped cache memory of 256 B storing blocks of 4 B (the size of a cache line is 4 B).

The number of lines (N_L) can be determined by dividing the capacity of the cache memory by the size of a block:

$$N_L = \frac{256}{4} = 64 = 2^6 \text{ lines}$$

Therefore, the basic memory circuits used for the data memory should have a capacity of 64 B ($64 \cdot 8$ bits). 4 such circuits have to be used to allow storing 4 words in each line.

This also means that we need $s = 6$ address bits to select the line, representing the index part of the address.

As the size of a line is 4 $B = 2^2$ B, $d = 2$ bits are needed to determine the offset or displacement of the word within the line (to address a byte in a line).

Because the address bus is 16-bit wide, the tag size is:

$$t = 16 - (s + d) = 16 - (6 + 2) = 16 - 8 = 8 \text{ bits}$$

Considering that the used write policy is *write-through*, the tag memory should have a capacity of $64 \cdot 9$ bits (an additional *valid* bit is required, but no *dirty* bit is needed).

2 Hardware Design

The block design of the direct-mapped cache memory is shown in Figure 1.

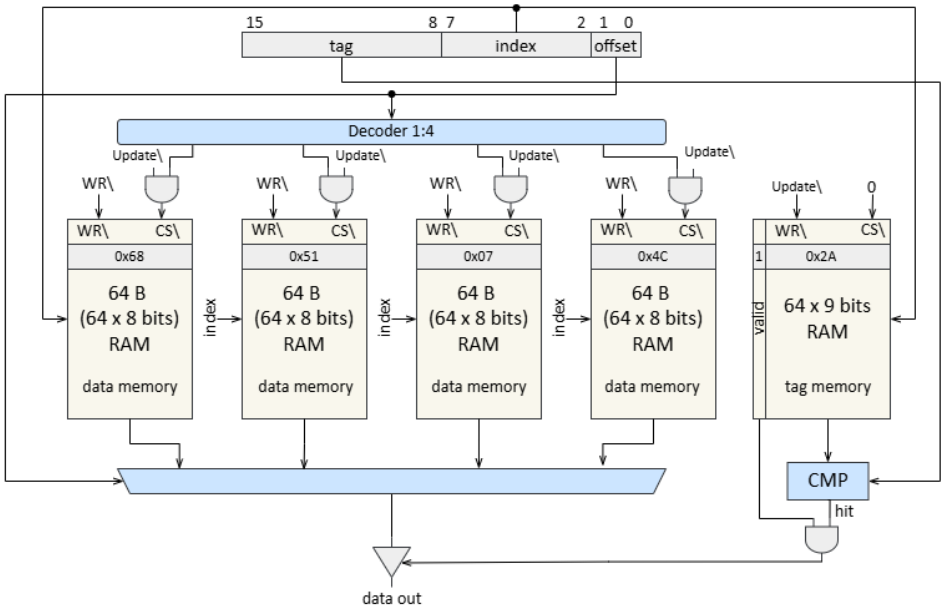

Figure 1: Block design of the 256 B direct-mapped cache

A control unit has to be designed as a finite-state machine (FSM) to allow implementing the operations performed by the cache memory. The states representing the operations are:

- **SEARCH**: finding information; if the information is not found (a miss occurs) it has to be brought from the main memory
- **UPDATE**: bringing an entire block in the cache as a consequence of a miss; the $Update\backslash$ signal is active in this state
- **RD/WR**: reading/writing data from/to the main memory; from the perspective of the cache memory this means outputting the required data from the cache

The FSM corresponding to the control unit is depicted in Figure 2.

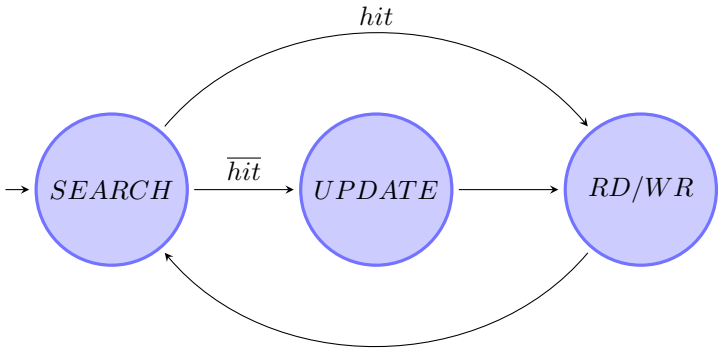

Figure 2: Control Unit Finite-State Machine