CPU performance monitoring using the Time-Stamp Counter register

Exercise1 :

musurment Number	CPU execution time
1	4
2	2
3	4
4	8
5	0
6	4
7	0
8	2
9	8
10	4
avarege time	3.6f

Table 1

musurment	ADD(REG)	ADD(VAR)	MUL	FDIV	FSUB
1	300	338	336	376	354
2	296	344	332	418	298
3	330	359	306	366	316
4	348	388	345	224	364
5	292	332	356	374	322
AVAREG	313	352	335	351	330

Table 2

addition with two registers is faster than addition with two variables. When using variables, the values need to be loaded from memory into registers before the addition operation. This involves additional memory access instructions, which can be slower than accessing values directly from registers.

Exercise 2 :

musurment number	RDTSC time(clock cycle)		clock time(clock cycle)	
	static array	dynamic array	static array	dynamic array
1	67900	51867	27	31
2	112000	13742	47	31
3	144488	134931	61	51
4	145200	51691	23	241
5	55427	131020	61	642
avarage	105003	76650,2	43,8	199,2
	table 3			

array length	initial sort time		optimized sort time	
	static array	dynamic array	static array	dynamic array
100	793	298	149	25
500	1091	585	231	31
1000	5164	2374	463	51
5000	42833	43221	999	241
10000	165339	166510	1456	642
	table 4			