NAND3 Simulation and Layout - Delay Analysis

Vladislav Pomogaev - 26951160

November 14, 2021

1 Problem 1

1.1 Specifications

Here are the specifications for my NAND3 gate:

- Area: 0.0981 micrometer squared
- Average delay: 25.61 pico-seconds
- Area delay: 2.5130 pico-seconds micrometer squared

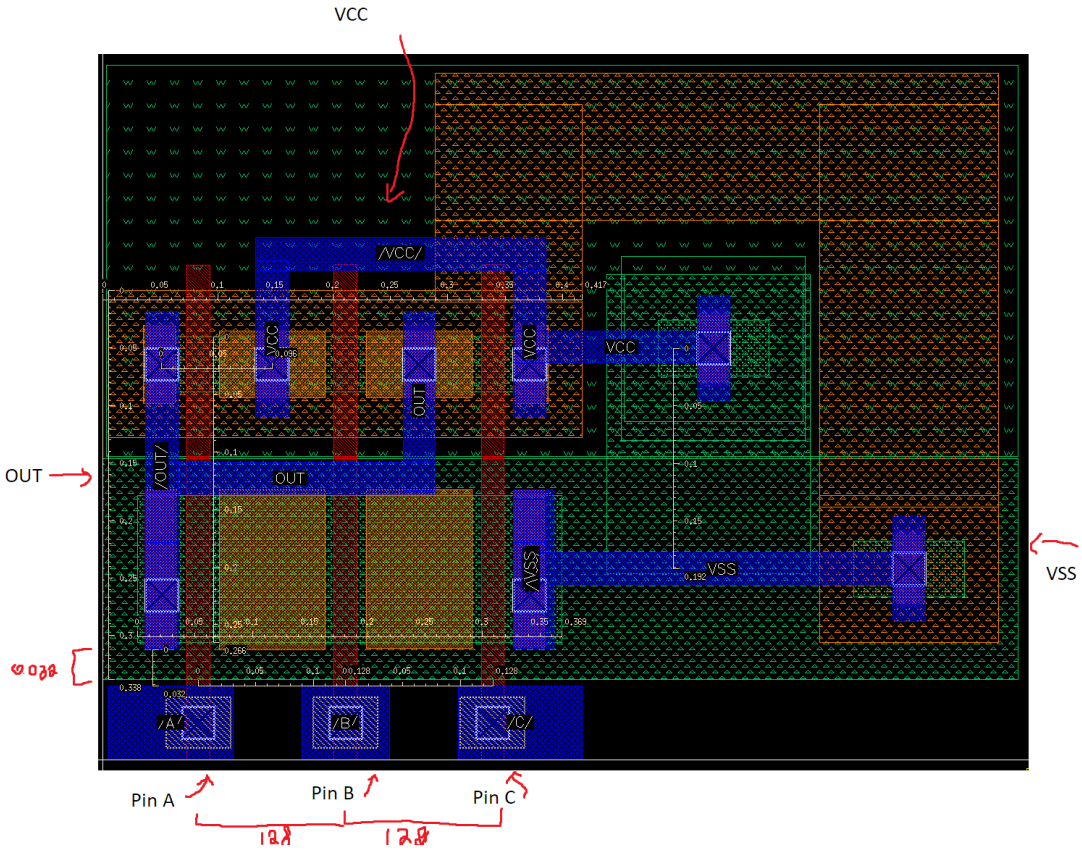

Figure 1: Layout of the gate. I had to add bulk connections otherwise I could not pass LVS for some reason. For the area, I measured the largest dimensions made by the active areas.

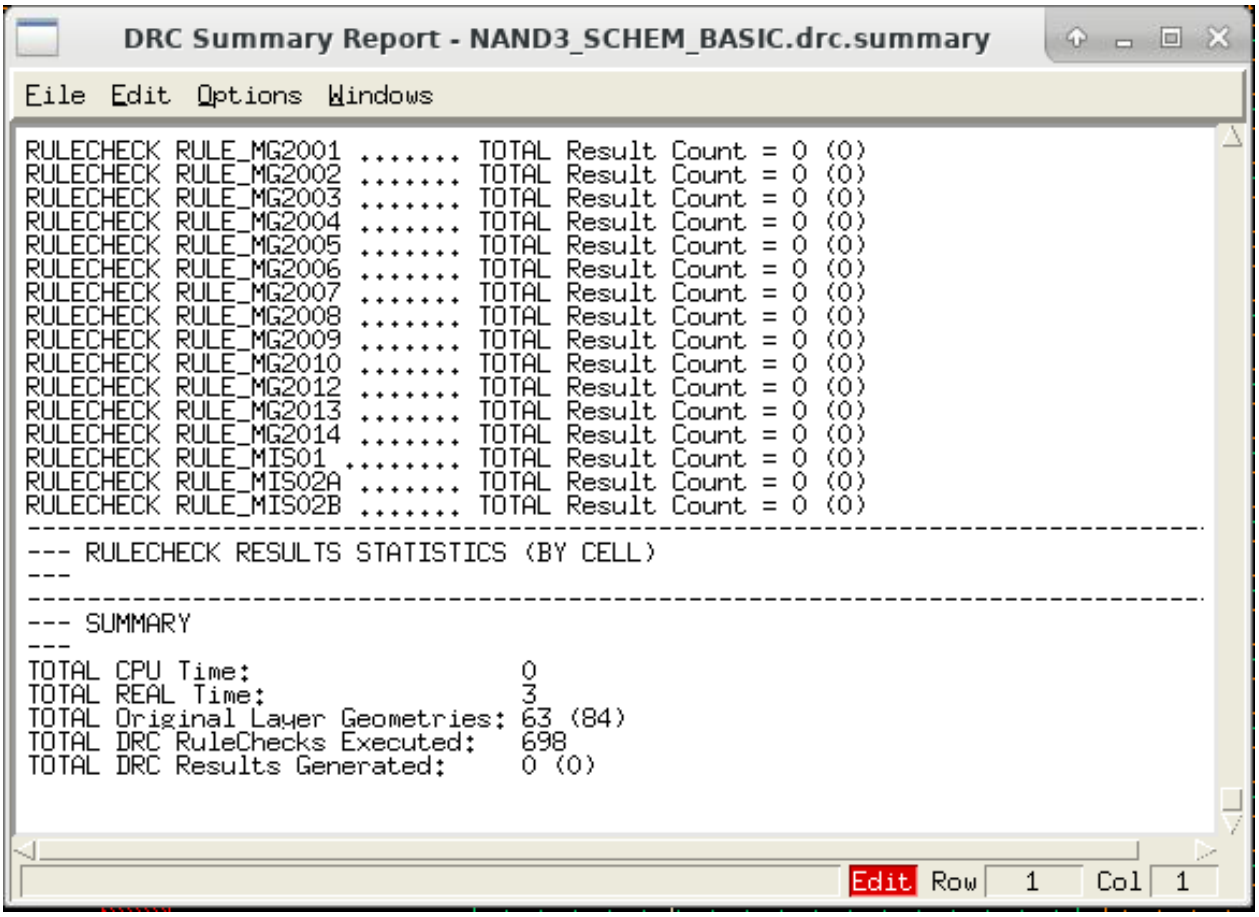

Figure 2: DRC Summary report (I solved the two rule checks that we were allowed to ignore)

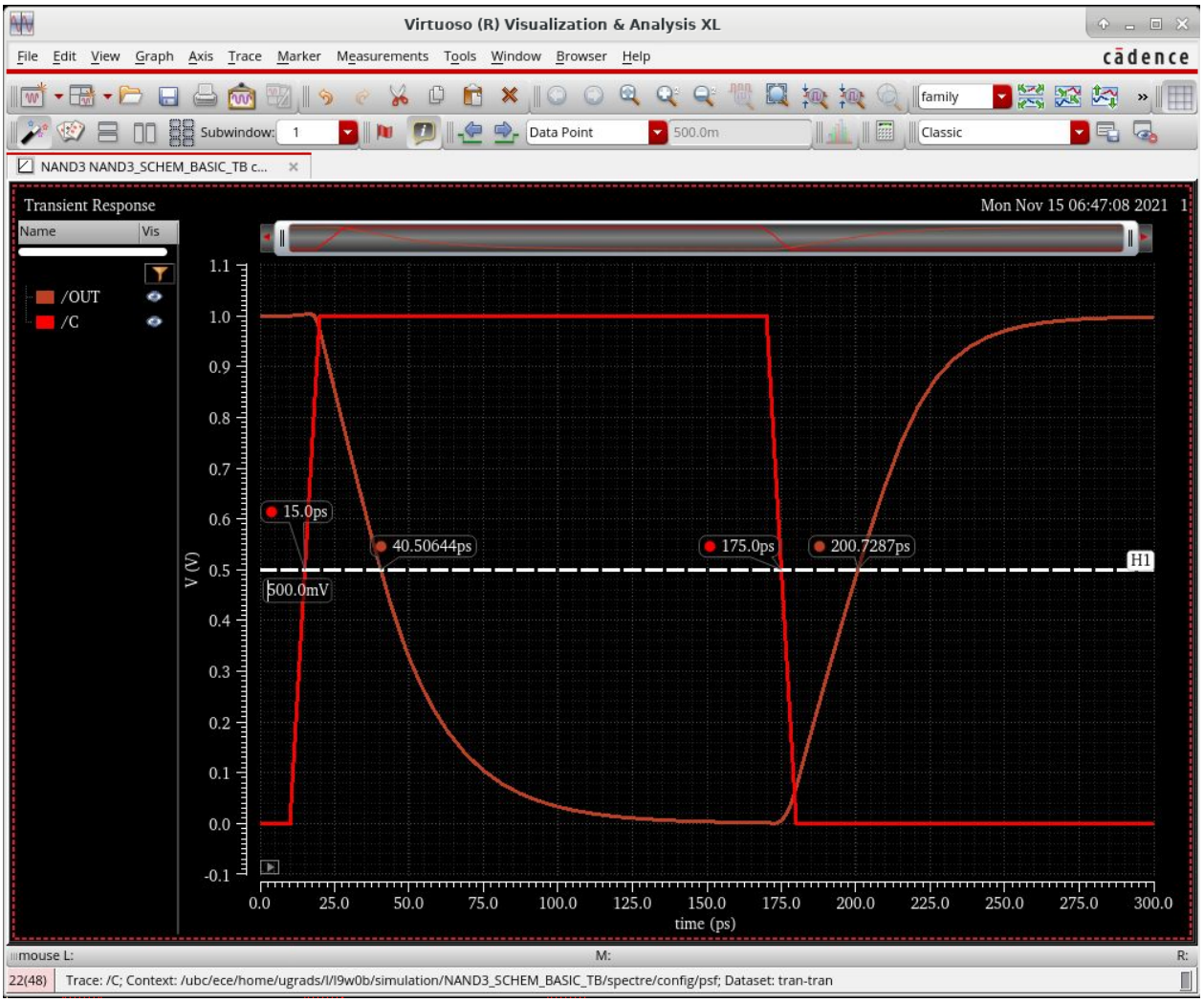

Figure 3: Timing of the gate. td,HL = 25.507ps, td,LD = 25.72ps. This graph was generated from the extracted view including all parasitics.

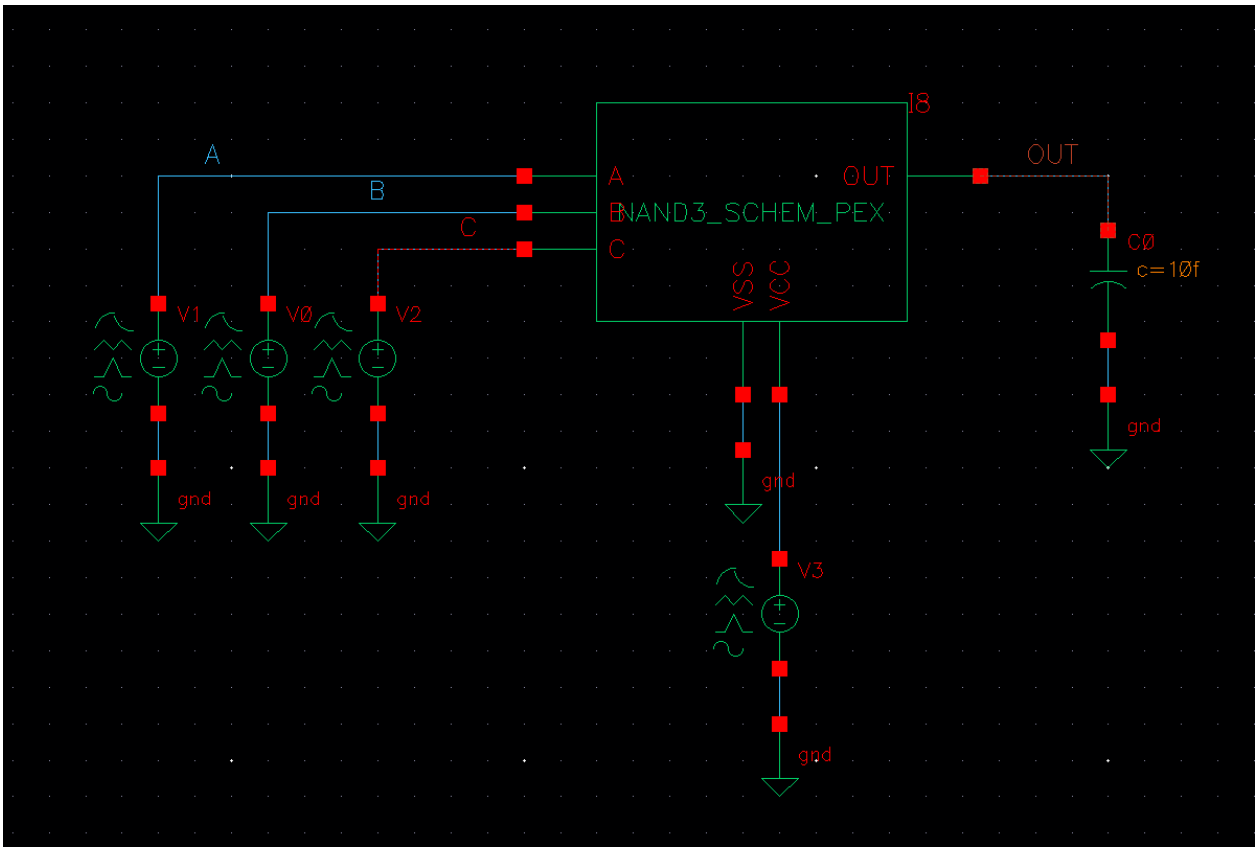

Figure 4: Screen-shot of my schematic. I used a 10pF capacitor as the load. Worst-case switching was used.

2 Problem 2

2.1 a)

Using demorgan's law:

$$\overline{F} = CD(B + A)$$

$$\overline{\overline{F}} = \overline{CD(B + A)}$$

$$F = \overline{C} + \overline{D} + \overline{B + A}$$

$$F = \overline{C} + \overline{D} + \overline{BA}$$

2.2 b)

2.3 c)