NAND3 Simulation and Layout - Delay Analysis

Vladislav Pomogaev - 26951160

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1 Problem 1

1.1 Specifications

Here are the specifications for my NAND3 gate:

- Area: 0.0981 micrometer squared
- Average delay: 25.61 pico-seconds
- Area delay: 2.5130 pico-seconds micrometer squared

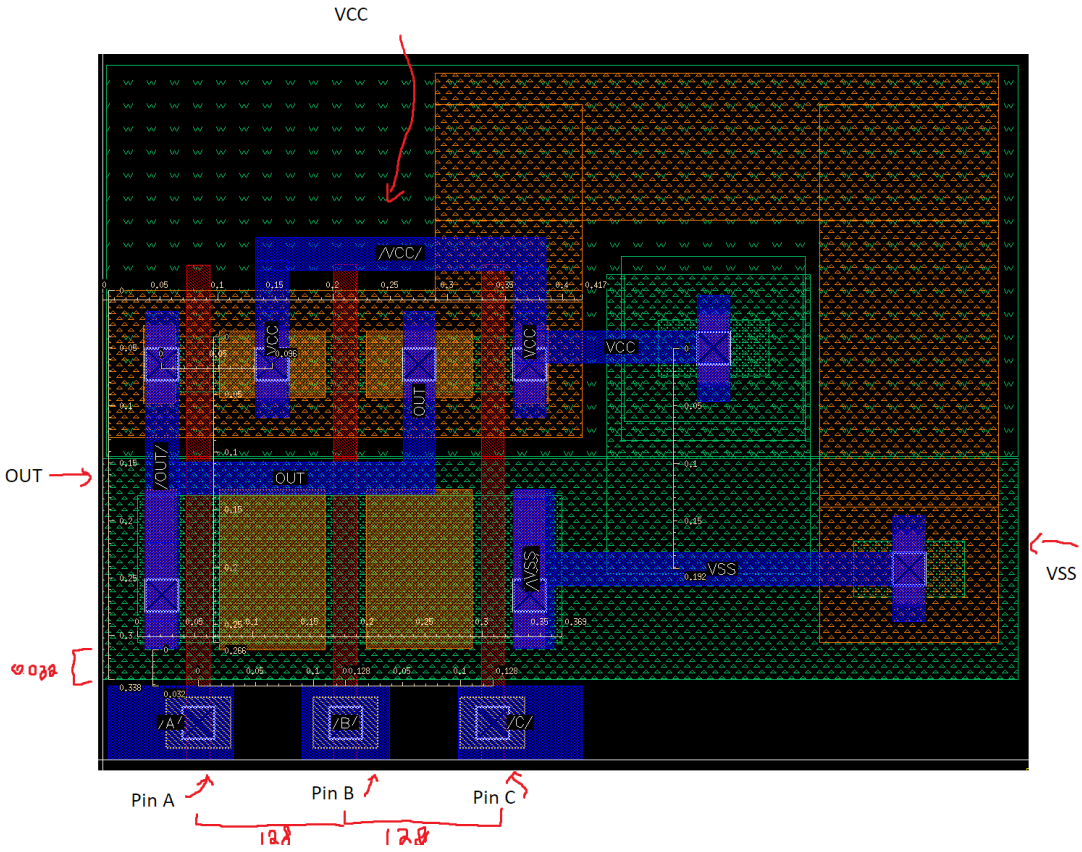


Figure 1: Layout of the gate. I had to add bulk connections otherwise I could not pass LVS for some reason. For the area, I measured the largest dimensions made by the active areas.

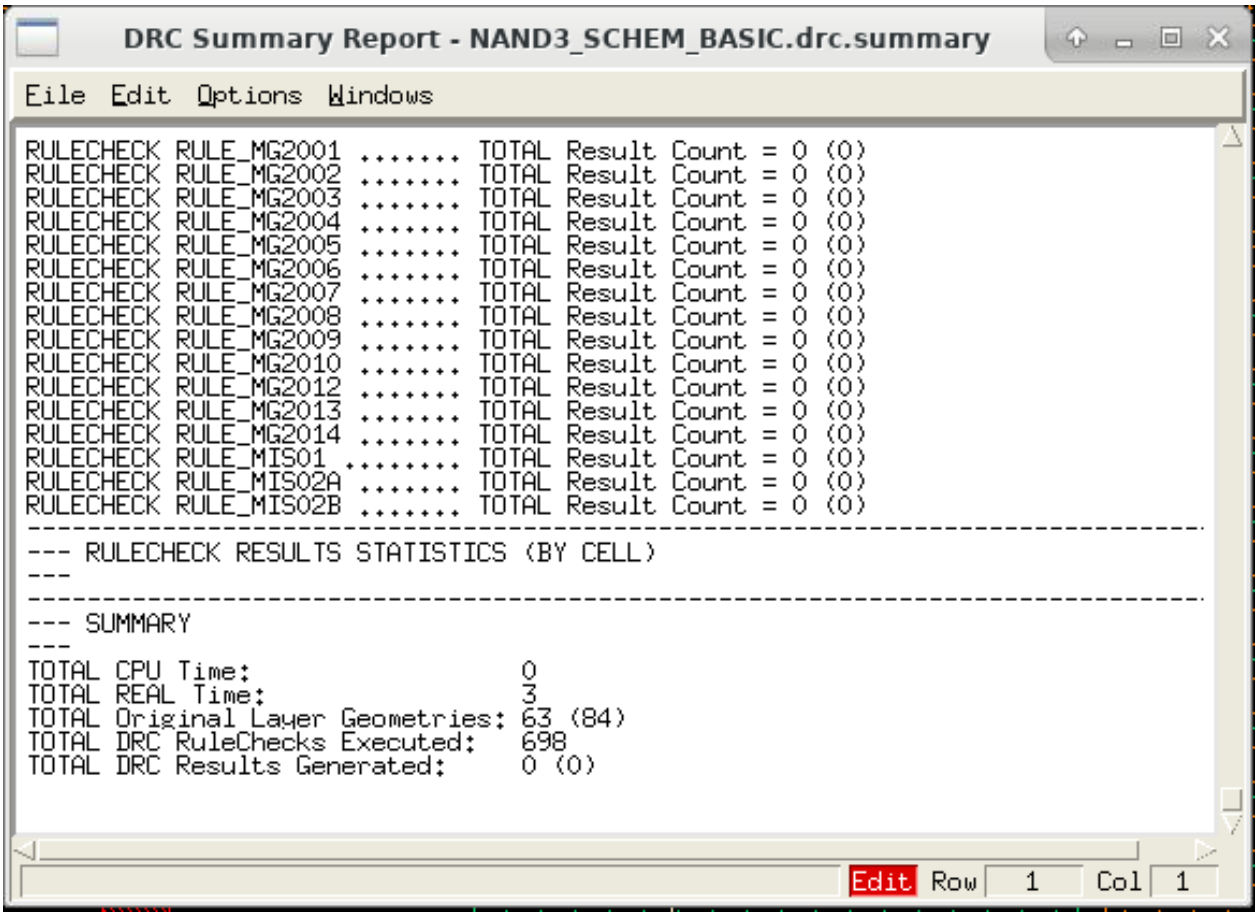


Figure 2: DRC Summary report (I solved the two rule checks that we were allowed to ignore)

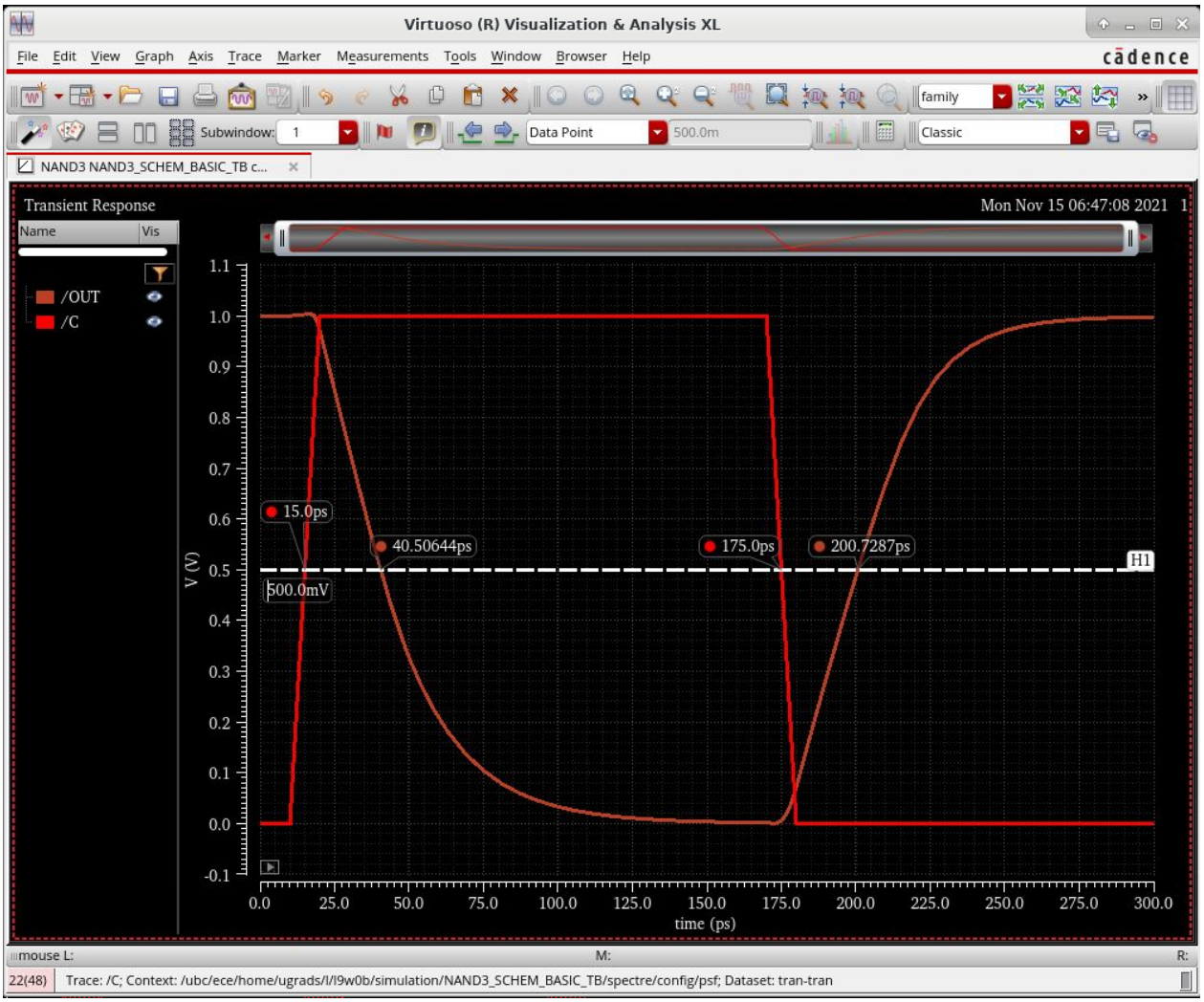


Figure 3: Timing of the gate. td,HL = 25.507ps, td,LD = 25.72ps. This graph was generated from the extracted view including all parasitics.

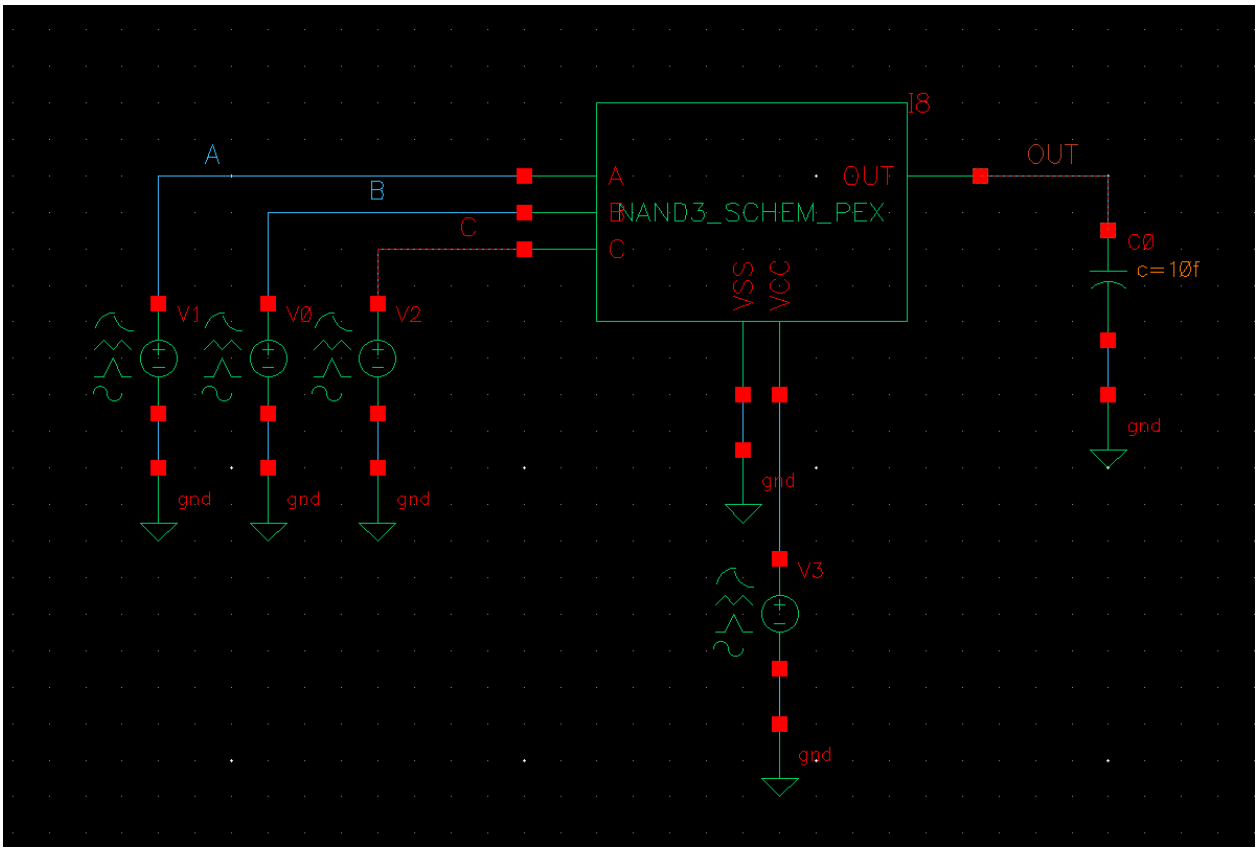


Figure 4: Screen-shot of my test bench schematic. I used a 10pF capacitor as the load. Worst-case switching was used (switching C, aka bottom n-fet results in worst switching).

2 Problem 2

2.1 a)

Using demorgan's law:

$$\overline{F} = CD(B + A)$$

$$\overline{\overline{F}} = \overline{CD(B + A)}$$

$$F = \overline{C} + \overline{D} + \overline{B + A}$$

$$F = \overline{C} + \overline{D} + \overline{BA}$$

2.2 b)

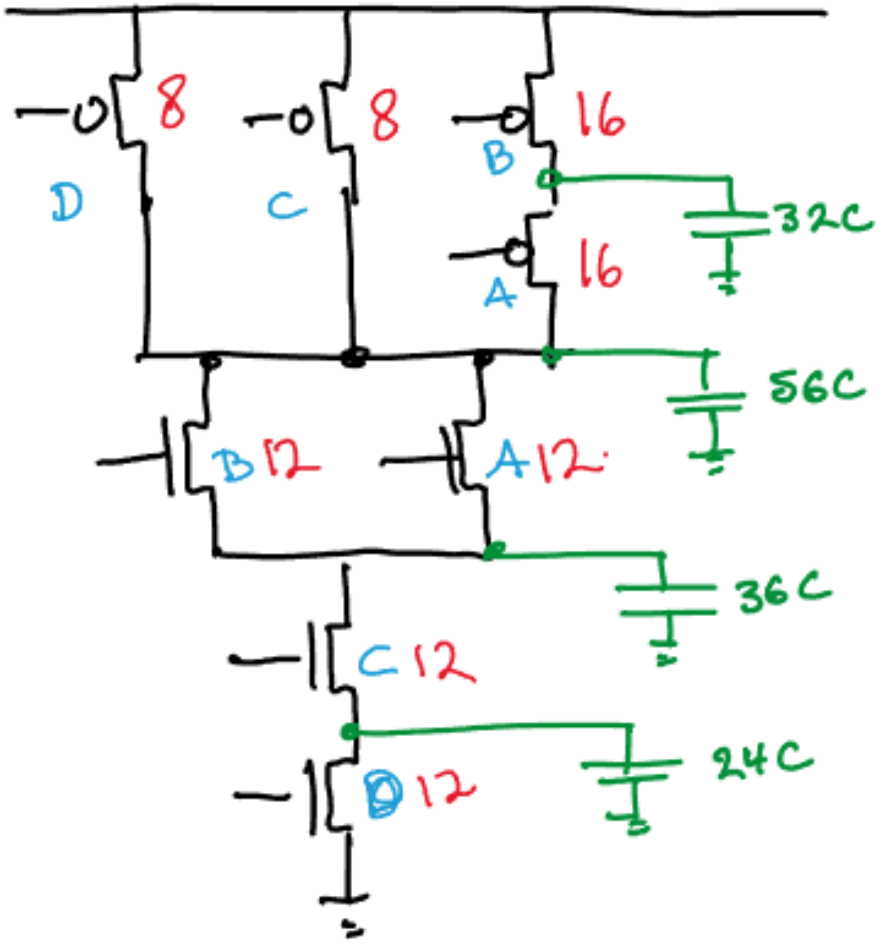


Figure 5: Drawing indicating the sizing of the gates when the output resistance is the same of that of a 8:4 P-N inverter.

2.3 c)

Worst-case t_{PHL}

time	A	B	C	D
0	1	0	1	0
1	0	1	1	1

Worst-case t_{PLH}

time	A	B	C	D
0	0	1	1	1
1	0	1	1	0

Figure 6: Two tables indicating the worse-case switching conditions for this gate. T=0 is the initial condition, T=1 is the second condition. These switching conditions switch the largest charged capacitances through the largest resistances.

In order to verify that these were in fact the worst-case conditions for this gate, I decided to compare them with what I thought were the second-worst case switching conditions for both t_{PHL} and t_{PLH}. Here are what I think the second worst-case scenarios are.

Second-worst-case t_{PHL}

time	A	B	C	D
0	1	0	1	0
1	1	0	1	1

Second-worst case t_{PLH}

time	A	B	C	D
0	1	0	1	1
1	1	0	1	0

Figure 7: Two tables indicating the **second** worse-case switching conditions for this gate. These conditions switch all but one set of capacitances.

Now I made this circuit in Cadence, and simulated all of the various switching conditions.

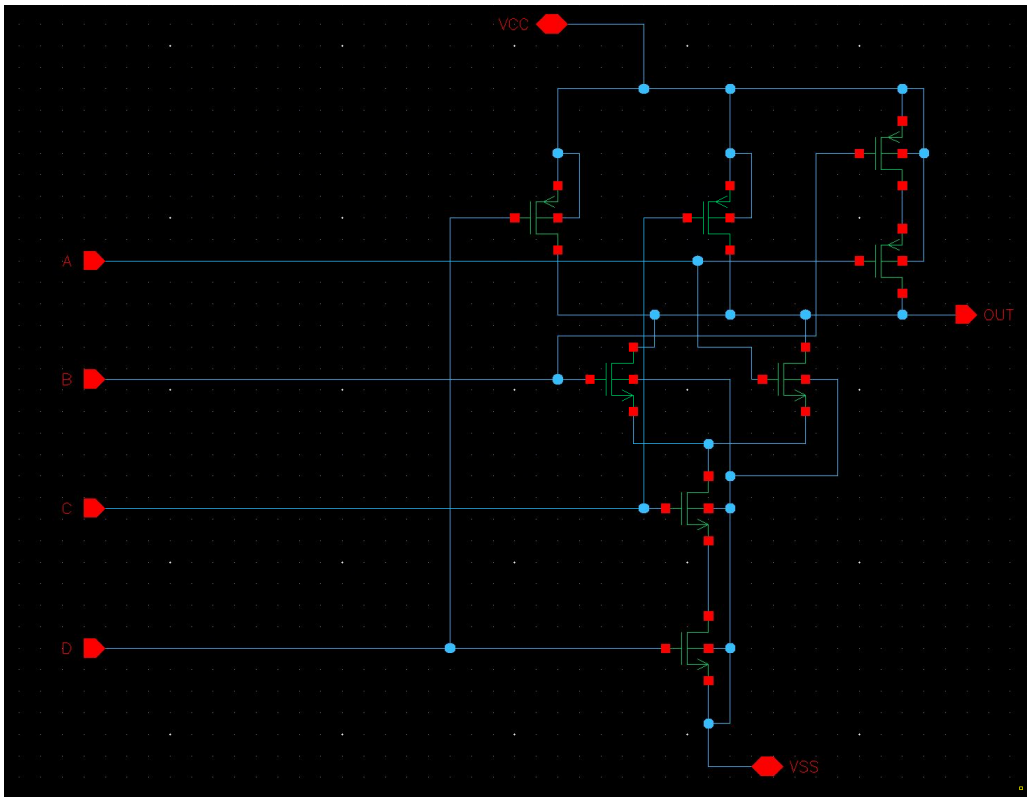


Figure 8: Schematic of the gate.

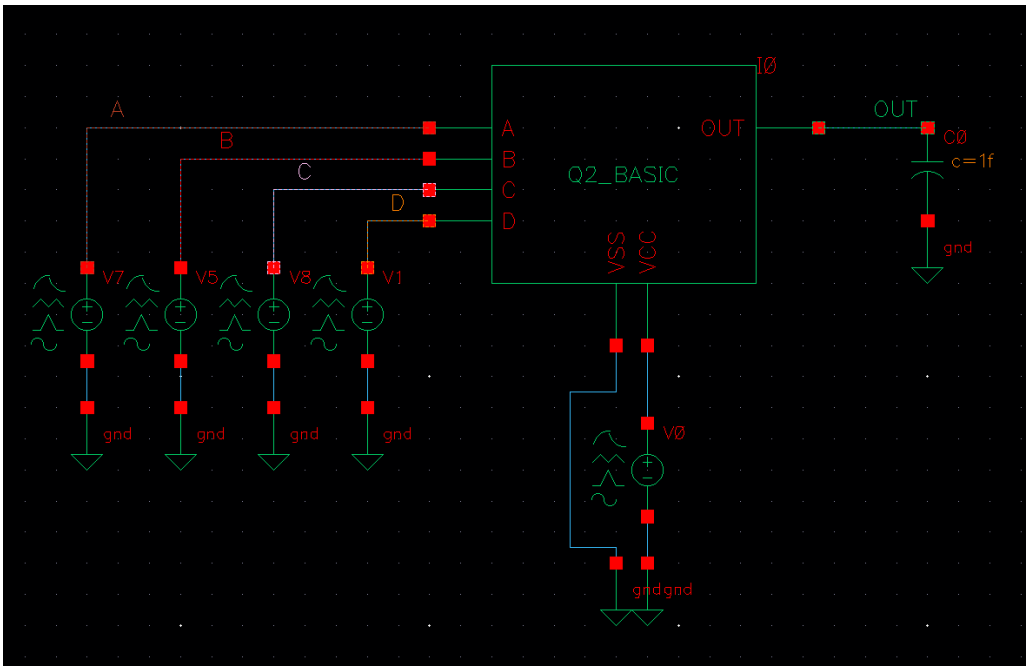


Figure 9: Test bench schematic. The signals generated for A, B, C, and D were generated depending on the test being run. They had a rise time of 0.

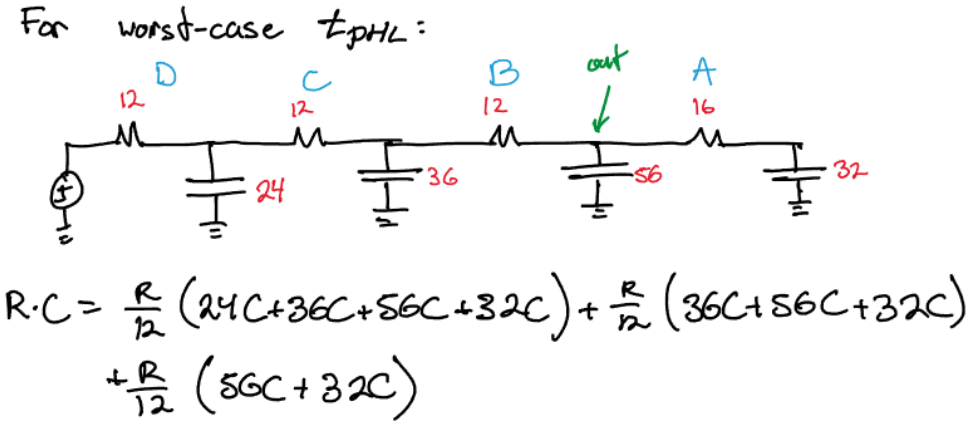


Figure 10: Elmore delay for this circuit, for figuring out worst-case switch conditions.

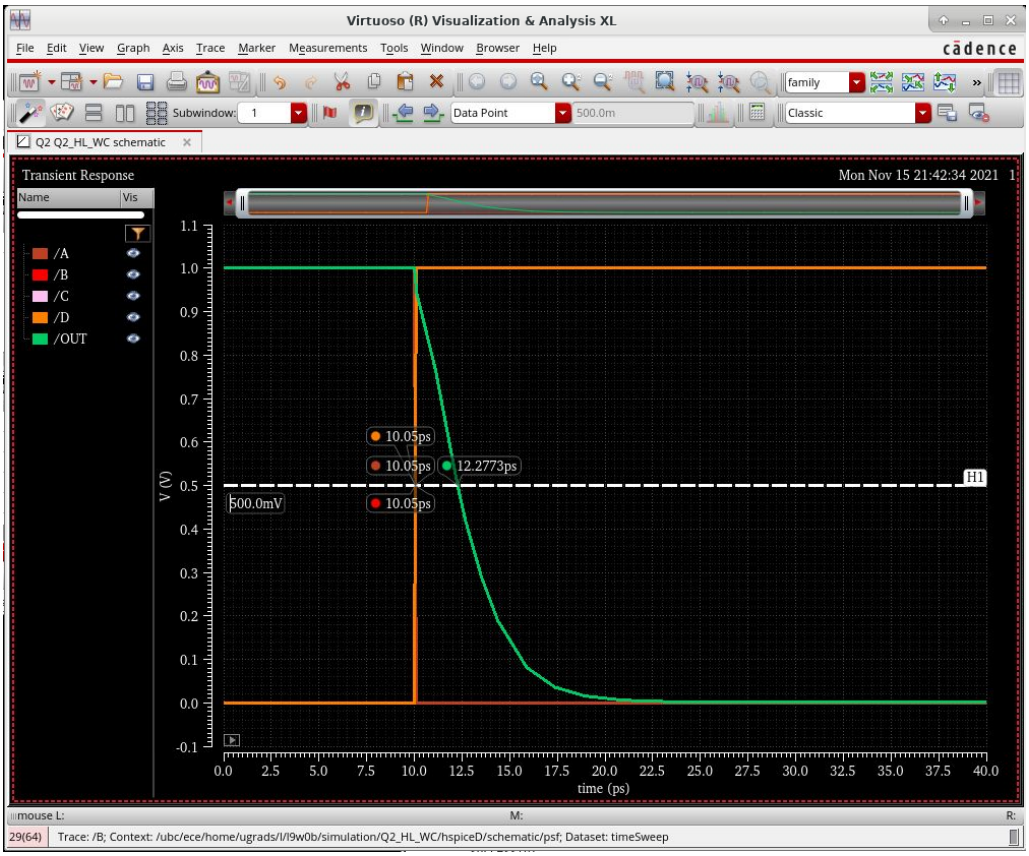


Figure 11: Switching waveform for worst-case t_{PHL}. The switching delay is 2.227ps

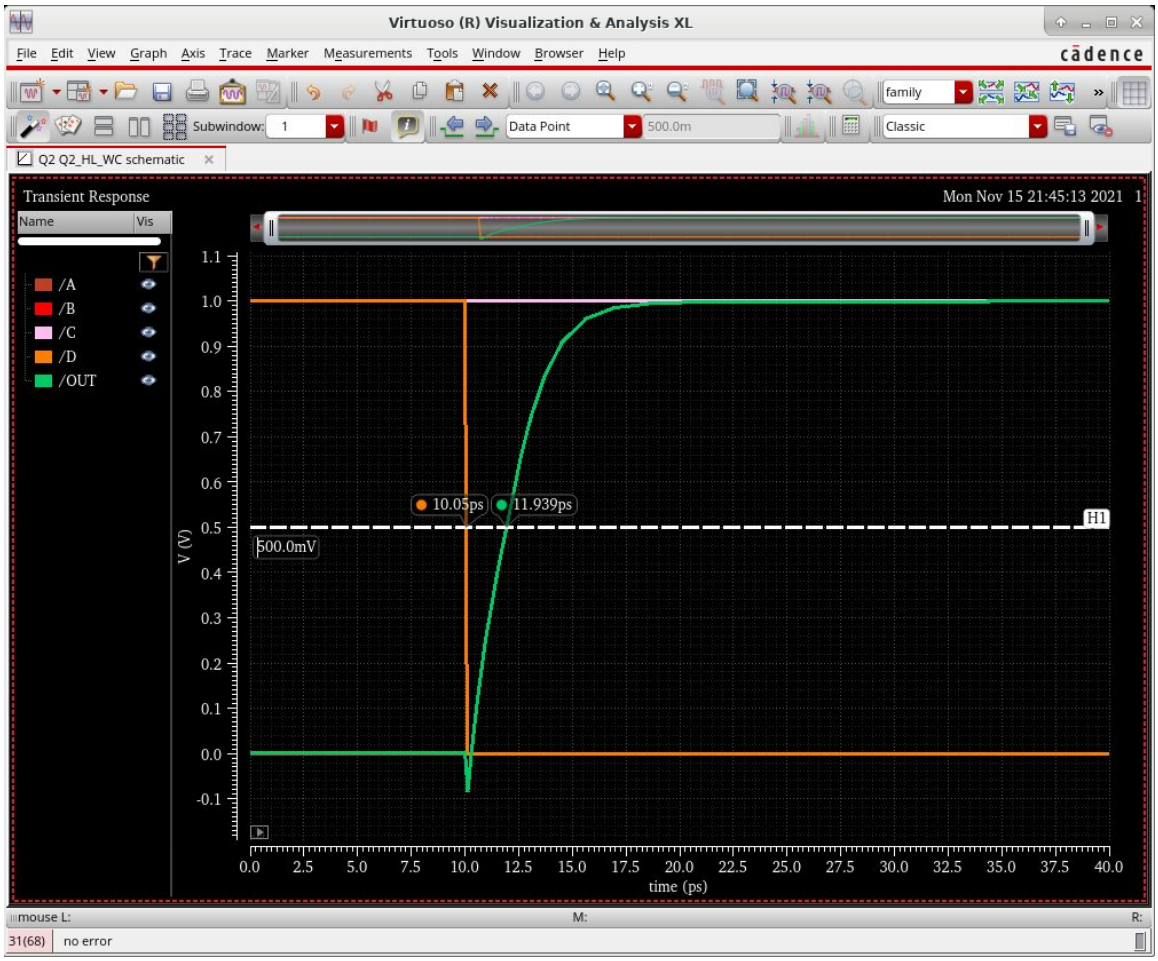


Figure 12: Switching waveform for worst-case t_{PLH}. The switching delay is 1.889ps

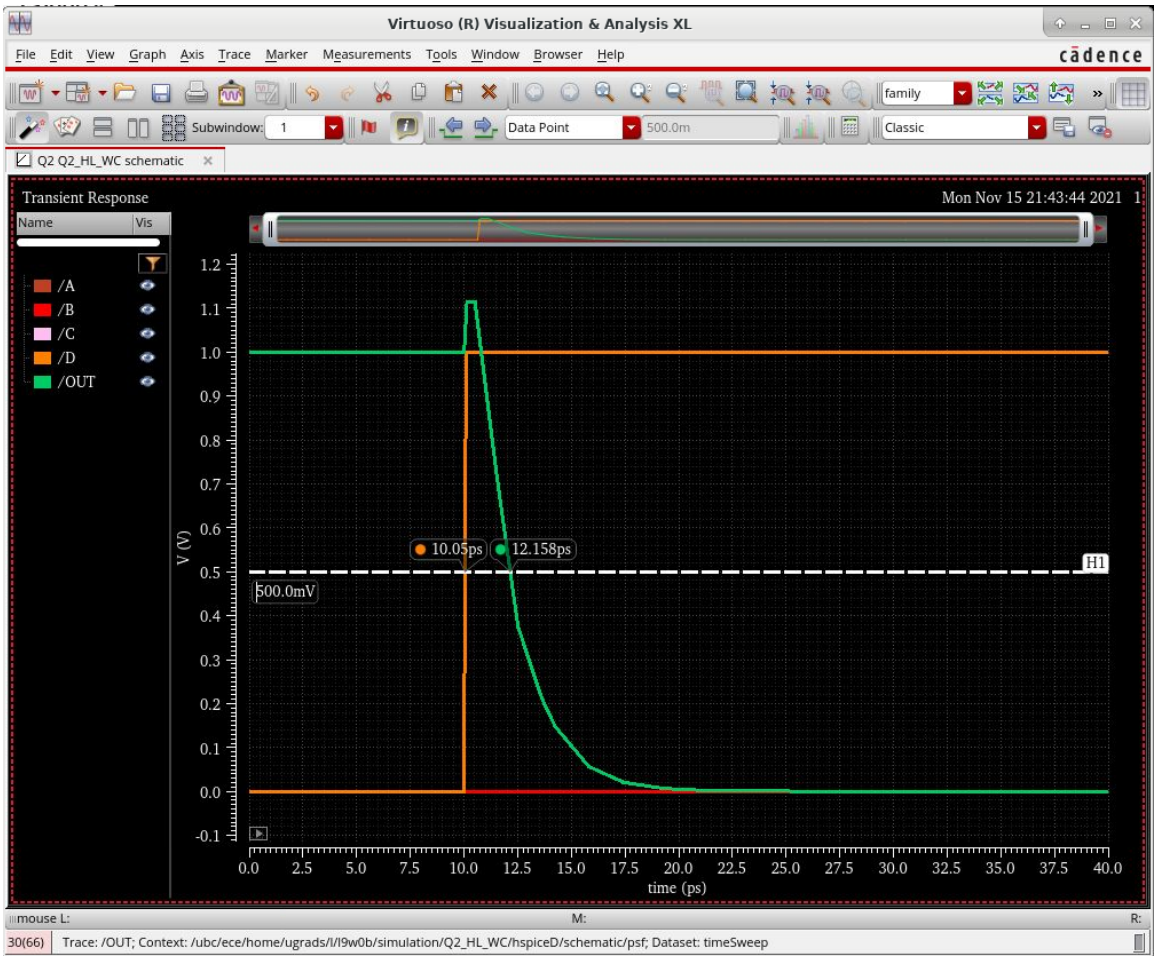


Figure 13: Switching waveform for **second** worst-case t_{PHL}. The switching delay is 2.108ps

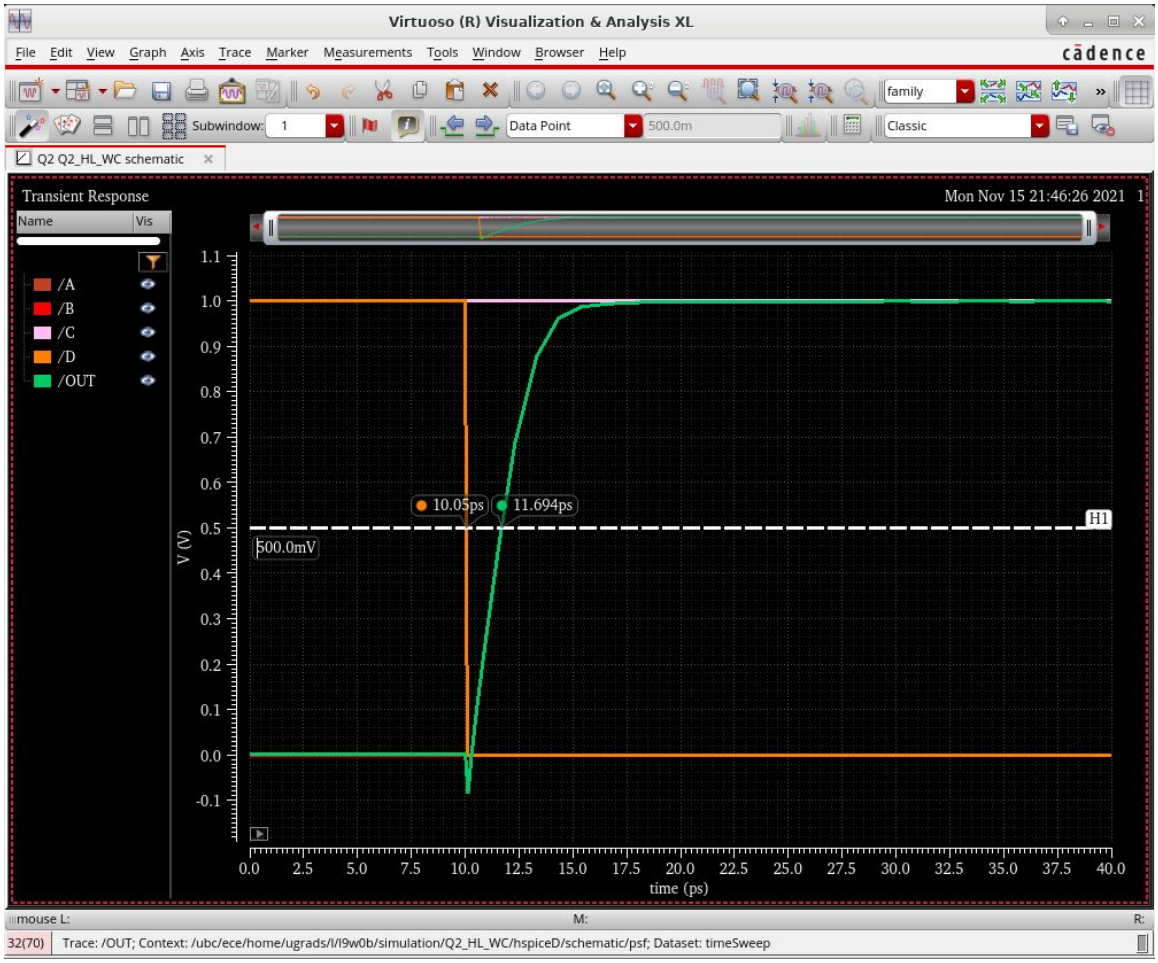


Figure 14: Switching waveform for **second** worst-case t_{PLH}. The switching delay is 1.644ps

Tallying it all up, here are the switching delays:

	t_{PHL}	t_{PLH}
Worst-case	2.227ps	1.889ps
Second-worst-case	2.108ps	1.644ps

As we can see, the worst-case delay is longer than the second-worst case delay. While this isn't exhaustive proof that we have in fact found the worst-case delay, it serves to reinforce my understanding of where the delays are coming from.

3 Problem 3

3.1 a)

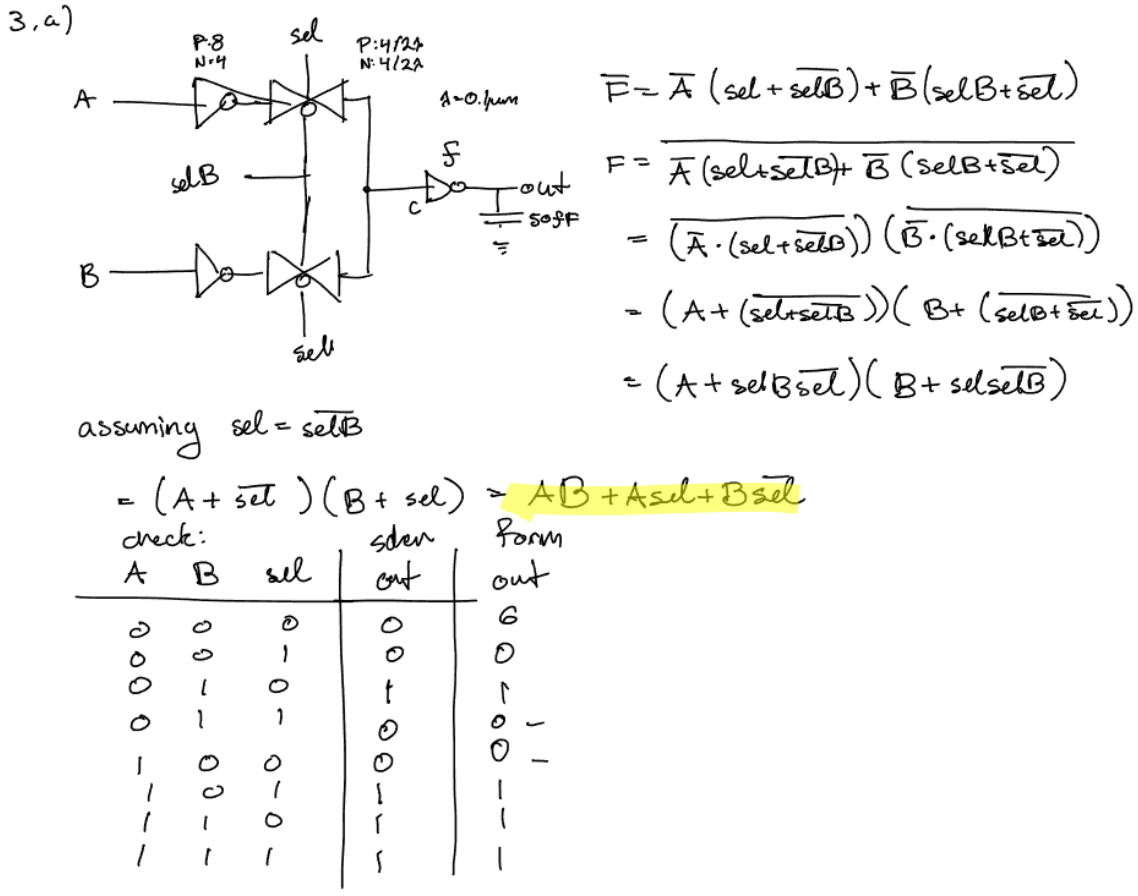
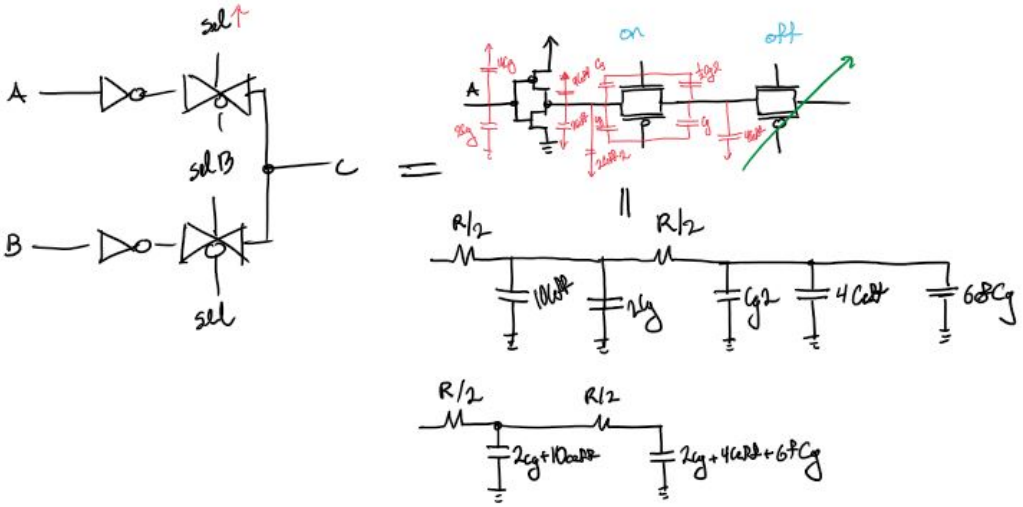


Figure 15: Derivation of the output expression. Here I made the assumption that sel and selB are inverses of each other.

b)



c) using Elmore delay:

$$t = \left(\frac{R}{2}\left[2C_g + 10C_{diff} + 2C_g + 4C_{diff} + 6.8C_g\right] + \frac{R}{2}\left[2C_g + 4C_{diff} + 6.8C_g\right]\right)$$

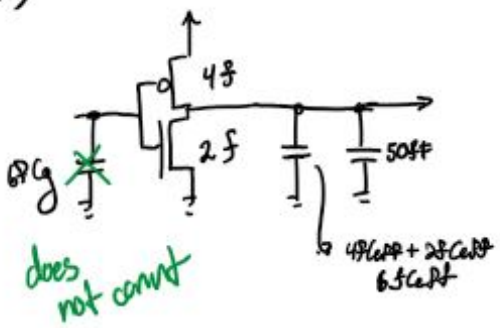
$$= \frac{R}{2}W\left[4C_g + 14C_{diff} + 2C_g + 4C_{diff} + 13.6C_g\right]$$

$$= \frac{R}{2}W\left[6C_g + 18C_{diff} + 13.6C_g\right] = RW\left[3C_g + 9C_{diff} + 6.8C_g\right]$$

$$= RW\left[(3+6.8)C_g + 9C_{diff}\right]$$

d)

d)



$$t = \ln 2 \cdot R \cdot C$$

$$= \ln 2 \cdot (2fR_{eff}W)(6fC_{eff}W + 50fF)$$

e) optimal size $\Rightarrow \frac{\delta t}{\delta f} = 0$

$$t = \ln 2 \cdot (2R)(6fC_{eff}W + 50fF)f + R[(3+6f)C_g + 9C_{eff}]W^2$$

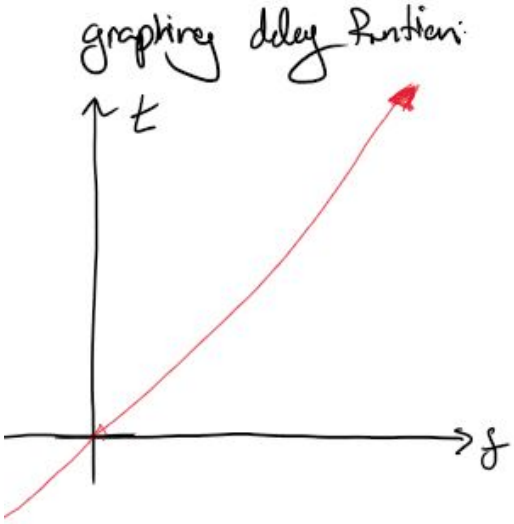
$$t = \ln 2 \cdot 2R\left[6f^2 C_{eff}W + (50fF)f\right] + R\left[(3+6f)C_g + 9C_{eff}\right]W^2$$

$$\frac{\delta t}{\delta f} = \ln 2 \cdot 2R\left[12fC_{eff}W + 50fF\right] + R \cdot 6C_g W^2 = 0$$

$$\left[\frac{-3 \cdot C_g W}{\ln 2} - 50fF\right] \cdot \frac{1}{12\,C_{eff}W} = f$$

assuming: $C_{eff} = 1fF/\mu m$ $C_g = 2fF/\mu m$ $R = 12.5k$

$$f = -4.167$$



looks like that
the inverter loads the
gate too much. (>4 times fan)
In order to improve
speed it would probably
make sense to place an intermediate
inverter.