Digital Bubble Level - Cadence RTL Synthesis

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October 10, 2021

1 Introduction

2 Outputs of RTL Compiler

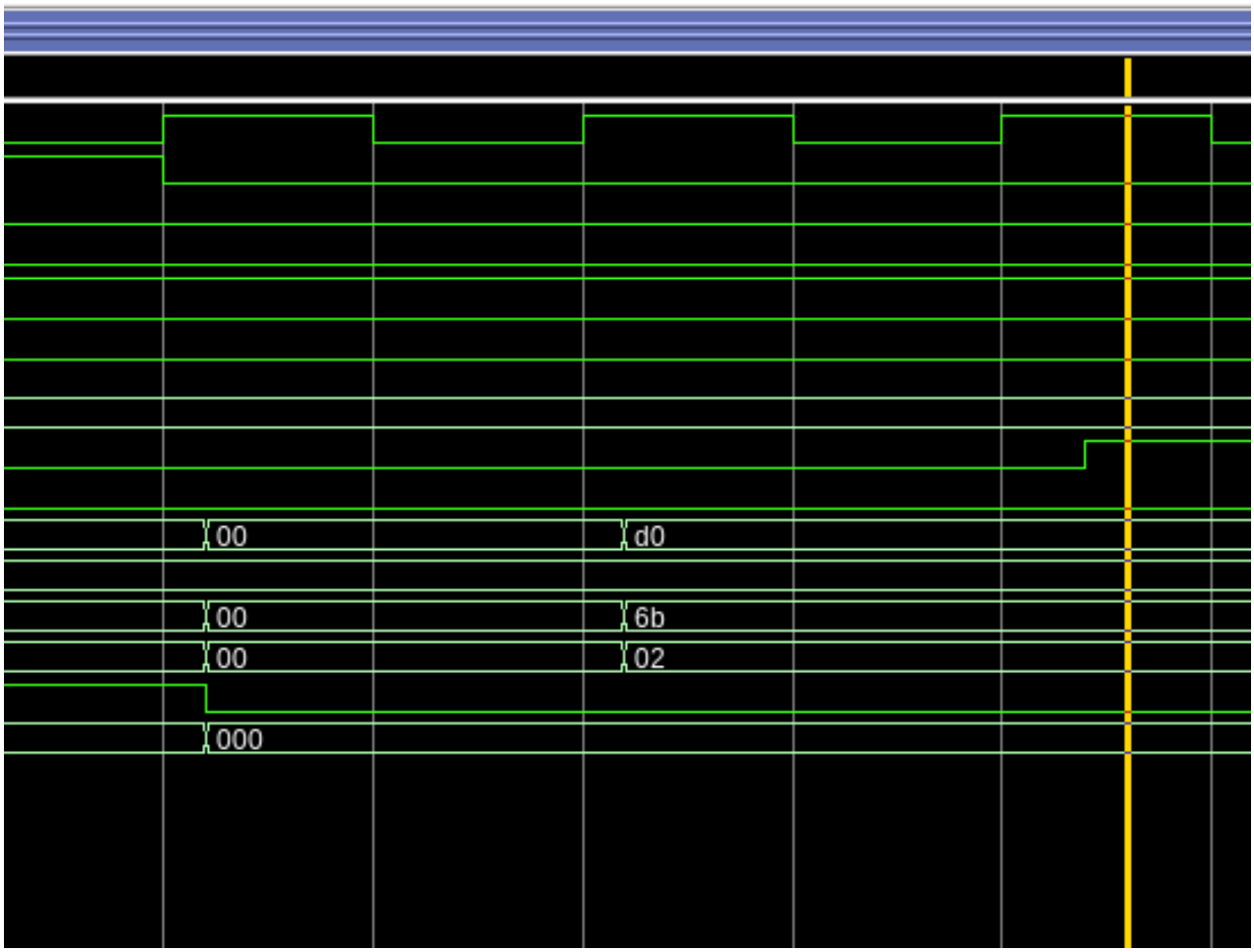

Figure 1:

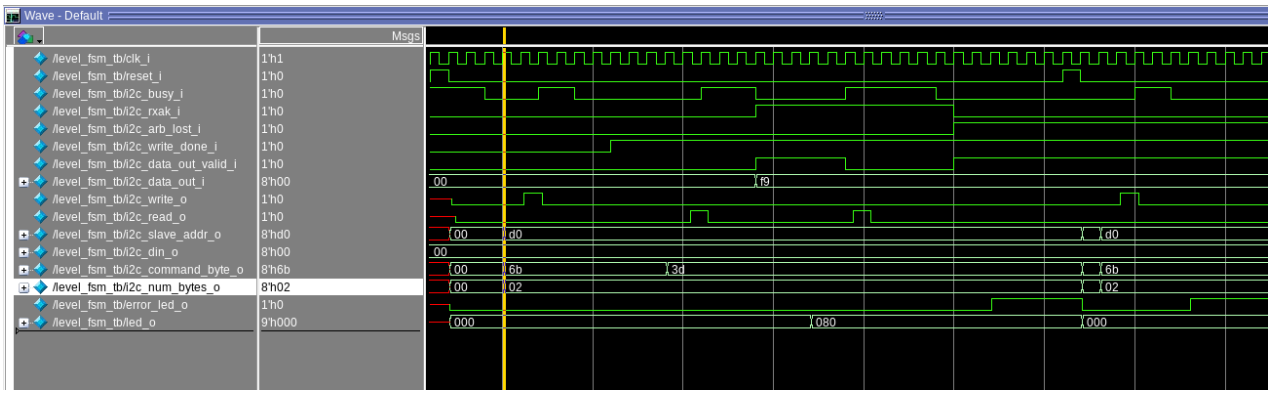

Figure 2:

3 Outputs of RTL Compiler

3.1 Reports

level_fsm_area.rpt

```
================================================================
  Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
  Generated on:           Oct 04 2021  02:49:37 pm
  Module:                 level_fsm
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   worst_low (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================

 Instance   Cells   Cell Area   Net Area   Total Area   Wireload
-----------------------------------------------------------------
level_fsm     273          94          0           94    <none> (D)

(D) = wireload is default in technology library
```

level_fsm_gates.rpt

```
================================================================
  Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
  Generated on:           Oct 04 2021  02:49:37 pm
  Module:                 level_fsm
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   worst_low (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================
```

Gate	Instances	Area	Library
AND2_X1	6	1.769	NanGate_15nm_OCL
AND2_X2	2	0.688	NanGate_15nm_OCL
AND3_X1	1	0.393	NanGate_15nm_OCL
AOI21_X1	6	1.769	NanGate_15nm_OCL
AOI22_X1	2	0.688	NanGate_15nm_OCL
BUF_X1	5	1.229	NanGate_15nm_OCL
BUF_X2	1	0.246	NanGate_15nm_OCL
BUF_X4	2	0.786	NanGate_15nm_OCL
CLKBUF_X1	3	0.737	NanGate_15nm_OCL
CLKBUF_X12	2	1.966	NanGate_15nm_OCL
CLKBUF_X2	6	1.475	NanGate_15nm_OCL
CLKBUF_X4	1	0.393	NanGate_15nm_OCL

DFFRNQ_X1	3	3.834	NanGate_15nm_OCL
DFFSNQ_X1	24	30.671	NanGate_15nm_OCL
INV_X1	53	7.815	NanGate_15nm_OCL
INV_X2	8	1.573	NanGate_15nm_OCL
NAND2_X1	40	7.864	NanGate_15nm_OCL
NAND2_X2	6	1.769	NanGate_15nm_OCL
NAND3_X1	13	3.834	NanGate_15nm_OCL
NAND3_X2	2	0.885	NanGate_15nm_OCL
NAND4_X1	6	2.064	NanGate_15nm_OCL
NAND4_X2	1	0.541	NanGate_15nm_OCL
NOR2_X1	37	7.274	NanGate_15nm_OCL
NOR2_X2	12	3.539	NanGate_15nm_OCL
NOR3_X1	5	1.475	NanGate_15nm_OCL
OAI21_X1	13	3.834	NanGate_15nm_OCL
OAI22_X1	8	2.753	NanGate_15nm_OCL
OR2_X1	2	0.590	NanGate_15nm_OCL
OR2_X2	1	0.344	NanGate_15nm_OCL
OR3_X1	1	0.393	NanGate_15nm_OCL
OR4_X1	1	0.442	NanGate_15nm_OCL
total	273	93.635	

Type	Instances	Area	Area %
sequential	27	34.505	36.9
inverter	61	9.388	10.0
buffer	20	6.832	7.3
logic	165	42.910	45.8
total	273	93.635	100.0

level_fsm_power.rpt

Generated by:	Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
Generated on:	Oct 04 2021 02:49:37 pm
Module:	level_fsm
Technology library:	NanGate_15nm_OCL revision 1.0
Operating conditions:	worst_low (balanced_tree)
Wireload mode:	enclosed
Area mode:	timing library

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
level_fsm	273	78.734	2505102.378	2505181.112

level_fsm_timing.rpt

Generated by:	Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
Generated on:	Oct 04 2021 02:49:37 pm
Module:	level_fsm
Technology library:	NanGate_15nm_OCL revision 1.0
Operating conditions:	worst_low (balanced_tree)
Wireload mode:	enclosed
Area mode:	timing library

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
(clock clk)	launch					0	R
state_reg[2]/CLK				0		0	R
state_reg[2]/Q	DFFSNQ_X1	5	4.1	7	+16	16	F
fopt24466/I					+0	16	
fopt24466/ZN	INV_X1	1	1.0	3	+4	20	R
g24554/A1					+0	20	
g24554/ZN	NAND2_X1	2	1.6	6	+4	24	F
g24529/A1					+0	24	
g24529/ZN	NOR2_X1	2	1.8	6	+5	29	R

```
g24528/A1                                           +0     29
g24528/Z            AND2_X2        5   7.0     7   +10     40 R
g24002/A1                                           +0     40
g24002/ZN           NAND2_X2       3   2.4     5    +4     44 F
g81/A1                                              +0     44
g81/ZN              OAI21_X1       1   0.6     4    +4     47 R
led_o_reg[6]/D      DFFSNQ_X1                       +0     47
led_o_reg[6]/CLK    setup                      0    +9     56 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)         capture                                20 R
-----------------------------------------------------------------
Cost Group    : 'clk' (path_group 'clk')
Timing slack  :     -36ps (TIMING VIOLATION)
Start-point   : state_reg[2]/CLK
End-point     : led_o_reg[6]/D
```

3.2 Mapped Verilog

level_fsm_map.v

```verilog

// Generated by Cadence Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1

// Verification Directory fv/level_fsm

module level_fsm(clk_i, reset_i, i2c_busy_i, i2c_rxak_i,
     i2c_arb_lost_i, i2c_write_done_i, i2c_data_out_valid_i,
     i2c_data_out_i, i2c_write_o, i2c_read_o, i2c_slave_addr_o,
     i2c_din_o, i2c_command_byte_o, i2c_num_bytes_o, error_led_o,
     led_o);
  input clk_i, reset_i, i2c_busy_i, i2c_rxak_i, i2c_arb_lost_i,
       i2c_write_done_i, i2c_data_out_valid_i;
  input [7:0] i2c_data_out_i;
  output i2c_write_o, i2c_read_o, error_led_o;
  output [7:0] i2c_slave_addr_o, i2c_din_o, i2c_command_byte_o,
       i2c_num_bytes_o;
  output [8:0] led_o;
  wire clk_i, reset_i, i2c_busy_i, i2c_rxak_i, i2c_arb_lost_i,
       i2c_write_done_i, i2c_data_out_valid_i;
  wire [7:0] i2c_data_out_i;
  wire i2c_write_o, i2c_read_o, error_led_o;
  wire [7:0] i2c_slave_addr_o, i2c_din_o, i2c_command_byte_o,
       i2c_num_bytes_o;
  wire [8:0] led_o;
  wire [7:0] raw_buffer;
  wire [6:0] state;
  wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
  wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
  wire n_16, n_19, n_24, n_25, n_28, n_33, n_36, n_37;
  wire n_41, n_44, n_45, n_46, n_49, n_50, n_51, n_53;
  wire n_57, n_58, n_60, n_61, n_62, n_66, n_68, n_71;
  wire n_72, n_75, n_77, n_79, n_80, n_82, n_85, n_87;
  wire n_88, n_93, n_95, n_100, n_101, n_104, n_114, n_116;
  wire n_121, n_129, n_130, n_135, n_136, n_138, n_141, n_142;
  wire n_143, n_144, n_148, n_149, n_153, n_154, n_155, n_158;
  wire n_160, n_173, n_175, n_176, n_178, n_179, n_181, n_182;
  wire n_184, n_187, n_189, n_191, n_192, n_204, n_205, n_206;
  wire n_207, n_208, n_209, n_212, n_213, n_246, n_262, n_286;
  wire n_317, n_320, n_324, n_326, n_327, n_332, n_381, n_401;
  wire n_527, n_541, n_543, n_550, n_551, n_555, n_559, n_562;
  wire n_563, n_565, n_566, n_567, n_573, n_582, n_587, n_588;
  wire n_590, n_591, n_596, n_606, n_607, n_609, n_619, n_628;
  wire n_630, n_631, n_632, n_634, n_635, n_638, n_639, n_642;
  wire n_645, n_653, n_655, n_657, n_659, n_664, n_676, n_677;
  wire n_680, n_688, n_689, n_690, n_699, n_700, n_701, n_702;
  wire n_703, n_713, n_714, n_715, n_716, n_717, n_718, n_720;
  wire n_721, n_724, n_725, n_727, n_728, n_734, n_736, n_737;
  wire n_738, n_740, n_748, n_749, n_751, n_753, n_755, n_757;
  wire n_758, n_760, n_761, n_763, n_764, n_765, n_767, n_770;
  wire n_775, n_777, n_778, n_781, n_784, n_850, n_851, n_898;
  wire n_899, n_900, n_901, n_902, n_903, n_904, n_905, n_908;
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```
52      wire n_935, n_936, n_937, n_938, n_968, n_969, n_970, n_971;
53      wire n_1009, n_1010, n_1012, n_1021, n_1024, n_1025, n_1026, n_1027;
54      wire n_1028, n_1029, n_1030, n_1031, n_1032, n_1033, n_1034, n_1035;
55      wire n_1036, n_1037, n_1038, n_1039, n_1040, n_1041, n_1042, n_1107;
56      wire n_1112, n_1113, n_1114, n_1117, n_1130, n_1131, n_1142, n_1143;
57      wire n_1144, n_1150, n_1151, n_1152;
58      assign i2c_num_bytes_o[0] = 1'b0;
59      assign i2c_num_bytes_o[1] = i2c_slave_addr_o[7];
60      assign i2c_num_bytes_o[2] = 1'b0;
61      assign i2c_num_bytes_o[3] = 1'b0;
62      assign i2c_num_bytes_o[4] = 1'b0;
63      assign i2c_num_bytes_o[5] = 1'b0;
64      assign i2c_num_bytes_o[6] = 1'b0;
65      assign i2c_num_bytes_o[7] = 1'b0;
66      assign i2c_command_byte_o[0] = i2c_slave_addr_o[7];
67      assign i2c_command_byte_o[1] = i2c_command_byte_o[6];
68      assign i2c_command_byte_o[2] = i2c_command_byte_o[4];
69      assign i2c_command_byte_o[3] = i2c_slave_addr_o[7];
70      assign i2c_command_byte_o[5] = i2c_slave_addr_o[7];
71      assign i2c_command_byte_o[7] = 1'b0;
72      assign i2c_din_o[0] = 1'b0;
73      assign i2c_din_o[1] = 1'b0;
74      assign i2c_din_o[2] = 1'b0;
75      assign i2c_din_o[3] = 1'b0;
76      assign i2c_din_o[4] = 1'b0;
77      assign i2c_din_o[5] = 1'b0;
78      assign i2c_din_o[6] = 1'b0;
79      assign i2c_din_o[7] = 1'b0;
80      assign i2c_slave_addr_o[0] = 1'b0;
81      assign i2c_slave_addr_o[1] = 1'b0;
82      assign i2c_slave_addr_o[2] = 1'b0;
83      assign i2c_slave_addr_o[3] = 1'b0;
84      assign i2c_slave_addr_o[4] = i2c_slave_addr_o[7];
85      assign i2c_slave_addr_o[5] = 1'b0;
86      assign i2c_slave_addr_o[6] = i2c_slave_addr_o[7];
87      DFFSNQ_X1 \raw_buffer_reg[0] (.SN (1'b1), .CLK (clk_i), .D (n_213),
88            .Q (raw_buffer[0]));
89      DFFSNQ_X1 \raw_buffer_reg[1] (.SN (1'b1), .CLK (clk_i), .D (n_212),
90            .Q (raw_buffer[1]));
91      DFFSNQ_X1 \raw_buffer_reg[2] (.SN (1'b1), .CLK (clk_i), .D (n_209),
92            .Q (raw_buffer[2]));
93      DFFSNQ_X1 \raw_buffer_reg[3] (.SN (1'b1), .CLK (clk_i), .D (n_208),
94            .Q (raw_buffer[3]));
95      DFFSNQ_X1 \raw_buffer_reg[4] (.SN (1'b1), .CLK (clk_i), .D (n_207),
96            .Q (raw_buffer[4]));
97      DFFSNQ_X1 \raw_buffer_reg[5] (.SN (1'b1), .CLK (clk_i), .D (n_204),
98            .Q (raw_buffer[5]));
99      DFFSNQ_X1 \raw_buffer_reg[6] (.SN (1'b1), .CLK (clk_i), .D (n_206),
100           .Q (raw_buffer[6]));
101     DFFSNQ_X1 \raw_buffer_reg[7] (.SN (1'b1), .CLK (clk_i), .D (n_205),
102           .Q (raw_buffer[7]));
103     DFFSNQ_X1 \state_reg[3] (.SN (1'b1), .CLK (clk_i), .D (n_573), .Q
104           (state[3]));
105     OAI22_X1 g23925(.A1 (n_718), .A2 (n_7), .B1 (n_566), .B2 (n_49), .ZN
106           (n_213));
107     OAI22_X1 g23926(.A1 (n_718), .A2 (n_3), .B1 (n_566), .B2 (n_50), .ZN
108           (n_212));
109     OAI22_X1 g23927(.A1 (n_718), .A2 (n_1), .B1 (n_566), .B2 (n_58), .ZN
110           (n_209));
111     OAI22_X1 g23928(.A1 (n_718), .A2 (n_6), .B1 (n_566), .B2 (n_2), .ZN
112           (n_208));
113     DFFSNQ_X1 \state_reg[4] (.SN (1'b1), .CLK (clk_i), .D (n_635), .Q
114           (state[4]));
115     DFFRNQ_X1 \i2c_command_byte_o_reg[1] (.RN (1'b1), .CLK (clk_i), .D
116           (n_1026), .Q (i2c_command_byte_o[6]));
117     DFFSNQ_X1 \state_reg[5] (.SN (1'b1), .CLK (clk_i), .D (n_938), .Q
118           (state[5]));
119     OAI22_X1 g23929(.A1 (n_718), .A2 (n_8), .B1 (n_566), .B2 (n_13), .ZN
120           (n_207));
121     OAI22_X1 g23930(.A1 (n_718), .A2 (n_12), .B1 (n_566), .B2 (n_14), .ZN
122           (n_206));
123     OAI22_X1 g23931(.A1 (n_718), .A2 (n_4), .B1 (n_566), .B2 (n_100), .ZN
124           (n_205));
125     OAI22_X1 g23932(.A1 (n_718), .A2 (n_15), .B1 (n_566), .B2 (n_10), .ZN
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126         (n_204));
127     DFFSNQ_X1 \state_reg[2] (.SN (1'b1), .CLK (clk_i), .D (n_703), .Q
128         (error_led_o));
129     DFFSNQ_X1 \state_reg[6] (.SN (1'b1), .CLK (clk_i), .D (n_757), .Q
130         (state[6]));
131     DFFSNQ_X1 \i2c_command_byte_o_reg[2] (.SN (1'b1), .CLK (clk_i), .D
132         (n_971), .Q (i2c_command_byte_o[4]));
133     DFFSNQ_X1 \led_o_reg[1] (.SN (1'b1), .CLK (clk_i), .D (n_1107), .Q
134         (led_o[1]));
135     DFFRNQ_X1 \i2c_slave_addr_o_reg[4] (.RN (1'b1), .CLK (clk_i), .D
136         (n_1027), .Q (i2c_slave_addr_o[7]));
137     DFFRNQ_X1 \led_o_reg[4] (.RN (1'b1), .CLK (clk_i), .D (n_189), .Q
138         (led_o[4]));
139     DFFSNQ_X1 \led_o_reg[0] (.SN (1'b1), .CLK (clk_i), .D (n_182), .Q
140         (led_o[0]));
141     DFFSNQ_X1 \led_o_reg[7] (.SN (1'b1), .CLK (clk_i), .D (n_1112), .Q
142         (led_o[7]));
143     DFFSNQ_X1 \led_o_reg[3] (.SN (1'b1), .CLK (clk_i), .D (n_179), .Q
144         (led_o[3]));
145     DFFSNQ_X1 \led_o_reg[5] (.SN (1'b1), .CLK (clk_i), .D (n_1117), .Q
146         (led_o[5]));
147     DFFSNQ_X1 \led_o_reg[2] (.SN (1'b1), .CLK (clk_i), .D (n_192), .Q
148         (led_o[2]));
149     DFFSNQ_X1 \led_o_reg[8] (.SN (1'b1), .CLK (clk_i), .D (n_181), .Q
150         (led_o[8]));
151     DFFSNQ_X1 \led_o_reg[6] (.SN (1'b1), .CLK (clk_i), .D (n_619), .Q
152         (led_o[6]));
153     OAI21_X1 g23965(.A1 (n_191), .A2 (n_175), .B (n_588), .ZN (n_192));
154     NAND3_X1 g23945(.A1 (n_144), .A2 (n_143), .A3 (n_130), .ZN (n_189));
155     OAI21_X1 g23949(.A1 (n_88), .A2 (n_135), .B (i2c_command_byte_o[6]),
156         .ZN (n_187));
157     OAI21_X1 g23958(.A1 (n_587), .A2 (n_11), .B (n_160), .ZN (n_182));
158     OAI21_X1 g23959(.A1 (n_587), .A2 (n_5), .B (n_148), .ZN (n_181));
159     OAI21_X1 g23960(.A1 (n_191), .A2 (n_178), .B (n_1010), .ZN (n_179));
160     DFFSNQ_X1 \state_reg[1] (.SN (1'b1), .CLK (clk_i), .D (n_138), .Q
161         (state[1]));
162     NAND2_X1 g23975(.A1 (n_121), .A2 (n_677), .ZN (n_160));
163     NAND2_X1 g23982(.A1 (n_778), .A2 (n_905), .ZN (n_158));
164     NAND2_X1 g23997(.A1 (n_153), .A2 (n_784), .ZN (n_154));
165     INV_X1 g24012(.I (n_184), .ZN (n_149));
166     NAND2_X1 g23974(.A1 (n_101), .A2 (n_677), .ZN (n_148));
167     NAND4_X1 g23985(.A1 (n_136), .A2 (n_142), .A3 (n_72), .A4 (n_141),
168         .ZN (n_144));
169     NAND4_X1 g23987(.A1 (n_129), .A2 (n_142), .A3 (n_25), .A4 (n_141),
170         .ZN (n_143));
171     NOR2_X1 g23994(.A1 (n_851), .A2 (n_62), .ZN (n_138));
172     NAND2_X2 g23995(.A1 (n_677), .A2 (n_136), .ZN (n_191));
173     AOI21_X1 g23996(.A1 (n_114), .A2 (n_82), .B (reset_i), .ZN (n_135));
174     DFFSNQ_X1 \state_reg[0] (.SN (1'b1), .CLK (clk_i), .D (n_1031), .Q
175         (state[0]));
176     NAND2_X2 g24013(.A1 (n_645), .A2 (n_68), .ZN (n_184));
177     INV_X1 g24015(.I (n_659), .ZN (n_130));
178     NAND2_X2 g24002(.A1 (n_677), .A2 (n_129), .ZN (n_176));
179     INV_X1 g24039(.I (n_851), .ZN (n_153));
180     AOI21_X1 g24000(.A1 (n_66), .A2 (n_24), .B (raw_buffer[7]), .ZN
181         (n_121));
182     NOR2_X2 g24022(.A1 (n_908), .A2 (n_93), .ZN (n_155));
183     AOI21_X1 g23999(.A1 (n_45), .A2 (n_71), .B (n_100), .ZN (n_101));
184     AOI22_X1 g24038(.A1 (n_1039), .A2 (n_85), .B1 (n_778), .B2 (n_46),
185         .ZN (n_95));
186     NAND2_X1 g24044(.A1 (n_41), .A2 (i2c_busy_i), .ZN (n_93));
187     CLKBUF_X1 g24056(.I (n_676), .Z (n_142));
188     NOR2_X1 g24059(.A1 (n_902), .A2 (n_724), .ZN (n_114));
189     INV_X1 g24100(.I (n_87), .ZN (n_88));
190     NOR2_X1 g24020(.A1 (n_1009), .A2 (raw_buffer[7]), .ZN (n_136));
191     NOR2_X1 g24049(.A1 (n_1040), .A2 (i2c_busy_i), .ZN (n_82));
192     NAND2_X1 g24051(.A1 (n_664), .A2 (n_332), .ZN (n_79));
193     AND2_X1 g24053(.A1 (n_781), .A2 (n_80), .Z (n_77));
194     OR2_X1 g24055(.A1 (n_80), .A2 (reset_i), .Z (n_75));
195     INV_X1 g24062(.I (n_71), .ZN (n_72));
196     NOR2_X1 g24067(.A1 (n_1040), .A2 (n_401), .ZN (n_68));
197     INV_X1 g24070(.I (n_1009), .ZN (n_66));
198     INV_X1 g24101(.I (n_61), .ZN (n_87));
199     NOR2_X1 g24105(.A1 (i2c_read_o), .A2 (n_33), .ZN (n_60));
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200     NOR2_X1 g24021(.A1 (n_44), .A2 (n_100), .ZN (n_129));
201     AOI22_X1 g24033(.A1 (n_19), .A2 (raw_buffer[2]), .B1 (raw_buffer[1]),
202           .B2 (n_58), .ZN (n_175));
203     INV_X1 g24112(.I (n_760), .ZN (n_57));
204     NAND2_X1 g24046(.A1 (n_51), .A2 (raw_buffer[2]), .ZN (n_173));
205     NAND2_X1 g24047(.A1 (n_51), .A2 (n_58), .ZN (n_178));
206     NAND3_X1 g24063(.A1 (n_50), .A2 (n_49), .A3 (n_58), .ZN (n_71));
207     INV_X1 g24072(.I (n_44), .ZN (n_45));
208     INV_X1 g24097(.I (n_781), .ZN (n_62));
209     CLKBUF_X1 g24068(.I (n_1037), .Z (n_141));
210     INV_X1 g24102(.I (n_609), .ZN (n_61));
211     INV_X1 g24099(.I (n_609), .ZN (n_41));
212     INV_X1 g24116(.I (n_1040), .ZN (n_104));
213     NAND4_X1 g24073(.A1 (raw_buffer[5]), .A2 (raw_buffer[3]), .A3
214           (raw_buffer[6]), .A4 (raw_buffer[4]), .ZN (n_44));
215     NAND2_X1 g24074(.A1 (n_9), .A2 (i2c_rxak_i), .ZN (n_80));
216     NAND2_X1 g24075(.A1 (led_o[4]), .A2 (n_968), .ZN (n_116));
217     NAND2_X1 g24077(.A1 (n_968), .A2 (n_46), .ZN (n_37));
218     NAND2_X1 g24078(.A1 (n_332), .A2 (n_46), .ZN (n_36));
219     NAND2_X1 g24106(.A1 (i2c_slave_addr_o[7]), .A2 (n_968), .ZN (n_28));
220     INV_X1 g24088(.I (n_24), .ZN (n_25));
221     NOR2_X1 g24086(.A1 (i2c_rxak_i), .A2 (i2c_arb_lost_i), .ZN (n_85));
222     NOR2_X1 g24087(.A1 (raw_buffer[1]), .A2 (raw_buffer[0]), .ZN (n_19));
223     INV_X2 g24136(.I (n_16), .ZN (n_53));
224     NAND2_X1 g24089(.A1 (raw_buffer[1]), .A2 (raw_buffer[2]), .ZN (n_24));
225     NAND2_X1 g24083(.A1 (raw_buffer[1]), .A2 (raw_buffer[0]), .ZN (n_51));
226     INV_X1 g24145(.I (i2c_data_out_i[5]), .ZN (n_15));
227     INV_X1 g24123(.I (raw_buffer[6]), .ZN (n_14));
228     INV_X1 g24144(.I (i2c_busy_i), .ZN (n_46));
229     INV_X1 g24141(.I (raw_buffer[0]), .ZN (n_49));
230     INV_X1 g24140(.I (raw_buffer[4]), .ZN (n_13));
231     INV_X1 g24127(.I (raw_buffer[7]), .ZN (n_100));
232     INV_X1 g24126(.I (i2c_write_o), .ZN (n_33));
233     INV_X1 g24148(.I (i2c_data_out_i[6]), .ZN (n_12));
234     INV_X1 g24121(.I (led_o[0]), .ZN (n_11));
235     INV_X1 g24129(.I (raw_buffer[5]), .ZN (n_10));
236     INV_X1 g24150(.I (i2c_arb_lost_i), .ZN (n_9));
237     INV_X1 g24151(.I (i2c_data_out_i[4]), .ZN (n_8));
238     INV_X1 g24147(.I (i2c_data_out_i[0]), .ZN (n_7));
239     INV_X1 g24119(.I (raw_buffer[1]), .ZN (n_50));
240     INV_X1 g24142(.I (i2c_data_out_i[3]), .ZN (n_6));
241     INV_X1 g24138(.I (led_o[8]), .ZN (n_5));
242     CLKBUF_X2 g24137(.I (state[1]), .Z (n_16));
243     INV_X1 g24149(.I (i2c_data_out_i[7]), .ZN (n_4));
244     INV_X1 g24152(.I (i2c_data_out_i[1]), .ZN (n_3));
245     INV_X1 g24118(.I (raw_buffer[2]), .ZN (n_58));
246     INV_X1 g24122(.I (raw_buffer[3]), .ZN (n_2));
247     INV_X1 g24146(.I (i2c_data_out_i[2]), .ZN (n_1));
248     INV_X1 fopt(.I (n_567), .ZN (n_246));
249     NAND3_X1 g24192(.A1 (n_699), .A2 (n_903), .A3 (i2c_read_o), .ZN
250           (n_262));
251     CLKBUF_X2 g24218(.I (error_led_o), .Z (n_286));
252     NOR2_X1 g24247(.A1 (n_327), .A2 (n_80), .ZN (n_317));
253     BUF_X2 g24251(.I (state[3]), .Z (n_320));
254     CLKBUF_X4 g24255(.I (n_320), .Z (n_324));
255     NAND2_X1 g24256(.A1 (n_0), .A2 (state[5]), .ZN (n_326));
256     CLKBUF_X2 g24258(.I (state[5]), .Z (n_327));
257     INV_X2 g24262(.I (state[5]), .ZN (n_332));
258     INV_X2 g24310(.I (n_0), .ZN (n_381));
259     NAND2_X1 g24327(.A1 (n_559), .A2 (n_327), .ZN (n_401));
260     OR2_X1 g45(.A1 (state[0]), .A2 (reset_i), .Z (n_527));
261     NOR3_X1 g99(.A1 (n_541), .A2 (n_724), .A3 (n_781), .ZN (n_543));
262     NAND2_X1 g103(.A1 (n_728), .A2 (n_725), .ZN (n_541));
263     NOR2_X1 g55(.A1 (n_908), .A2 (n_550), .ZN (n_551));
264     NAND2_X1 g56(.A1 (n_736), .A2 (n_1041), .ZN (n_550));
265     INV_X1 fopt24466(.I (error_led_o), .ZN (n_555));
266     INV_X2 fopt34(.I (error_led_o), .ZN (n_559));
267     NAND2_X2 g24467(.A1 (n_565), .A2 (n_968), .ZN (n_566));
268     NAND4_X2 g24468(.A1 (n_57), .A2 (n_317), .A3 (n_755), .A4 (n_781),
269           .ZN (n_565));
270     INV_X1 fopt24469(.I (n_562), .ZN (n_563));
271     CLKBUF_X12 fopt62(.I (state[4]), .Z (n_562));
272     INV_X1 fopt61(.I (n_562), .ZN (n_567));
273     NAND4_X1 g24470(.A1 (n_717), .A2 (n_628), .A3 (n_689), .A4 (n_1144),
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274         .ZN (n_573));
275     NOR2_X1 g23(.A1 (n_700), .A2 (n_753), .ZN (n_582));
276     INV_X1 g24477(.I (n_740), .ZN (n_587));
277     NAND2_X1 g24478(.A1 (n_740), .A2 (led_o[2]), .ZN (n_588));
278     NAND2_X1 g24481(.A1 (n_104), .A2 (n_60), .ZN (n_590));
279     NAND2_X1 g24482(.A1 (n_61), .A2 (n_761), .ZN (n_591));
280     INV_X1 g21(.I (i2c_write_done_i), .ZN (n_596));
281     CLKBUF_X1 g24490(.I (n_606), .Z (n_607));
282     NOR2_X1 g24491(.A1 (state[5]), .A2 (reset_i), .ZN (n_606));
283     INV_X1 g24492(.I (n_606), .ZN (n_609));
284     OAI21_X1 g81(.A1 (n_176), .A2 (n_175), .B (n_639), .ZN (n_619));
285     NOR2_X1 g528(.A1 (n_1028), .A2 (n_632), .ZN (n_628));
286     NAND3_X1 g253(.A1 (n_630), .A2 (n_634), .A3 (n_631), .ZN (n_635));
287     OAI21_X1 g255(.A1 (n_153), .A2 (n_701), .B (n_104), .ZN (n_630));
288     AOI21_X1 g256(.A1 (n_155), .A2 (n_664), .B (n_1032), .ZN (n_631));
289     NOR2_X1 g254(.A1 (n_632), .A2 (n_677), .ZN (n_634));
290     NOR2_X1 g257(.A1 (n_590), .A2 (n_591), .ZN (n_632));
291     NAND2_X1 g26(.A1 (n_655), .A2 (n_638), .ZN (n_639));
292     AND2_X1 g27(.A1 (led_o[6]), .A2 (n_1114), .Z (n_638));
293     AND2_X1 g24504(.A1 (n_559), .A2 (n_765), .Z (n_642));
294     AND2_X1 g24505(.A1 (n_755), .A2 (n_765), .Z (n_645));
295     NAND2_X1 g24514(.A1 (n_738), .A2 (n_899), .ZN (n_655));
296     NOR2_X1 g24516(.A1 (n_286), .A2 (i2c_write_o), .ZN (n_653));
297     AND2_X2 g63_dup(.A1 (n_653), .A2 (n_1038), .Z (n_657));
298     AOI21_X1 g24519(.A1 (n_657), .A2 (n_899), .B (n_116), .ZN (n_659));
299     BUF_X1 fopt24521(.I (n_1039), .Z (n_664));
300     AND2_X2 g24528(.A1 (n_676), .A2 (n_1037), .Z (n_677));
301     NOR2_X1 g24529(.A1 (n_760), .A2 (n_326), .ZN (n_676));
302     NOR2_X1 g28(.A1 (n_758), .A2 (n_85), .ZN (n_680));
303     NOR2_X1 g24535(.A1 (n_688), .A2 (n_149), .ZN (n_689));
304     NOR2_X1 g25(.A1 (n_851), .A2 (n_1042), .ZN (n_688));
305     CLKBUF_X2 fopt24536(.I (n_326), .Z (n_690));
306     NAND2_X1 g48(.A1 (n_716), .A2 (n_702), .ZN (n_703));
307     NAND2_X1 g49(.A1 (n_701), .A2 (n_77), .ZN (n_702));
308     INV_X2 g50(.I (n_700), .ZN (n_701));
309     NAND3_X2 g51(.A1 (n_775), .A2 (n_607), .A3 (n_699), .ZN (n_700));
310     NOR2_X2 g52(.A1 (n_286), .A2 (i2c_write_o), .ZN (n_699));
311     NOR2_X1 g61(.A1 (n_1143), .A2 (n_715), .ZN (n_716));
312     NOR2_X1 g62(.A1 (n_713), .A2 (n_714), .ZN (n_715));
313     NAND3_X1 g64(.A1 (n_680), .A2 (n_1039), .A3 (n_736), .ZN (n_713));
314     NAND2_X1 g65(.A1 (n_699), .A2 (n_53), .ZN (n_714));
315     NOR2_X1 g60(.A1 (n_582), .A2 (n_715), .ZN (n_717));
316     OR2_X2 g63(.A1 (n_714), .A2 (n_158), .Z (n_718));
317     NOR2_X1 g76(.A1 (n_720), .A2 (n_332), .ZN (n_721));
318     INV_X1 g80(.I (n_559), .ZN (n_720));
319     NAND2_X1 g79(.A1 (n_53), .A2 (n_559), .ZN (n_724));
320     NOR2_X1 g77(.A1 (n_758), .A2 (n_332), .ZN (n_725));
321     NOR2_X2 g10(.A1 (i2c_write_o), .A2 (reset_i), .ZN (n_727));
322     BUF_X4 g24540(.I (state[0]), .Z (i2c_write_o));
323     CLKBUF_X2 g24541(.I (n_727), .Z (n_728));
324     NAND4_X1 g71(.A1 (n_904), .A2 (n_734), .A3 (n_1039), .A4 (n_736), .ZN
325         (n_737));
326     NOR2_X1 g72(.A1 (i2c_write_o), .A2 (n_381), .ZN (n_734));
327     NOR2_X2 g24543(.A1 (n_332), .A2 (reset_i), .ZN (n_736));
328     AOI21_X1 g92(.A1 (n_738), .A2 (n_901), .B (reset_i), .ZN (n_740));
329     AND2_X1 g93(.A1 (n_653), .A2 (n_1038), .Z (n_738));
330     NOR2_X1 g287(.A1 (n_751), .A2 (n_1036), .ZN (n_753));
331     OAI21_X1 g288(.A1 (n_748), .A2 (n_749), .B (n_1034), .ZN (n_751));
332     INV_X1 g292(.I (n_324), .ZN (n_748));
333     NAND2_X1 g291(.A1 (n_567), .A2 (n_46), .ZN (n_749));
334     NOR2_X2 g32(.A1 (n_381), .A2 (i2c_write_o), .ZN (n_755));
335     CLKBUF_X12 fopt24551(.I (state[6]), .Z (n_758));
336     NAND3_X1 g24552(.A1 (n_154), .A2 (n_1144), .A3 (n_770), .ZN (n_757));
337     NAND2_X1 g24554(.A1 (n_555), .A2 (state[6]), .ZN (n_760));
338     NOR2_X1 g24555(.A1 (state[6]), .A2 (error_led_o), .ZN (n_761));
339     INV_X1 fopt24557(.I (n_763), .ZN (n_764));
340     BUF_X1 g24558(.I (state[6]), .Z (n_763));
341     NOR2_X1 g24559(.A1 (state[6]), .A2 (n_37), .ZN (n_765));
342     INV_X2 g24562(.I (n_1038), .ZN (n_767));
343     NAND2_X1 g24563(.A1 (n_767), .A2 (n_701), .ZN (n_770));
344     INV_X2 g24566(.I (state[1]), .ZN (n_0));
345     NOR2_X2 g24567(.A1 (n_381), .A2 (n_764), .ZN (n_775));
346     BUF_X1 g24570(.I (n_381), .Z (i2c_read_o));
347     NOR2_X2 g24571(.A1 (n_327), .A2 (n_777), .ZN (n_778));
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348     INV_X2 g24572(.I (state[3]), .ZN (n_777));
349     NOR2_X2 g24575(.A1 (n_563), .A2 (n_777), .ZN (n_781));
350     OAI21_X1 g24577(.A1 (n_777), .A2 (n_85), .B (n_62), .ZN (n_784));
351     NAND3_X2 g2(.A1 (n_728), .A2 (n_850), .A3 (n_721), .ZN (n_851));
352     NOR2_X1 g3(.A1 (n_758), .A2 (n_16), .ZN (n_850));
353     NOR2_X2 g24700(.A1 (n_690), .A2 (n_898), .ZN (n_899));
354     INV_X1 fopt24701(.I (state[6]), .ZN (n_898));
355     NOR2_X1 g94_dup24702(.A1 (n_690), .A2 (n_900), .ZN (n_901));
356     INV_X1 fopt24703(.I (state[6]), .ZN (n_900));
357     NAND2_X1 g24704(.A1 (n_898), .A2 (n_33), .ZN (n_902));
358     INV_X1 fopt24705(.I (n_898), .ZN (n_903));
359     NOR2_X1 g24706(.A1 (n_900), .A2 (n_559), .ZN (n_904));
360     NOR3_X1 g24707(.A1 (n_900), .A2 (n_567), .A3 (n_75), .ZN (n_905));
361     NAND2_X1 g7(.A1 (n_755), .A2 (n_559), .ZN (n_908));
362     NAND2_X1 g24734(.A1 (n_935), .A2 (n_937), .ZN (n_938));
363     NOR3_X1 g95(.A1 (n_1143), .A2 (n_543), .A3 (n_551), .ZN (n_935));
364     OAI21_X1 g94(.A1 (n_701), .A2 (n_155), .B (n_936), .ZN (n_937));
365     INV_X1 g96(.I (n_62), .ZN (n_936));
366     NAND2_X1 g24757(.A1 (n_970), .A2 (n_184), .ZN (n_971));
367     NAND2_X1 g24758(.A1 (n_1029), .A2 (n_969), .ZN (n_970));
368     AND2_X1 g1(.A1 (i2c_command_byte_o[4]), .A2 (n_968), .Z (n_969));
369     INV_X1 g24760(.I (reset_i), .ZN (n_968));
370     OR4_X1 g24786(.A1 (raw_buffer[4]), .A2 (raw_buffer[3]), .A3
371         (raw_buffer[6]), .A4 (raw_buffer[5]), .Z (n_1009));
372     NAND3_X1 g24787(.A1 (n_655), .A2 (led_o[3]), .A3 (n_1114), .ZN
373         (n_1010));
374     NAND4_X1 g24789(.A1 (n_778), .A2 (n_755), .A3 (n_642), .A4 (n_246),
375         .ZN (n_1012));
376     NAND2_X1 g24794(.A1 (n_187), .A2 (n_1025), .ZN (n_1026));
377     BUF_X1 fopt132(.I (n_1024), .Z (n_1025));
378     NAND2_X2 g126(.A1 (n_1021), .A2 (n_1131), .ZN (n_1024));
379     NOR2_X2 g130(.A1 (n_767), .A2 (n_36), .ZN (n_1021));
380     NAND3_X1 g123(.A1 (n_1025), .A2 (n_184), .A3 (n_28), .ZN (n_1027));
381     NAND2_X1 g122(.A1 (n_1024), .A2 (n_1012), .ZN (n_1028));
382     NAND2_X1 g127(.A1 (n_1021), .A2 (n_114), .ZN (n_1029));
383     NOR2_X1 g124(.A1 (n_1030), .A2 (n_79), .ZN (n_1031));
384     CLKBUF_X2 fopt24795(.I (n_1130), .Z (n_1030));
385     NOR2_X1 g125(.A1 (n_1030), .A2 (n_95), .ZN (n_1032));
386     NAND3_X1 g24796(.A1 (n_1033), .A2 (n_777), .A3
387         (i2c_data_out_valid_i), .ZN (n_1034));
388     BUF_X4 g24797(.I (state[4]), .Z (n_1033));
389     AND3_X1 g24798(.A1 (n_324), .A2 (n_1035), .A3 (n_80), .Z (n_1036));
390     BUF_X1 fopt24799(.I (n_1033), .Z (n_1035));
391     NOR3_X1 g24800(.A1 (n_320), .A2 (n_1033), .A3 (n_527), .ZN (n_1037));
392     NOR2_X2 g24801(.A1 (n_320), .A2 (n_1033), .ZN (n_1038));
393     NOR2_X2 g24802(.A1 (n_1033), .A2 (n_777), .ZN (n_1039));
394     NAND2_X1 g24803(.A1 (n_777), .A2 (n_1033), .ZN (n_1040));
395     NOR2_X1 g57_dup24804(.A1 (n_324), .A2 (n_1035), .ZN (n_1041));
396     OR3_X1 g24805(.A1 (n_596), .A2 (n_1035), .A3 (n_324), .Z (n_1042));
397     OAI21_X1 g24873(.A1 (n_191), .A2 (n_173), .B (n_1150), .ZN (n_1107));
398     OAI21_X1 g24879(.A1 (n_176), .A2 (n_178), .B (n_1151), .ZN (n_1112));
399     NAND2_X2 g24884(.A1 (n_657), .A2 (n_899), .ZN (n_1113));
400     OAI21_X1 g24885(.A1 (n_176), .A2 (n_173), .B (n_1152), .ZN (n_1117));
401     INV_X1 g24888(.I (reset_i), .ZN (n_1114));
402     INV_X1 g19(.I (n_1130), .ZN (n_1131));
403     NAND3_X1 g20(.A1 (n_727), .A2 (n_761), .A3 (n_53), .ZN (n_1130));
404     NOR2_X1 g24909(.A1 (n_1142), .A2 (n_1143), .ZN (n_1144));
405     NOR3_X1 g53(.A1 (n_262), .A2 (n_87), .A3 (n_767), .ZN (n_1142));
406     INV_X1 g54(.I (n_737), .ZN (n_1143));
407     NAND3_X1 g24915(.A1 (n_1113), .A2 (led_o[1]), .A3 (n_1114), .ZN
408         (n_1150));
409     NAND3_X1 g24916(.A1 (n_1113), .A2 (led_o[7]), .A3 (n_1114), .ZN
410         (n_1151));
411     NAND3_X1 g24917(.A1 (n_1113), .A2 (led_o[5]), .A3 (n_1114), .ZN
412         (n_1152));
413 endmodule
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