Digital Bubble Level - Cadence RTL Synthesis

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1 Introduction

2 Outputs of RTL Compiler

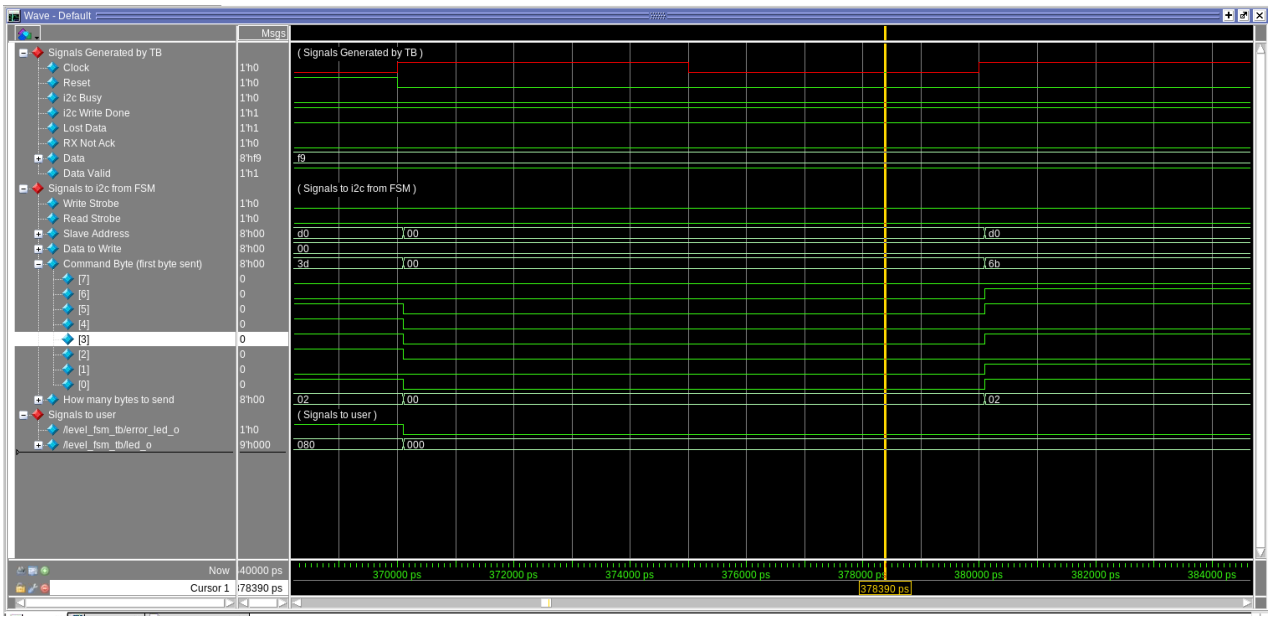

Figure 1:

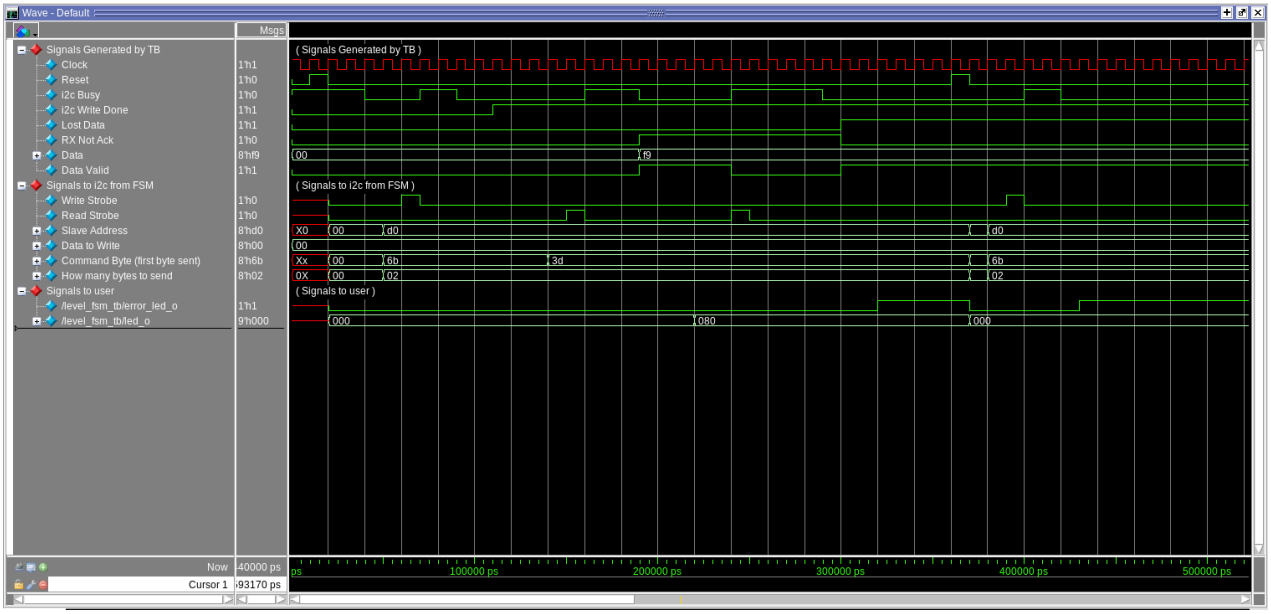

Figure 2:

3 Outputs of RTL Compiler

3.1 Reports

level_fsm_area.rpt

```
=============================================================
  Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
  Generated on:           Oct 10 2021  08:38:55 pm
  Module:                 level_fsm
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   worst_low (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

 Instance   Cells   Cell Area   Net Area   Total Area   Wireload
-------------------------------------------------------------------
level_fsm     170          68          0           68    <none> (D)

 (D) = wireload is default in technology library
```

level_fsm_gates.rpt

```
=============================================================
  Generated by:           Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
  Generated on:           Oct 10 2021  08:38:55 pm
  Module:                 level_fsm
  Technology library:     NanGate_15nm_OCL revision 1.0
  Operating conditions:   worst_low (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
=============================================================

   Gate     Instances   Area        Library
-------------------------------------------------
AOI21_X1            7   2.064   NanGate_15nm_OCL
AOI22_X1           11   3.785   NanGate_15nm_OCL
```

DFFRNQ_X1	8	10.224	NanGate_15nm_OCL
DFFSNQ_X1	19	24.281	NanGate_15nm_OCL
INV_X1	36	5.308	NanGate_15nm_OCL
NAND2_X1	24	4.719	NanGate_15nm_OCL
NAND3_X1	6	1.769	NanGate_15nm_OCL
NAND4_X1	2	0.688	NanGate_15nm_OCL
NOR2_X1	29	5.702	NanGate_15nm_OCL
NOR3_X1	7	2.064	NanGate_15nm_OCL
NOR4_X1	6	2.064	NanGate_15nm_OCL
OAI21_X1	4	1.180	NanGate_15nm_OCL
OAI22_X1	9	3.097	NanGate_15nm_OCL
OR4_X1	2	0.885	NanGate_15nm_OCL
total	170	67.830	

Type	Instances	Area	Area %
sequential	27	34.505	50.9
inverter	36	5.308	7.8
logic	107	28.017	41.3
total	170	67.830	100.0

level_fsm_power.rpt

Generated by:	Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
Generated on:	Oct 10 2021 08:38:55 pm
Module:	level_fsm
Technology library:	NanGate_15nm_OCL revision 1.0
Operating conditions:	worst_low (balanced_tree)
Wireload mode:	enclosed
Area mode:	timing library

Instance	Cells	Leakage Power(nW)	Dynamic Power(nW)	Total Power(nW)
level_fsm	170	51.137	9019.221	9070.358

level_fsm_timing.rpt

Generated by:	Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
Generated on:	Oct 10 2021 08:38:55 pm
Module:	level_fsm
Technology library:	NanGate_15nm_OCL revision 1.0
Operating conditions:	worst_low (balanced_tree)
Wireload mode:	enclosed
Area mode:	timing library

Pin	Type	Fanout	Load (fF)	Slew (ps)	Delay (ps)	Arrival (ps)	
(clock clk)	launch					0	R
state_reg[2]/CLK				0		0	R
state_reg[2]/Q	DFFSNQ_X1	4	2.6	5	+15	15	F
g4006/A2					+0	15	
g4006/ZN	NOR2_X1	2	1.9	6	+6	21	R
g3997/A1					+0	21	
g3997/ZN	NAND2_X1	3	2.4	7	+6	27	F
g3989/A1					+0	27	
g3989/ZN	NOR2_X1	4	4.1	12	+9	36	R
g3983/A1					+0	36	
g3983/ZN	NAND2_X1	3	2.4	8	+7	43	F
g3974/A1					+0	43	
g3974/ZN	NOR2_X1	3	3.0	10	+8	50	R
g3942/A1					+0	50	
g3942/ZN	NAND3_X1	9	8.0	27	+17	67	F
g3941/I					+0	67	
g3941/ZN	INV_X1	8	8.0	18	+16	83	R

```
g3912/A1                                                    +0      83
g3912/ZN                 AOI22_X1      1   0.8     8      +6      89 F
g3890/A1                                                    +0      89
g3890/ZN                 NOR2_X1       1   0.6     4      +4      93 R
raw_buffer_reg[0]/D      DFFRNQ_X1                          +0      93
raw_buffer_reg[0]/CLK    setup                      0       +9     101 R
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
(clock clk)              capture                                 10000 R
-------------------------------------------------------------------------

Cost Group   : 'clk' (path_group 'clk')
Timing slack :    9899ps
Start-point  : state_reg[2]/CLK
End-point    : raw_buffer_reg[0]/D
```

3.2 Mapped Verilog

level_fsm_map.v

```
1
2  // Generated by Cadence Encounter(R) RTL Compiler RC14.13 - v14.10-s027_1
3
4  // Verification Directory fv/level_fsm
5
6  module level_fsm(clk_i, reset_i, i2c_busy_i, i2c_rxak_i,
7       i2c_arb_lost_i, i2c_write_done_i, i2c_data_out_valid_i,
8       i2c_data_out_i, i2c_write_o, i2c_read_o, i2c_slave_addr_o,
9       i2c_din_o, i2c_command_byte_o, i2c_num_bytes_o, error_led_o,
10      led_o);
11   input clk_i, reset_i, i2c_busy_i, i2c_rxak_i, i2c_arb_lost_i,
12        i2c_write_done_i, i2c_data_out_valid_i;
13   input [7:0] i2c_data_out_i;
14   output i2c_write_o, i2c_read_o, error_led_o;
15   output [7:0] i2c_slave_addr_o, i2c_din_o, i2c_command_byte_o,
16        i2c_num_bytes_o;
17   output [8:0] led_o;
18   wire clk_i, reset_i, i2c_busy_i, i2c_rxak_i, i2c_arb_lost_i,
19        i2c_write_done_i, i2c_data_out_valid_i;
20   wire [7:0] i2c_data_out_i;
21   wire i2c_write_o, i2c_read_o, error_led_o;
22   wire [7:0] i2c_slave_addr_o, i2c_din_o, i2c_command_byte_o,
23        i2c_num_bytes_o;
24   wire [8:0] led_o;
25   wire [6:0] state;
26   wire [7:0] raw_buffer;
27   wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
28   wire n_8, n_9, n_10, n_11, n_12, n_13, n_14, n_15;
29   wire n_16, n_17, n_18, n_19, n_20, n_21, n_22, n_23;
30   wire n_24, n_25, n_26, n_27, n_28, n_29, n_30, n_31;
31   wire n_32, n_33, n_34, n_35, n_36, n_37, n_38, n_39;
32   wire n_40, n_41, n_42, n_43, n_44, n_45, n_46, n_47;
33   wire n_48, n_49, n_50, n_51, n_52, n_53, n_54, n_55;
34   wire n_56, n_57, n_58, n_59, n_60, n_61, n_62, n_63;
35   wire n_64, n_65, n_66, n_67, n_68, n_69, n_70, n_71;
36   wire n_72, n_73, n_74, n_75, n_76, n_77, n_78, n_79;
37   wire n_80, n_81, n_82, n_83, n_84, n_85, n_86, n_87;
38   wire n_88, n_89, n_90, n_91, n_92, n_93, n_94, n_95;
39   wire n_96, n_97, n_98, n_99, n_100, n_101, n_102, n_103;
40   wire n_104, n_105, n_106, n_107, n_108, n_109, n_110, n_111;
41   wire n_112, n_113, n_114, n_115, n_116, n_117, n_118, n_119;
42   wire n_120, n_121, n_122, n_123, n_124, n_125, n_126, n_127;
43   wire n_128, n_129, n_130, n_131, n_132, n_133, n_134, n_135;
44   wire n_136, n_137, n_138, n_139, n_140, n_142, n_143;
45   assign i2c_num_bytes_o[0] = 1'b0;
46   assign i2c_num_bytes_o[1] = i2c_slave_addr_o[7];
47   assign i2c_num_bytes_o[2] = 1'b0;
48   assign i2c_num_bytes_o[3] = 1'b0;
49   assign i2c_num_bytes_o[4] = 1'b0;
50   assign i2c_num_bytes_o[5] = 1'b0;
51   assign i2c_num_bytes_o[6] = 1'b0;
52   assign i2c_num_bytes_o[7] = 1'b0;
53   assign i2c_command_byte_o[0] = i2c_slave_addr_o[7];
```

```
54      assign i2c_command_byte_o[1] = i2c_command_byte_o[6];
55      assign i2c_command_byte_o[2] = i2c_command_byte_o[4];
56      assign i2c_command_byte_o[3] = i2c_slave_addr_o[7];
57      assign i2c_command_byte_o[5] = i2c_slave_addr_o[7];
58      assign i2c_command_byte_o[7] = 1'b0;
59      assign i2c_din_o[0] = 1'b0;
60      assign i2c_din_o[1] = 1'b0;
61      assign i2c_din_o[2] = 1'b0;
62      assign i2c_din_o[3] = 1'b0;
63      assign i2c_din_o[4] = 1'b0;
64      assign i2c_din_o[5] = 1'b0;
65      assign i2c_din_o[6] = 1'b0;
66      assign i2c_din_o[7] = 1'b0;
67      assign i2c_slave_addr_o[0] = 1'b0;
68      assign i2c_slave_addr_o[1] = 1'b0;
69      assign i2c_slave_addr_o[2] = 1'b0;
70      assign i2c_slave_addr_o[3] = 1'b0;
71      assign i2c_slave_addr_o[4] = i2c_slave_addr_o[7];
72      assign i2c_slave_addr_o[5] = 1'b0;
73      assign i2c_slave_addr_o[6] = i2c_slave_addr_o[7];
74      DFFSNQ_X1 \state_reg[3] (.SN (1'b1), .CLK (clk_i), .D (n_143), .Q
75          (state[3]));
76      NAND3_X1 g3867(.A1 (n_120), .A2 (n_142), .A3 (n_105), .ZN (n_143));
77      NOR4_X1 g3869(.A1 (n_140), .A2 (n_68), .A3 (n_110), .A4 (n_54), .ZN
78          (n_142));
79      DFFSNQ_X1 \i2c_command_byte_o_reg[1] (.SN (1'b1), .CLK (clk_i), .D
80          (n_139), .Q (i2c_command_byte_o[6]));
81      NAND2_X1 g3898(.A1 (n_138), .A2 (n_57), .ZN (n_140));
82      DFFSNQ_X1 \state_reg[4] (.SN (1'b1), .CLK (clk_i), .D (n_135), .Q
83          (state[4]));
84      DFFSNQ_X1 \led_o_reg[5] (.SN (1'b1), .CLK (clk_i), .D (n_131), .Q
85          (led_o[5]));
86      DFFSNQ_X1 \i2c_slave_addr_o_reg[4] (.SN (1'b1), .CLK (clk_i), .D
87          (n_134), .Q (i2c_slave_addr_o[7]));
88      DFFSNQ_X1 \led_o_reg[7] (.SN (1'b1), .CLK (clk_i), .D (n_133), .Q
89          (led_o[7]));
90      DFFSNQ_X1 \led_o_reg[4] (.SN (1'b1), .CLK (clk_i), .D (n_136), .Q
91          (led_o[4]));
92      DFFSNQ_X1 \led_o_reg[1] (.SN (1'b1), .CLK (clk_i), .D (n_137), .Q
93          (led_o[1]));
94      DFFSNQ_X1 \led_o_reg[3] (.SN (1'b1), .CLK (clk_i), .D (n_128), .Q
95          (led_o[3]));
96      DFFRNQ_X1 \raw_buffer_reg[7] (.RN (1'b1), .CLK (clk_i), .D (n_126),
97          .Q (raw_buffer[7]));
98      DFFRNQ_X1 \raw_buffer_reg[1] (.RN (1'b1), .CLK (clk_i), .D (n_118),
99          .Q (raw_buffer[1]));
100     DFFRNQ_X1 \raw_buffer_reg[2] (.RN (1'b1), .CLK (clk_i), .D (n_117),
101         .Q (raw_buffer[2]));
102     DFFRNQ_X1 \raw_buffer_reg[3] (.RN (1'b1), .CLK (clk_i), .D (n_116),
103         .Q (raw_buffer[3]));
104     DFFRNQ_X1 \raw_buffer_reg[4] (.RN (1'b1), .CLK (clk_i), .D (n_114),
105         .Q (raw_buffer[4]));
106     DFFRNQ_X1 \raw_buffer_reg[5] (.RN (1'b1), .CLK (clk_i), .D (n_115),
107         .Q (raw_buffer[5]));
108     DFFRNQ_X1 \raw_buffer_reg[6] (.RN (1'b1), .CLK (clk_i), .D (n_113),
109         .Q (raw_buffer[6]));
110     DFFRNQ_X1 \raw_buffer_reg[0] (.RN (1'b1), .CLK (clk_i), .D (n_119),
111         .Q (raw_buffer[0]));
112     DFFSNQ_X1 \state_reg[6] (.SN (1'b1), .CLK (clk_i), .D (n_121), .Q
113         (state[6]));
114     DFFSNQ_X1 \led_o_reg[6] (.SN (1'b1), .CLK (clk_i), .D (n_125), .Q
115         (led_o[6]));
116     OAI22_X1 g3904(.A1 (n_107), .A2 (reset_i), .B1 (n_4), .B2 (n_71), .ZN
117         (n_139));
118     DFFSNQ_X1 \led_o_reg[2] (.SN (1'b1), .CLK (clk_i), .D (n_124), .Q
119         (led_o[2]));
120     AOI22_X1 g3921(.A1 (n_99), .A2 (n_83), .B1 (state[4]), .B2 (n_109),
121         .ZN (n_138));
122     OAI22_X1 g3922(.A1 (n_127), .A2 (n_129), .B1 (n_0), .B2 (n_132), .ZN
123         (n_137));
124     OAI21_X1 g3899(.A1 (n_22), .A2 (n_122), .B (n_112), .ZN (n_136));
125     NAND2_X1 g3883(.A1 (n_111), .A2 (n_76), .ZN (n_135));
126     AOI21_X1 g3901(.A1 (n_3), .A2 (n_102), .B (reset_i), .ZN (n_134));
127     OAI22_X1 g3902(.A1 (n_130), .A2 (raw_buffer[2]), .B1 (n_1), .B2
```

```
128         (n_132), .ZN (n_133));
129     OAI22_X1 g3903(.A1 (n_130), .A2 (n_129), .B1 (n_12), .B2 (n_132), .ZN
130         (n_131));
131     DFFSNQ_X1 \state_reg[2] (.SN (1'b1), .CLK (clk_i), .D (n_106), .Q
132         (error_led_o));
133     DFFSNQ_X1 \i2c_command_byte_o_reg[2] (.SN (1'b1), .CLK (clk_i), .D
134         (n_108), .Q (i2c_command_byte_o[4]));
135     OAI22_X1 g3920(.A1 (n_127), .A2 (raw_buffer[2]), .B1 (n_13), .B2
136         (n_132), .ZN (n_128));
137     NOR2_X1 g3897(.A1 (n_88), .A2 (reset_i), .ZN (n_126));
138     OAI22_X1 g3924(.A1 (n_123), .A2 (n_81), .B1 (n_14), .B2 (n_132), .ZN
139         (n_125));
140     OAI22_X1 g3934(.A1 (n_123), .A2 (n_122), .B1 (n_7), .B2 (n_132), .ZN
141         (n_124));
142     NAND2_X1 g3910(.A1 (n_120), .A2 (n_103), .ZN (n_121));
143     NOR2_X1 g3890(.A1 (n_97), .A2 (reset_i), .ZN (n_119));
144     NOR2_X1 g3891(.A1 (n_96), .A2 (reset_i), .ZN (n_118));
145     NOR2_X1 g3892(.A1 (n_93), .A2 (reset_i), .ZN (n_117));
146     NOR2_X1 g3893(.A1 (n_92), .A2 (reset_i), .ZN (n_116));
147     NOR2_X1 g3894(.A1 (n_90), .A2 (reset_i), .ZN (n_115));
148     NOR2_X1 g3895(.A1 (n_91), .A2 (reset_i), .ZN (n_114));
149     NOR2_X1 g3896(.A1 (n_89), .A2 (reset_i), .ZN (n_113));
150     AOI22_X1 g3923(.A1 (n_27), .A2 (n_104), .B1 (led_o[4]), .B2 (n_61),
151         .ZN (n_112));
152     NOR4_X1 g3900(.A1 (n_110), .A2 (n_62), .A3 (n_109), .A4 (n_74), .ZN
153         (n_111));
154     OAI21_X1 g3928(.A1 (n_69), .A2 (reset_i), .B (n_84), .ZN (n_108));
155     AOI21_X1 g3929(.A1 (i2c_command_byte_o[6]), .A2 (n_98), .B (n_101),
156         .ZN (n_107));
157     DFFSNQ_X1 \state_reg[5] (.SN (1'b1), .CLK (clk_i), .D (n_80), .Q
158         (state[5]));
159     DFFSNQ_X1 \led_o_reg[8] (.SN (1'b1), .CLK (clk_i), .D (n_87), .Q
160         (led_o[8]));
161     NAND2_X1 g3909(.A1 (n_79), .A2 (n_105), .ZN (n_106));
162     DFFSNQ_X1 \led_o_reg[0] (.SN (1'b1), .CLK (clk_i), .D (n_77), .Q
163         (led_o[0]));
164     NAND2_X1 g3925(.A1 (n_100), .A2 (n_104), .ZN (n_130));
165     NOR3_X1 g3927(.A1 (n_85), .A2 (n_86), .A3 (n_55), .ZN (n_103));
166     AOI21_X1 g3931(.A1 (n_17), .A2 (n_82), .B (n_101), .ZN (n_102));
167     NAND2_X1 g3936(.A1 (n_100), .A2 (n_78), .ZN (n_127));
168     NAND2_X1 g3940(.A1 (n_98), .A2 (n_64), .ZN (n_99));
169     AOI22_X1 g3912(.A1 (n_95), .A2 (i2c_data_out_i[0]), .B1
170         (raw_buffer[0]), .B2 (n_94), .ZN (n_97));
171     AOI22_X1 g3913(.A1 (n_95), .A2 (i2c_data_out_i[1]), .B1
172         (raw_buffer[1]), .B2 (n_94), .ZN (n_96));
173     AOI22_X1 g3914(.A1 (n_95), .A2 (i2c_data_out_i[2]), .B1
174         (raw_buffer[2]), .B2 (n_94), .ZN (n_93));
175     AOI22_X1 g3915(.A1 (n_95), .A2 (i2c_data_out_i[3]), .B1
176         (raw_buffer[3]), .B2 (n_94), .ZN (n_92));
177     AOI22_X1 g3916(.A1 (n_95), .A2 (i2c_data_out_i[4]), .B1
178         (raw_buffer[4]), .B2 (n_94), .ZN (n_91));
179     AOI22_X1 g3917(.A1 (n_95), .A2 (i2c_data_out_i[5]), .B1
180         (raw_buffer[5]), .B2 (n_94), .ZN (n_90));
181     AOI22_X1 g3918(.A1 (n_95), .A2 (i2c_data_out_i[6]), .B1
182         (raw_buffer[6]), .B2 (n_94), .ZN (n_89));
183     AOI22_X1 g3919(.A1 (n_95), .A2 (i2c_data_out_i[7]), .B1
184         (raw_buffer[7]), .B2 (n_94), .ZN (n_88));
185     AOI21_X1 g3926(.A1 (state[6]), .A2 (n_56), .B (n_66), .ZN (n_120));
186     OAI22_X1 g3930(.A1 (n_33), .A2 (n_75), .B1 (n_2), .B2 (n_132), .ZN
187         (n_87));
188     DFFSNQ_X1 \state_reg[1] (.SN (1'b1), .CLK (clk_i), .D (n_86), .Q
189         (i2c_read_o));
190     AOI21_X1 g3933(.A1 (n_50), .A2 (n_85), .B (n_73), .ZN (n_105));
191     NAND2_X1 g3937(.A1 (n_83), .A2 (n_82), .ZN (n_84));
192     INV_X1 g3938(.I (n_104), .ZN (n_81));
193     NAND4_X1 g3911(.A1 (n_79), .A2 (n_51), .A3 (n_59), .A4 (n_49), .ZN
194         (n_80));
195     INV_X1 g3958(.I (n_78), .ZN (n_122));
196     OAI22_X1 g3932(.A1 (n_29), .A2 (n_76), .B1 (n_6), .B2 (n_132), .ZN
197         (n_77));
198     NOR2_X1 g3939(.A1 (n_32), .A2 (n_75), .ZN (n_104));
199     AOI21_X1 g3943(.A1 (n_70), .A2 (n_72), .B (n_42), .ZN (n_74));
200     INV_X1 g3947(.I (n_82), .ZN (n_98));
201     NOR3_X1 g3959(.A1 (n_28), .A2 (raw_buffer[7]), .A3 (n_76), .ZN
```

```
202         (n_78));
203     INV_X1 g3941(.I (n_94), .ZN (n_95));
204     NOR3_X1 g3944(.A1 (n_72), .A2 (n_71), .A3 (n_65), .ZN (n_73));
205     NOR2_X1 g3948(.A1 (n_70), .A2 (i2c_busy_i), .ZN (n_82));
206     NOR2_X1 g3950(.A1 (n_70), .A2 (n_71), .ZN (n_86));
207     NAND2_X1 g3951(.A1 (i2c_command_byte_o[4]), .A2 (n_67), .ZN (n_69));
208     NOR2_X1 g3955(.A1 (n_67), .A2 (reset_i), .ZN (n_68));
209     INV_X1 g3961(.I (n_79), .ZN (n_66));
210     NAND3_X1 g3942(.A1 (n_63), .A2 (state[3]), .A3 (n_65), .ZN (n_94));
211     NAND2_X1 g3946(.A1 (raw_buffer[7]), .A2 (n_60), .ZN (n_75));
212     NAND2_X1 g3949(.A1 (n_63), .A2 (i2c_data_out_valid_i), .ZN (n_64));
213     NAND3_X1 g3962(.A1 (state[6]), .A2 (state[5]), .A3 (n_43), .ZN
214         (n_79));
215     DFFSNQ_X1 \state_reg[0] (.SN (1'b1), .CLK (clk_i), .D (n_47), .Q
216         (i2c_write_o));
217     NOR2_X1 g3952(.A1 (n_45), .A2 (n_52), .ZN (n_62));
218     INV_X1 g3953(.I (n_132), .ZN (n_61));
219     NAND2_X1 g3966(.A1 (n_58), .A2 (state[4]), .ZN (n_70));
220     INV_X1 g3968(.I (n_60), .ZN (n_76));
221     INV_X1 g3970(.I (n_101), .ZN (n_67));
222     OAI21_X1 g3972(.A1 (n_83), .A2 (n_15), .B (n_58), .ZN (n_59));
223     INV_X1 g3973(.I (n_63), .ZN (n_72));
224     NAND3_X1 g3977(.A1 (n_58), .A2 (n_36), .A3 (i2c_write_done_i), .ZN
225         (n_57));
226     NAND2_X1 g3954(.A1 (n_41), .A2 (n_18), .ZN (n_132));
227     NOR4_X1 g3956(.A1 (state[5]), .A2 (i2c_write_o), .A3 (error_led_o),
228         .A4 (n_31), .ZN (n_56));
229     NOR3_X1 g3957(.A1 (n_53), .A2 (n_40), .A3 (reset_i), .ZN (n_55));
230     NOR3_X1 g3960(.A1 (n_53), .A2 (n_52), .A3 (i2c_busy_i), .ZN (n_54));
231     NOR3_X1 g3964(.A1 (n_44), .A2 (n_71), .A3 (n_16), .ZN (n_85));
232     OR4_X1 g3965(.A1 (n_46), .A2 (n_50), .A3 (n_71), .A4 (n_38), .Z
233         (n_51));
234     NOR2_X1 g3967(.A1 (n_48), .A2 (n_71), .ZN (n_109));
235     NOR2_X1 g3969(.A1 (n_35), .A2 (n_49), .ZN (n_60));
236     NOR2_X1 g3971(.A1 (n_24), .A2 (n_48), .ZN (n_101));
237     NOR2_X1 g3974(.A1 (n_53), .A2 (n_50), .ZN (n_63));
238     NOR3_X1 g3976(.A1 (n_46), .A2 (state[6]), .A3 (n_52), .ZN (n_47));
239     AOI21_X1 g3978(.A1 (n_39), .A2 (i2c_busy_i), .B (n_34), .ZN (n_45));
240     INV_X1 g3984(.I (n_44), .ZN (n_58));
241     NOR4_X1 g3986(.A1 (i2c_read_o), .A2 (n_11), .A3 (i2c_write_o), .A4
242         (n_52), .ZN (n_43));
243     NOR4_X1 g3963(.A1 (n_26), .A2 (n_50), .A3 (state[6]), .A4 (n_42), .ZN
244         (n_110));
245     NAND3_X1 g3979(.A1 (n_37), .A2 (n_40), .A3 (state[6]), .ZN (n_41));
246     NAND2_X1 g3980(.A1 (n_39), .A2 (n_38), .ZN (n_48));
247     NAND2_X1 g3982(.A1 (n_37), .A2 (n_36), .ZN (n_49));
248     NAND2_X1 g3983(.A1 (n_39), .A2 (state[6]), .ZN (n_53));
249     NAND2_X1 g3985(.A1 (n_37), .A2 (n_35), .ZN (n_44));
250     INV_X1 g3988(.I (n_39), .ZN (n_46));
251     NOR4_X1 g3994(.A1 (n_30), .A2 (state[6]), .A3 (i2c_rxak_i), .A4
252         (i2c_arb_lost_i), .ZN (n_34));
253     NOR2_X1 g3981(.A1 (n_23), .A2 (n_32), .ZN (n_33));
254     NAND2_X1 g3987(.A1 (i2c_read_o), .A2 (n_36), .ZN (n_31));
255     NOR2_X1 g3989(.A1 (n_30), .A2 (state[5]), .ZN (n_39));
256     NOR2_X1 g3990(.A1 (n_30), .A2 (n_25), .ZN (n_37));
257     NAND2_X1 g4000(.A1 (n_50), .A2 (n_19), .ZN (n_52));
258     OAI21_X1 g3975(.A1 (n_28), .A2 (n_27), .B (n_10), .ZN (n_29));
259     NAND3_X1 g3991(.A1 (n_25), .A2 (n_21), .A3 (i2c_write_o), .ZN (n_26));
260     AOI22_X1 g3995(.A1 (n_20), .A2 (raw_buffer[2]), .B1 (n_129), .B2
261         (raw_buffer[1]), .ZN (n_123));
262     NOR2_X1 g3996(.A1 (n_24), .A2 (reset_i), .ZN (n_36));
263     INV_X1 g3998(.I (n_22), .ZN (n_23));
264     NAND2_X1 g3997(.A1 (n_21), .A2 (n_5), .ZN (n_30));
265     NAND2_X1 g3999(.A1 (n_20), .A2 (n_129), .ZN (n_22));
266     INV_X1 g4003(.I (n_24), .ZN (n_40));
267     INV_X1 g4013(.I (n_71), .ZN (n_19));
268     NAND4_X1 g3992(.A1 (raw_buffer[6]), .A2 (raw_buffer[4]), .A3
269         (raw_buffer[5]), .A4 (raw_buffer[3]), .ZN (n_32));
270     OR4_X1 g3993(.A1 (raw_buffer[5]), .A2 (raw_buffer[3]), .A3
271         (raw_buffer[6]), .A4 (raw_buffer[4]), .Z (n_28));
272     NOR2_X1 g4001(.A1 (n_8), .A2 (i2c_arb_lost_i), .ZN (n_65));
273     NOR2_X1 g4005(.A1 (n_9), .A2 (n_129), .ZN (n_27));
274     INV_X1 g4010(.I (n_83), .ZN (n_42));
275     NAND2_X1 g4014(.A1 (state[3]), .A2 (n_18), .ZN (n_71));
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276     NAND2_X1 g4004(.A1 (n_50), .A2 (n_17), .ZN (n_24));
277     NOR2_X1 g4002(.A1 (raw_buffer[1]), .A2 (raw_buffer[0]), .ZN (n_20));
278     NAND2_X1 g4007(.A1 (raw_buffer[1]), .A2 (raw_buffer[0]), .ZN (n_100));
279     NOR2_X1 g4009(.A1 (state[6]), .A2 (i2c_busy_i), .ZN (n_38));
280     NOR2_X1 g4006(.A1 (i2c_read_o), .A2 (error_led_o), .ZN (n_21));
281     NOR2_X1 g4008(.A1 (i2c_rxak_i), .A2 (i2c_arb_lost_i), .ZN (n_16));
282     NOR2_X1 g4011(.A1 (state[3]), .A2 (reset_i), .ZN (n_83));
283     NOR2_X1 g4012(.A1 (state[4]), .A2 (reset_i), .ZN (n_15));
284     INV_X1 g4029(.I (led_o[6]), .ZN (n_14));
285     INV_X1 g4030(.I (led_o[3]), .ZN (n_13));
286     INV_X1 g4027(.I (led_o[5]), .ZN (n_12));
287     INV_X1 g4031(.I (error_led_o), .ZN (n_11));
288     INV_X1 g4026(.I (state[6]), .ZN (n_35));
289     INV_X1 g4016(.I (raw_buffer[7]), .ZN (n_10));
290     INV_X1 g4023(.I (raw_buffer[1]), .ZN (n_9));
291     INV_X1 g4034(.I (i2c_rxak_i), .ZN (n_8));
292     INV_X1 g4032(.I (led_o[2]), .ZN (n_7));
293     INV_X1 g4019(.I (state[5]), .ZN (n_25));
294     INV_X1 g4015(.I (led_o[0]), .ZN (n_6));
295     INV_X1 g4035(.I (reset_i), .ZN (n_18));
296     INV_X1 g4028(.I (raw_buffer[2]), .ZN (n_129));
297     INV_X1 g4017(.I (i2c_write_o), .ZN (n_5));
298     INV_X1 g4024(.I (i2c_command_byte_o[6]), .ZN (n_4));
299     INV_X1 g4021(.I (i2c_slave_addr_o[7]), .ZN (n_3));
300     INV_X1 g4022(.I (state[4]), .ZN (n_50));
301     INV_X1 g4025(.I (state[3]), .ZN (n_17));
302     INV_X1 g4020(.I (led_o[8]), .ZN (n_2));
303     INV_X1 g4033(.I (led_o[7]), .ZN (n_1));
304     INV_X1 g4018(.I (led_o[1]), .ZN (n_0));
305 endmodule
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