

## Title: TEI0185 - System Overview

A4 Number: TEI0185  
P001

Rev. 03

Date: 2024-02-14 Copyright: Trenz Electronic GmbH

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Filename: System Overview.SchDoc

REV	Description	
-01	Initial revision	VT
-02	1. Change <a href="#">J29</a> power connector 2. Added clock signal 25MHz <a href="#">HPS_OSC_CLK1</a> to HPS_IOA_12 3. Added series resistor <a href="#">R394</a> to <a href="#">HPS_OSC_CLK1</a> 4. Changed resistors value <a href="#">R169</a> , <a href="#">R172</a> , <a href="#">R179</a> , <a href="#">R190</a> 33R to 100R 5. <a href="#">DIPSW1</a> connected from HPS_IO12 to HPS_IO2	VT
-03	1. Swapped nets ETH1_RXCK and ETH1_RXD1 2. Changed voltage 1.2V to VIO_CRUVI on the pull-up R371, R374 3. Fixed I2C connection on the I2C Mux (U57): SFPA_SDA<>SFPA_SCL, SFPB_SDA<>SFPB_SCL 4. Added additional resistors R397, R398 (assembly option) for select voltage VCCIO_PIO_SDM	VT

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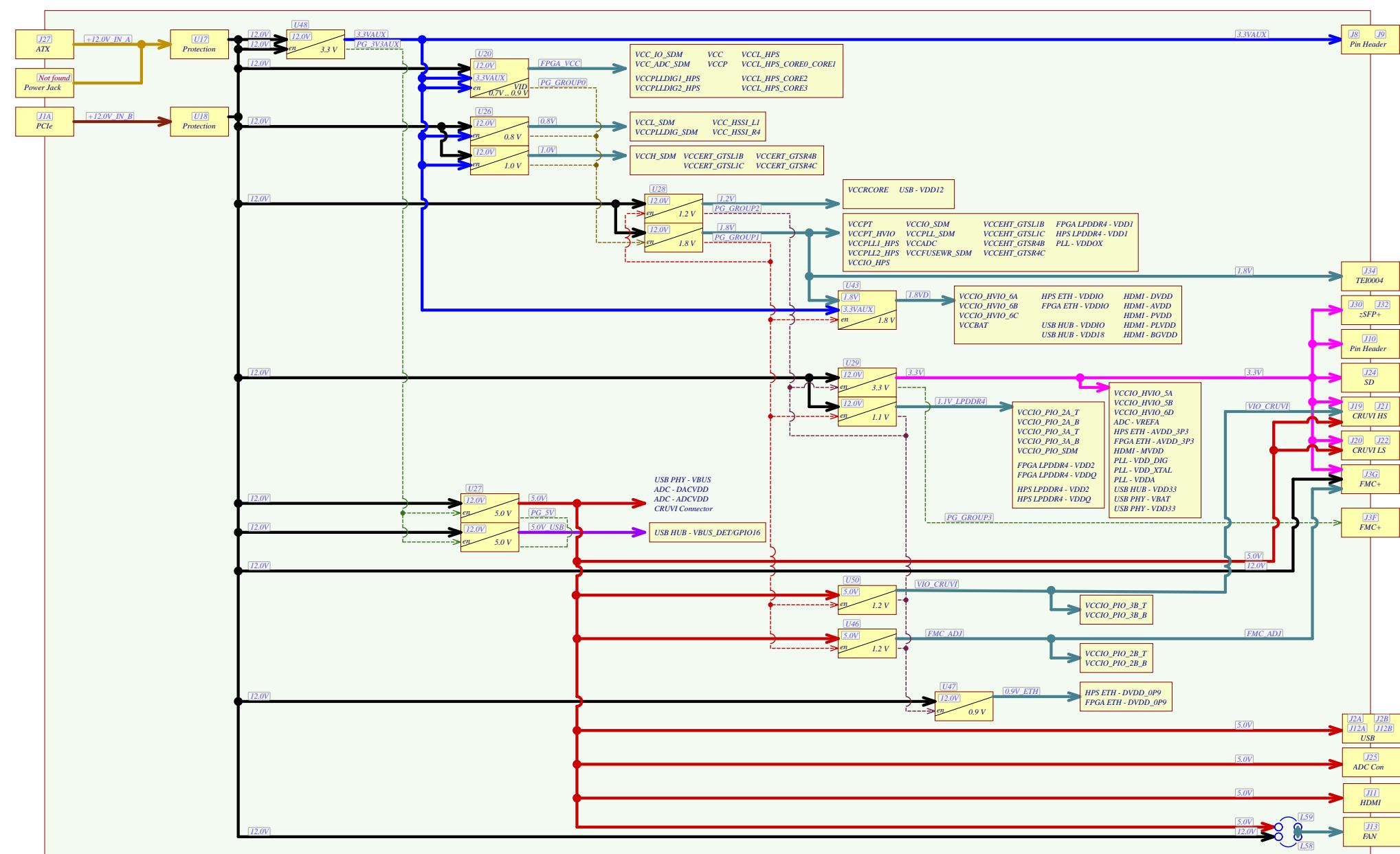
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	Title: TEI0185 - Revision Changes		
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[12.0V]  
Net name  
Power bus  
Control signal  
PL\_DCIN  
0.9V

Series	Device Group	Speed-grade	Power Option	FPGA_VCC
E	A (VID support)	1	V	0.70 V - 0.90 V *
		2	E	
	B	2	V	0.8 V
		3	V	
		4	S	
		5	S	0.78 V
		6	S	0.75 V
		6	X	0.75 V

\*: The typical value is based on SmartVID programmed value.

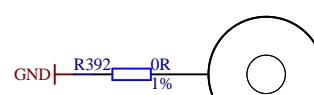
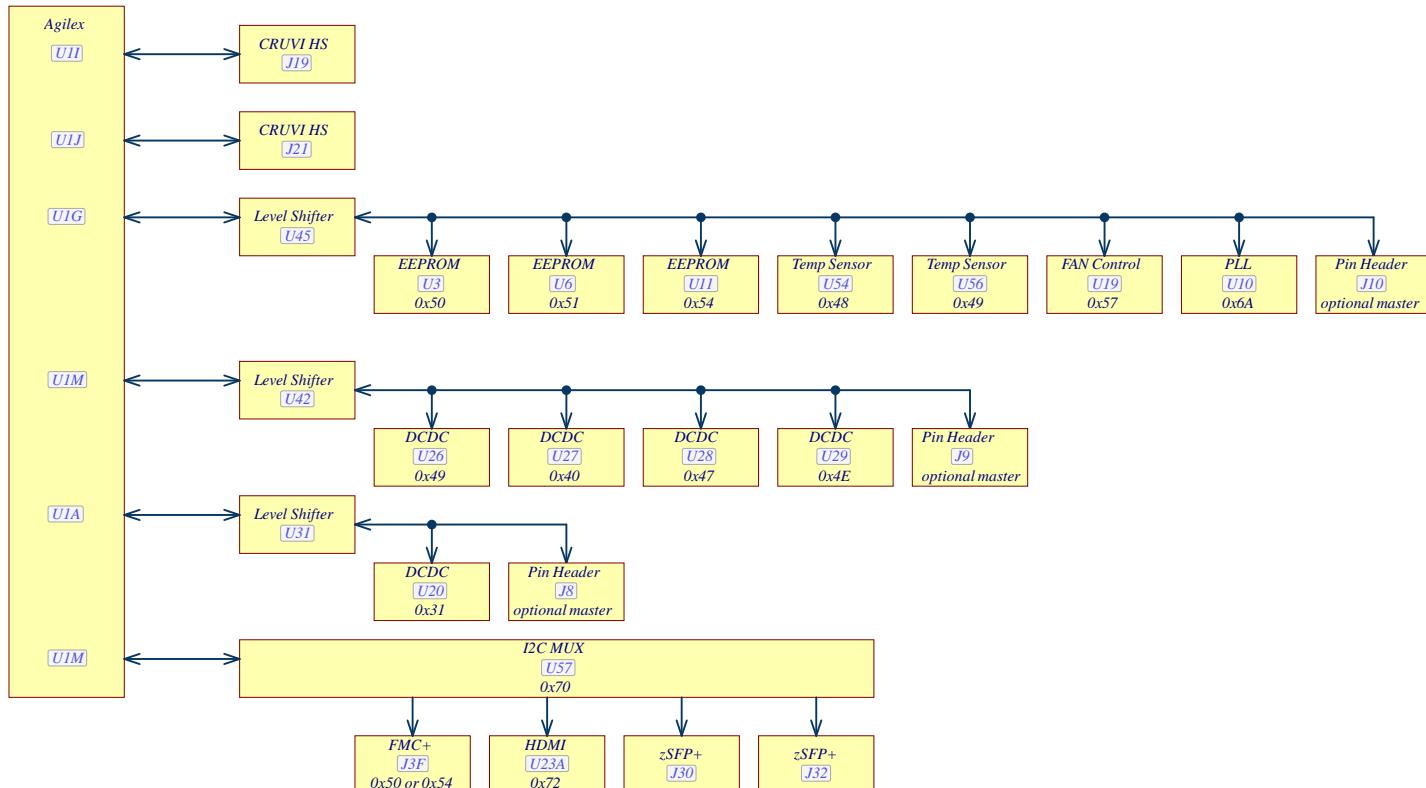
#### Power Option Index:

V - standard power (VID)  
E - low power (VID)  
S - standard power (fixed voltage)  
X - low power (fixed voltage)

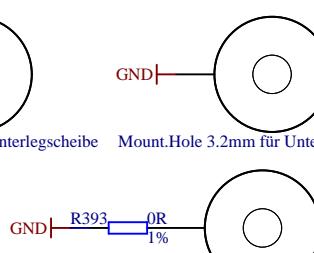
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A3	Nummer: TEI0185 P01	Rev. 03
Datum: 2024-02-14 Copyright:Trenz Electronic GmbH		Page 3 of 51
Filename: Power_Diagram.SchDoc		

1 2 3 4

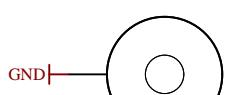
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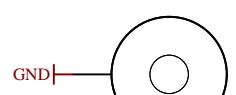
Mount.Hole 3.2mm für Unterlegscheibe



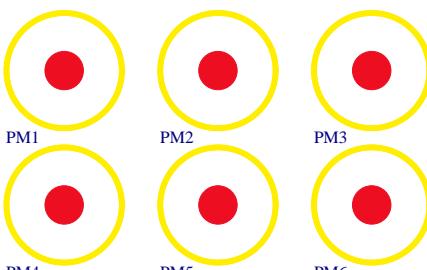
Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



Mount.Hole 3.2mm für Unterlegscheibe



CE Logo on Top Overlay

CE-TOPOVERLAY  
RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY  
WEEE

WEEE Logo on Top Overlay

WEEE-TOPOVERLAY  
Serial1  
Serial

Serialnumber 6,3 x 6,3mm

Design drawn by: VT	Title: TEI0185
Checked by:	
Assembly variant: P001	
Created by: VT	
Modified by: VT	

Modified at: 2023-09-20

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1 2 3 4

A

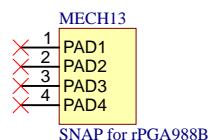
A

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B

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C



SNAP for rPGA988B

D

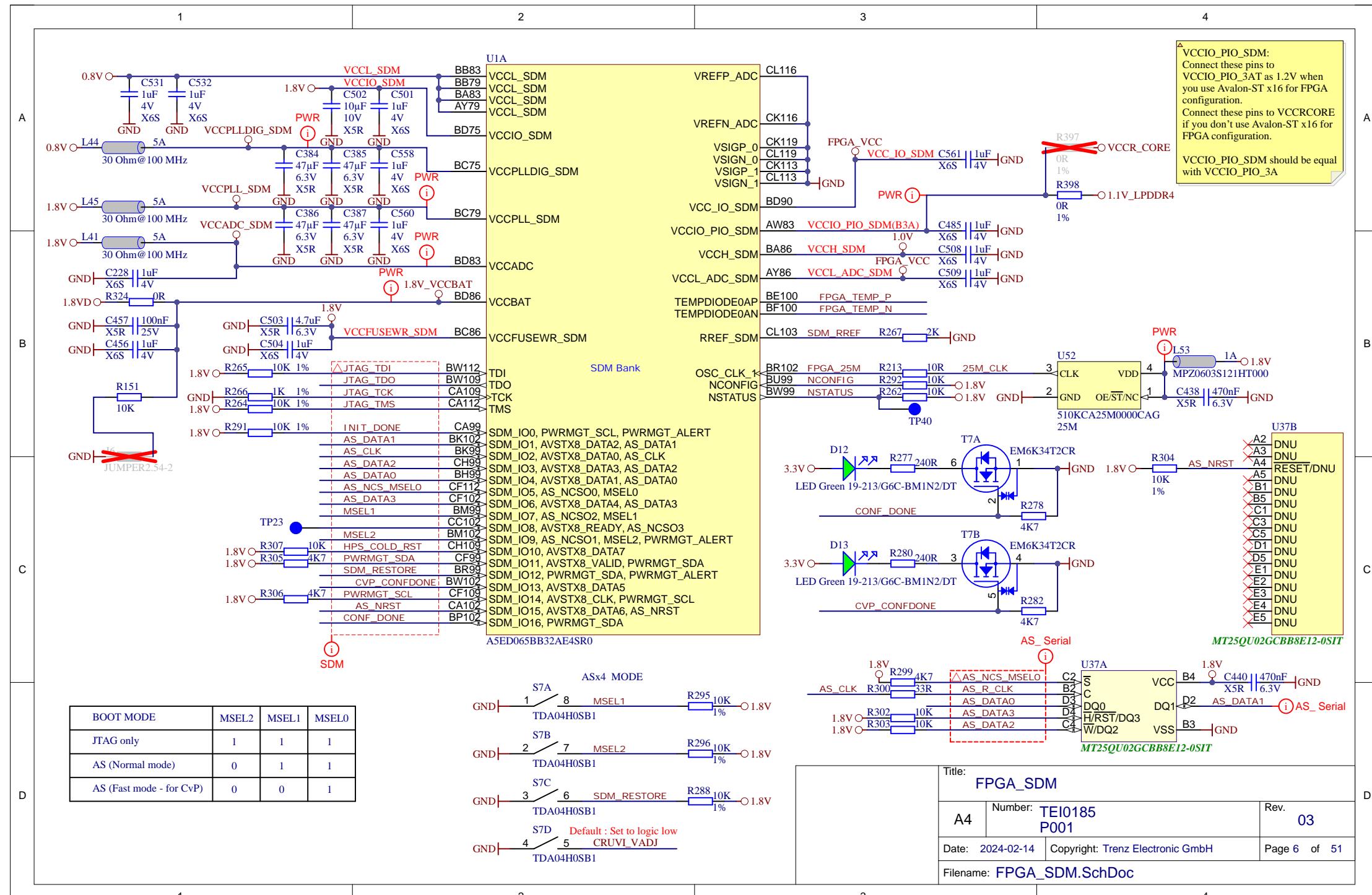
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Title:  
FPGAA4 | Number: TEI0185  
P001Rev.  
03

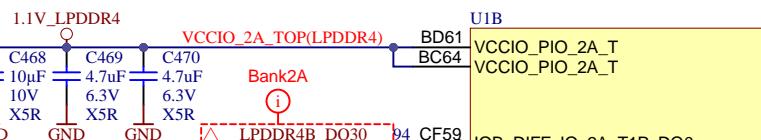
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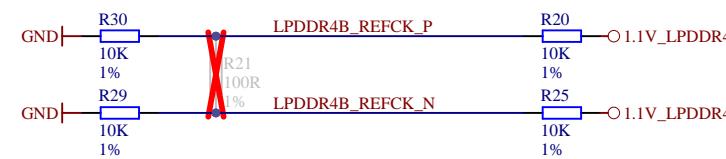
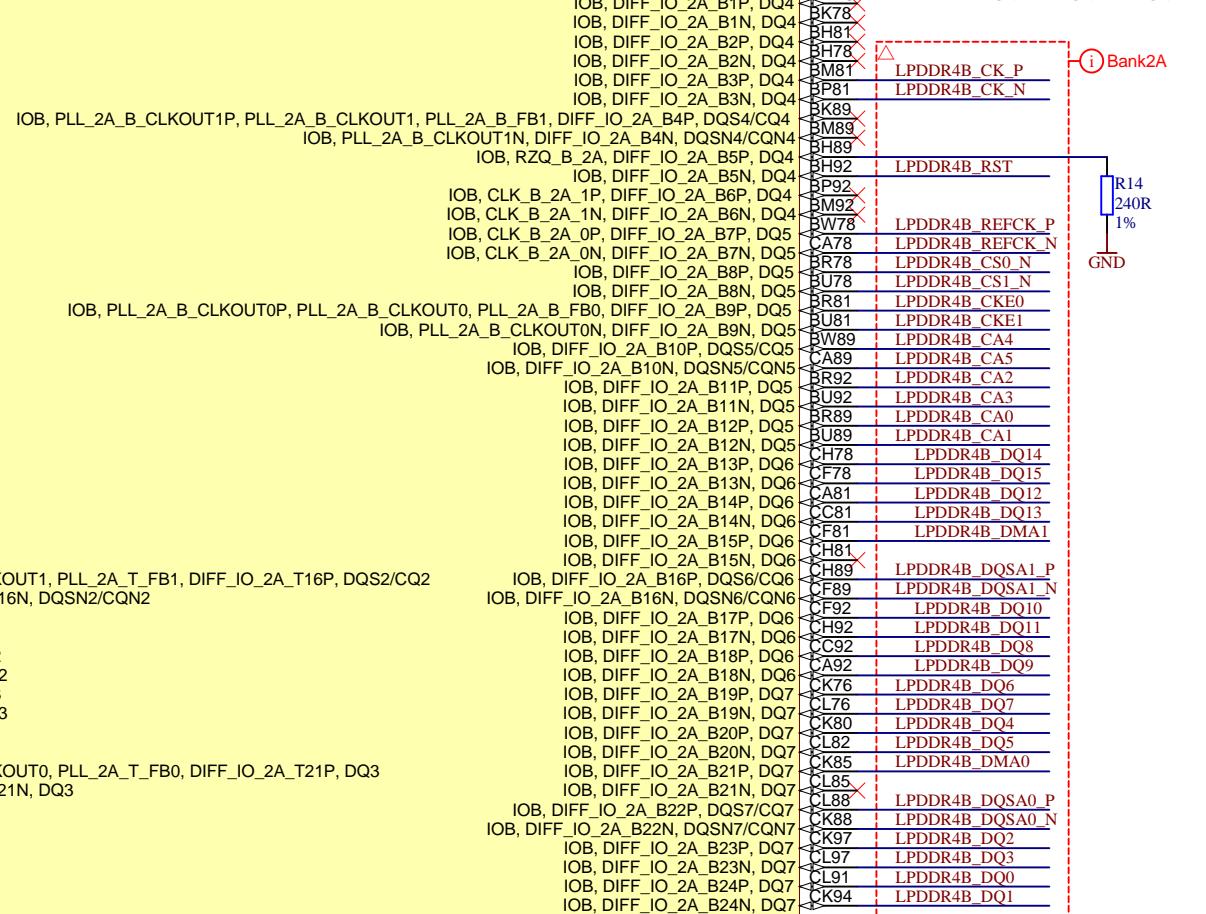


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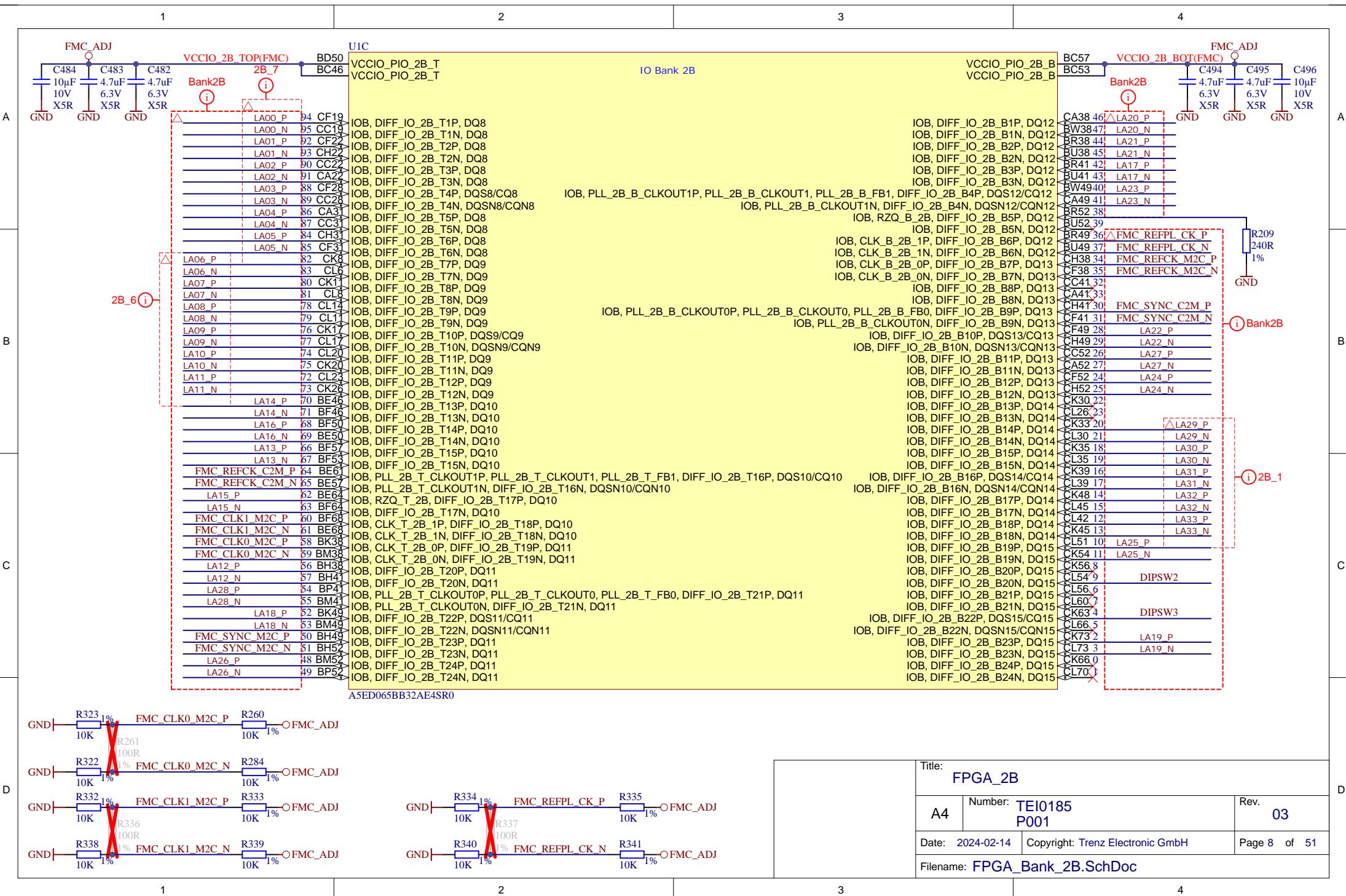
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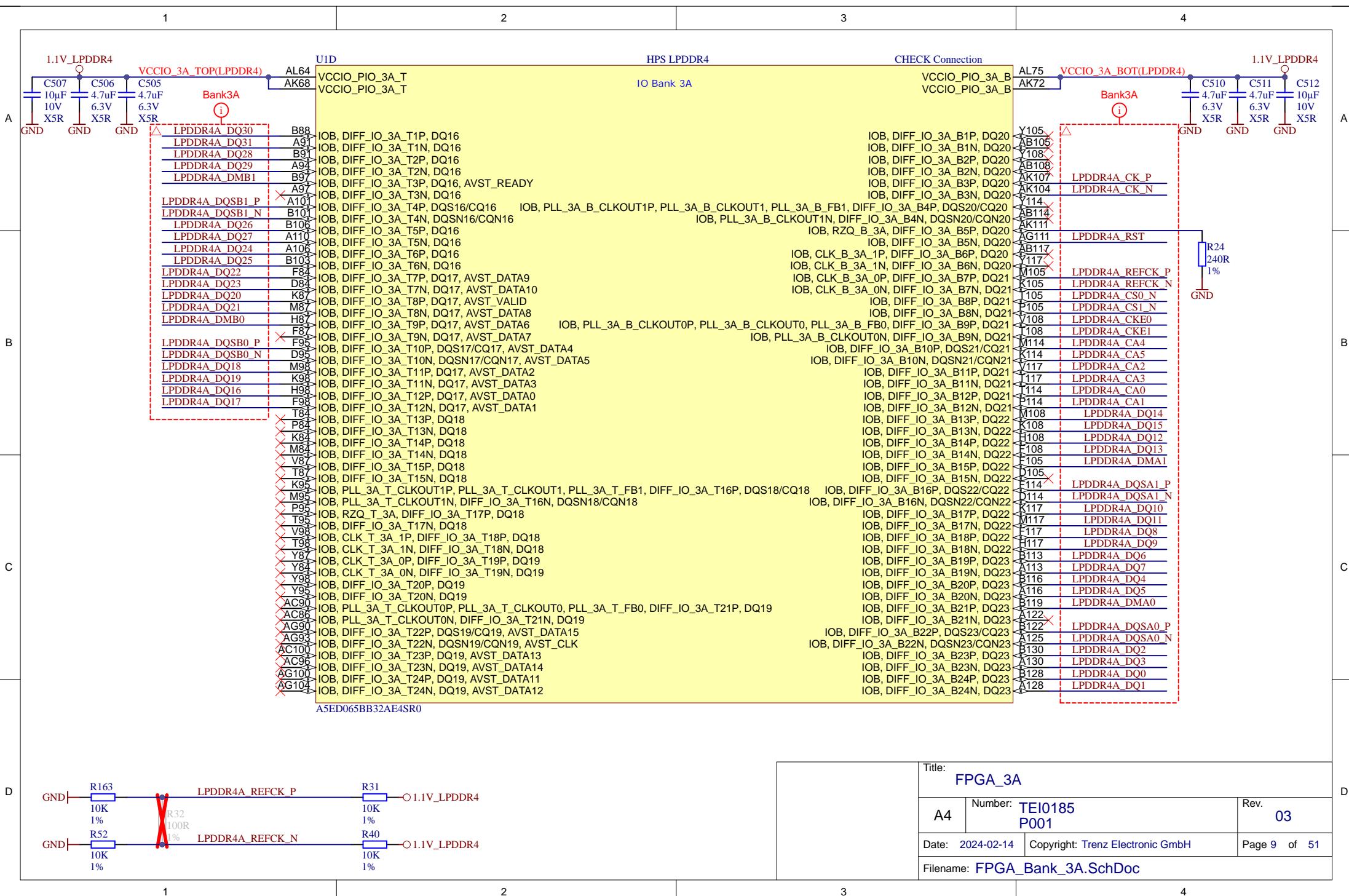
IO Bank 2A

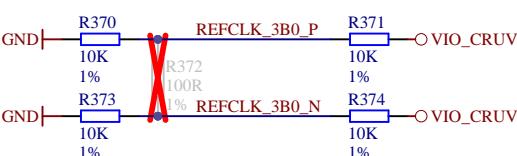
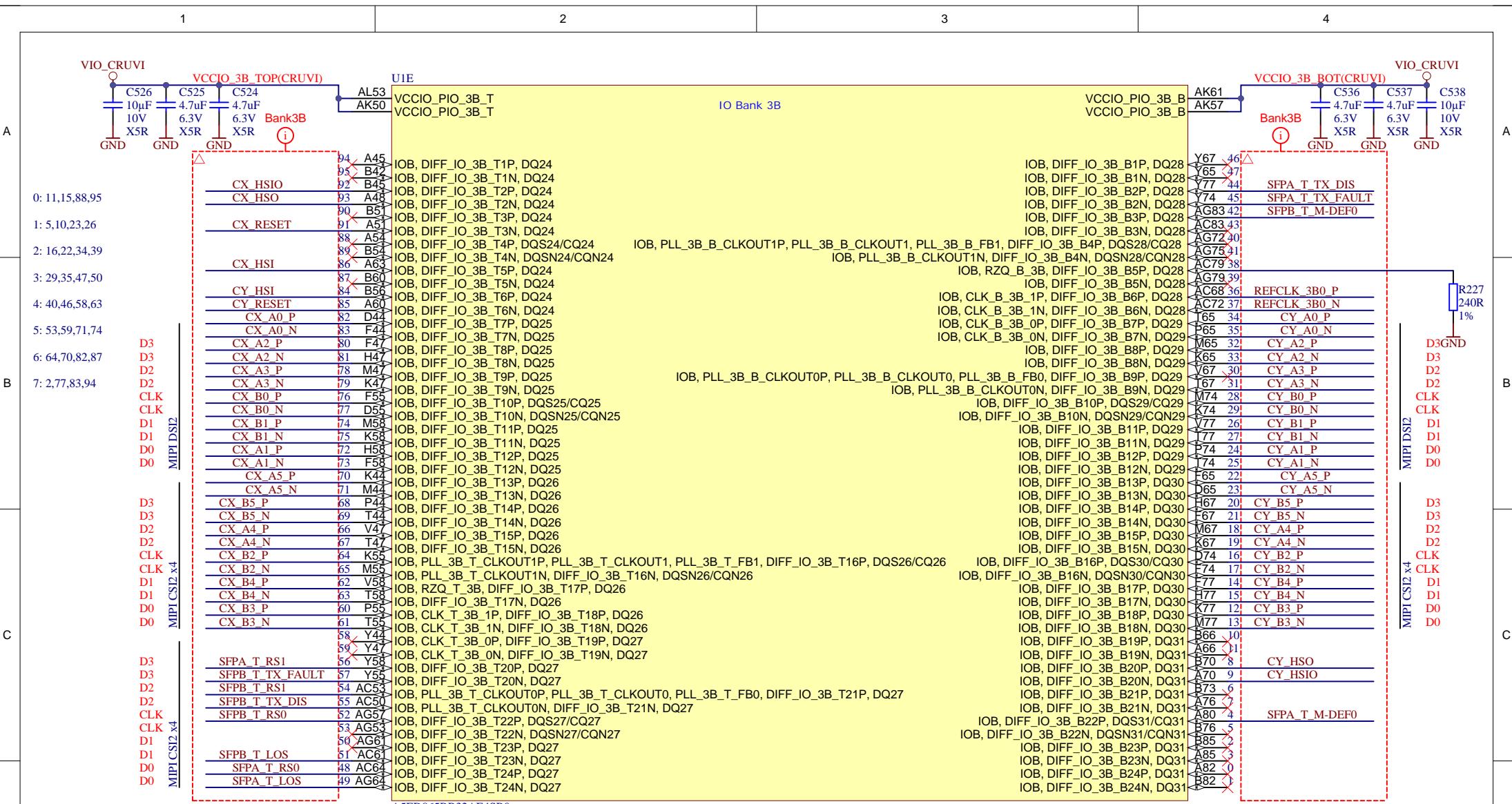


Title: FPGA_2A		
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1 2 3 4







	Title: <b>FPGA_3B</b>		
A4	Number: <b>TEI0185 P001</b>	Rev. <b>03</b>	
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Filename: <b>FPGA_Bank_3B.SchDoc</b>			

1.8VIO

HPS

(i)

U1G

A			
A			
B			
B			
C			
C			
D			
D			

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U1H

SD_RDATA0 R8	OR1%	SD_DATO E135	HPS_IOB_1, GPIO1_IO0, SPIM1_CLK, UART0_CTS_N, EMAC0_PPS0, NAND_ADQ0, SDMMC_DATA0, EMAC1_TX_CLK, TRACE_D10
SD_RDAT1 R360	OR1%	SD_DAT1 F132	HPS_IOB_2, GPIO1_IO1, SPIM1_MOSI, UART0 RTS_N, EMAC0_PPSTRIG0, NAND_ADQ1, SDMMC_DATA1, EMAC1_RX_CTL, TRACE_D9
SD_RCLK R361	OR1%	SD_CLK D13	HPS_IOB_3, GPIO1_IO2, SPIM1_MISO, UART0 TX, I2C_SDA, NAND_WE_N, SDMMC_CLK, EMAC1_RX_CLK, TRACE_D8
		X AG123	HPS_IOB_4, GPIO1_IO3, SPIM1_SS0_N, UART0_RX, I2C_SCL, NAND_NE_N, EMAC1_RX_CTL, TRACE_D7
SD_RDATA2 R362	OR1%	USB_RST B134	HPS_IOB_5, GPIO1_IO4, SPIM1_SS1_N, SPI1_CLK, UART1_CTS_N, EMAC2_PPS2, NAND_WP_N, SDMMC_WRITE_PROTECT, I3C1_SDA, EMAC1_TXD0, TRACE_D6
SD_RDATA3 R363	OR1%	SD_DAT2 AA135	HPS_IOB_6, GPIO1_IO5, SPI1_MOSI, SPI1_RTS_N, EMAC2_PPSTRIG2, NAND_ADQ2, SDMMC_DATA2, I3C1_SCL, EMAC1_TXD1, TRACE_D5
SD_RCMD R364	OR1%	SD_DAT3 V127	HPS_IOB_7, GPIO1_IO6, SPI1_SS0_N, UART1_RX, I2C_SDA, NAND_ADQ3, SDMMC_DATA3, I3C0_SDA, EMAC1_RXD0, TRACE_D4
		X AB13	HPS_IOB_8, GPIO1_IO7, SPI1_MISO, SPI1_SS0_N, UART0_RX, I2C_SCL, NAND_CLE, SDMMC_CMD, I3C0_SCL, EMAC1_RXD1, TRACE_D15
		ETH_MDI0 T12	HPS_IOB_9, GPIO1_IO8, JTAG_TCK, SPI0_CLK, MDIO2_MDI0, I2C_EMAC2_SDA, NAND_ADQ4, SDMMC_DATA4, EMAC1_TXD2, TRACE_D14
		ETH_MDC Y132	HPS_IOB_10, GPIO1_IO9, JTAG_TMS, SPI0_MOSI, MDIO2_MDC, I2C_EMAC2_SCL, NAND_ADQ5, SDMMC_DATA5, EMAC1_RXD3, TRACE_D13
		ETH_RST T12	HPS_IOB_11, GPIO1_IO10, JTAG_TDO, SPI0_SS0_N, MDIO0_MDI0, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, EMAC1_RXD2, TRACE_D12
		SD_DETECT P124	HPS_IOB_12, GPIO1_IO11, JTAG_TDI, SPI0_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, EMAC1_RXD3, TRACE_D11
		ETH_TXCK M12	HPS_IOB_13, GPIO1_IO12, I2C_SDA, NAND_ALE, SDMMC_PU_PD_DATA2, EMAC2_TX_CLK, TRACE_D10
		ETH_RXCTL K12	HPS_IOB_14, GPIO1_IO13, I2C_SCL, NAND_RB_N, SDMMC_PWR_ENA, EMAC2_RX_CTL, TRACE_D9
		ETH_RXCK M124	HPS_IOB_15, GPIO1_IO14, UART1_RX, NAND_CE_N, I3C1_SDA, EMAC2_RX_CLK, TRACE_D8
		ETH_TXDO K124	HPS_IOB_16, GPIO1_IO15, UART1_RX, NAND_DQS, SDMMC_DATA_STROBE, I3C1_SCL, EMAC2_RX_CTL, TRACE_D7
		ETH_RXD1 Y127	HPS_IOB_17, GPIO1_IO16, UART1_CTS_N, NAND_ADQ8, I3C0_SDA, EMAC2_RXD0, TRACE_D6
		ETH_RXD0 H12	HPS_IOB_18, GPIO1_IO17, SPI0_SS1_N, UART1_RTS_N, NAND_ADQ9, I3C0_SCL, EMAC2_RXD1, TRACE_D5
		ETH_RXD1 AB124	HPS_IOB_19, GPIO1_IO18, SPI0_MISO, MDIO1_MDI0, I2C_EMAC1_SDA, NAND_ADQ10, EMAC2_RXD0, TRACE_D4
		ETH_RXD2 F12	HPS_IOB_20, GPIO1_IO19, SPI0_SS0_N, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ11, EMAC2_RXD1, TRACE_CLK
		ETH_RXD3 Y12	HPS_IOB_21, GPIO1_IO20, SPI0_CLK, SPI1_CLK, I2C_EMAC2_SDA, NAND_ADQ12, EMAC2_RXD2, TRACE_D0
		ETH_RXD2 F124	HPS_IOB_22, GPIO1_IO21, SPI0_MOSI, SPI1_MOSI, I2C_EMAC2_SCL, NAND_ADQ13, EMAC2_RXD3, TRACE_D1
		ETH_RXD3 D12	HPS_IOB_23, GPIO1_IO22, SPI0_MISO, SPI1_SS0_N, MDIO0_MDI0, I2C_EMAC0_SDA, NAND_ADQ14, EMAC2_RXD2, TRACE_D2
			HPS_IOB_24, GPIO1_IO23, SPI0_SS0_N, SPI1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ15, EMAC2_RXD3, TRACE_D3

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R394

10R

1%

R212

10R

1%

PWR

25M CK

GND

VDD

4

1

L52

O 1.8V

X5R

1A

C437

6.3V

1

MPZ0603S121HT000

510KCA25M0000CAG

25M

Title: FPGA\_HPS

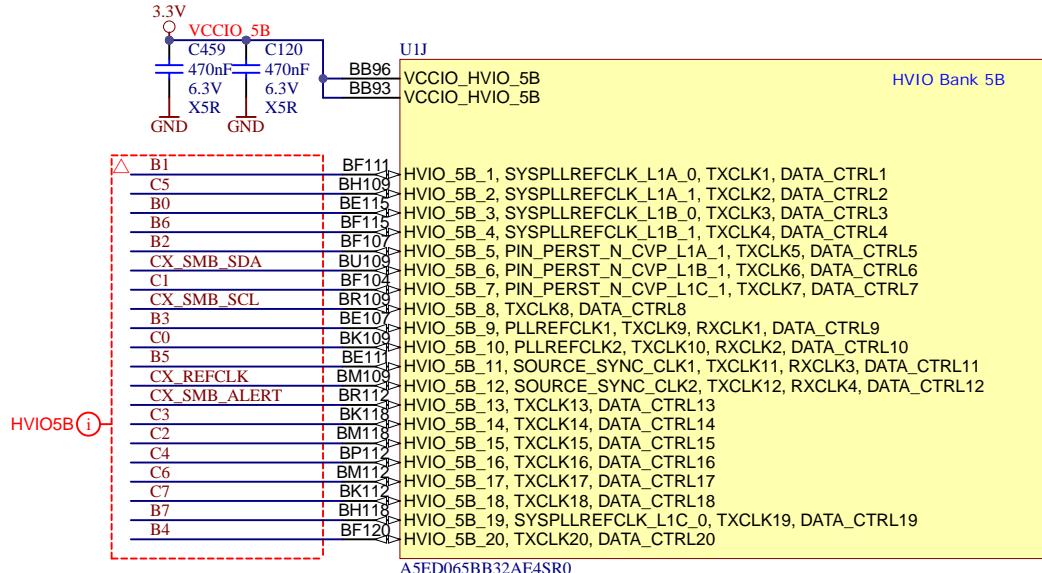
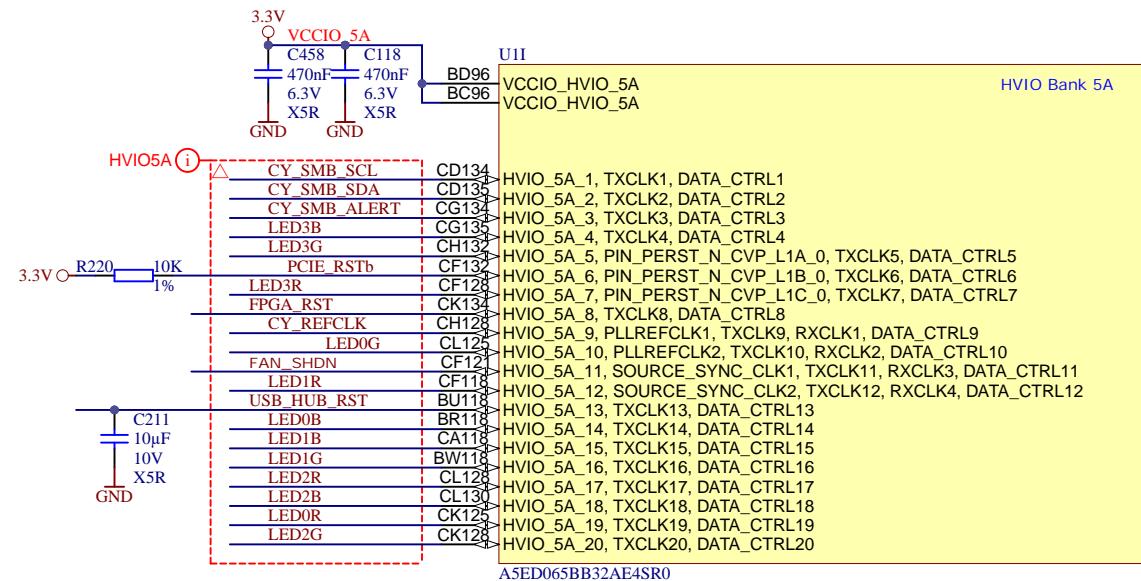
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P001

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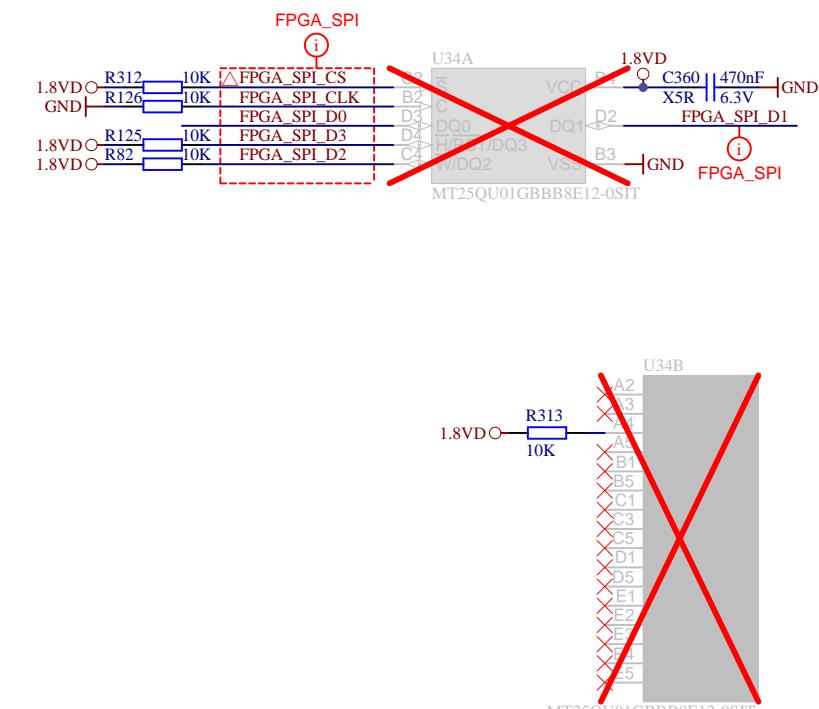
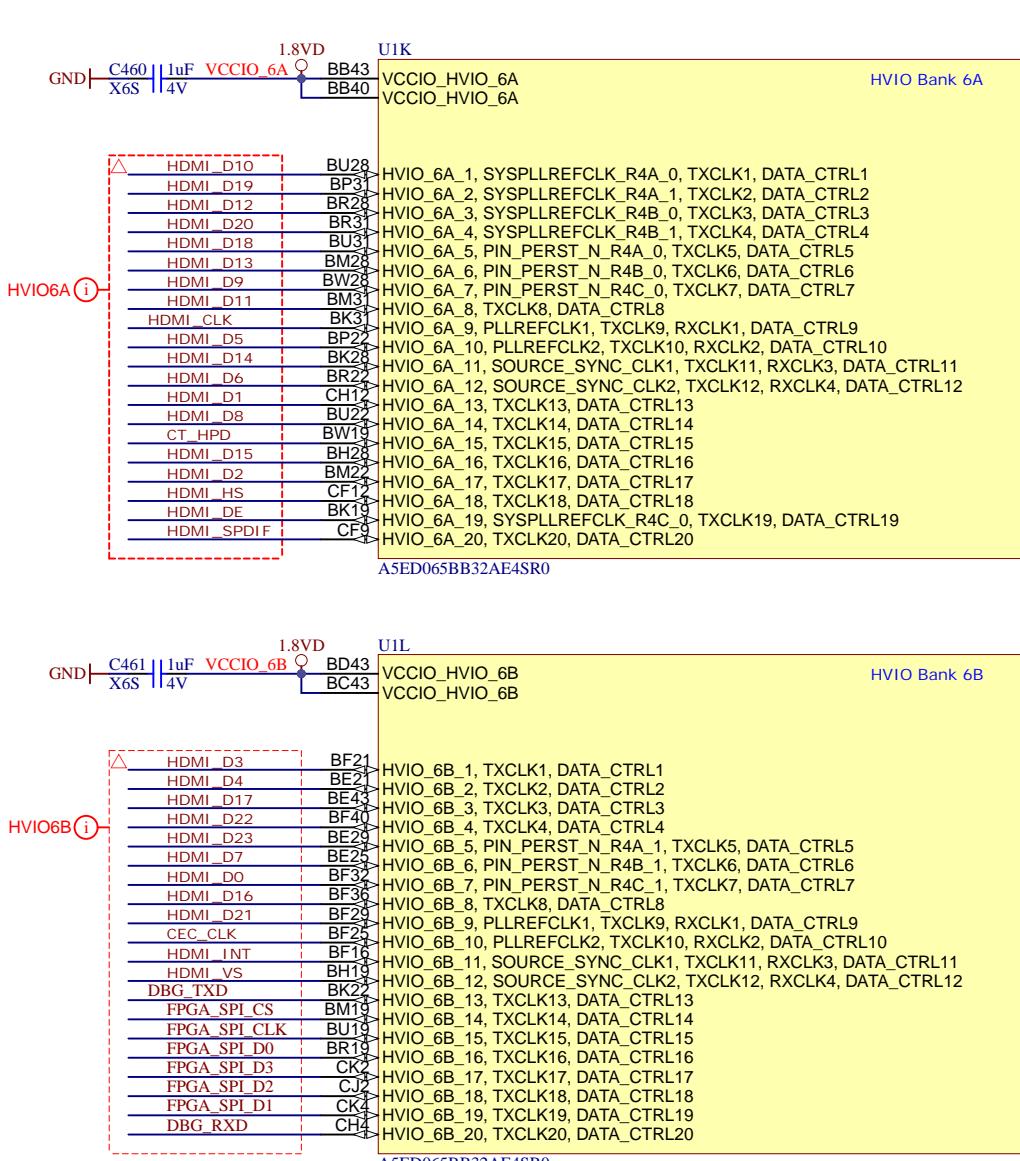
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Filename: FPGA\_Bank\_HPS.SchDoc



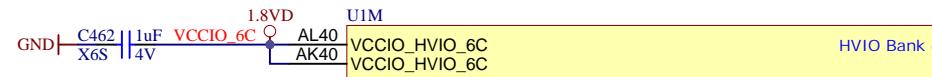
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A4	Number: <b>TEI0185 P001</b>	Rev. <b>03</b>
Date: 2024-02-14	Copyright: Trenz Electronic GmbH	Page <b>12</b> of <b>51</b>
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		Title: <b>FPGA_6A_6B</b>		Rev. <b>03</b>
A4	Number: <b>TEI0185 P001</b>	Date: <b>2024-02-14</b>	Copyright: <b>Trenz Electronic GmbH</b>	
Filename: <b>FPGA_Bank_HVIO_6A_6B.SchDoc</b>		Page 13 of 51		

A

Hvio Bank 6C



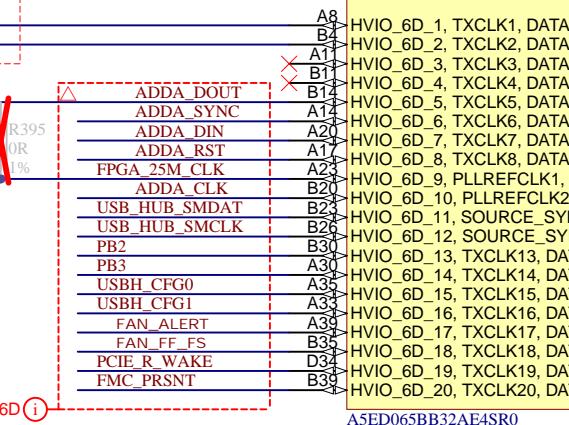
ETH1_RST	F27	HVIO_6C_1, TXCLK1, DATA_CTRL1
ETH1_TXCK	F24	HVIO_6C_2, TXCLK2, DATA_CTRL2
ETH1_RXDO	H23	HVIO_6C_3, TXCLK3, DATA_CTRL3
ETH1_TXD1	D24	HVIO_6C_4, TXCLK4, DATA_CTRL4
ETH1_RXD2	H18	HVIO_6C_5, TXCLK5, DATA_CTRL5
ETH1_RXD3	D15	HVIO_6C_6, TXCLK6, DATA_CTRL6
ETH1_RXCTL	F18	HVIO_6C_7, TXCLK7, DATA_CTRL7
ETH1_RXD1	F13	HVIO_6C_8, TXCLK8, DATA_CTRL8
ETH1_RXD0	D8	HVIO_6C_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
ETH1_RXCK	K8	HVIO_6C_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
ETH1_RXD2	F8	HVIO_6C_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
ETH1_RXD3	H8	HVIO_6C_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
MUX_I2C_SCL	C2	HVIO_6C_13, TXCLK13, DATA_CTRL13
MUX_I2C_SDA	D1	HVIO_6C_14, TXCLK14, DATA_CTRL14
MUX_I2C_INT	F4	HVIO_6C_15, TXCLK15, DATA_CTRL15
PWR_SCL	G1	HVIO_6C_16, TXCLK16, DATA_CTRL16
PWR_SDA	J2	HVIO_6C_17, TXCLK17, DATA_CTRL17
ETH1_MDIO	J1	HVIO_6C_18, TXCLK18, DATA_CTRL18
ETH1_MDC	G1	HVIO_6C_19, TXCLK19, DATA_CTRL19

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B

Hvio Bank 6D

PCB Board Version



A5ED065BB32AE4SR0

C

Hvio Bank 6D

REV_ID0	A8	HVIO_6D_1, TXCLK1, DATA_CTRL1
REV_ID1	B4	HVIO_6D_2, TXCLK2, DATA_CTRL2
GND	A1	HVIO_6D_3, TXCLK3, DATA_CTRL3
R395	B11	HVIO_6D_4, TXCLK4, DATA_CTRL4
10R	B12	HVIO_6D_5, TXCLK5, DATA_CTRL5
1%	A13	HVIO_6D_6, TXCLK6, DATA_CTRL6
ADD_A_DOUT	A20	HVIO_6D_7, TXCLK7, DATA_CTRL7
ADD_A_SYNC	A17	HVIO_6D_8, TXCLK8, DATA_CTRL8
ADD_A_DIN	A23	HVIO_6D_9, PLLREFCLK1, TXCLK9, RXCLK1, DATA_CTRL9
ADD_A_RST	B20	HVIO_6D_10, PLLREFCLK2, TXCLK10, RXCLK2, DATA_CTRL10
FPGA_25M_CLK	B23	HVIO_6D_11, SOURCE_SYNC_CLK1, TXCLK11, RXCLK3, DATA_CTRL11
ADD_A_CLK	B26	HVIO_6D_12, SOURCE_SYNC_CLK2, TXCLK12, RXCLK4, DATA_CTRL12
USB_HUB_SMDAT	PB2	HVIO_6D_13, TXCLK13, DATA_CTRL13
USB_HUB_SMCLK	PB3	HVIO_6D_14, TXCLK14, DATA_CTRL14
USBH_CFG0	A35	HVIO_6D_15, TXCLK15, DATA_CTRL15
USBH_CFG1	A33	HVIO_6D_16, TXCLK16, DATA_CTRL16
FAN_ALERT	A39	HVIO_6D_17, TXCLK17, DATA_CTRL17
FAN_FF_FS	B35	HVIO_6D_18, TXCLK18, DATA_CTRL18
PCIE_R_WAKE	D34	HVIO_6D_19, TXCLK19, DATA_CTRL19
FMC_PRSNT	B39	HVIO_6D_20, TXCLK20, DATA_CTRL20

D

Title: FPGA\_6C\_6D

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A

A

B

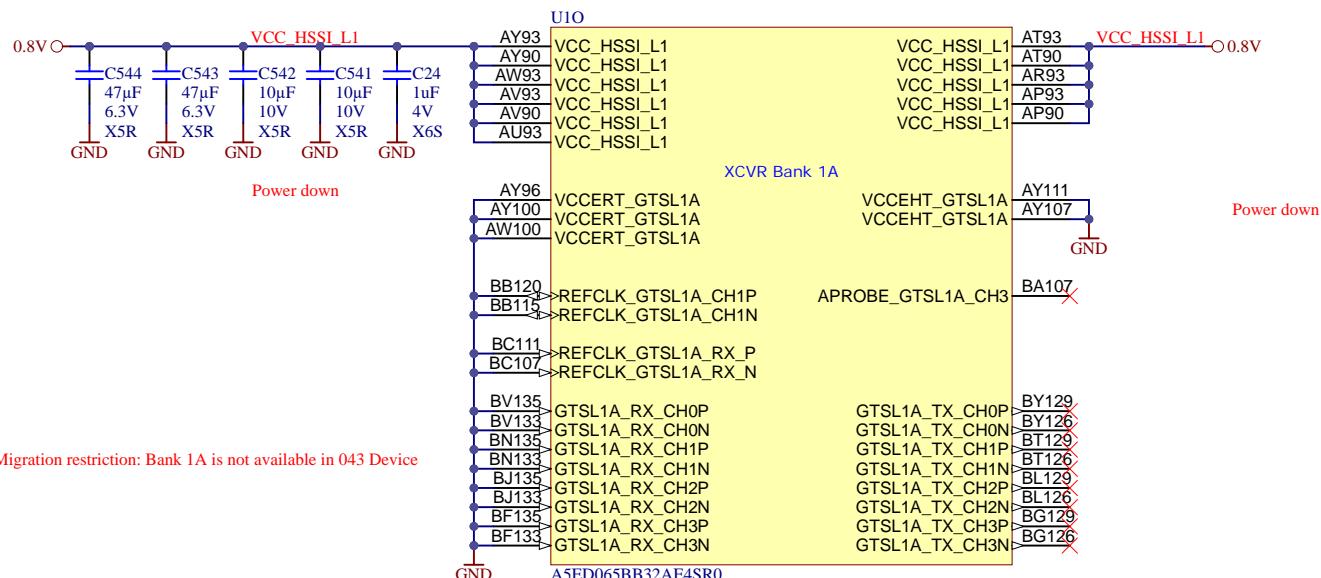
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C

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D



Title:  
**FPGA\_1A**

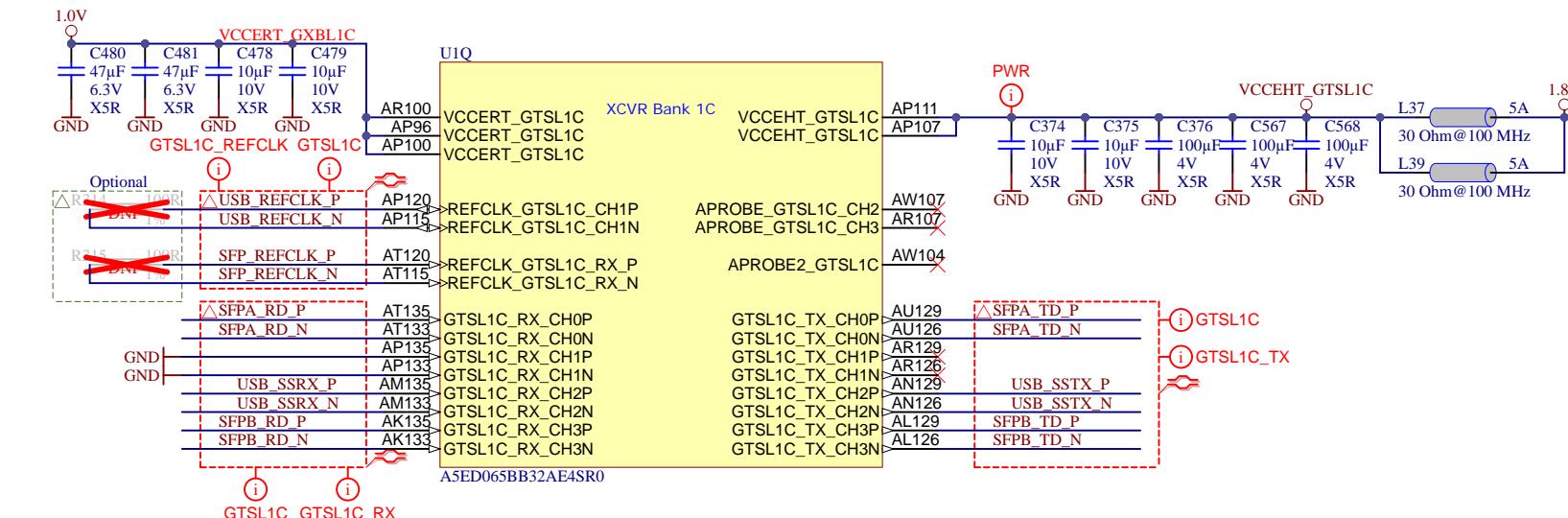
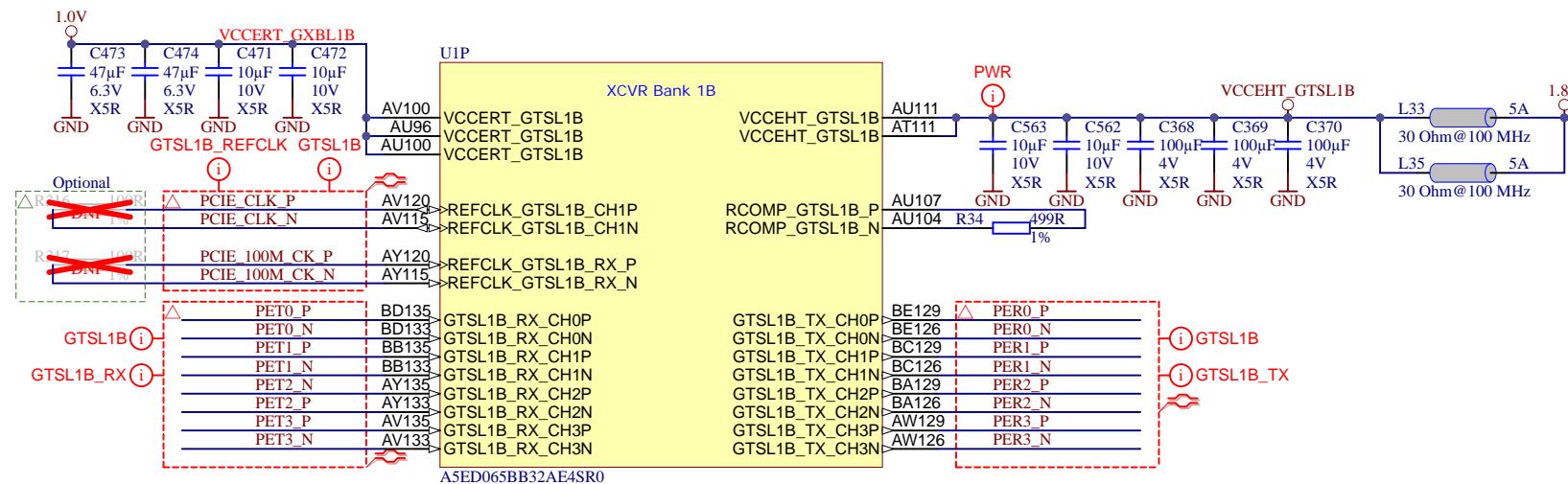
A4 | Number: **TEI0185  
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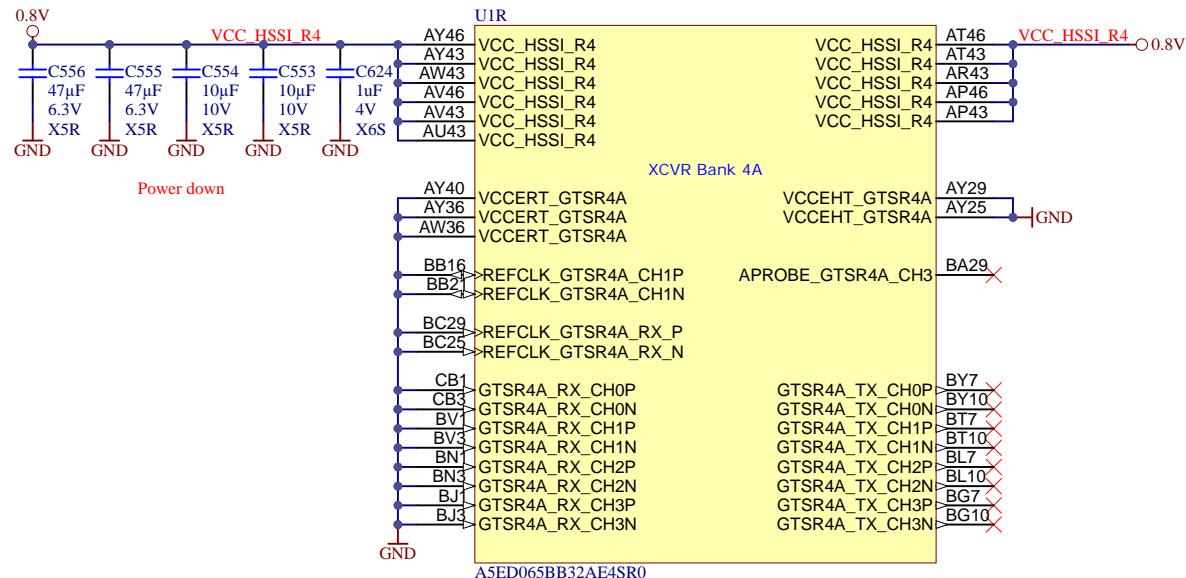
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Filename: **FPGA\_XCVR\_1A.SchDoc**

Title: **FPGA\_1B\_1C**A4 Number: **TEI0185  
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A

A



B

B

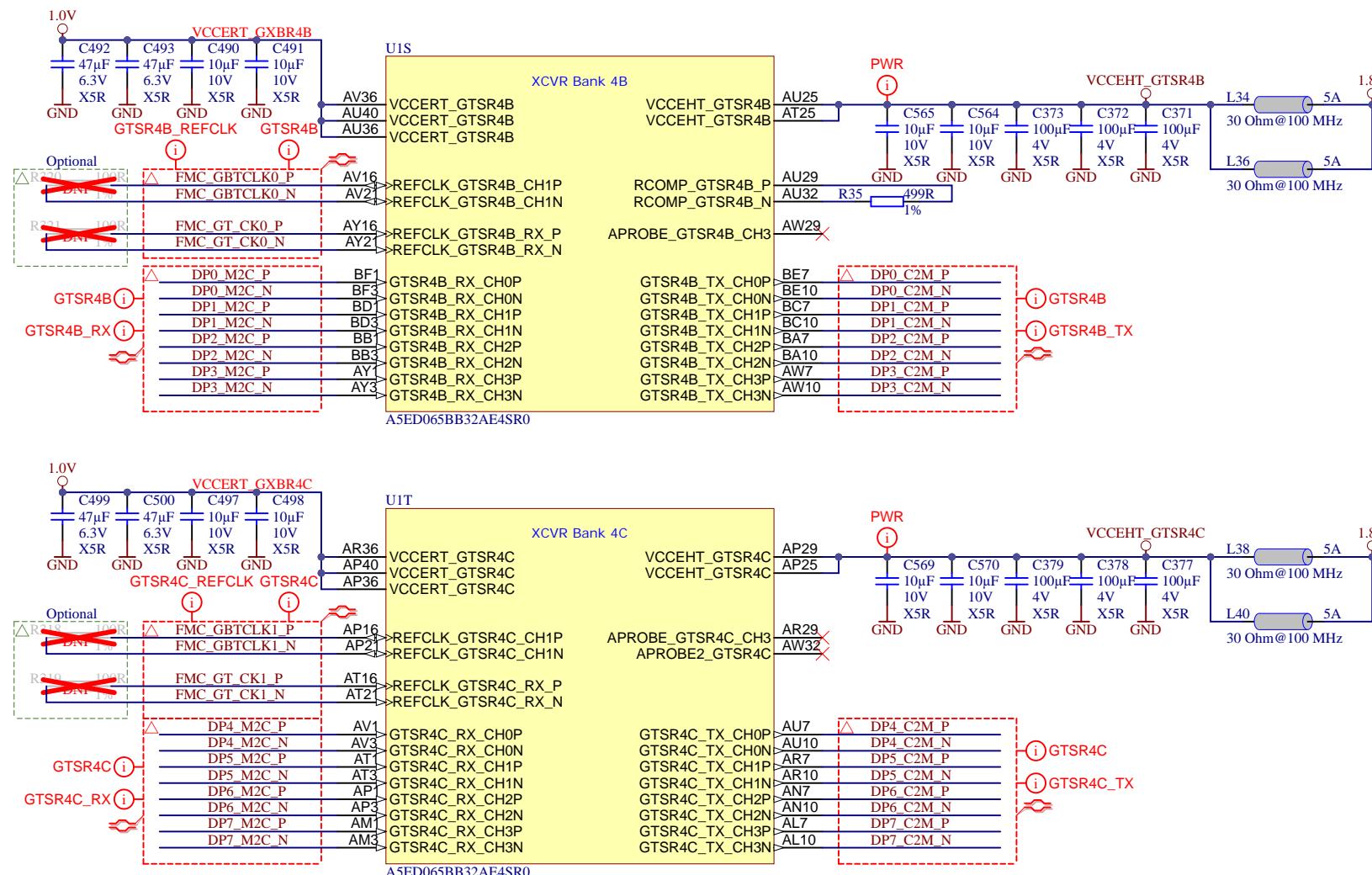
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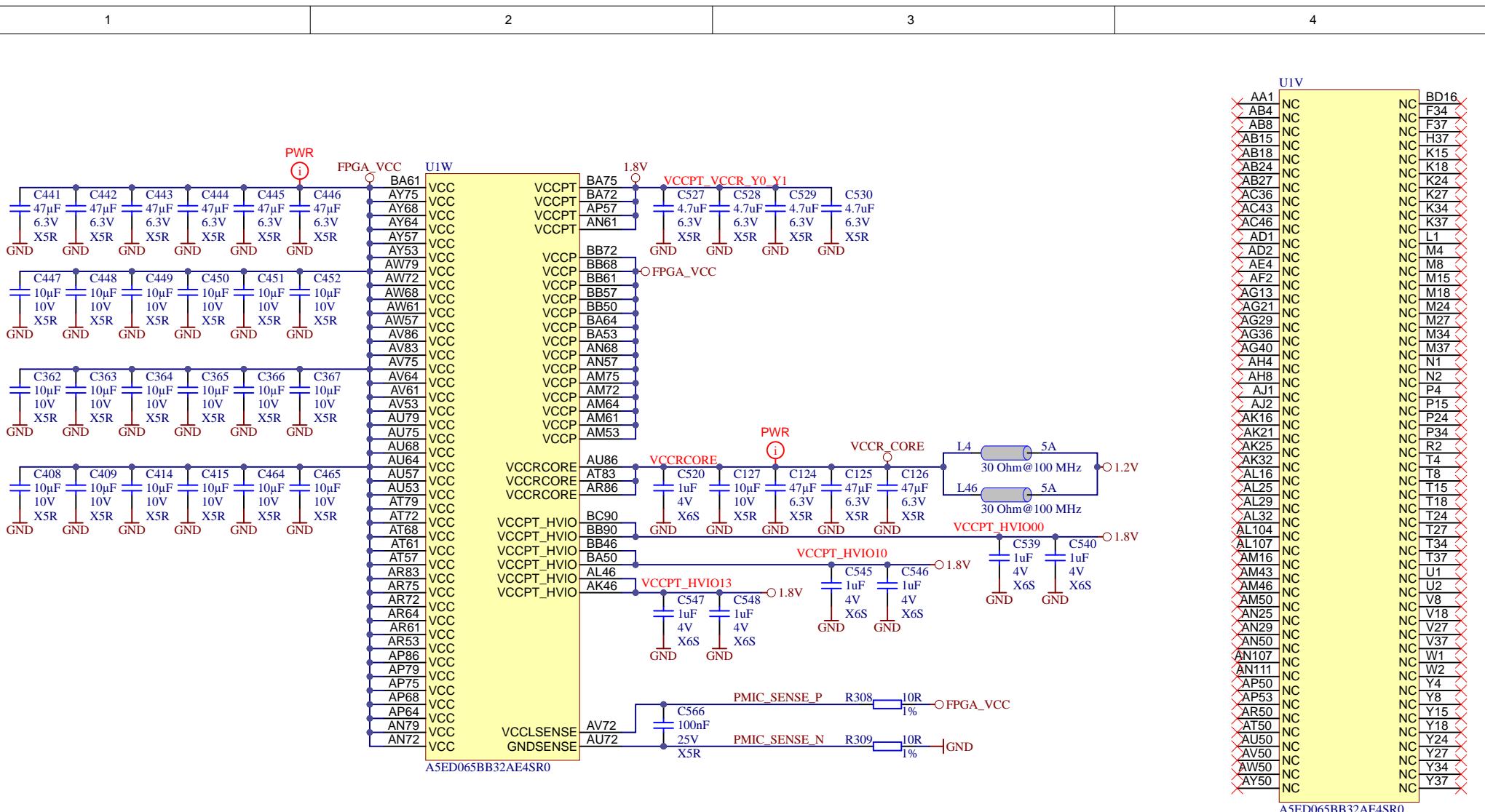
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D

Title: <b>FPGA_4A</b>		
A4	Number: <b>TEI0185 P001</b>	Rev. <b>03</b>
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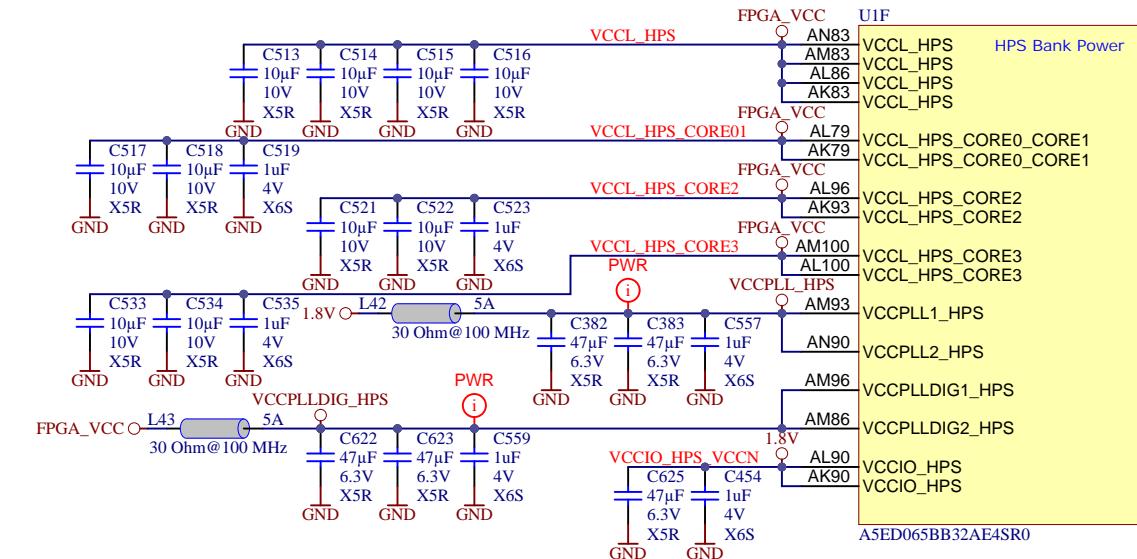
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A4	Number: <b>TEI0185 P001</b>	Rev. <b>03</b>
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Title: <b>FPGA_Power</b>		
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A



B

U1U	
AL43	DNU
AL57	DNU
AL68	DNU
AL115	DNU
AM36	DNU
AM40	DNU
AM120	DNU
AR32	DNU
AR104	DNU
BA32	DNU
BA104	DNU
BC36	DNU
BC40	BC100
BD36	BD53
BD64	BD100
BD120	CK101
CK103	CL101
CL106	CL106

A5ED065BB32AE4SR0

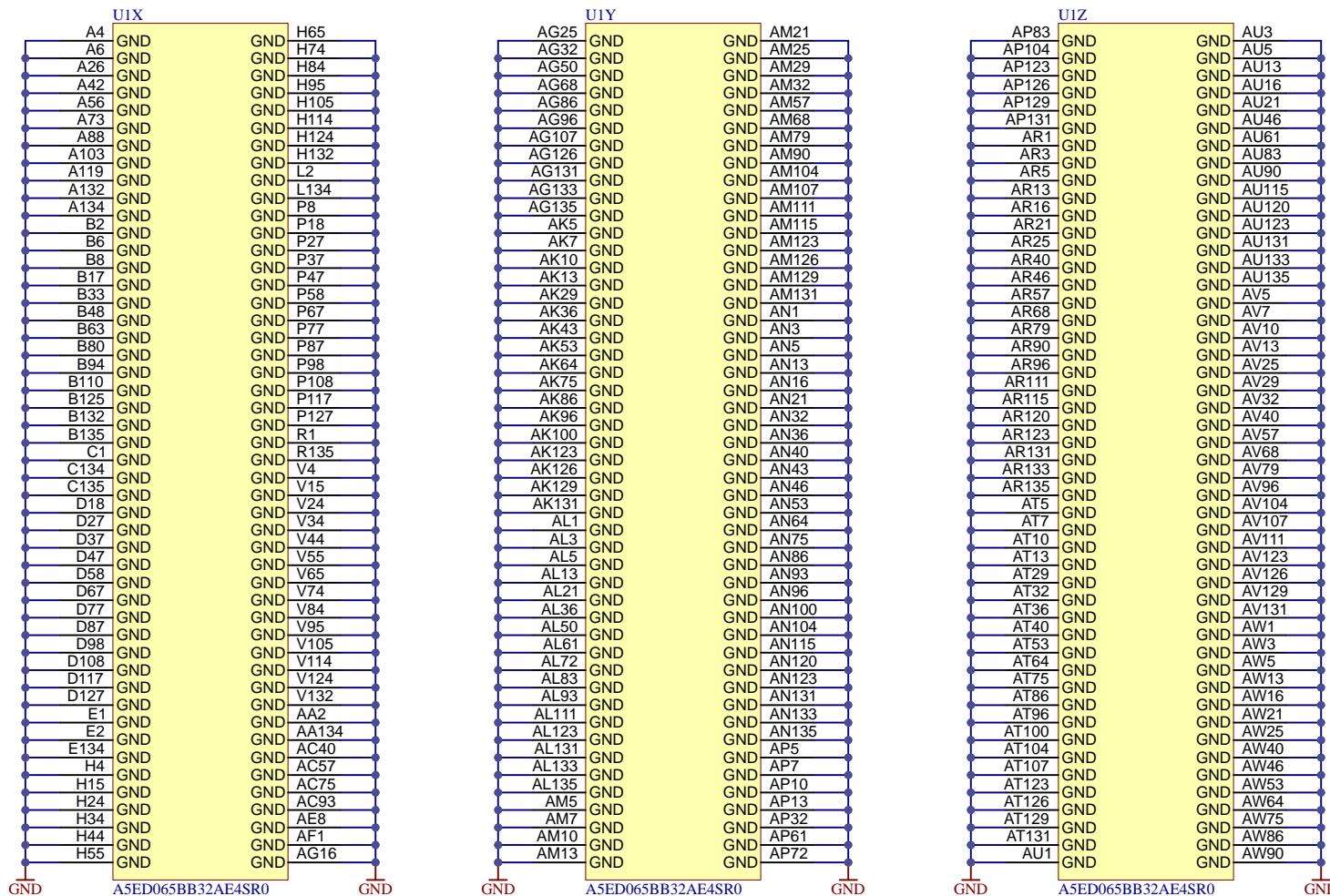
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Title: **FPGA\_Power**  
 A4 Number: **TEI0185**  
**P001** Rev. **03**

Date: **2024-02-14** Copyright: **Trenz Electronic GmbH** Page **20** of **51**

Filename: **FPGA\_PWR2.SchDoc**



Title:  
**FPGA\_GND**

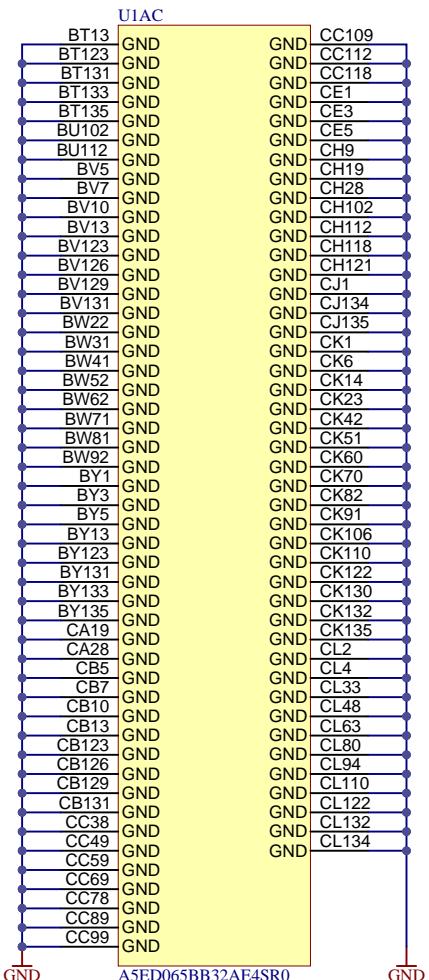
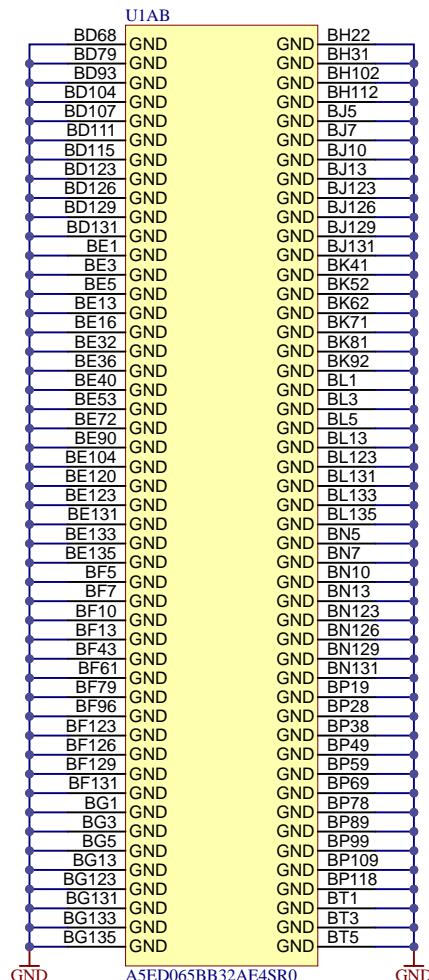
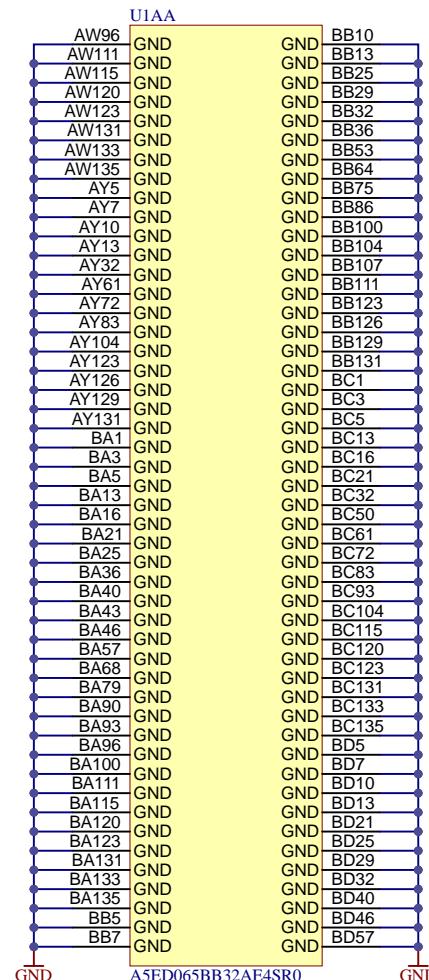
A4 | Number: **TEI0185  
P001**

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Filename: **FPGA\_GND\_1.SchDoc**



Title: ERCA-GRD

A4 Number: TEI0185  
P001

Date: 2024-02-14 Copyright: Trenz Electronic GmbH

Rev.  
03

1

2

3

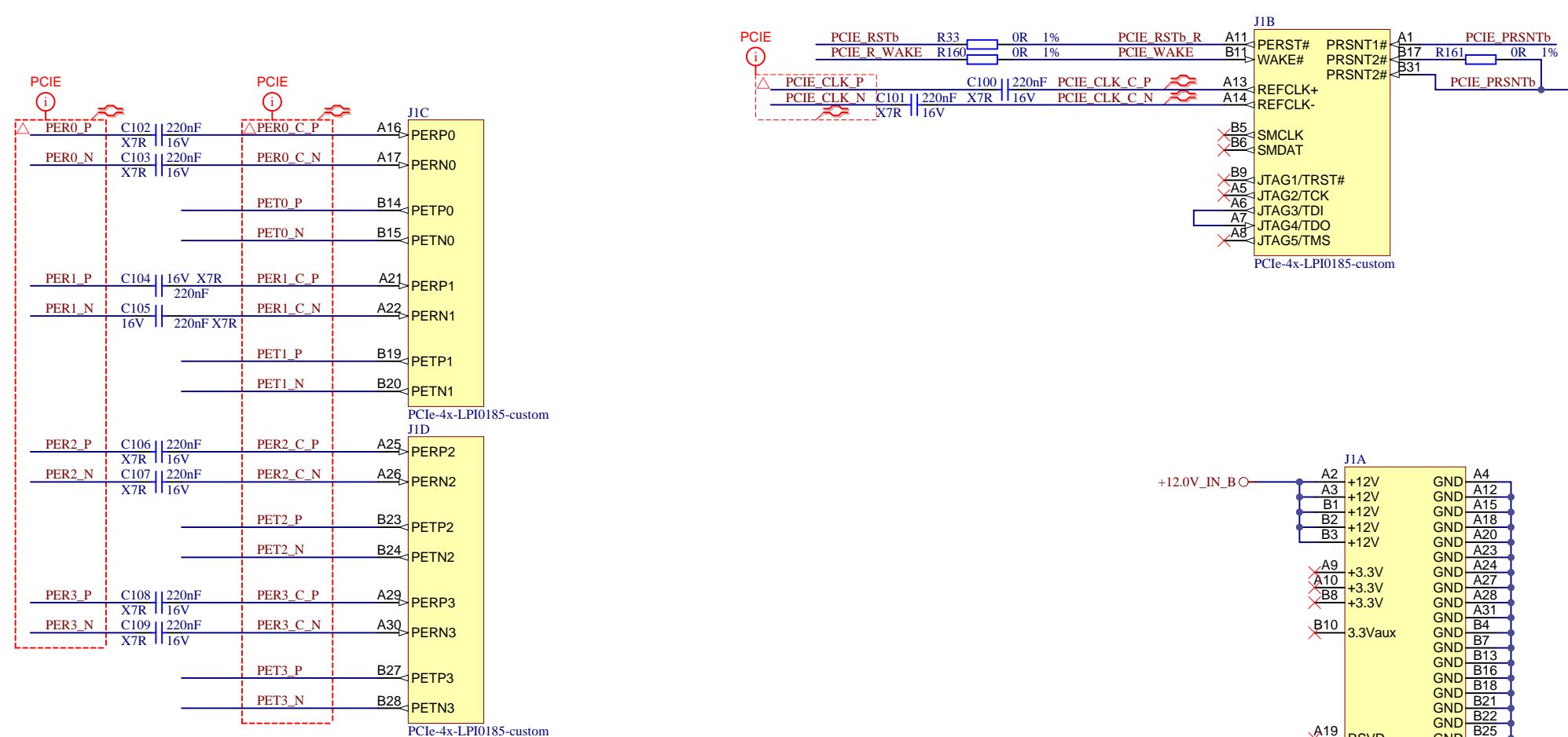
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1

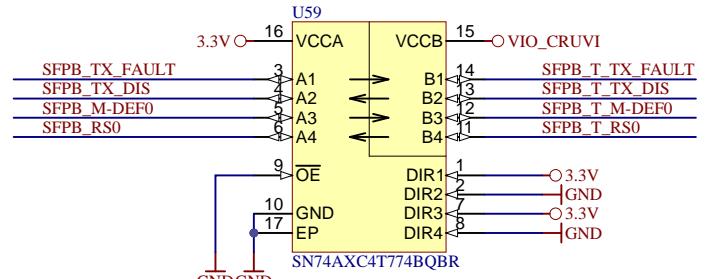
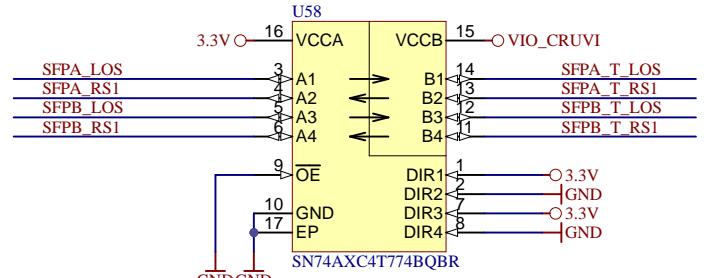
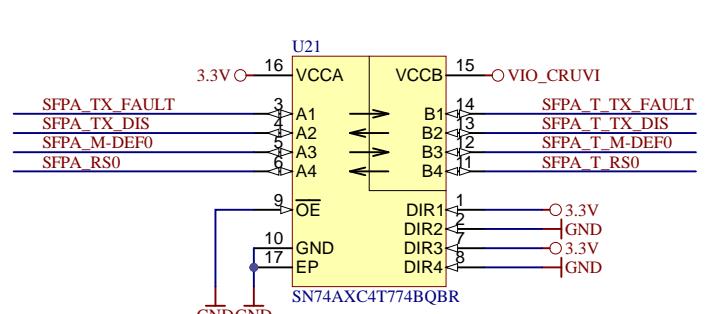
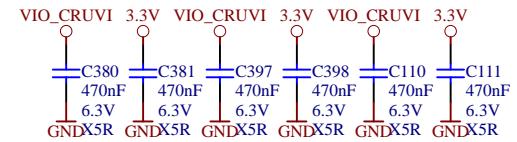
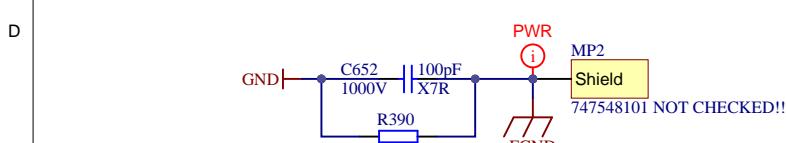
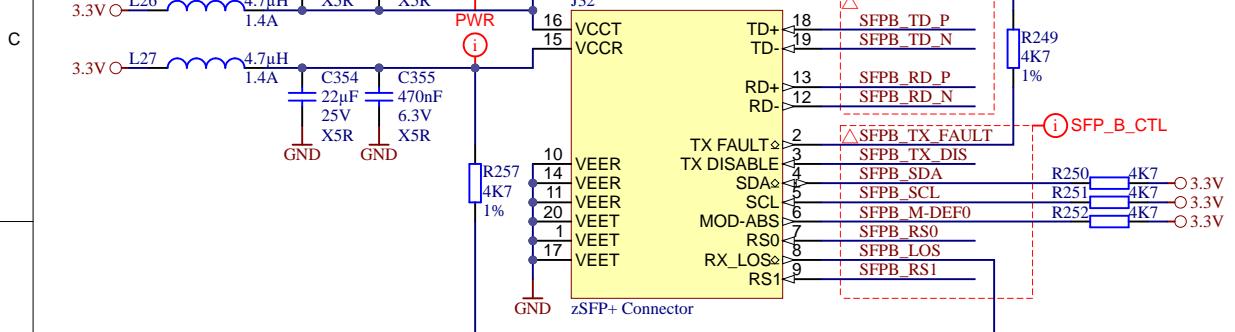
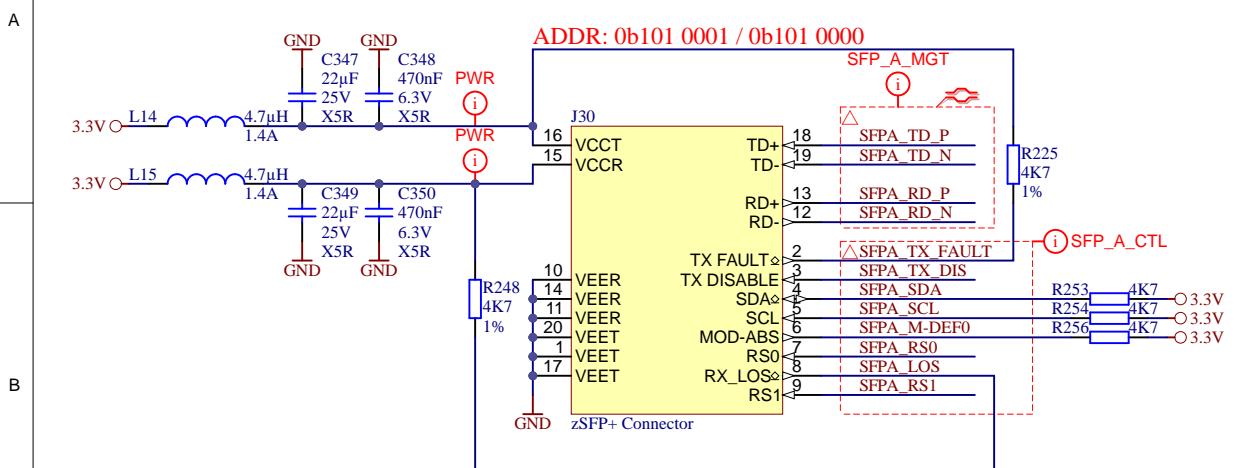
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3

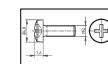
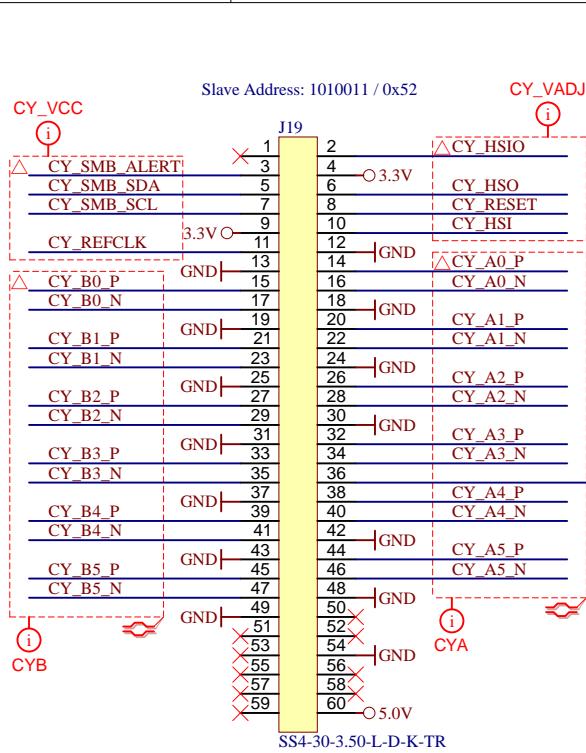
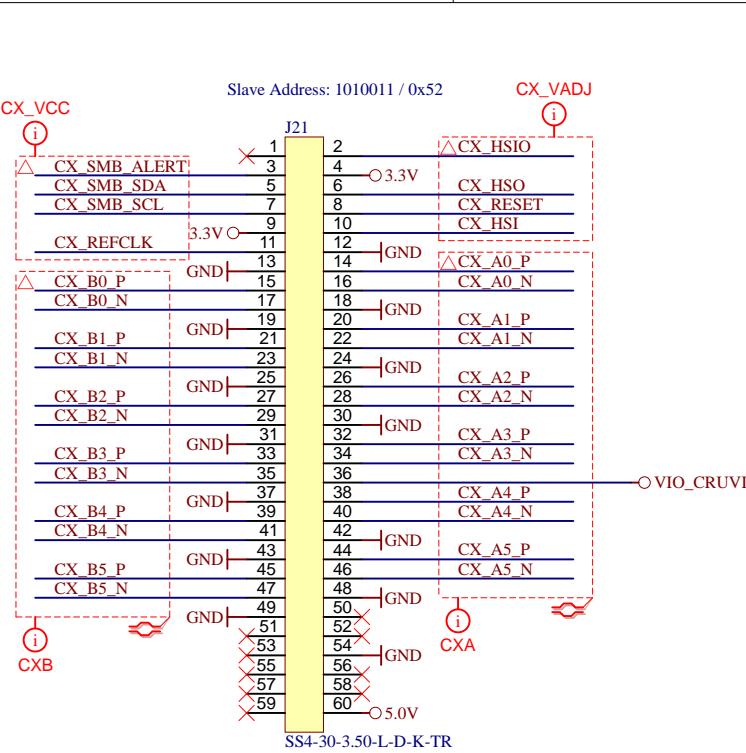
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Title: PCIE x4		Rev. 03
A4	Number: TEI0185 P001	
Date: 2024-02-14 Copyright: Trenz Electronic GmbH		Page 23 of 51
Filename: PCIE_CONN.SchDoc		



		Title: zSFP+	
A4	Number: TEI0185 P001		Rev. 03
Date: 2024-02-14	Copyright: Trenz Electronic GmbH		Page 24 of 51
Filename: zSFP+.SchDoc			



Screw M2x6



Steel Spacer M2 5mm SMD



Steel Spacer M2 5mm SMD



Steel Spacers M2.5mm SMD



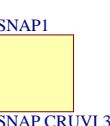
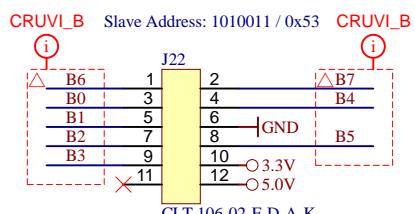
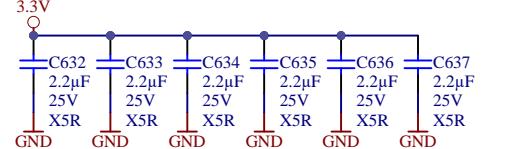
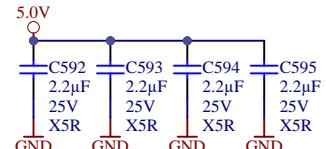
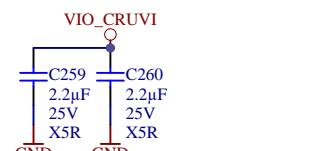
卷之三



ANSWER

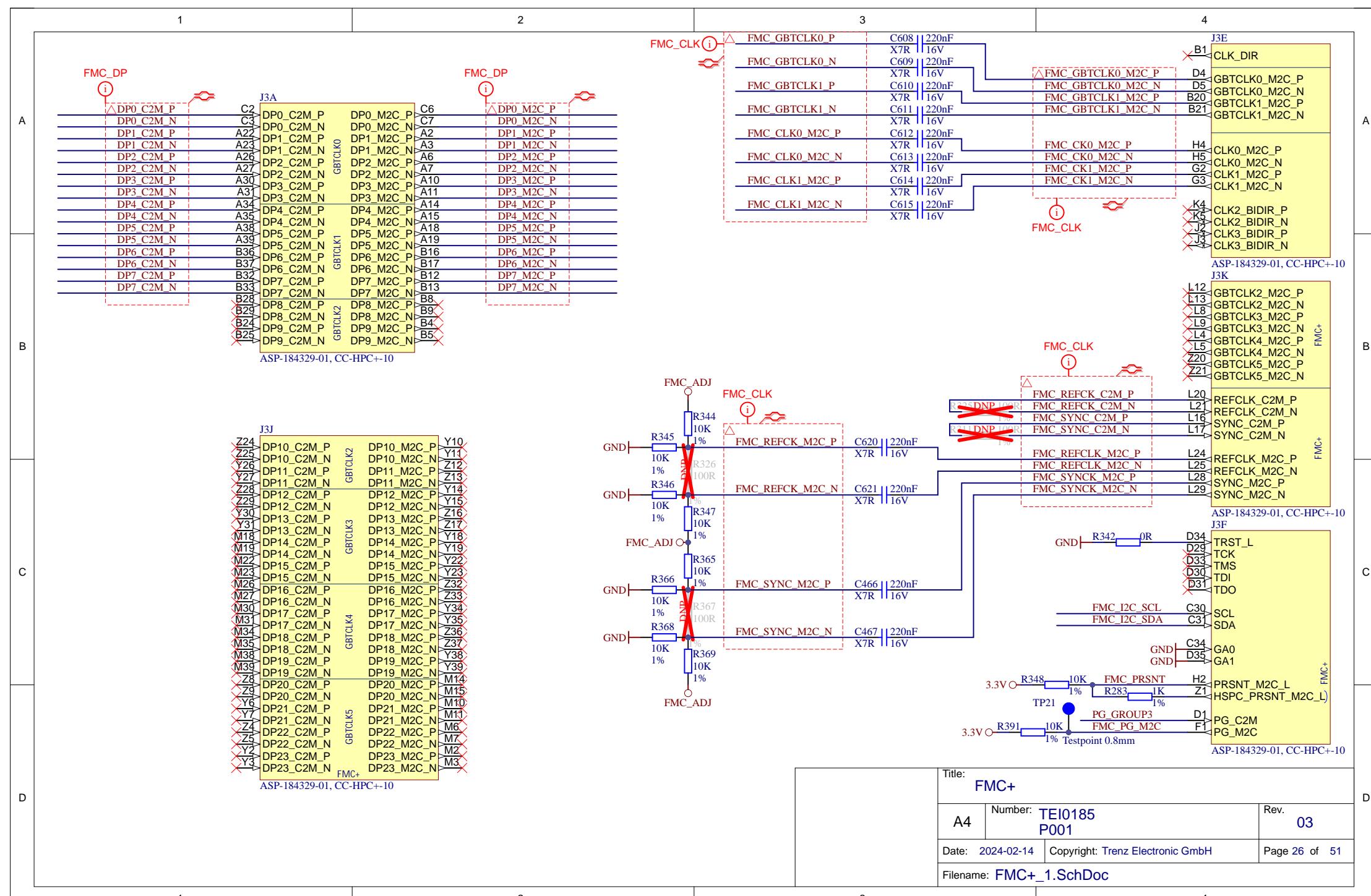


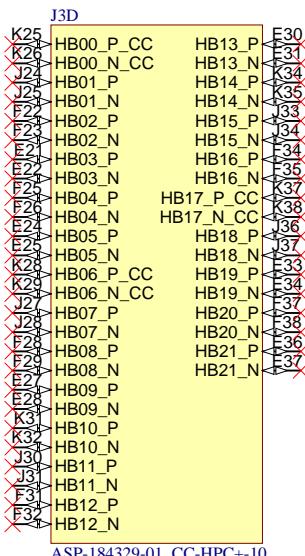
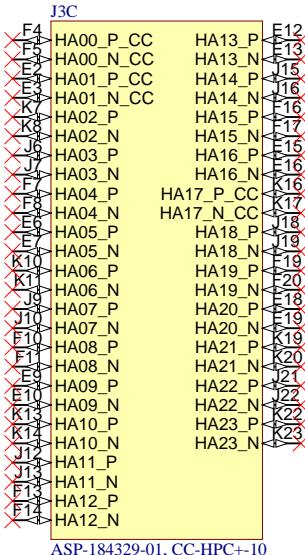
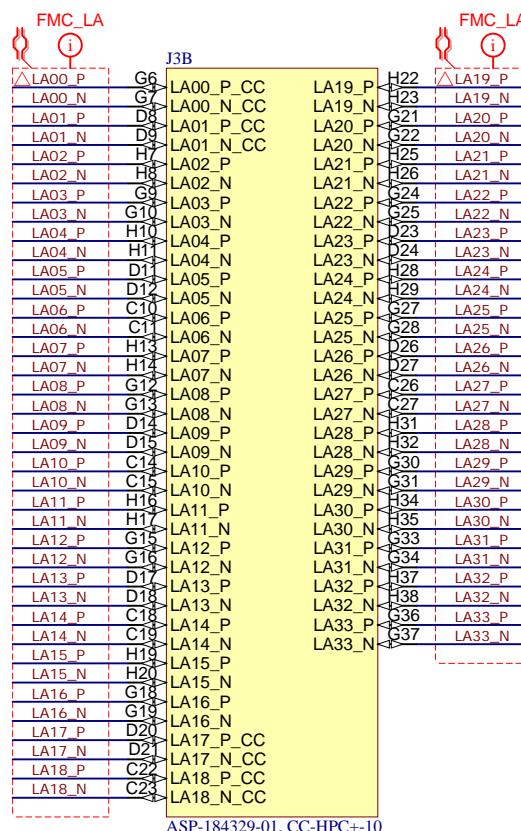
Page 1



Title: CPH 411

CRUVI		
A4	Number: TEI0185 P001	Rev. 03
Date: 2024-02-14	Copyright: Trenz Electronic GmbH	Page 25 of 51
Filename: CRUVI.SchDoc		





Title:  
**FMC+**

A4 Number: **TEI0185  
P001**

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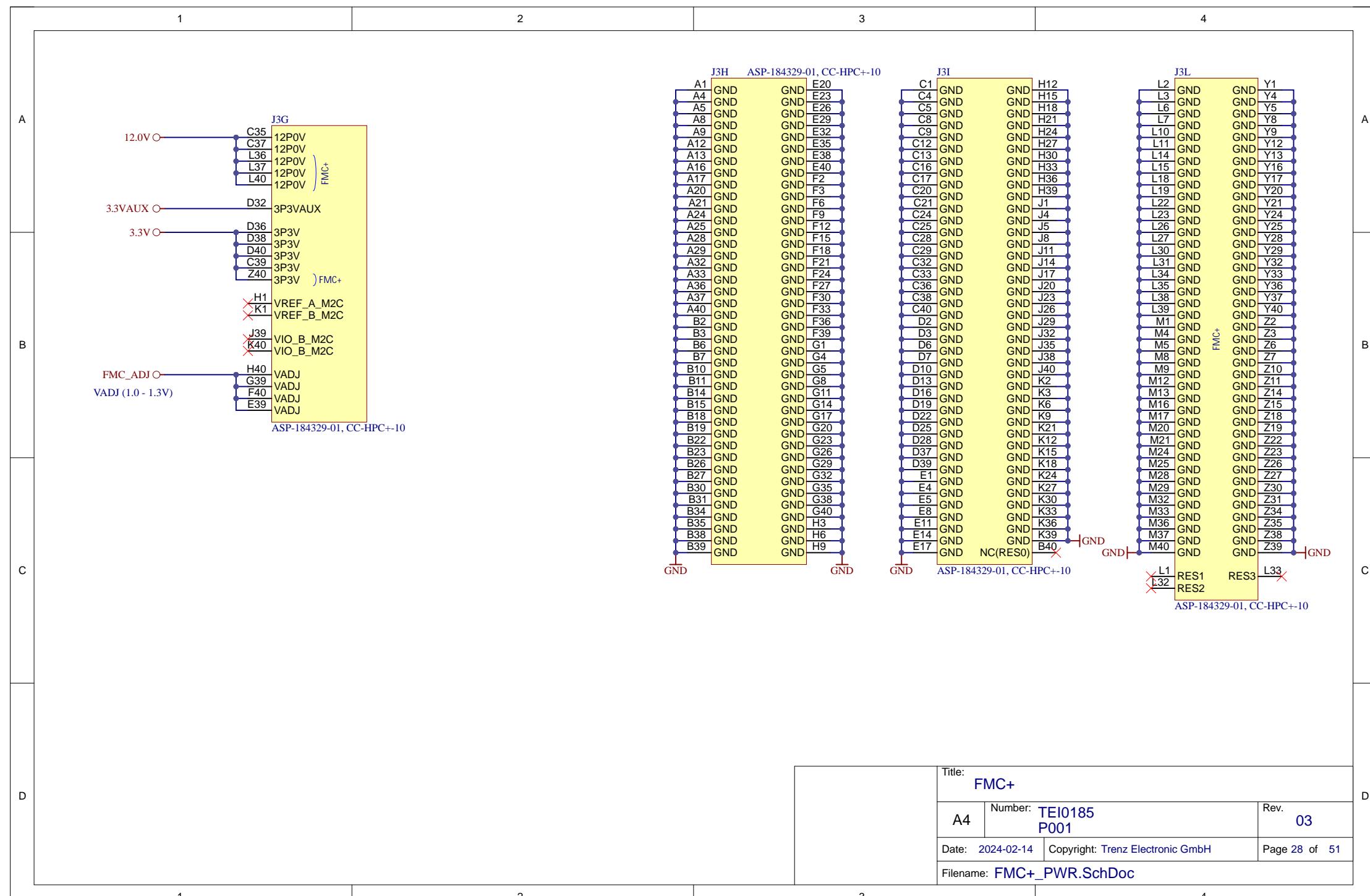
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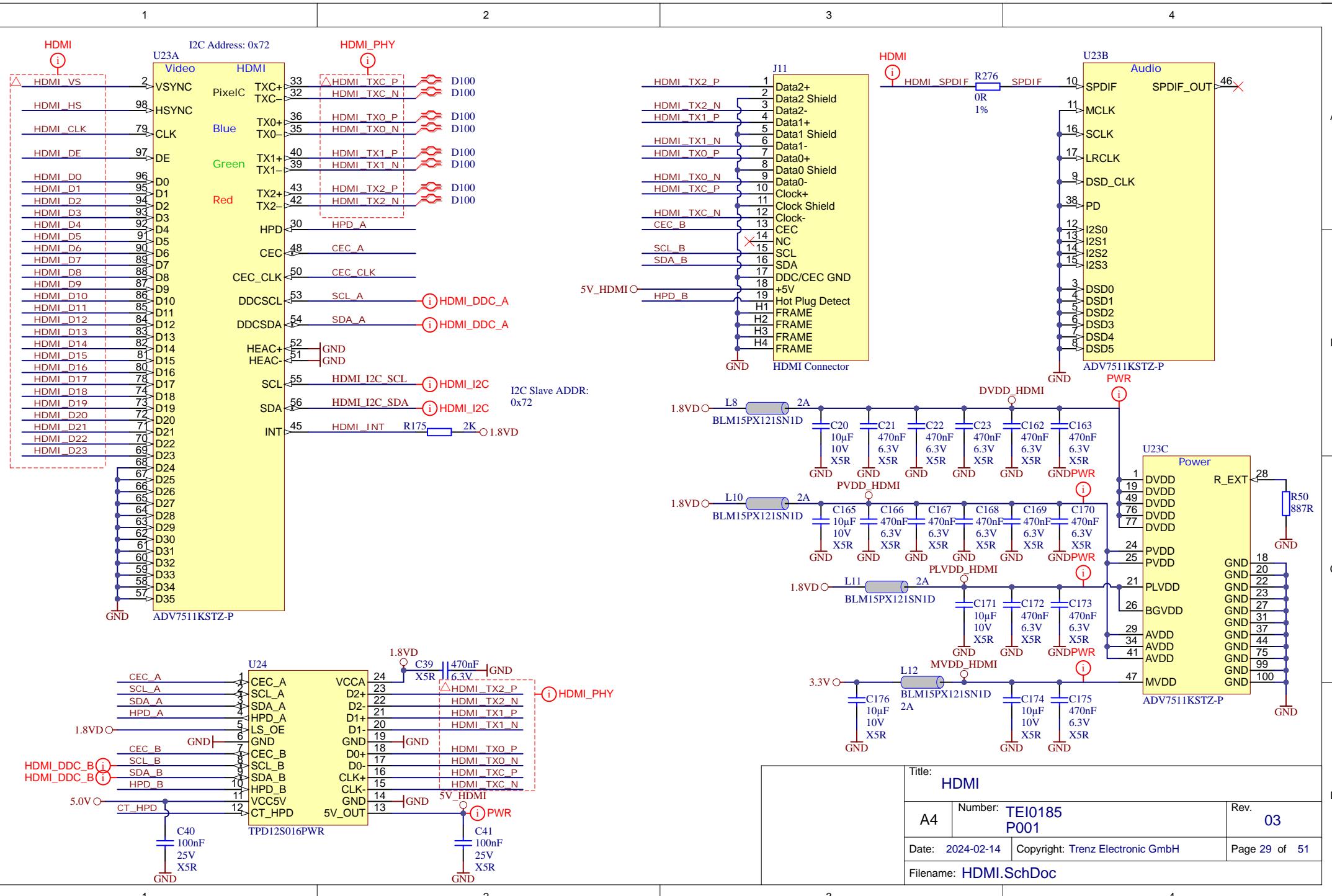
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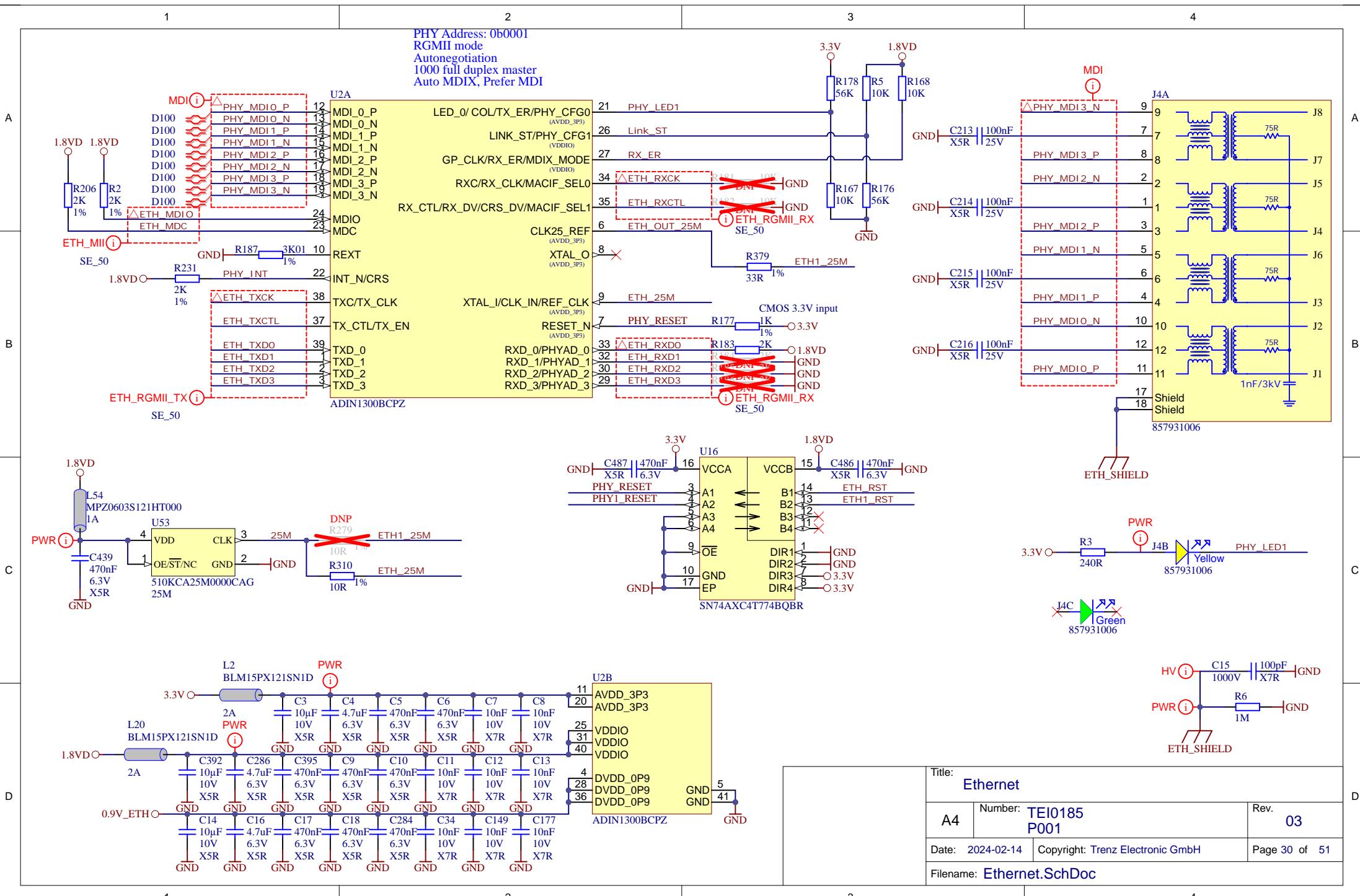
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3

4

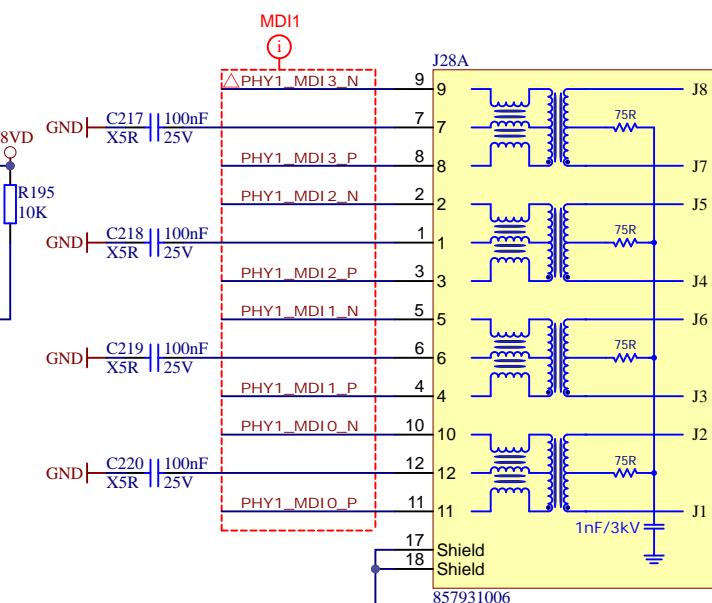
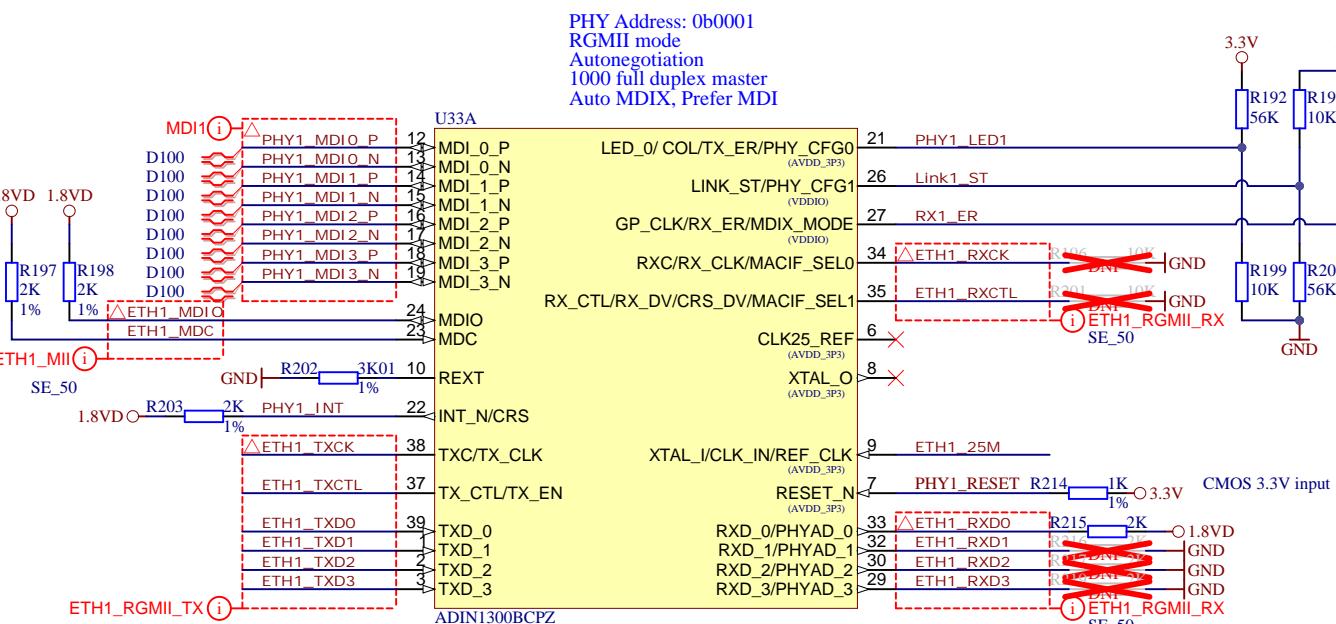




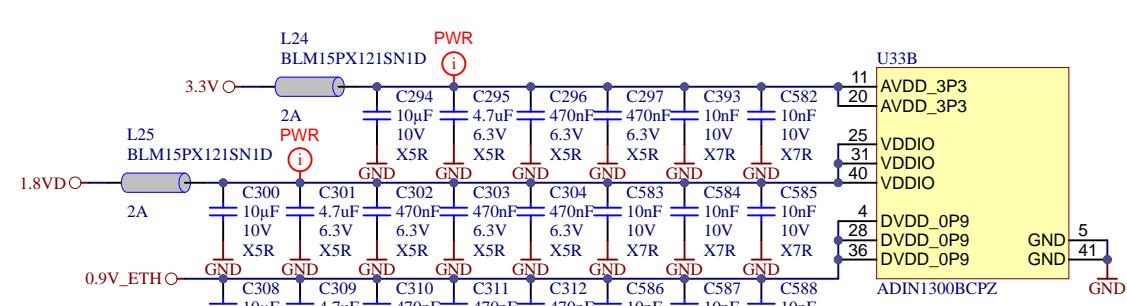


1 2 3 4

A

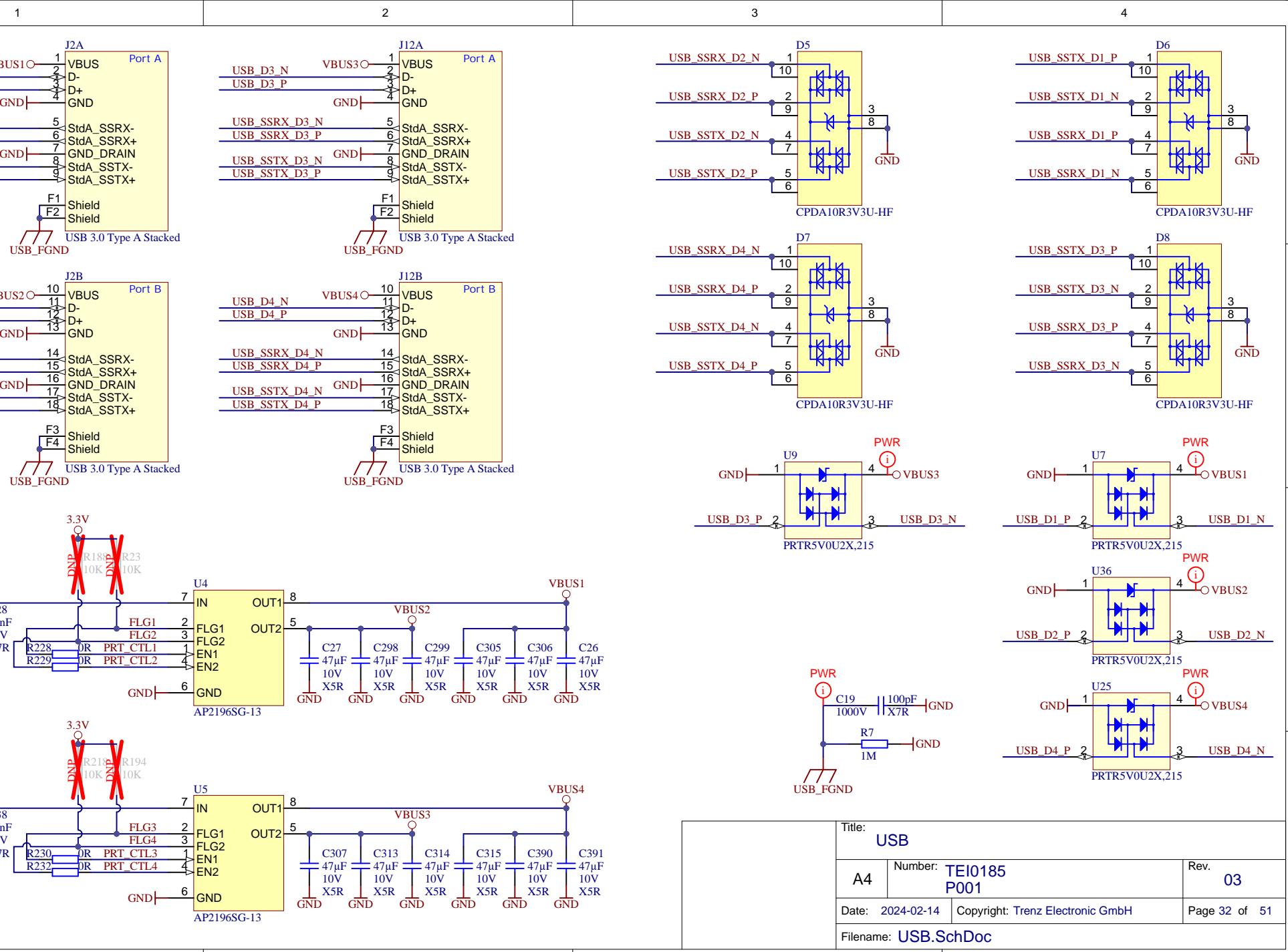


857931006



Title: Ethernet HVIO		Rev. 03
A4	Number: TEI0185 P001	Date: 2024-02-14 Copyright: Trenz Electronic GmbH Page 31 of 51
Filename: Ethernet_HVIO.SchDoc		

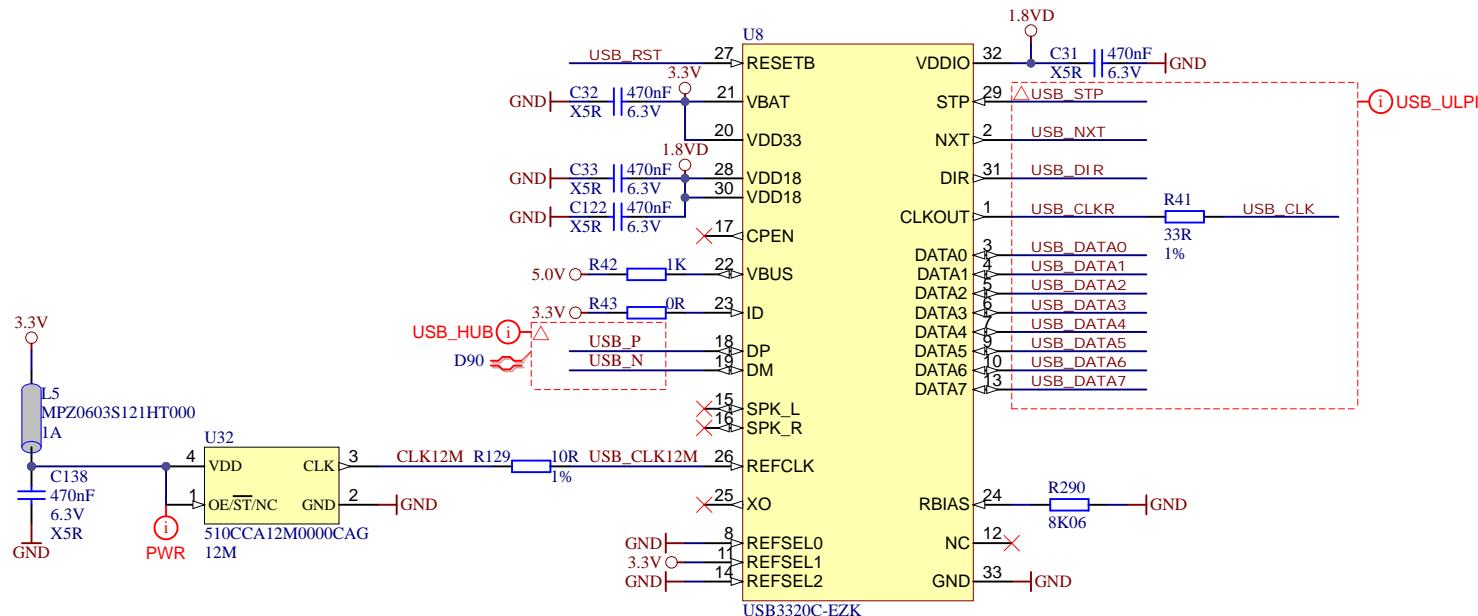
1 2 3 4



A

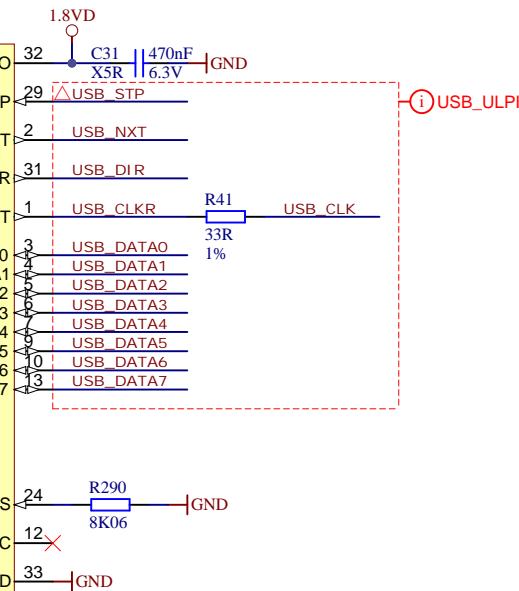
A

VBAT, VDD33, and VDD18 can be applied in any order.  
 The VDD18 supply must be turned on and stable before  
 the VDDIO supply is applied. This does not apply in  
 cases where the VDD18 and VDDIO are tied together.



B

B



C

C

D

D

Title:  
**USB-PHY**

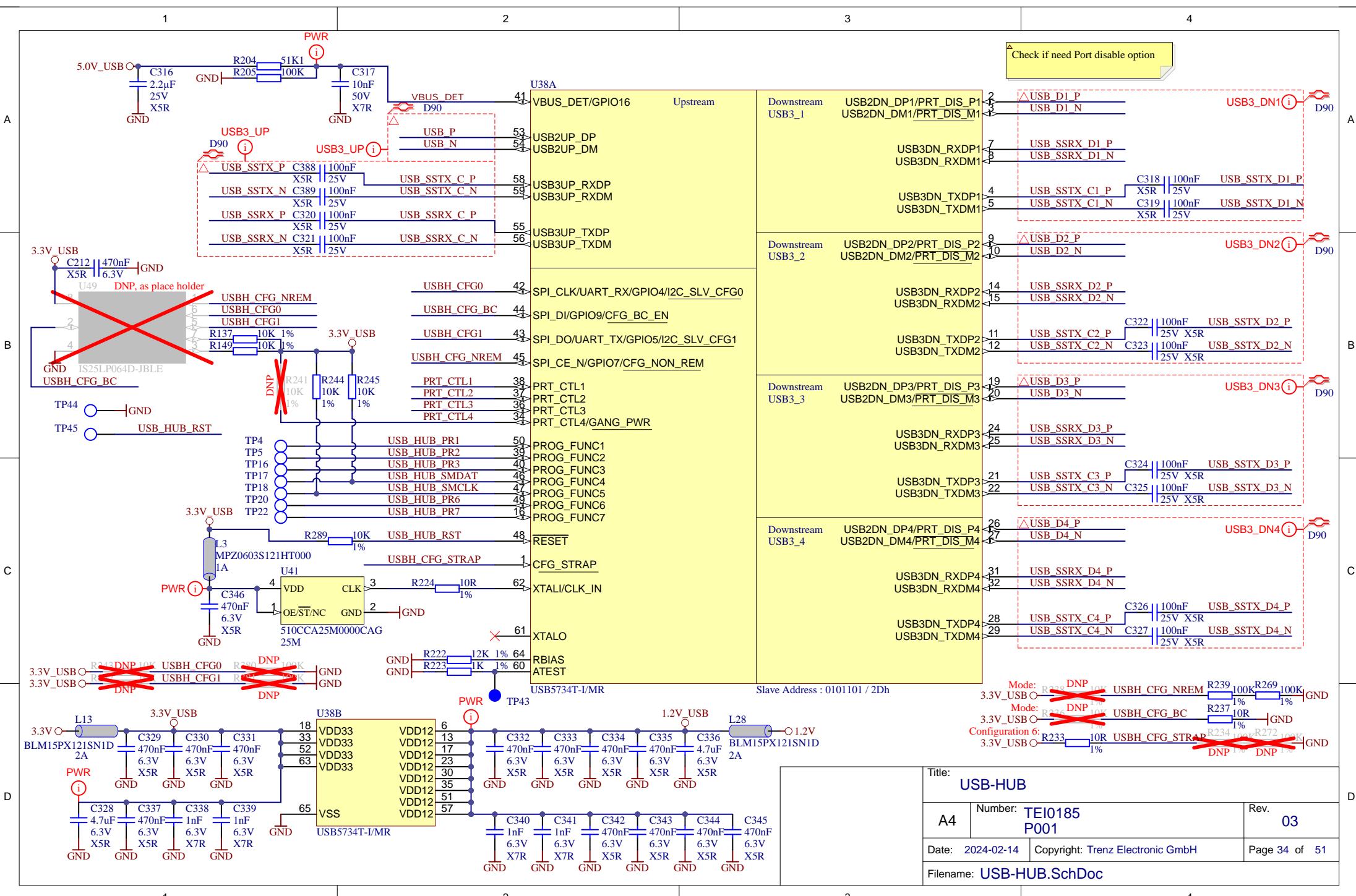
A4 | Number: **TEI0185  
P001**

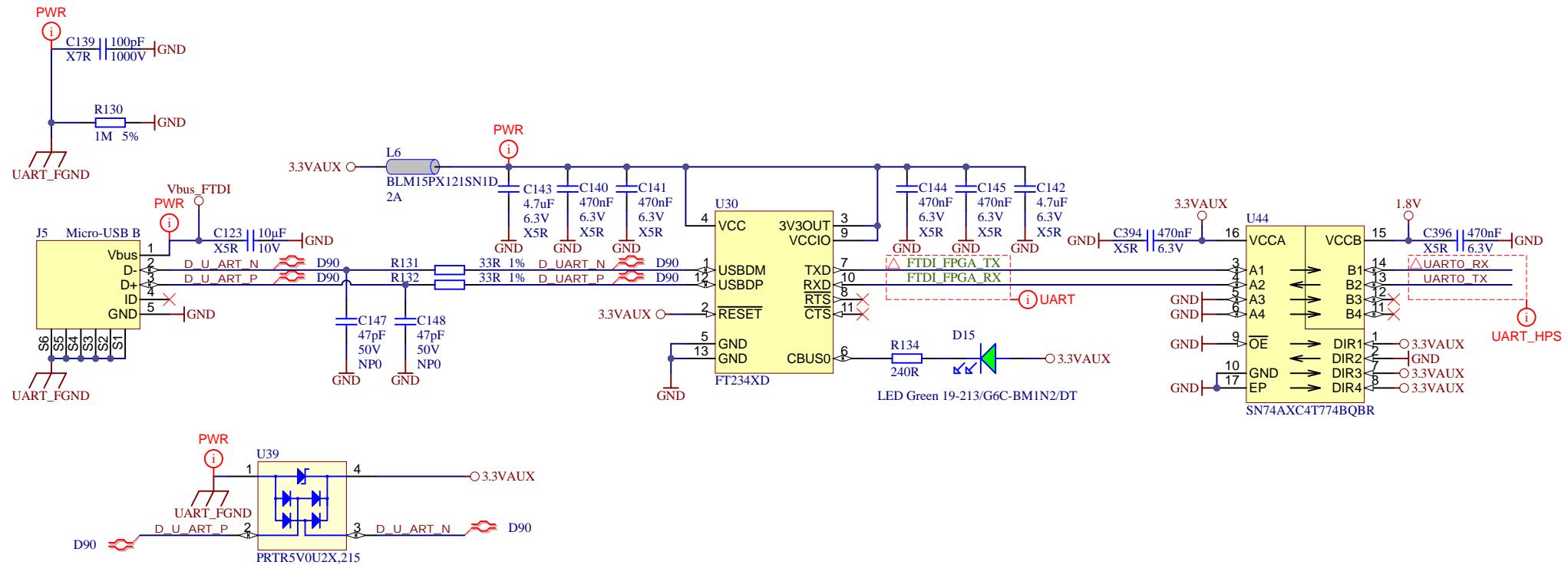
Rev.  
**03**

Date: 2024-02-14 | Copyright: Trenz Electronic GmbH

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Filename: **USB-PHY.SchDoc**



**USB/UART Bridge**

Title: **FTDI\_UART**

A4 | Number: **TEI0185  
P001**

Rev. **03**

Date: 2024-02-14 | Copyright: Trenz Electronic GmbH

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Filename: **FTDI\_UART.SchDoc**

A

A

B

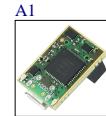
B

C

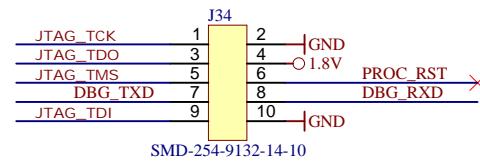
C

D

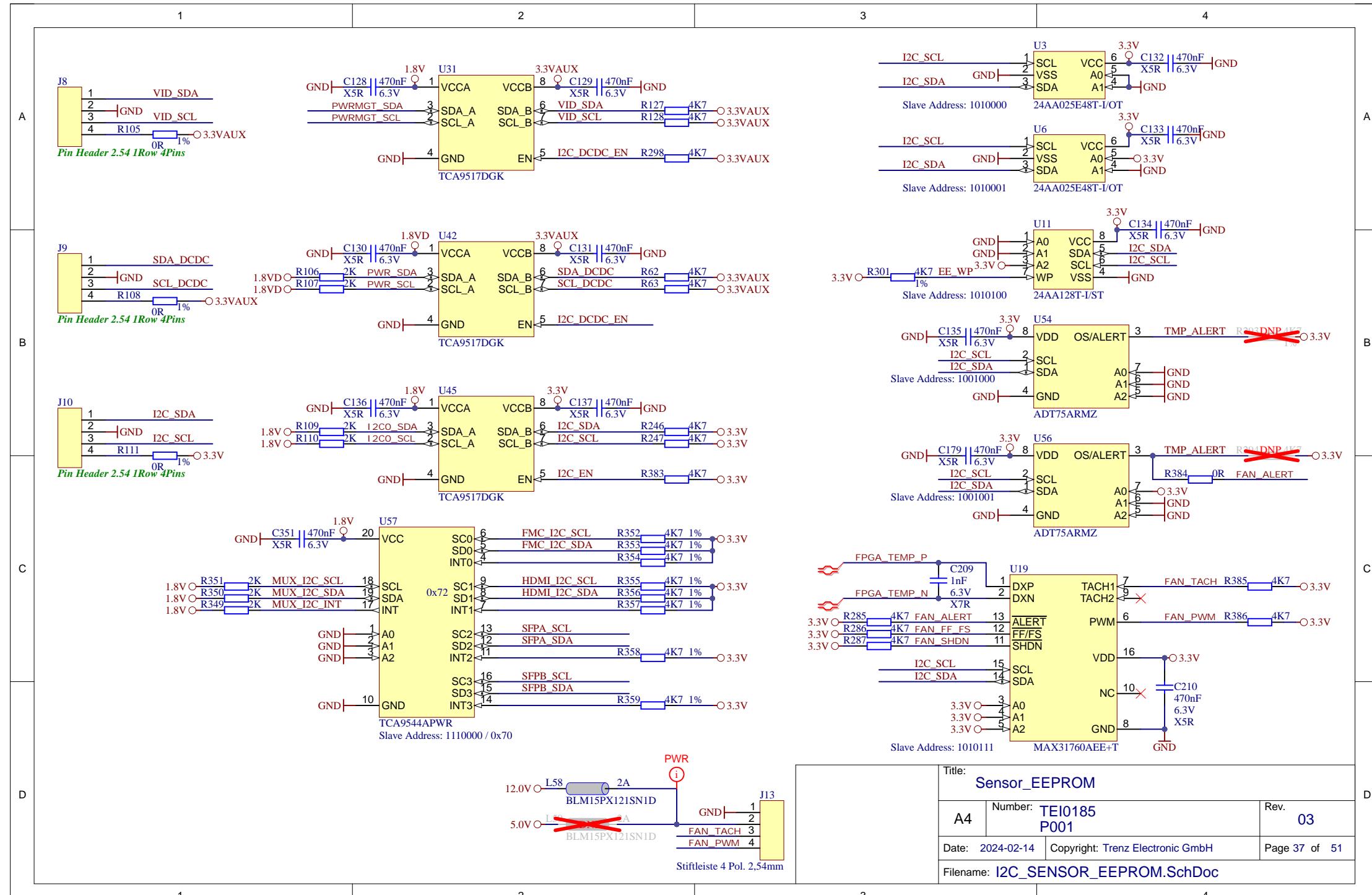
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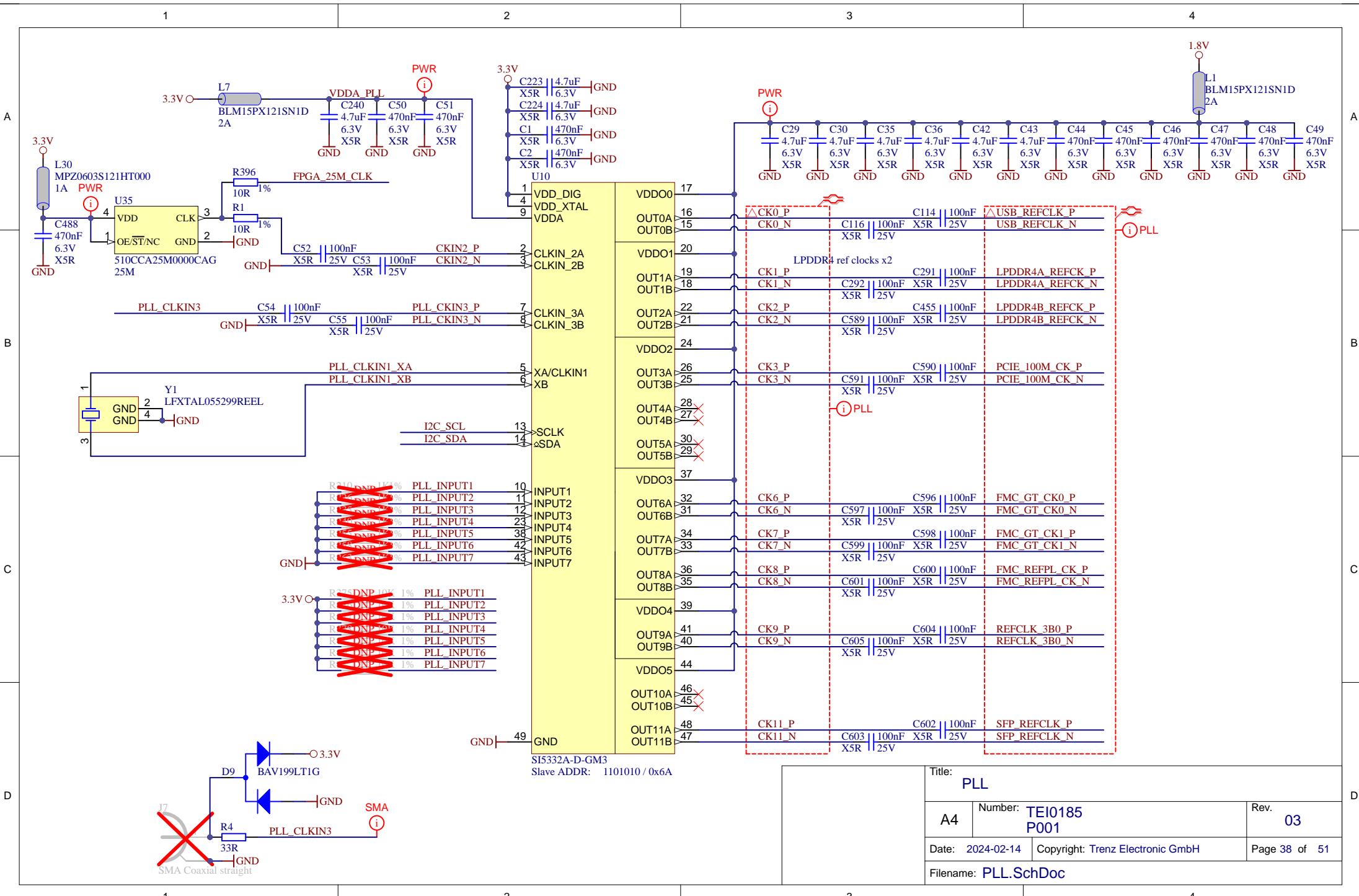


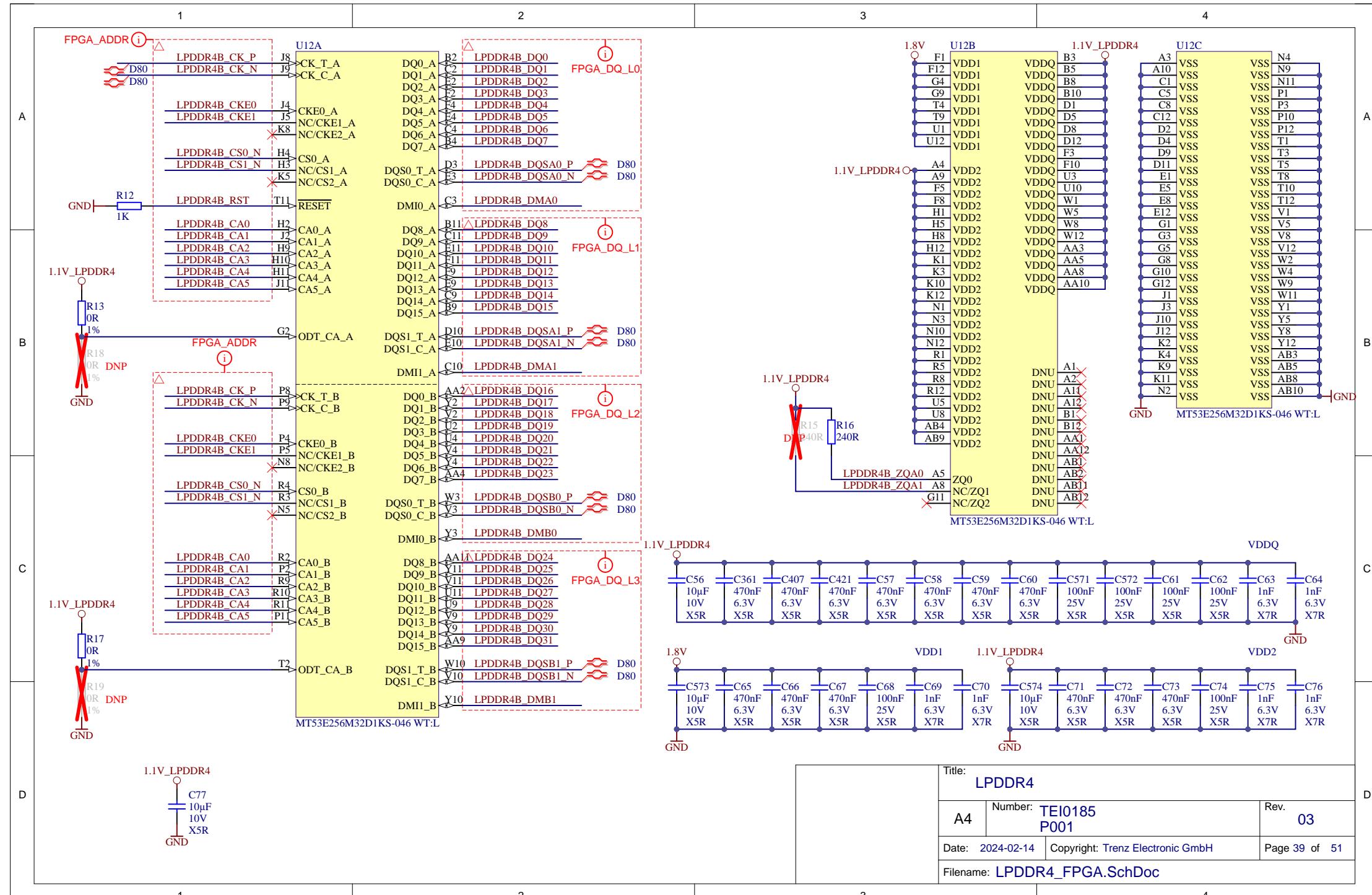
TEI0004 ARROW USB Programmer2

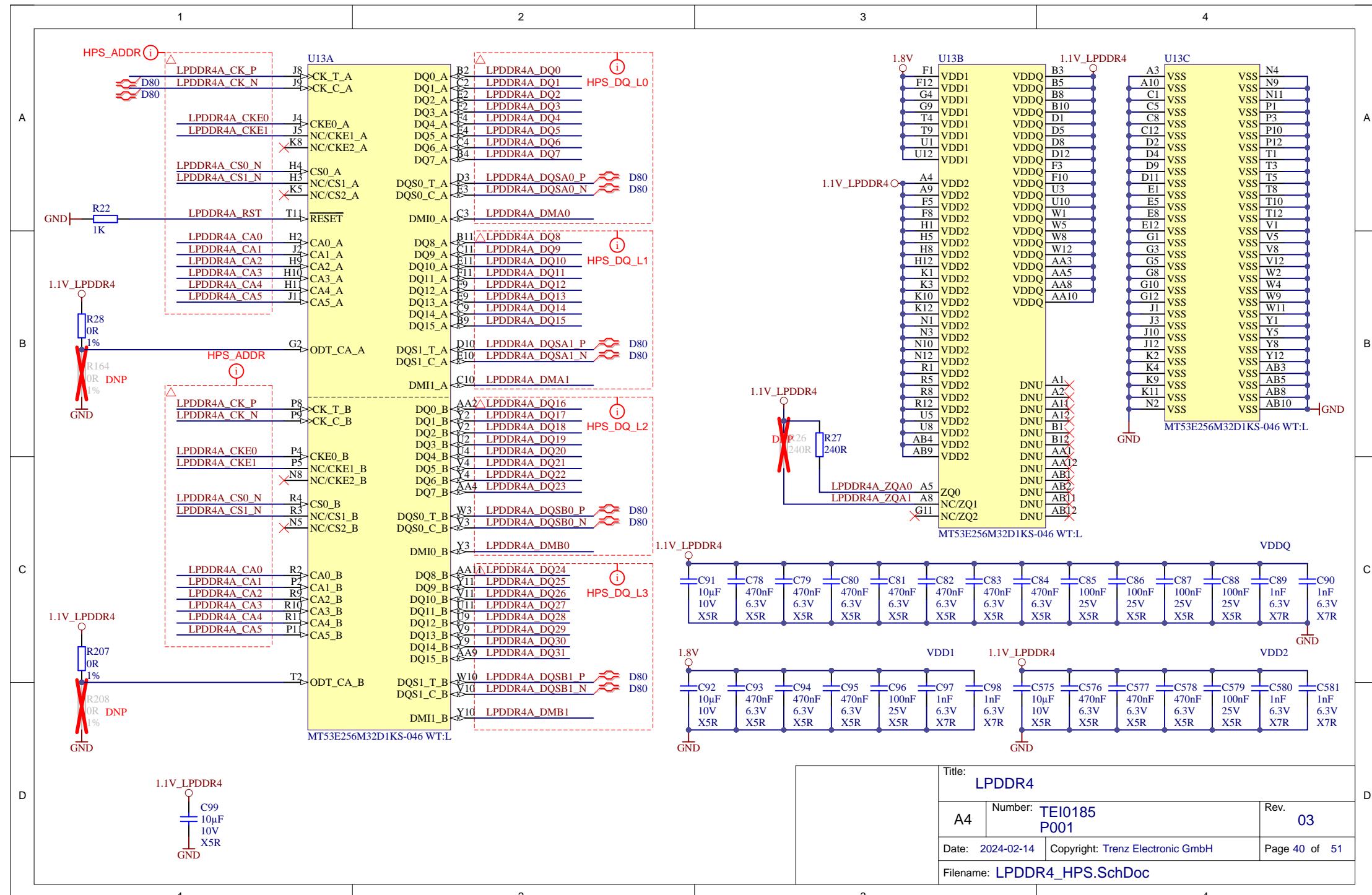


		Title: FTDI_JTAG	
A4	Number: TEI0185 P001		Rev. 03
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Filename: FTDI_JTAG.SchDoc			









1

2

3

4

A

A

B

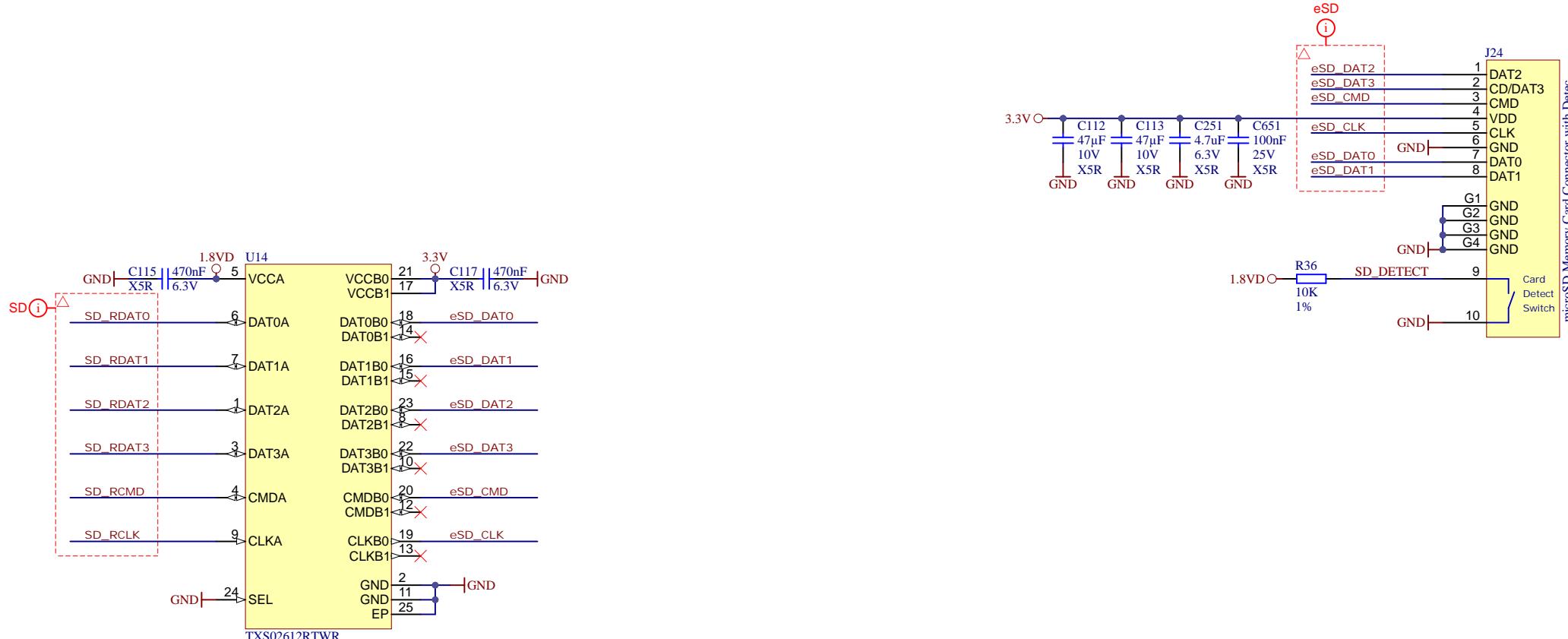
B

C

C

D

D



		Title: SD	
A4	Number: TEI0185 P001	Rev. 03	
Date: 2024-02-14	Copyright: Trenz Electronic GmbH	Page 41 of 51	
Filename: SD.schdoc			

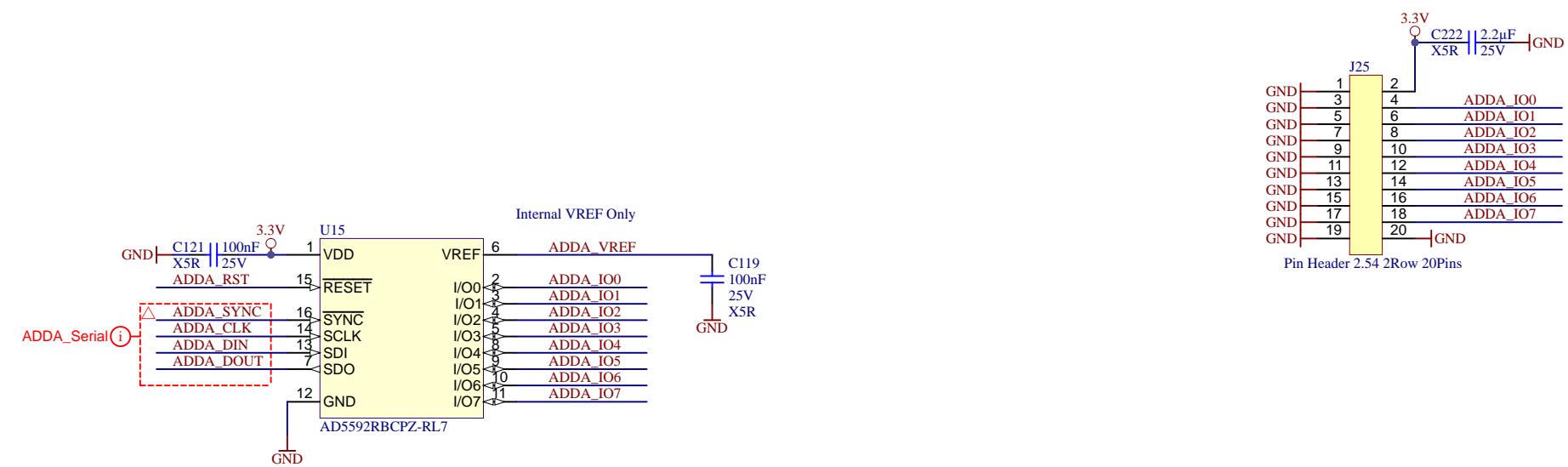
1

2

3

4

A



B

C

D

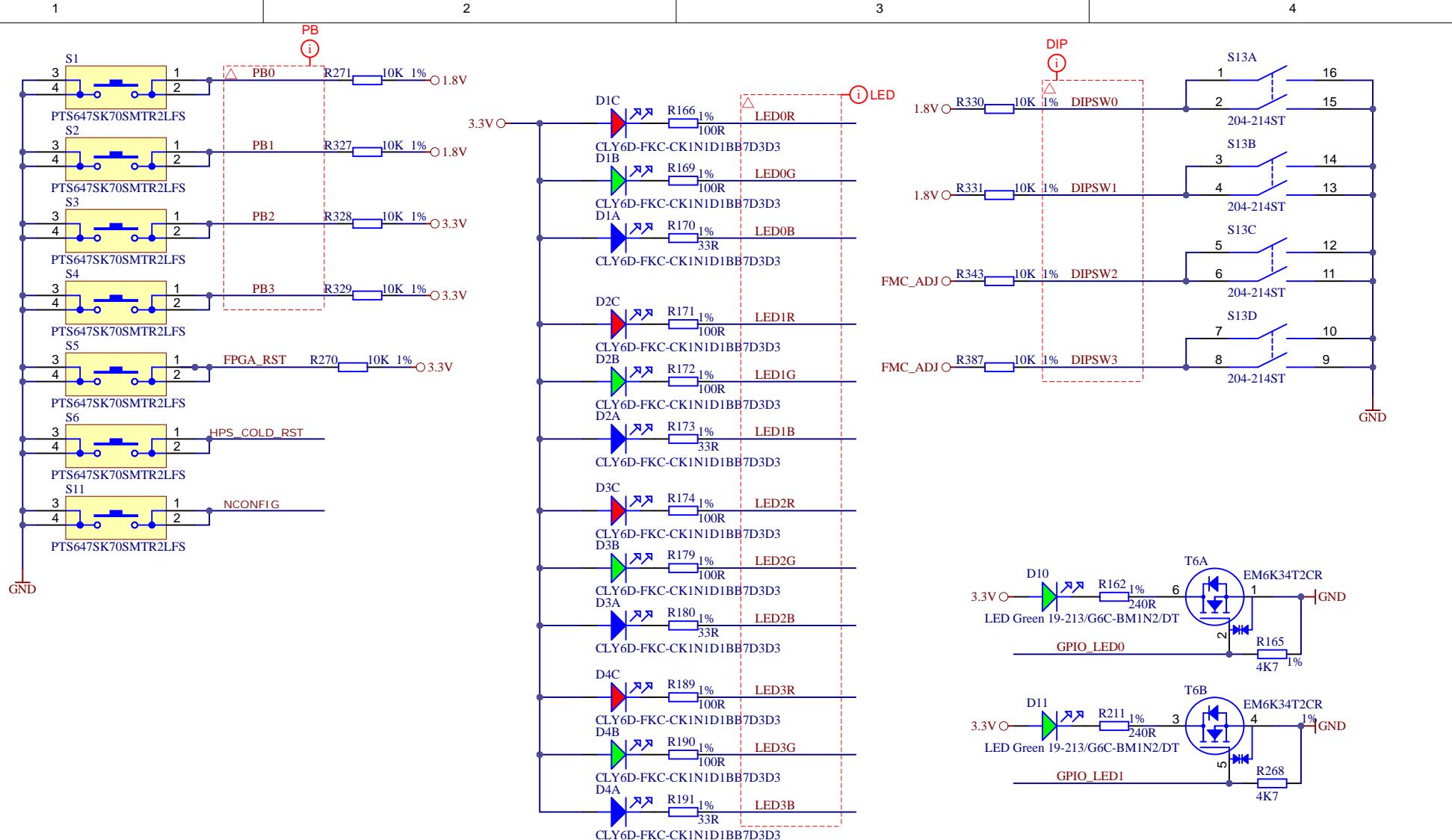
A

B

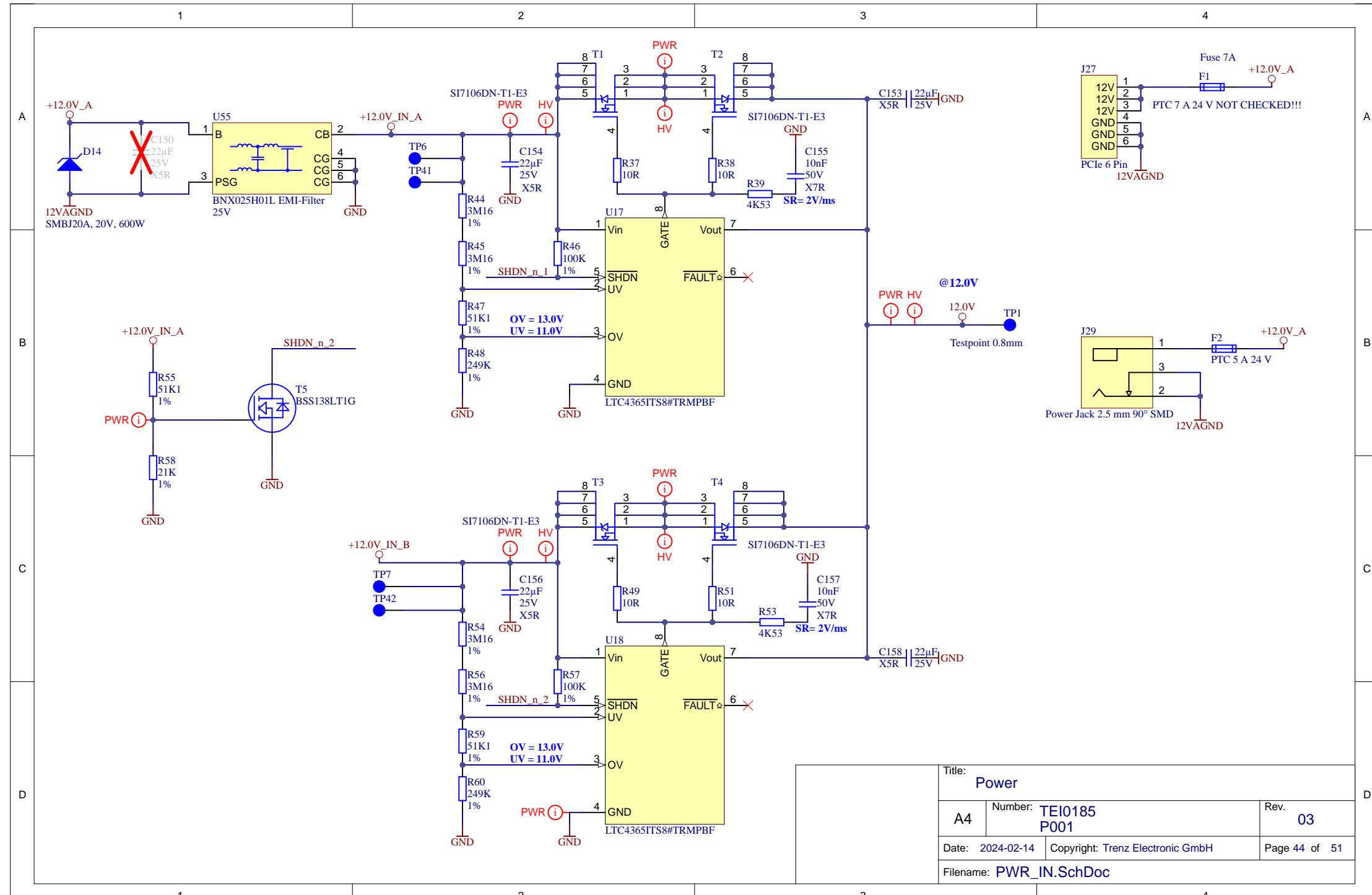
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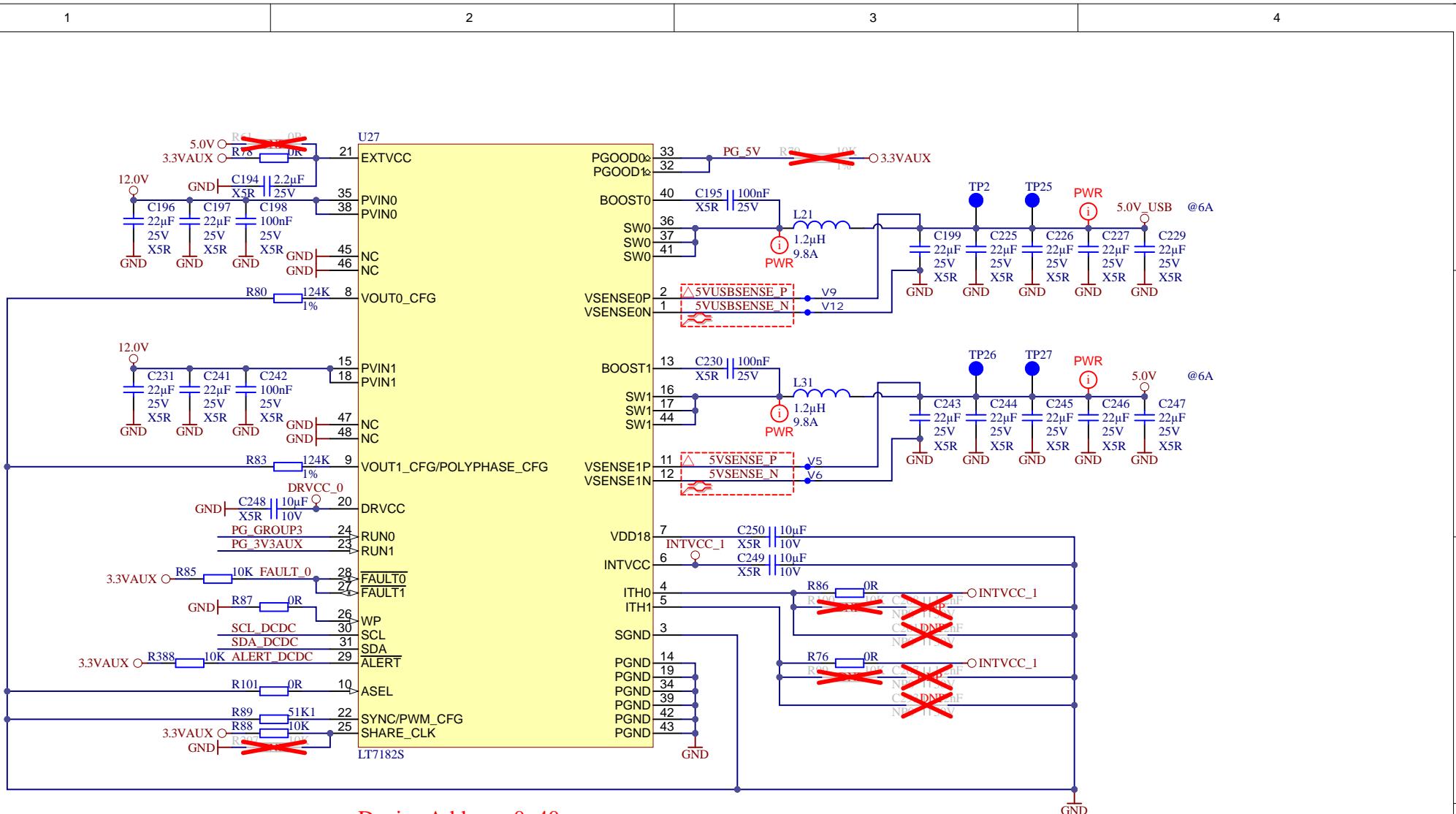
D

		Title: ADC - DAC	
A4	Number: TEI0185 P001		Rev. 03
Date: 2024-02-14		Copyright: Trenz Electronic GmbH	Page 42 of 51
Filename: ADC.SchDoc			



Title: <b>Misc</b>		
A4	Number: <b>TEI0185 P001</b>	Rev. <b>03</b>
Date: <b>2024-02-14</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>43</b> of <b>51</b>
Filename: <b>MISC.SchDoc</b>		





**Device Address:** 0x40  
**PWM Frequency:** 2MHz  
**PWM Mode:** Forced Continuous Mode  
**PWM Phase:** 0°/180°

Title: Power	
A4	Number: TEI0185 P001
Rev. 03	
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Filename: PWR_1.SchDoc	

A

B

C

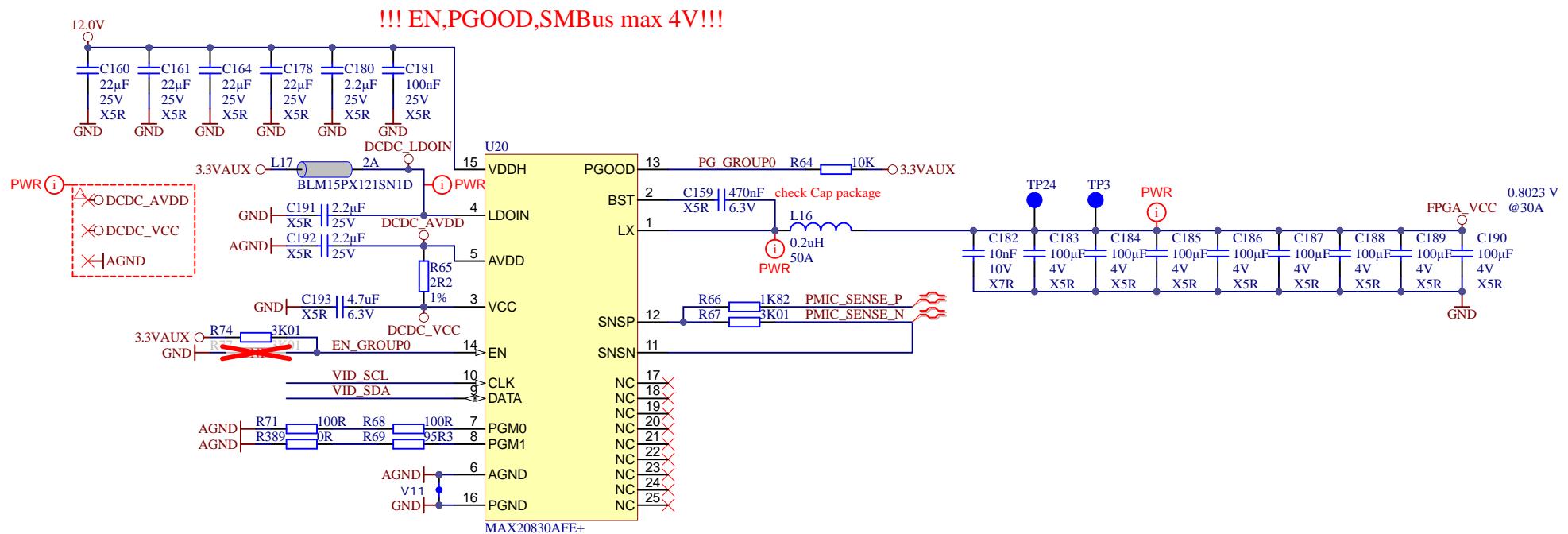
D

A

B

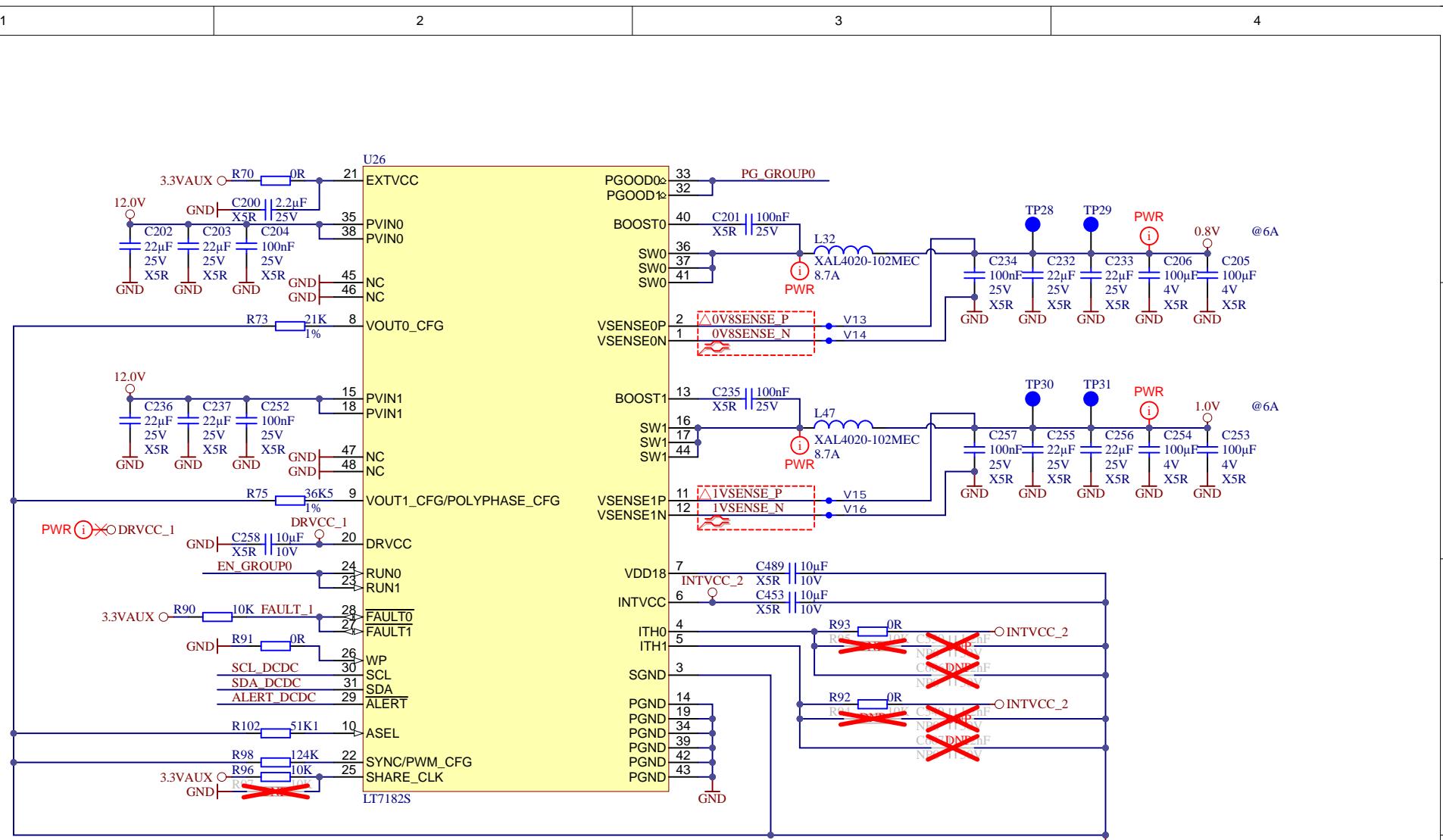
C

D



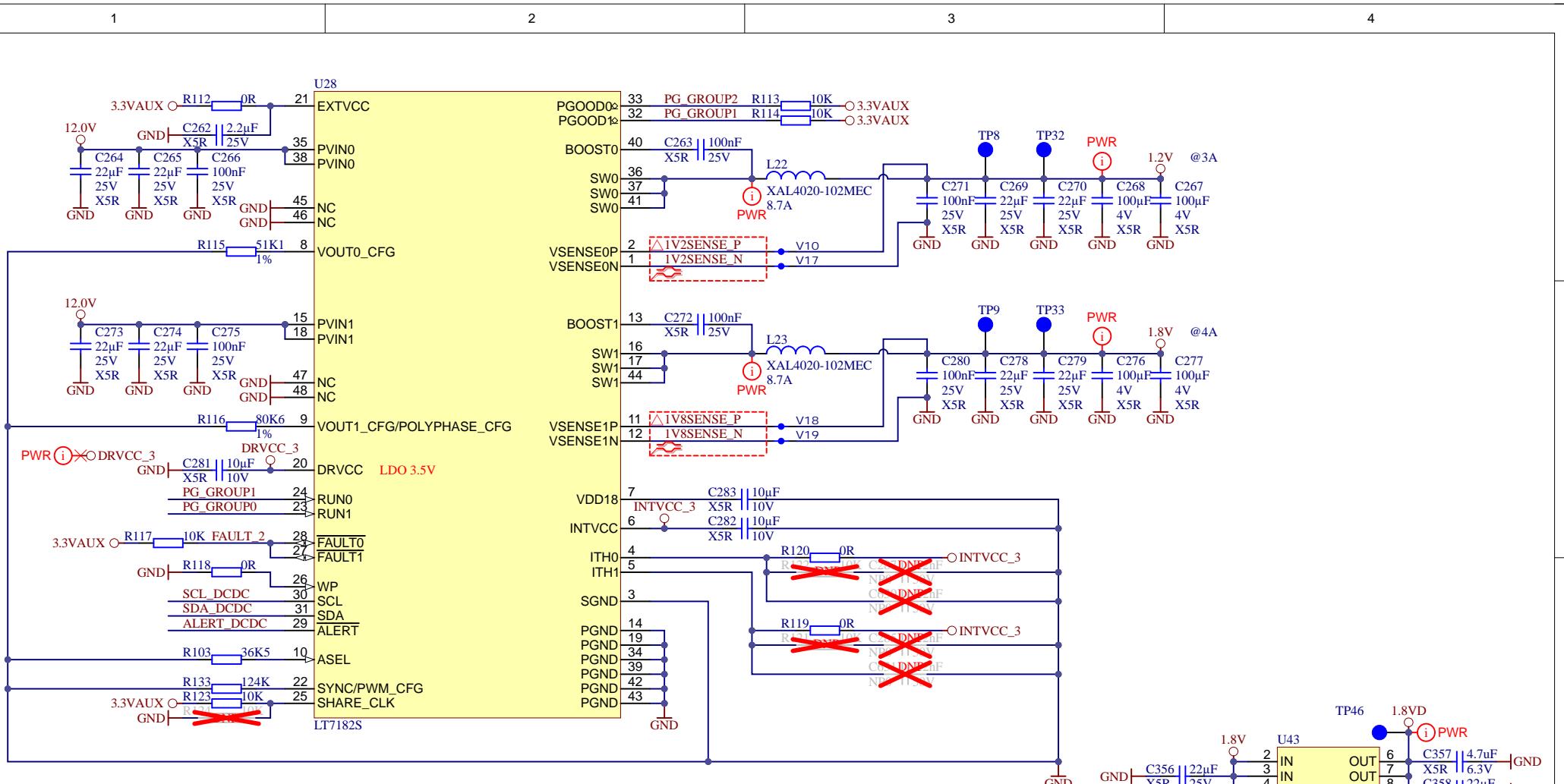
!!! EN,PGOOD,SMBus max 4V!!!  
 I2C ADDRESS: 0X31h  
 POCP=38A  
 FSW=500kHz  
 Scenario A

		Title: Power	
A4	Number: TEI0185 P001		Rev. 03
Date: 2024-02-14	Copyright: Trenz Electronic GmbH		Page 46 of 51
Filename: PWR_2.SchDoc			

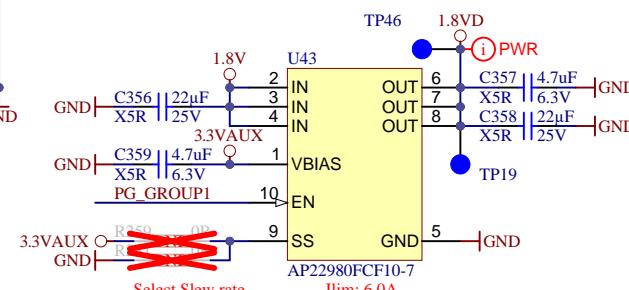


Device Address: 0x49  
PWM Frequency: 500kHz  
PWM Mode: Forced Continuous Mode  
PWM Phase: 0°/180°

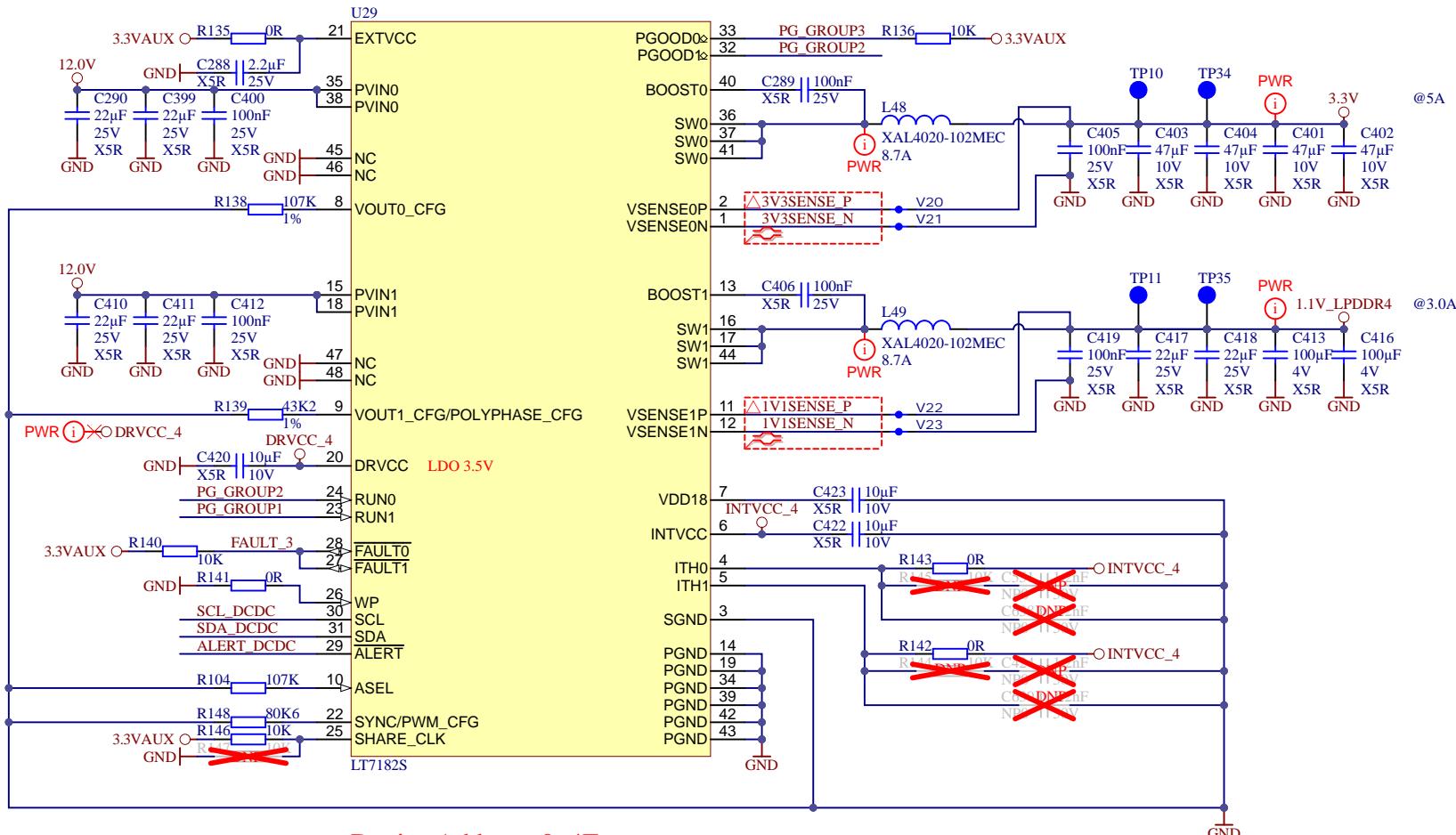
	Title: <b>Power</b>		
A4	Number: TEI0185 P001	Rev. 03	
Date: 2024-02-14	Copyright: Trenz Electronic GmbH		Page 47 of 51
Filename: PWR_3.SchDoc			



Device Address: 0x47  
 PWM Frequency: 500kHz  
 PWM Mode: Forced Continuous Mode  
 PWM Phase: 0°/180°



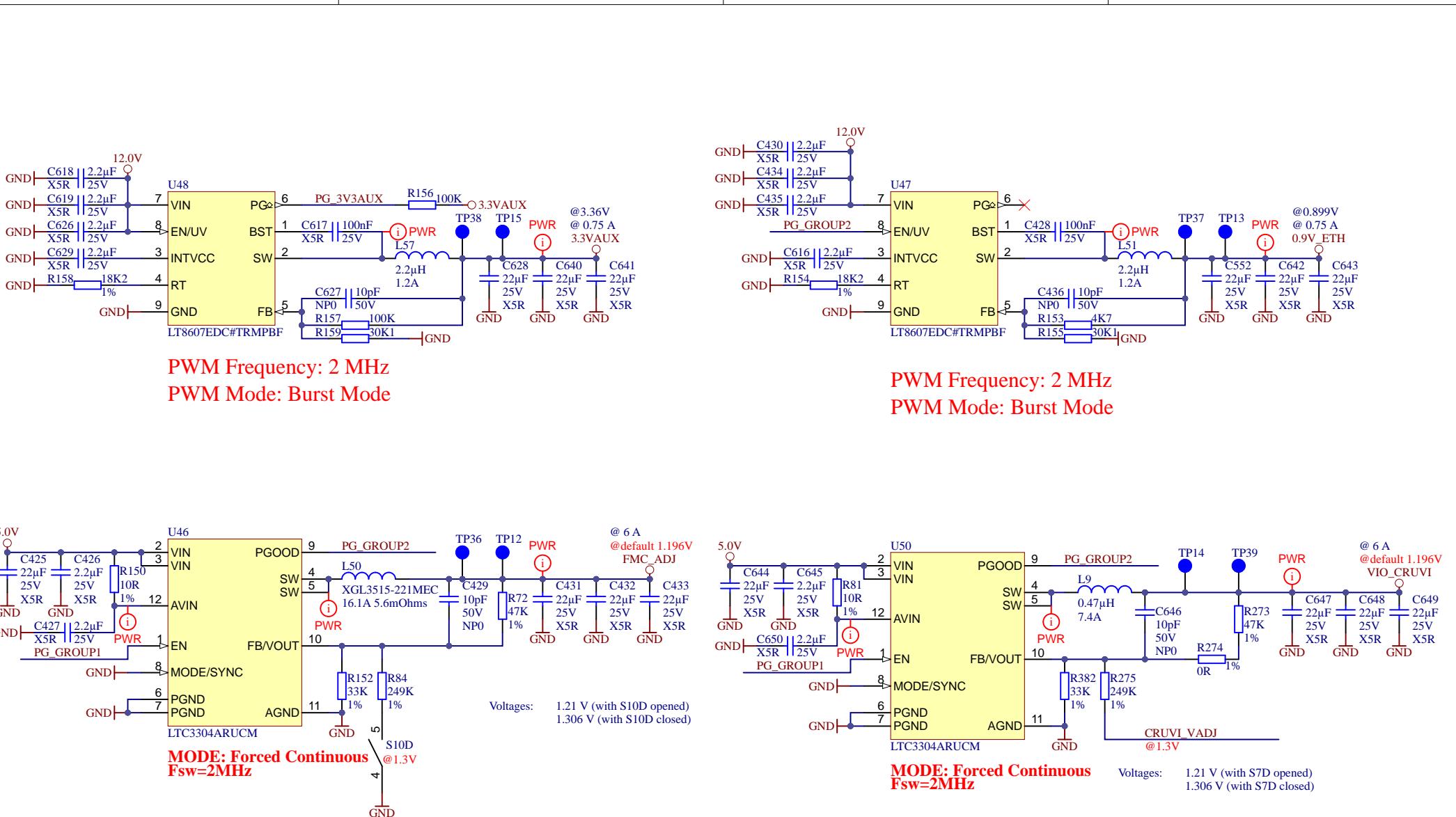
Title: Power		
A4	Number: TEI0185 P001	Rev. 03
Date: 2024-02-14	Copyright: Trenz Electronic GmbH	Page 48 of 51
	Filename: PWR_4.SchDoc	



Device Address: 0x4E  
 PWM Frequency: 1MHz  
 PWM Mode: Forced Continuous Mode  
 PWM Phase: 0°/180°

Title: Power		
A4	Number: TEI0185 P001	Rev. 03
Date: 2024-02-14 Copyright: Trenz Electronic GmbH		Page 49 of 51
Filename: PWR_5.SchDoc		

1 2 3 4



Title: Power		
A4	Number: TEI0185 P001	Rev. 03
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1 2 3 4