


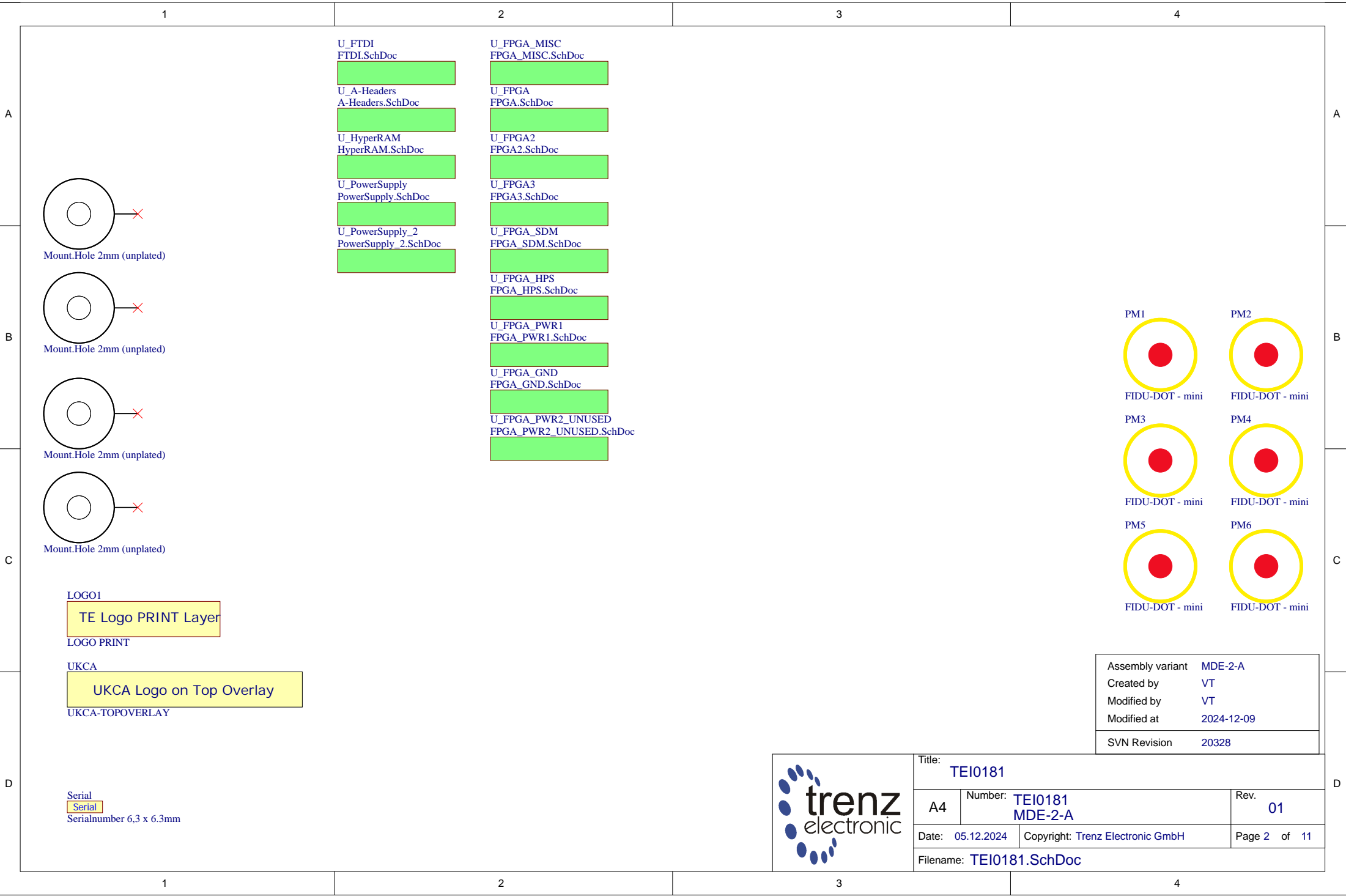
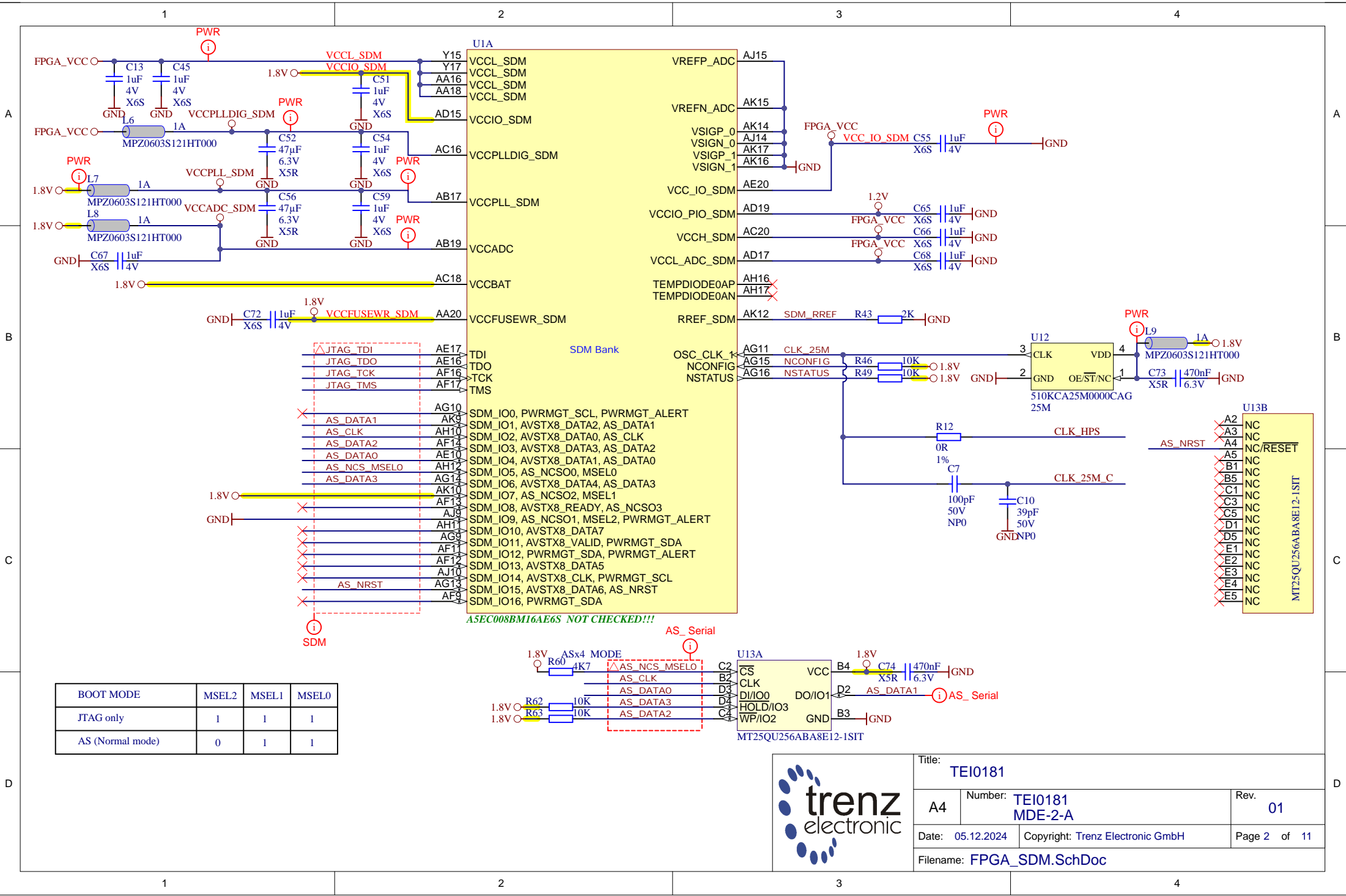


	1	2	3	4													
A	<table><tr><td>REV</td><td>Description</td><td></td></tr><tr><td>-01</td><td>Initial revision</td><td>VT</td></tr><tr><td></td><td></td><td></td></tr></table>				REV	Description		-01	Initial revision	VT							
REV	Description																
-01	Initial revision	VT															
B																	
C																	
D	<table><tr><td rowspan="4"></td><td colspan="3">Title: Revision Changes</td></tr><tr><td>A4</td><td>Number: TEI0181 MDE-2-A</td><td>Rev. 01</td></tr><tr><td>Date: 2024-11-19</td><td>Copyright: Trenz Electronic GmbH</td><td>Page1 of 11</td></tr><tr><td colspan="3">Filename: Revision_Changes.SchDoc</td></tr></table>					Title: Revision Changes			A4	Number: TEI0181 MDE-2-A	Rev. 01	Date: 2024-11-19	Copyright: Trenz Electronic GmbH	Page1 of 11	Filename: Revision_Changes.SchDoc		
	Title: Revision Changes																
	A4	Number: TEI0181 MDE-2-A	Rev. 01														
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	1	2	3	4													





BOOT MODE	MSEL2	MSEL1	MSEL0
JTAG only	1	1	1
AS (Normal mode)	0	1	1

Title:TEI0181

A4

Number:TEI0181
MDE-2-A

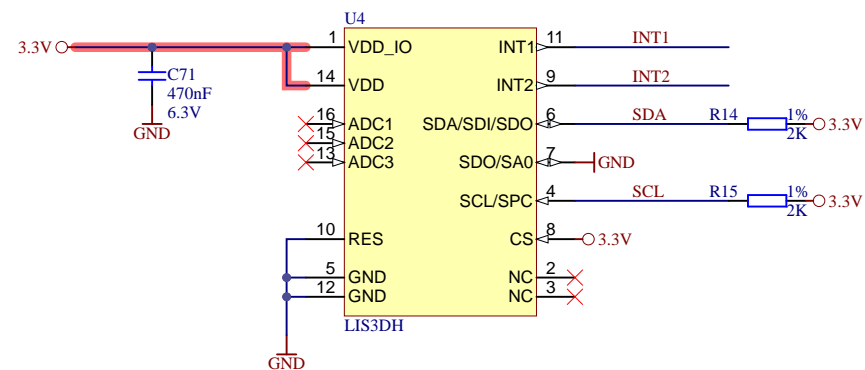
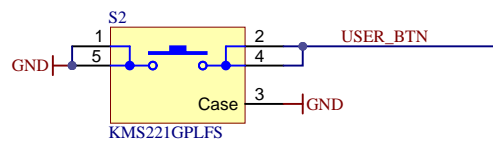
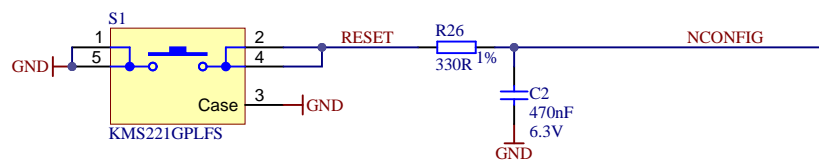
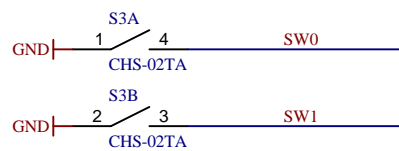
Rev.01


Date:05.12.2024

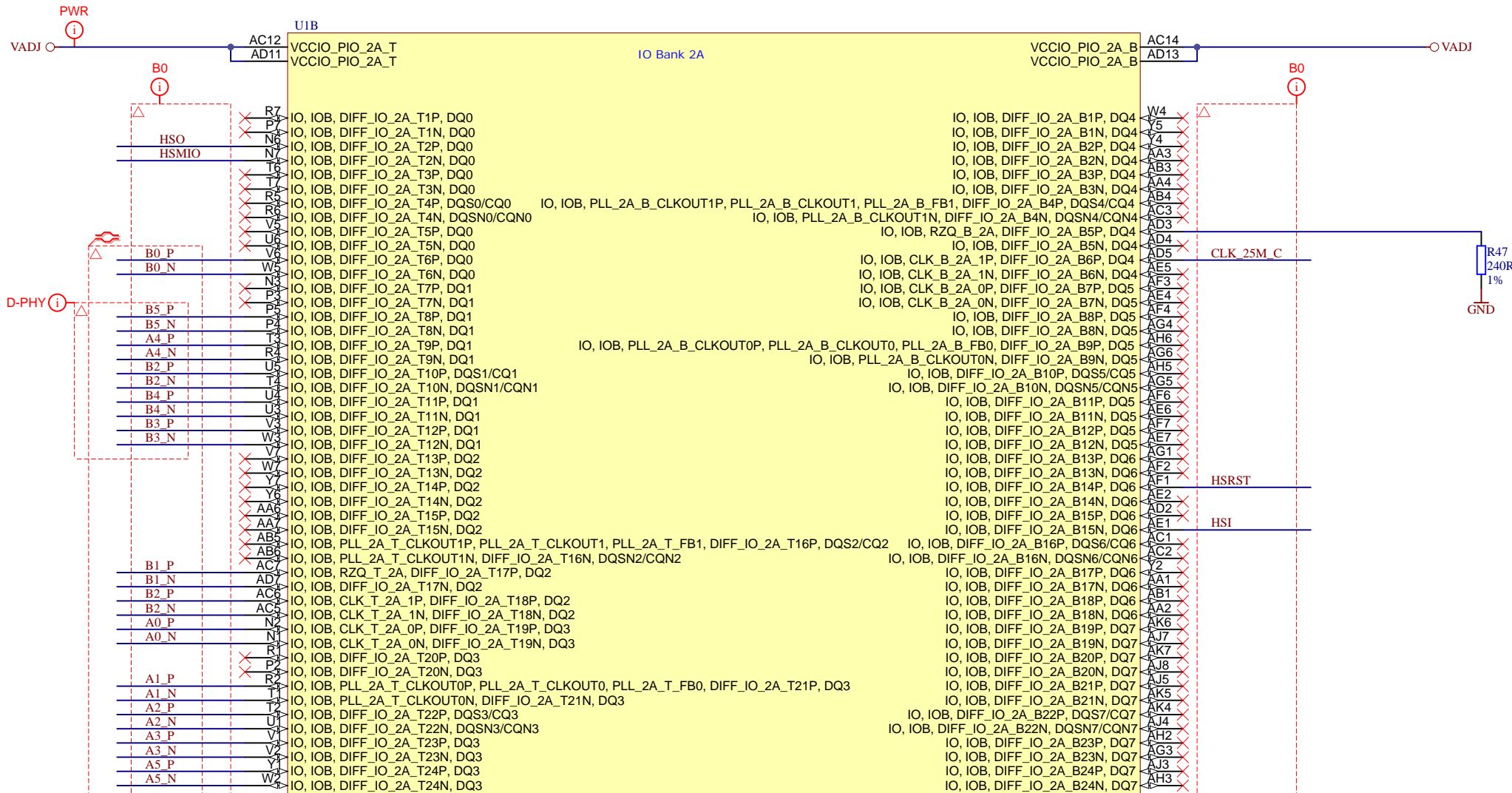
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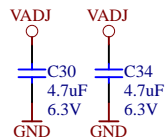
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	Title: TE0181		
	A4	Number: TEI0181 MDE-2-A	Rev. 01
	Date: 05.12.2024	Copyright: Trenz Electronic GmbH	Page 4 of 11
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A5EC008BM16AE6S NOT CHECKED!!!



		Title: FPGA	
		A4	Number: TEI0181 MDE-2-A
Date: 05.12.2024		Copyright: Trenz Electronic GmbH	
Filename: FPGA.SchDoc		Page 5 of 11	

1

2

3

4

UIC

1.2V

G12
H11VCCIO_PIO_3A_T
VCCIO_PIO_3A_T

IO Bank 3A

VCCIO_PIO_3A_B
VCCIO_PIO_3A_B

PWR

1.2V

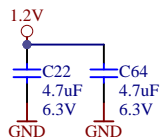
3A

M5 IO, HPS_DDR, IOB, DIFF_IO_3A_T1P, DQ8
N5 IO, HPS_DDR, IOB, DIFF_IO_3A_T1N, DQ8
P5 IO, HPS_DDR, IOB, DIFF_IO_3A_T2P, DQ8
R5 IO, HPS_DDR, IOB, DIFF_IO_3A_T2N, DQ8
S5 IO, HPS_DDR, IOB, DIFF_IO_3A_T3P, DQ8, AVST_READY
T5 IO, HPS_DDR, IOB, DIFF_IO_3A_T3N, DQ8
U5 IO, HPS_DDR, IOB, DIFF_IO_3A_T4P, DQS8/CQ8 IO, HPS_DDR, IOB, PLL_3A_B_CLKOUT1P, PLL_3A_B_CLKOUT1, PLL_3A_B_CLKOUT1N, DIFF_IO_3A_B4N, DQSN12/CQ12
V5 IO, HPS_DDR, IOB, DIFF_IO_3A_T4N, DQS8/CQ8
W5 IO, HPS_DDR, IOB, DIFF_IO_3A_T5P, DQ8
X5 IO, HPS_DDR, IOB, DIFF_IO_3A_T5N, DQ8
Y5 IO, HPS_DDR, IOB, DIFF_IO_3A_T6P, DQ8
Z5 IO, HPS_DDR, IOB, DIFF_IO_3A_T6N, DQ8
[A5] IO, HPS_DDR, IOB, DIFF_IO_3A_T7P, DQ9, AVST_DATA9
[B5] IO, HPS_DDR, IOB, DIFF_IO_3A_T7N, DQ9, AVST_DATA10
[C5] IO, HPS_DDR, IOB, DIFF_IO_3A_T8P, DQ9, AVST_VALID
[D5] IO, HPS_DDR, IOB, DIFF_IO_3A_T8N, DQ9, AVST_DATA8
[E5] IO, HPS_DDR, IOB, DIFF_IO_3A_T9P, DQ9, AVST_DATA6 IO, HPS_DDR, IOB, PLL_3A_B_CLKOUT0P, PLL_3A_B_CLKOUT0, PLL_3A_B_CLKOUT0N, DIFF_IO_3A_B9N, DQ13
[F5] IO, HPS_DDR, IOB, DIFF_IO_3A_T9N, DQ9, AVST_DATA7
[G5] IO, HPS_DDR, IOB, DIFF_IO_3A_T10P, DQS9/CQ9, AVST_DATA4
[H5] IO, HPS_DDR, IOB, DIFF_IO_3A_T10N, DQS9/CQ9, AVST_DATA5
[I5] IO, HPS_DDR, IOB, DIFF_IO_3A_T11P, DQ9, AVST_DATA2
[J5] IO, HPS_DDR, IOB, DIFF_IO_3A_T11N, DQ9, AVST_DATA3
[K5] IO, HPS_DDR, IOB, DIFF_IO_3A_T12P, DQ9, AVST_DATA0
[L5] IO, HPS_DDR, IOB, DIFF_IO_3A_T12N, DQ9, AVST_DATA1
[M5] IO, HPS_DDR, IOB, DIFF_IO_3A_T13P, DQ10
[N5] IO, HPS_DDR, IOB, DIFF_IO_3A_T13N, DQ10
[O5] IO, HPS_DDR, IOB, DIFF_IO_3A_T14P, DQ10
[P5] IO, HPS_DDR, IOB, DIFF_IO_3A_T14N, DQ10
[Q5] IO, HPS_DDR, IOB, DIFF_IO_3A_T15P, DQ10
[R5] IO, HPS_DDR, IOB, DIFF_IO_3A_T15N, DQ10
[S5] IO, HPS_DDR, IOB, PLL_3A_T_CLKOUT1P, PLL_3A_T_CLKOUT1, PLL_3A_T_FB1, DIFF_IO_3A_T16P, DQS10/CQ10, HPS_DDR, IOB, DIFF_IO_3A_B16P, DQS14/CQ14
[T5] IO, HPS_DDR, IOB, PLL_3A_T_CLKOUT1N, DIFF_IO_3A_T16N, DQS10/CQ10
[U5] IO, HPS_DDR, IOB, RZQ_T_3A, DIFF_IO_3A_T17P, DQ10
[V5] IO, HPS_DDR, IOB, DIFF_IO_3A_T17N, DQ10
[W5] IO, HPS_DDR, IOB, CLK_T_3A_1P, DIFF_IO_3A_T18P, DQ10
[X5] IO, HPS_DDR, IOB, CLK_T_3A_1N, DIFF_IO_3A_T18N, DQ10
[Y5] IO, HPS_DDR, IOB, CLK_T_3A_0P, DIFF_IO_3A_T19P, DQ11
[Z5] IO, HPS_DDR, IOB, CLK_T_3A_0N, DIFF_IO_3A_T19N, DQ11
[A6] IO, HPS_DDR, IOB, DIFF_IO_3A_T20P, DQ11
[B6] IO, HPS_DDR, IOB, DIFF_IO_3A_T20N, DQ11
[C6] IO, HPS_DDR, IOB, PLL_3A_T_CLKOUT0P, PLL_3A_T_CLKOUT0, PLL_3A_T_FB0, DIFF_IO_3A_T21P, DQ11
[D6] IO, HPS_DDR, IOB, PLL_3A_T_CLKOUT0N, DIFF_IO_3A_T21N, DQ11
[E6] IO, HPS_DDR, IOB, DIFF_IO_3A_T22P, DQS11/CQ11, AVST_DATA15
[F6] IO, HPS_DDR, IOB, DIFF_IO_3A_T22N, DQS11/CQ11, AVST_CLK
[G6] IO, HPS_DDR, IOB, DIFF_IO_3A_T23P, DQ11, AVST_DATA13
[H6] IO, HPS_DDR, IOB, DIFF_IO_3A_T23N, DQ11, AVST_DATA14
[I6] IO, HPS_DDR, IOB, DIFF_IO_3A_T24P, DQ11, AVST_DATA11
[J6] IO, HPS_DDR, IOB, DIFF_IO_3A_T24N, DQ11, AVST_DATA12

A5EC008BM16AE6S NOT CHECKED!!!

D7 IO, HPS_DDR, IOB, DIFF_IO_3A_B1P, DQ12
D8 IO, HPS_DDR, IOB, DIFF_IO_3A_B1N, DQ12
E7 IO, HPS_DDR, IOB, DIFF_IO_3A_B2P, DQ12
E8 IO, HPS_DDR, IOB, DIFF_IO_3A_B2N, DQ12
E9 IO, HPS_DDR, IOB, DIFF_IO_3A_B3P, DQ12
F9 IO, HPS_DDR, IOB, DIFF_IO_3A_B3N, DQ12
F10 IO, HPS_DDR, IOB, DIFF_IO_3A_B4P, DQS12/CQ12
F11 IO, HPS_DDR, IOB, DIFF_IO_3A_B4N, DQS12/CQ12
F14 IO, HPS_DDR, IOB, RZQ_B_3A, DIFF_IO_3A_B5P, DQ12
F15 IO, HPS_DDR, IOB, DIFF_IO_3A_B5N, DQ12
F13 IO, HPS_DDR, IOB, CLK_B_3A_1P, DIFF_IO_3A_B6P, DQ12
F12 IO, HPS_DDR, IOB, CLK_B_3A_1N, DIFF_IO_3A_B6N, DQ12
A7 IO, HPS_DDR, IOB, CLK_B_3A_0P, DIFF_IO_3A_B7P, DQ13
A6 IO, HPS_DDR, IOB, CLK_B_3A_0N, DIFF_IO_3A_B7N, DQ13
A7 IO, HPS_DDR, IOB, DIFF_IO_3A_B8P, DQ13
A6 IO, HPS_DDR, IOB, DIFF_IO_3A_B8N, DQ13
A4 IO, HPS_DDR, IOB, PLL_3A_B_FB0, DIFF_IO_3A_B9P, DQ13
A4 IO, HPS_DDR, IOB, PLL_3A_B_CLKOUT0N, DIFF_IO_3A_B9N, DQ13
A6 IO, HPS_DDR, IOB, DIFF_IO_3A_B10P, DQS13/CQ13
A5 IO, HPS_DDR, IOB, DIFF_IO_3A_B10N, DQS13/CQ13
A3 IO, HPS_DDR, IOB, DIFF_IO_3A_B11P, DQ13
A3 IO, HPS_DDR, IOB, DIFF_IO_3A_B11N, DQ13
A2 IO, HPS_DDR, IOB, DIFF_IO_3A_B12P, DQ13
A2 IO, HPS_DDR, IOB, DIFF_IO_3A_B12N, DQ13
C14 IO, HPS_DDR, IOB, DIFF_IO_3A_B13P, DQ14
C13 IO, HPS_DDR, IOB, DIFF_IO_3A_B13N, DQ14
C15 IO, HPS_DDR, IOB, DIFF_IO_3A_B14P, DQ14
C15 IO, HPS_DDR, IOB, DIFF_IO_3A_B14N, DQ14
C13 IO, HPS_DDR, IOB, DIFF_IO_3A_B15P, DQ14
C12 IO, HPS_DDR, IOB, DIFF_IO_3A_B15N, DQ14
C12 IO, HPS_DDR, IOB, DIFF_IO_3A_B16P, DQS14/CQ14
C11 IO, HPS_DDR, IOB, DIFF_IO_3A_B16N, DQS14/CQ14
C8 IO, HPS_DDR, IOB, DIFF_IO_3A_B17P, DQ14
C9 IO, HPS_DDR, IOB, DIFF_IO_3A_B17N, DQ14
D10 IO, HPS_DDR, IOB, DIFF_IO_3A_B18P, DQ14
C10 IO, HPS_DDR, IOB, DIFF_IO_3A_B18N, DQ14
B13 IO, HPS_DDR, IOB, DIFF_IO_3A_B19P, DQ15
B14 IO, HPS_DDR, IOB, DIFF_IO_3A_B19N, DQ15
A14 IO, HPS_DDR, IOB, DIFF_IO_3A_B20P, DQ15
A14 IO, HPS_DDR, IOB, DIFF_IO_3A_B20N, DQ15
B11 IO, HPS_DDR, IOB, DIFF_IO_3A_B21P, DQ15
A12 IO, HPS_DDR, IOB, DIFF_IO_3A_B21N, DQ15
B10 IO, HPS_DDR, IOB, DIFF_IO_3A_B22P, DQS15/CQ15
A11 IO, HPS_DDR, IOB, DIFF_IO_3A_B22N, DQS15/CQ15
A8 IO, HPS_DDR, IOB, DIFF_IO_3A_B23P, DQ15
A8 IO, HPS_DDR, IOB, DIFF_IO_3A_B23N, DQ15
A9 IO, HPS_DDR, IOB, DIFF_IO_3A_B24P, DQ15
A9 IO, HPS_DDR, IOB, DIFF_IO_3A_B24N, DQ15

CLK
CS
HRESET
CLK_25M_C
DQ3
DQ7
DQ5
DQ2
RWDS
DQ0
DQ6
DQ1
DQ4
SW1
SW0
USER_BTN

R52
240R
1%
GND

Title:

FPGA

A4

Number:

TEI0181
MDE-2-A

Rev.

01

Date: 06.12.2024

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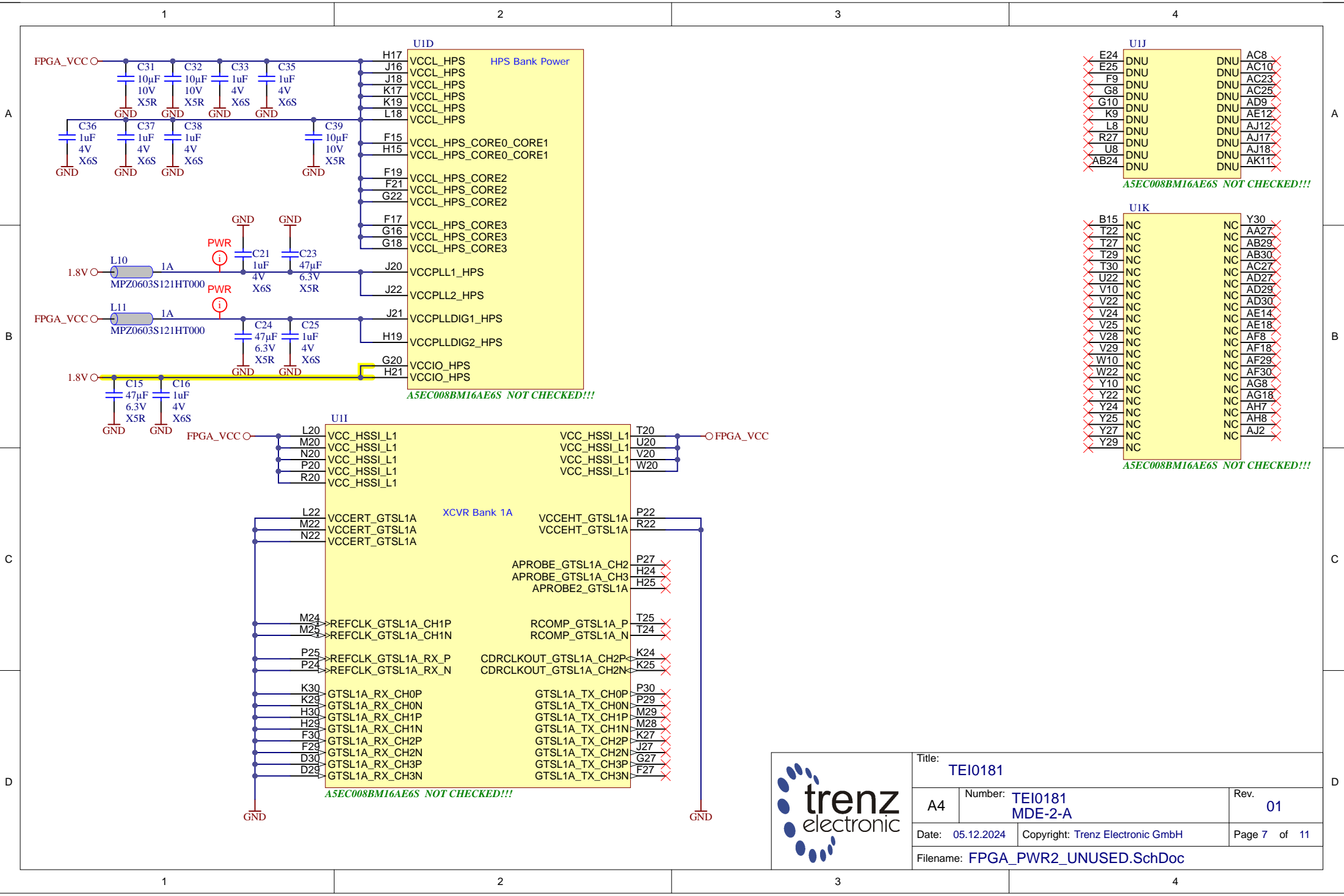
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1

2

3

4



A

A

B

B

C

C

D

D

UIE

B29	HPS_IOA_1, GPIO0_IO0, SPIM0_SS1_N, SPIS0_CLK, UART0_CTS_N, NAND_ADQ0, SDMMC_DATA0, USB0_CLK, EMAC0_PPS0, TRACE_D10	HPS Bank IOA
A27	HPS_IOA_2, GPIO0_IO1, SPIM1_SS1_N, SPIS0_MOSI, UART0_RTS_N, NAND_ADQ1, SDMMC_DATA1, USB0_STP, EMAC0_PPSTRIG0, TRACE_D9	
C27	HPS_IOA_3, GPIO0_IO2, SPIS0_SS0_N, UART0_TX, I2C1_SDA, NAND_WE_N, SDMMC_CLK, USB0_DIR, EMAC1_PPS1, TRACE_D8	
F24	HPS_IOA_4, GPIO0_IO3, SPIS0_MISO, UART0_RX, I2C1_SCL, NAND_RE_N, USB0_DATA0, EMAC1_PPSTRIG1, TRACE_D7	
B28	HPS_IOA_5, GPIO0_IO4, SPIM0_CLK, UART1_CTS_N, I2C0_SDA, NAND_WP_N, SDMMC_WRITE_PROTECT, USB0_DATA1, EMAC2_PPS2, TRACE_D6	
F23	HPS_IOA_6, GPIO0_IO5, SPIM0_MOSI, UART1_RTS_N, I2C0_SCL, NAND_ADQ2, SDMMC_DATA2, USB0_NXT, EMAC2_PPSTRIG2, TRACE_D5	
D27	HPS_IOA_7, GPIO0_IO6, SPIM0_MISO, MDIO2_MDIO, UART1_TX, I2C_EMAC2_SDA, NAND_ADQ3, SDMMC_DATA3, USB0_DATA2, TRACE_D4	
E27	HPS_IOA_8, GPIO0_IO7, SPIM0_SS0_N, MDIO2_MDC, UART1_RX, I2C_EMAC2_SCL, NAND_CLE, SDMMC_CMD, USB0_DATA3, TRACE_D15	
C26	HPS_IOA_9, GPIO0_IO8, SPIM1_CLK, SPIS1_CLK, MDIO1_MDIO, I2C_EMAC1_SDA, NAND_ADQ4, SDMMC_DATA4, USB0_DATA4, I3C1_SDA, TRACE_D14	
D22	HPS_IOA_10, GPIO0_IO9, SPIM1_MOSI, SPIS1_MOSI, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ5, SDMMC_DATA5, USB0_DATA5, I3C1_SCL, TRACE_D13	
A23	HPS_IOA_11, GPIO0_IO10, SPIM1_MISO, SPIS1_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, USB0_DATA6, I3C0_SDA, TRACE_D12	
A26	HPS_IOA_12, GPIO0_IO11, SPIM1_SS0_N, SPIS1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, USB0_DATA7, I3C0_SCL, TRACE_D11	
D25	HPS_IOA_13, GPIO0_IO12, NAND_ALE, SDMMC_PU_PD_DATA2, USB1_CLK, EMAC0_TX_CLK, TRACE_D10	
B26	HPS_IOA_14, GPIO0_IO13, NAND_RB_N, SDMMC_PWR_ENA, USB1_STP, EMAC0_TX_CTL, TRACE_D9	
B25	HPS_IOA_15, GPIO0_IO14, NAND_CE_N, USB1_DIR, EMAC0_RX_CLK, TRACE_D8	
E17	HPS_IOA_16, GPIO0_IO15, NAND_DQS, SDMMC_DATA_STROBE, USB1_DATA0, EMAC0_RX_CTL, TRACE_D7	
A16	HPS_IOA_17, GPIO0_IO16, I3C1_SDA, NAND_ADQ8, USB1_DATA1, EMAC0_TXD0, TRACE_D6	
E16	HPS_IOA_18, GPIO0_IO17, I3C1_SCL, NAND_ADQ9, USB1_NXT, EMAC0_TXD1, TRACE_D5	
D24	HPS_IOA_19, GPIO0_IO18, I3C0_SDA, NAND_ADQ10, USB1_DATA2, EMAC0_RXD0, TRACE_D4	
E21	HPS_IOA_20, GPIO0_IO19, SPIM1_SS1_N, I3C0_SCL, NAND_ADQ11, USB1_DATA3, EMAC0_RXD1, TRACE_CLK	
B23	HPS_IOA_21, GPIO0_IO20, SPIM1_CLK, SPIS0_CLK, UART0_CTS_N, I2C1_SDA, NAND_ADQ12, USB1_DATA4, EMAC0_TXD2, TRACE_D0	
D21	HPS_IOA_22, GPIO0_IO21, SPIM1_MOSI, SPIS0_MOSI, UART0_RTS_N, I2C1_SCL, NAND_ADQ13, USB1_DATA5, EMAC0_TXD3, TRACE_D1	
B24	HPS_IOA_23, GPIO0_IO22, SPIM1_MISO, SPIS0_SS0_N, UART0_TX, I2C0_SDA, NAND_ADQ14, USB1_DATA6, EMAC0_RXD2, TRACE_D2	
A24	HPS_IOA_24, GPIO0_IO23, SPIM1_SS0_N, SPIS0_MISO, UART0_RX, I2C0_SCL, NAND_ADQ15, USB1_DATA7, EMAC0_RXD3, TRACE_D3	

ASEC008BM16AE6S NOT CHECKED!!!

UIF

D23	HPS_IOB_1, GPIO1_IO0, SPIM1_CLK, UART0_CTS_N, EMAC0_PPS0, NAND_ADQ0, SDMMC_DATA0, EMAC1_TX_CLK, TRACE_D10	HPS Bank IOB
C25	HPS_IOB_2, GPIO1_IO1, SPIM1_MOSI, UART0_RTS_N, EMAC0_PPSTRIG0, NAND_ADQ1, SDMMC_DATA1, EMAC1_TX_CTL, TRACE_D9	
A18	HPS_IOB_3, GPIO1_IO2, SPIM1_MISO, UART0_TX, I2C0_SDA, NAND_WE_N, SDMMC_CLK, EMAC1_RX_CLK, TRACE_D8	
C20	HPS_IOB_4, GPIO1_IO3, SPIM1_SS0_N, UART0_RX, I2C0_SCL, NAND_RE_N, EMAC1_RX_CTL, TRACE_D7	
A17	HPS_IOB_5, GPIO1_IO4, SPIM1_SS1_N, SPIS1_CLK, UART1_CTS_N, EMAC2_PPS2, NAND_WP_N, SDMMC_WRITE_PROTECT, I3C1_SDA, EMAC1_TXD0, TRACE_D6	
C21	HPS_IOB_6, GPIO1_IO5, SPIS1_MOSI, UART1_RTS_N, EMAC2_PPSTRIG2, NAND_ADQ2, SDMMC_DATA2, I3C1_SCL, EMAC1_TXD1, TRACE_D5	
C23	HPS_IOB_7, GPIO1_IO6, SPIS1_SS0_N, UART1_TX, I2C1_SDA, NAND_ADQ3, SDMMC_DATA3, I3C0_SDA, EMAC1_RXD0, TRACE_D4	
E20	HPS_IOB_8, GPIO1_IO7, SPIS1_MISO, UART1_RX, I2C1_SCL, NAND_CLE, SDMMC_CMD, I3C0_SCL, EMAC1_RXD1, TRACE_D15	
C22	HPS_IOB_9, GPIO1_IO8, JTAG_TCK, SPIS0_CLK, MDIO2_MDIO, I2C_EMAC2_SDA, NAND_ADQ4, SDMMC_DATA4, EMAC1_TXD2, TRACE_D14	
D19	HPS_IOB_10, GPIO1_IO9, JTAG_TMS, SPIS0_MOSI, MDIO2_MDC, I2C_EMAC2_SCL, NAND_ADQ5, SDMMC_DATA5, EMAC1_TXD3, TRACE_D13	
B21	HPS_IOB_11, GPIO1_IO10, JTAG_TDO, SPIS0_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, EMAC1_RXD2, TRACE_D12	
A22	HPS_IOB_12, GPIO1_IO11, JTAG_TDI, SPIS0_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, EMAC1_RXD3, TRACE_D11	
B16	HPS_IOB_13, GPIO1_IO12, I2C1_SDA, NAND_ALE, SDMMC_PU_PD_DATA2, EMAC2_TX_CLK, TRACE_D10	
B18	HPS_IOB_14, GPIO1_IO13, I2C1_SCL, NAND_RB_N, SDMMC_PWR_ENA, EMAC2_TX_CTL, TRACE_D9	
E19	HPS_IOB_15, GPIO1_IO14, UART1_TX, NAND_CE_N, I3C1_SDA, EMAC2_RX_CLK, TRACE_D8	
B20	HPS_IOB_16, GPIO1_IO15, UART1_RX, NAND_DQS, SDMMC_DATA_STROBE, I3C1_SCL, EMAC2_RX_CTL, TRACE_D7	
C18	HPS_IOB_17, GPIO1_IO16, UART1_CTS_N, NAND_ADQ8, I3C0_SDA, EMAC2_TXD0, TRACE_D6	
A21	HPS_IOB_18, GPIO1_IO17, SPIM0_SS1_N, UART1_RTS_N, NAND_ADQ9, I3C0_SCL, EMAC2_TXD1, TRACE_D5	
D17	HPS_IOB_19, GPIO1_IO18, SPIM0_MISO, MDIO1_MDIO, I2C_EMAC1_SDA, NAND_ADQ10, EMAC2_RXD0, TRACE_D4	
A19	HPS_IOB_20, GPIO1_IO19, SPIM0_SS0_N, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ11, EMAC2_RXD1, TRACE_CLK	
D18	HPS_IOB_21, GPIO1_IO20, SPIM0_CLK, SPIS1_CLK, I2C_EMAC2_SDA, NAND_ADQ12, EMAC2_TXD2, TRACE_D0	
B19	HPS_IOB_22, GPIO1_IO21, SPIM0_MOSI, SPIS1_MOSI, I2C_EMAC2_SCL, NAND_ADQ13, EMAC2_TXD3, TRACE_D1	
C17	HPS_IOB_23, GPIO1_IO22, SPIM0_MISO, SPIS1_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ14, EMAC2_RXD2, TRACE_D2	
C16	HPS_IOB_24, GPIO1_IO23, SPIM0_SS0_N, SPIS1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ15, EMAC2_RXD3, TRACE_D3	

ASEC008BM16AE6S NOT CHECKED!!!



Title: TE0181		
A4	Number: TEI0181 MDE-2-A	Rev. 01
Date: 05.12.2024	Copyright: Trenz Electronic GmbH	Page 7 of 11
Filename: FPGA_HPS.SchDoc		

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A

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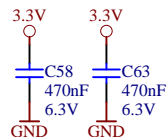
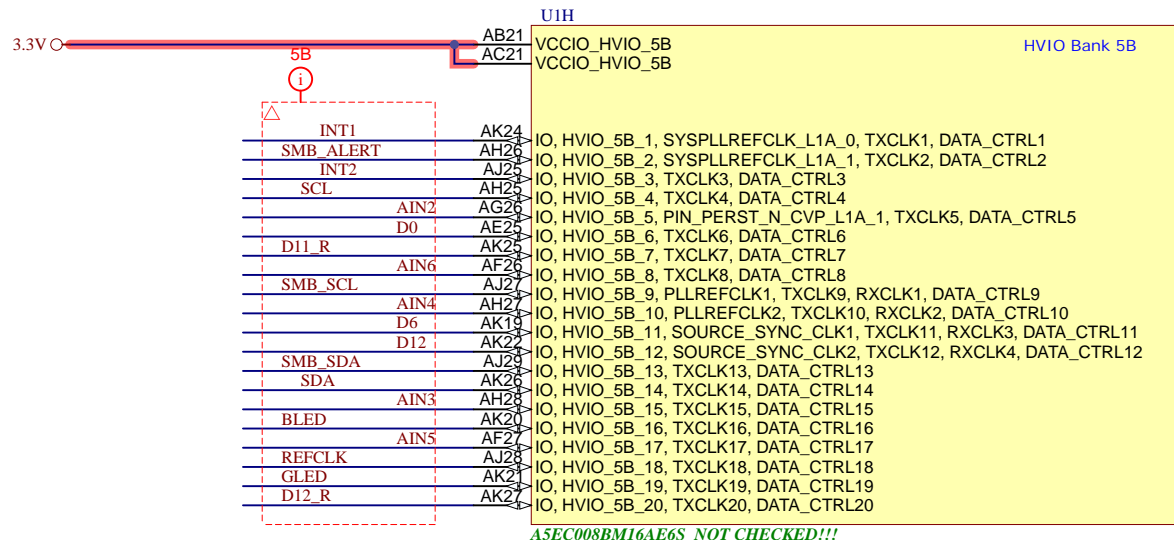
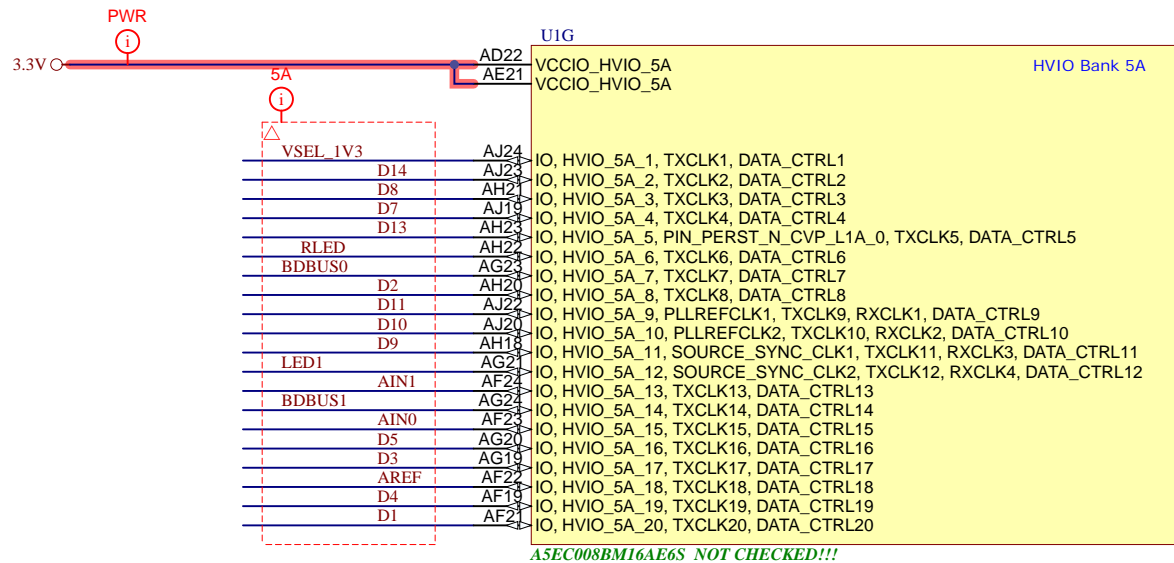
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Date: 05.12.2024	Copyright: Trenz Electronic GmbH		Page 7 of 11
Filename: FPGA3.SchDoc			

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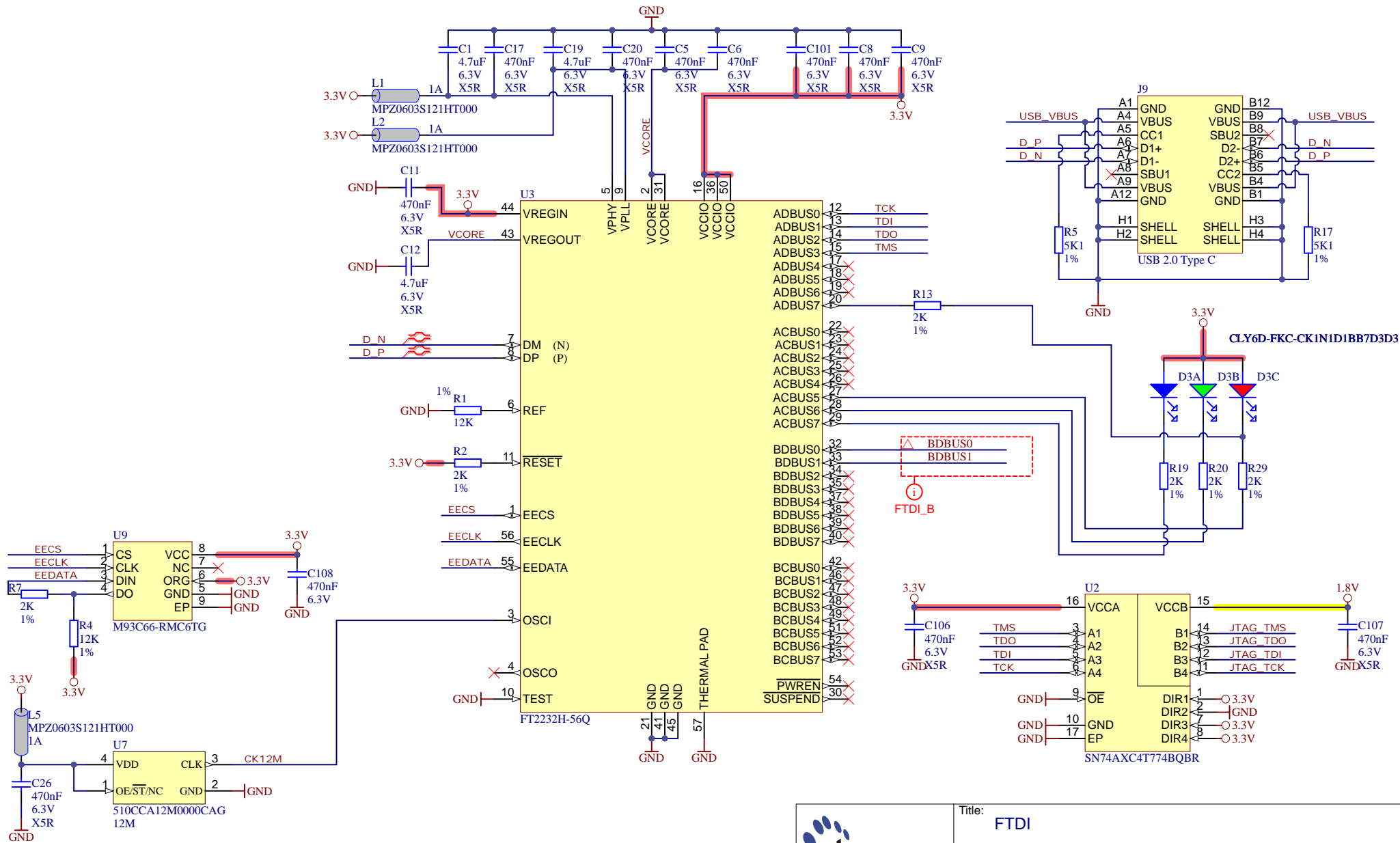
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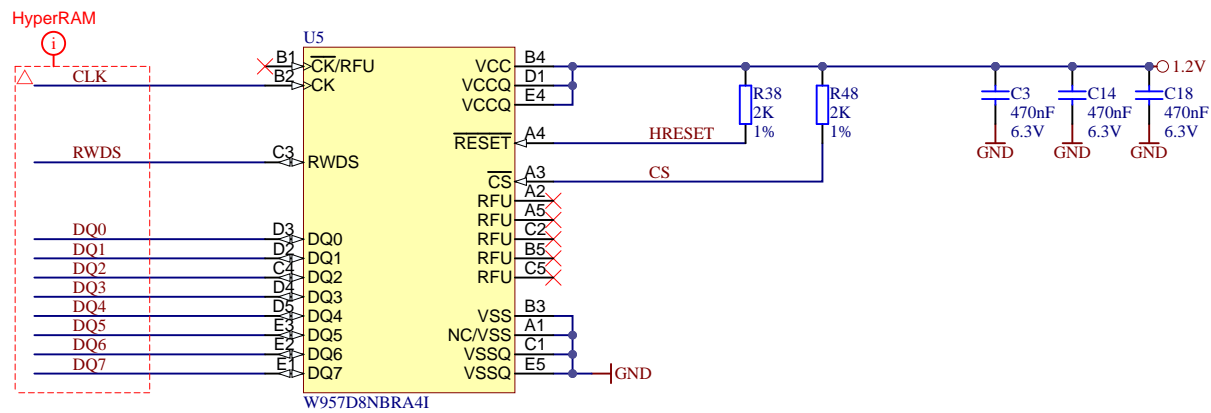
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Date: 05.12.2024	Copyright: Trenz Electronic GmbH	Page 9 of 11
Filename: FTDI.SchDoc		



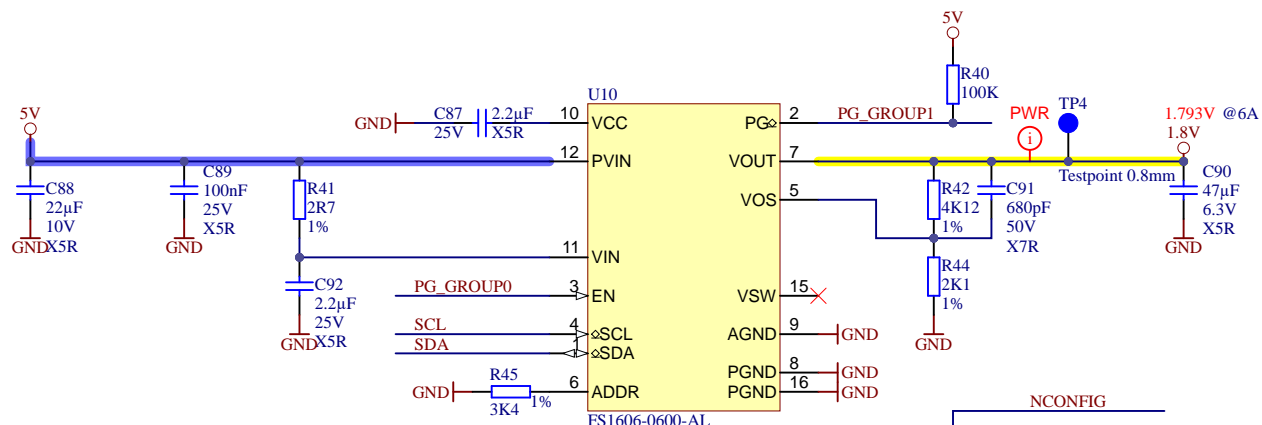
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Date: 05.12.2024		Copyright: Trenz Electronic GmbH	
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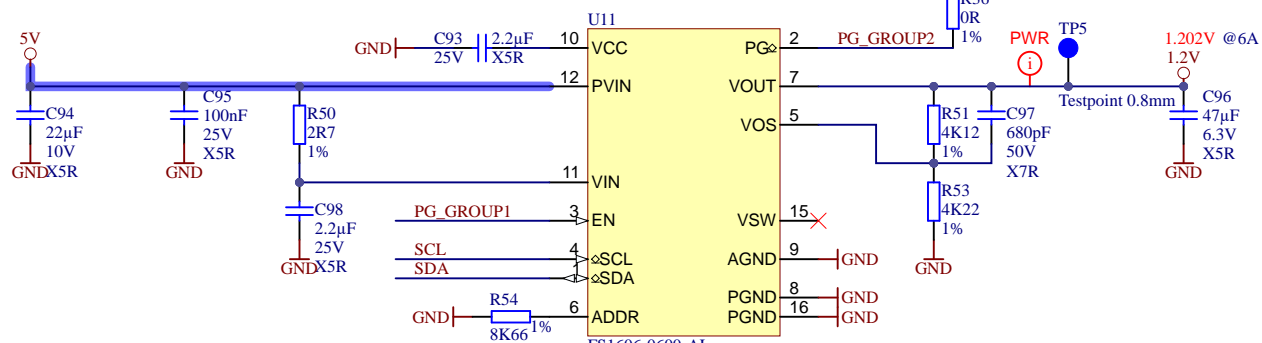
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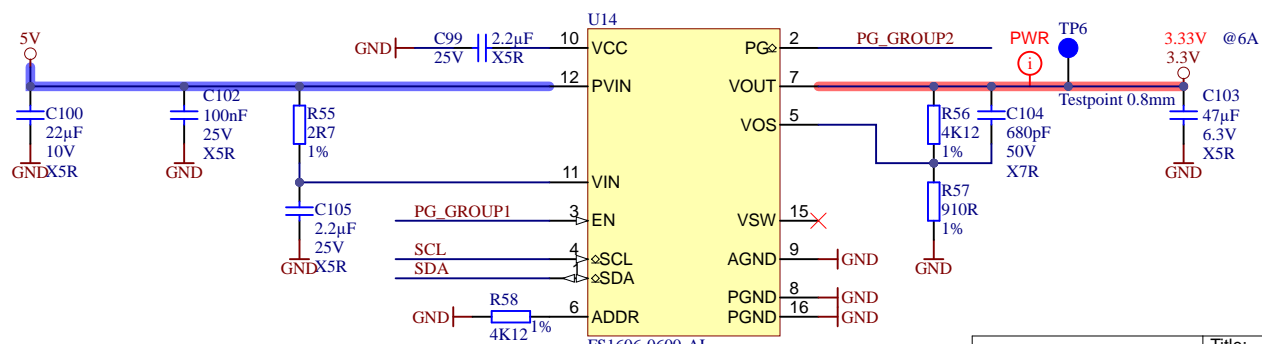
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Device Address: 0x13



Device Address: 0x15



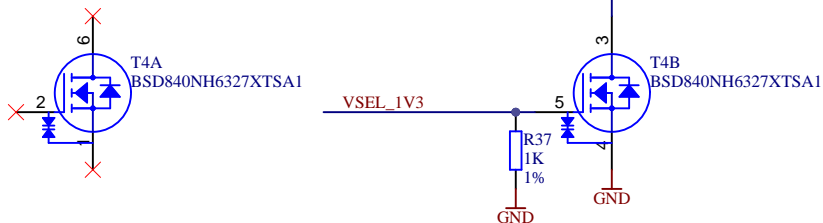
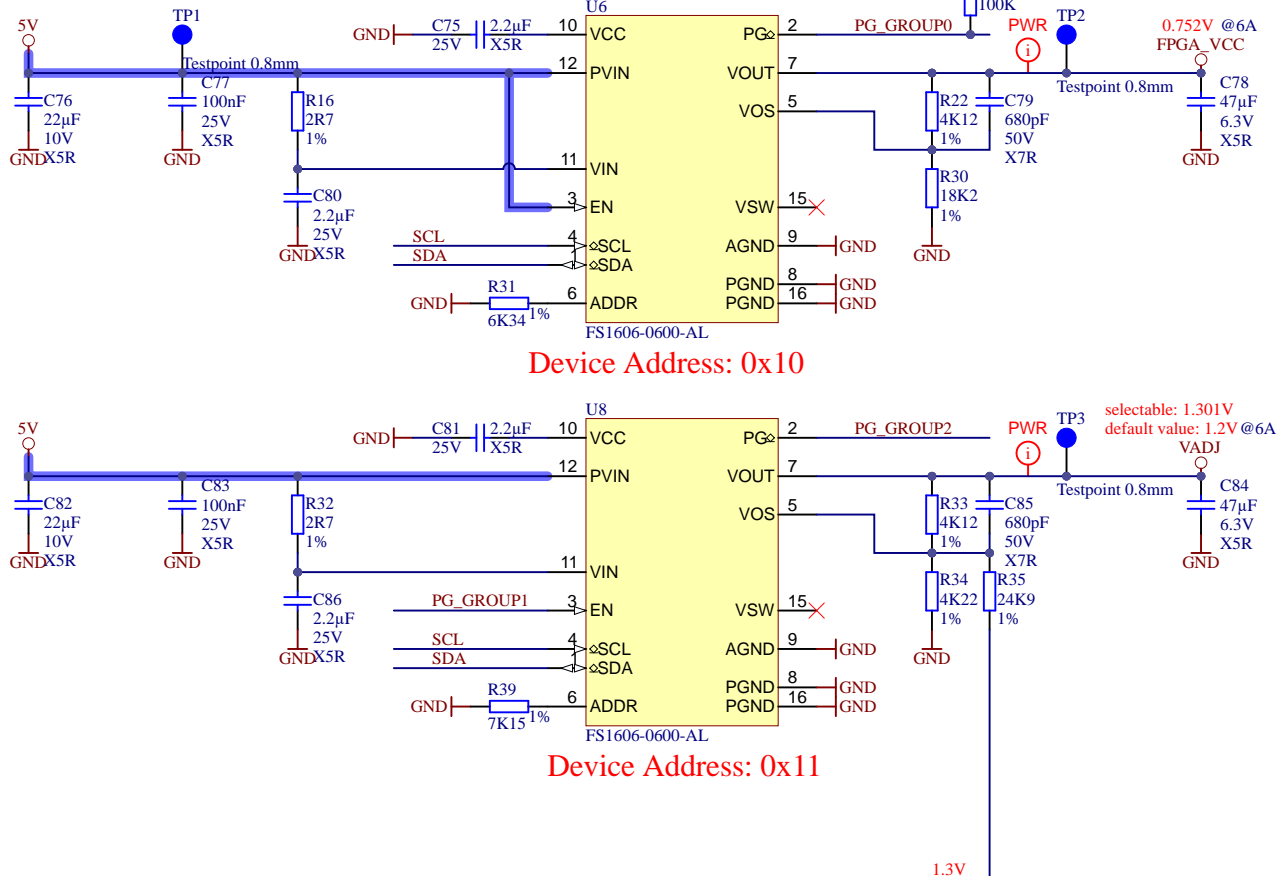
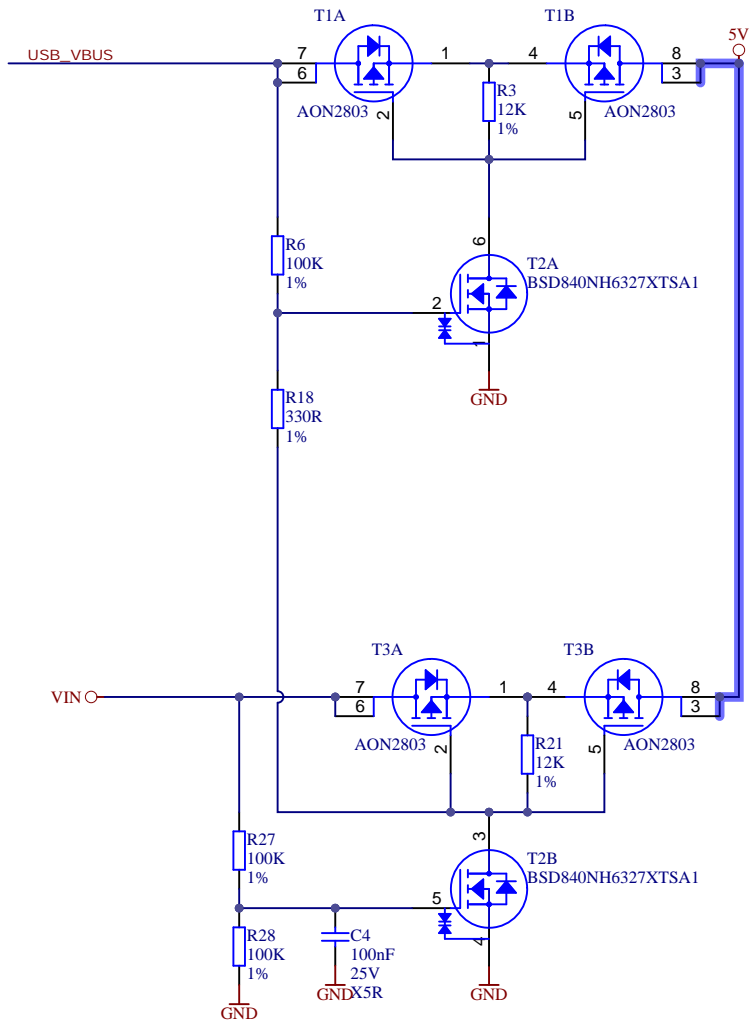
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Date: 09.12.2024	Copyright: Trenz Electronic GmbH	Page 11 of 11
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Title: PowerSupply		
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