

Attracting Tomorrow



μPOL Chip-Embedded DC-DC Power Modules

Power for Altera FPGA/SoC Series

New: TDK power for Agilex 5E and Agilex 7/9/11/13

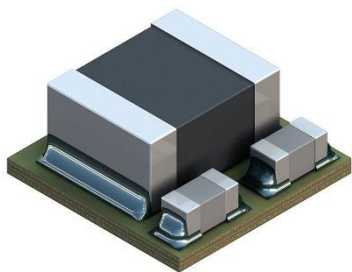
Tony Ochoa
Director
TDK μPOL Group

www.us.tdk.com/POL

TDK Corporation
Communication Devices Business Group • μPOL
Q2 2025

μPOL Chip-Embedded DC-DC Power Modules

Completely Integrated Solution



- ✓ TDK Component Quality
 - Entire BOM supplied by TDK

IC+Driver+
MOSFET

+

Inductor

+

Local
Bypass

+

Embedded
Package
(SESUB)

Controller, driver, MOSFETs and digital core are monolithically integrated within a single IC. Short signal paths enable high frequency operation and minimize parasitic inductance

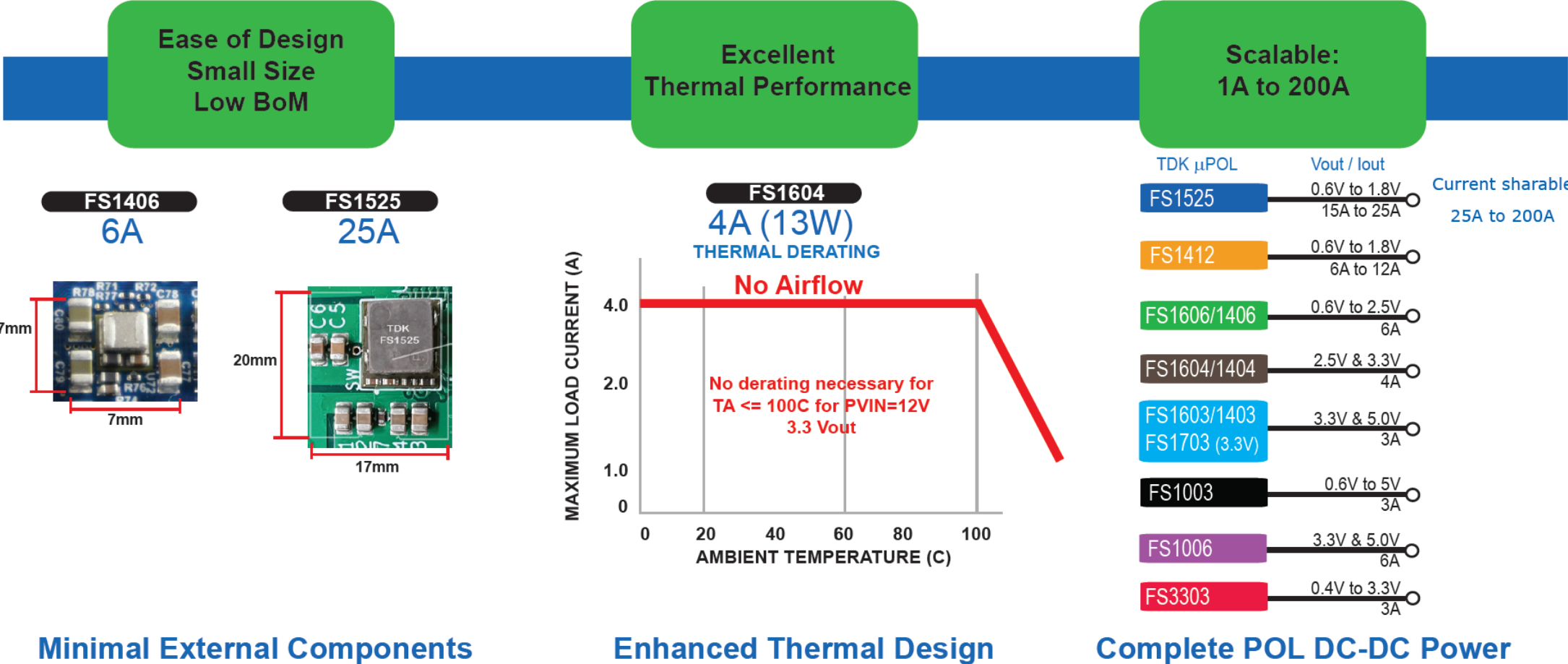
Custom inductor to exactly match the Q requirements of FETs and drivers which lowers interconnect and power losses

Boot and Vcc capacitors are integrated as part of the total power solution

Semiconductor **E**mbedded in **SUB**strate package reduces size, eliminates wire bonds & enhances thermal performance

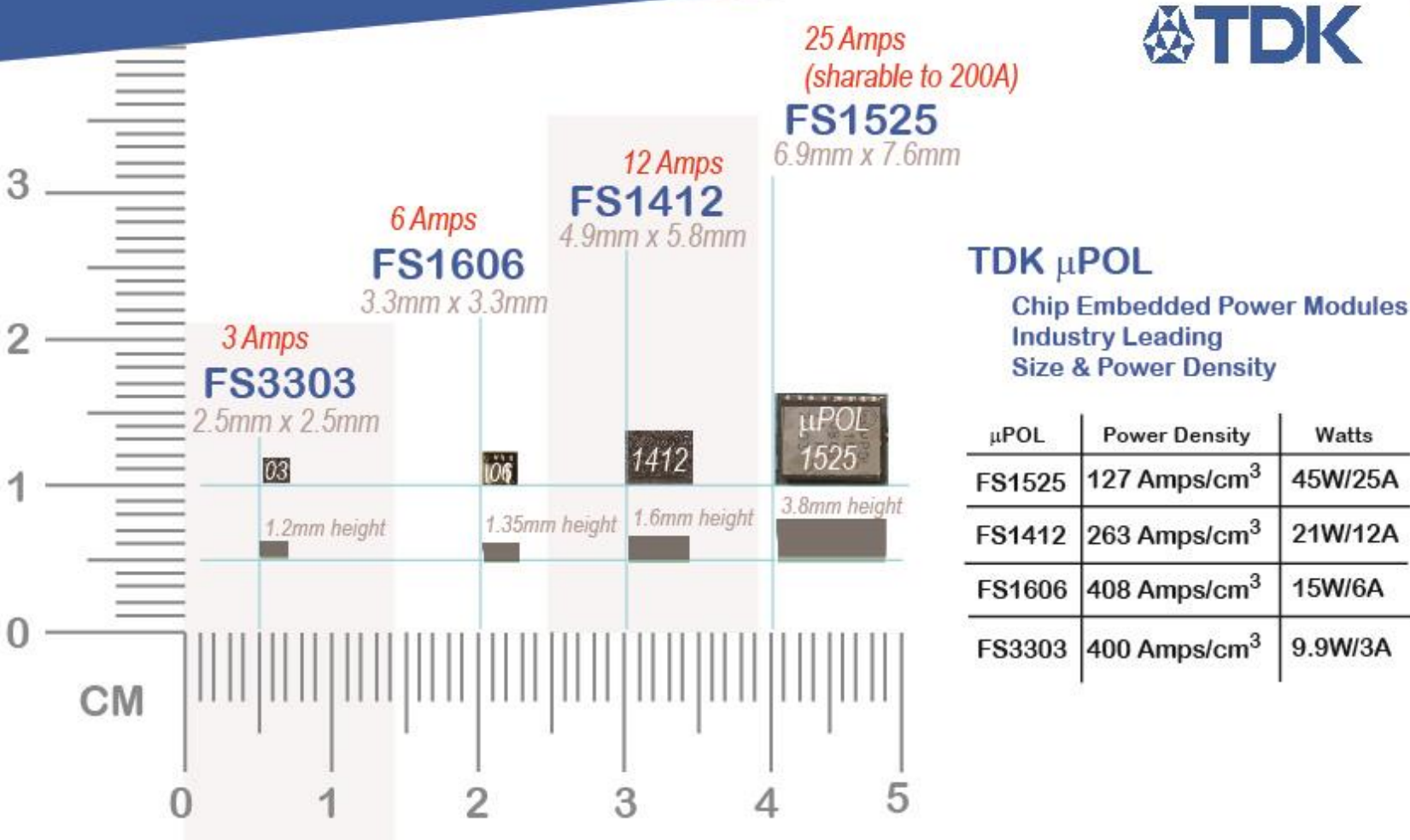
Quick Power Selection Guide

TDK’s μ POL Chip Embedded Technology provides endless opportunities to save space, design time without compromising in performance. These power modules contain matching MOSFET, Driver, Inductor and thermally enhanced package make it possible to provide the most optimum solution without comprising performance, while reducing the number of external components to reduce the overall system cost.



Best in Size and Performance

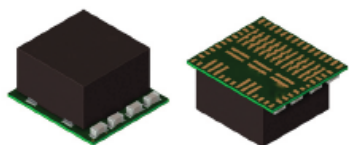
Leading solutions for Vertical Power



*x2 to x4
Higher power density
Over competitors*

FS1525

45 Watts

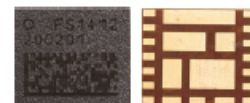


- 25A Power module
- Current sharable:
n=1 to 8 phase: 25A to 200A
- Vout: 0.6V to 1.8V
- Vin: 4.5V to 16V
- Analog, I2C/PMBus plus Telemetry

6.8 mm x 7.6 mm x 3.8 mm height

FS1412

21 Watts

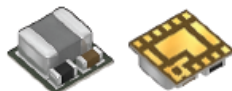


- 12A Power Module
- Vout: 0.6V to 1.8V
- Vin: 4.5V to 16V
- Analog, I2C/PMBus plus Telemetry

4.9 mm x 5.8 mm x 1.6 mm height

FS160x, FS140x, FS1703 Series

15 Watts



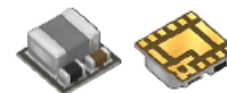
- 3A to 6A Power modules
- All same pinout
 - *FS1606 / FS1406: 0.6V to 2.5V Vout
 - *FS1603 / FS1403: 3.3V & 5.0V Vout
 - *FS1604 / FS1404: 2.5V & 3.3V Vout
 - FS1703 5V Vin to 3.3V Vout
- FS160x, I2C plus Telemetry

140x: 3.3mm x 3.3 mm x 1.5 mm height
160x: 3.3mm x 3.3 mm x 1.35 mm height

* Vin see datasheet

FS1006

30 Watts



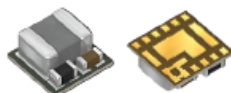
- 6A Power modules
- *FS1006 3.3V & 5.0V Vout @ 6A
- I2C plus Telemetry
- Same pinout as FS160x, FS140x

3.3mm x 3.3 mm x 1.35 mm height

* Vin see datasheet

FS1003

15 Watts

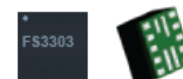


- 3A Power modules
- Vout: 0.6V to 5V
- Vin: 4.2V to 16V
- I2C plus Telemetry
- Same pinout as FS160x, FS140x

3.3mm x 3.3 mm x 1.35 mm height

FS3303 - Coming Soon

<10 Watts



- 3A Power modules
- 0.4V to 3.3V Vout @ 3A
- 2.7V to 5.5V Vin
- Ishutdown: <1uA max

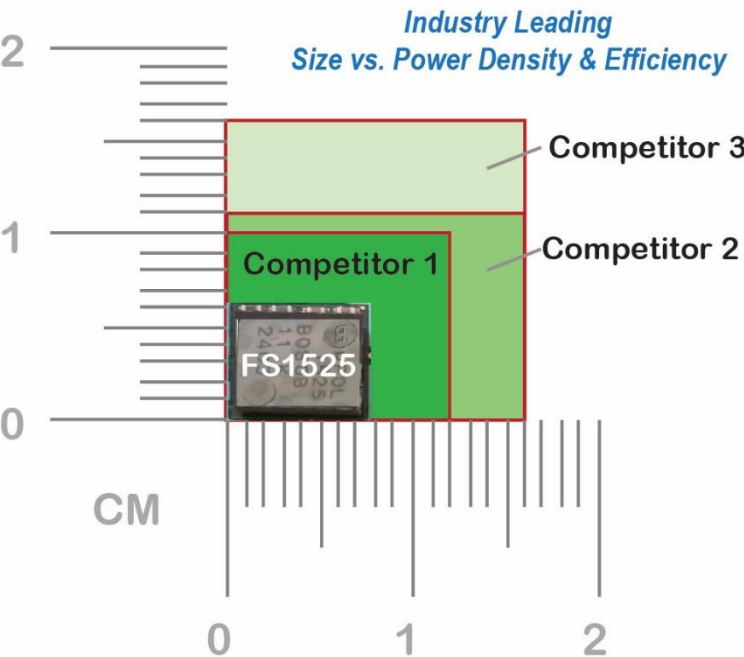
2.5mm x 2.5 mm x 1.2 mm height

Leading Power Density & Size



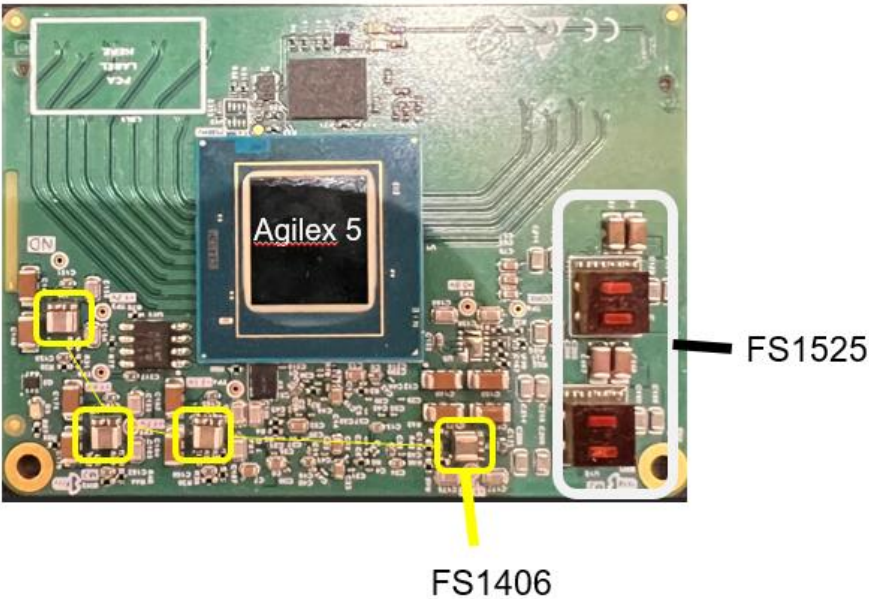
TDK μ POL

Chip Embedded Power Modules

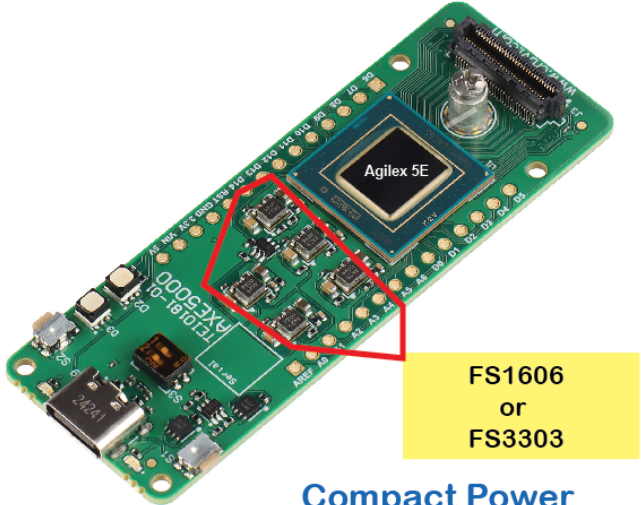


	TDK-FS1525 6.8mm x 7.6mm x 3.8mm	Competitor 1 10mm x 12mm x 4mm	Competitor 2 16mm x 16mm x 5mm	Competitor 3 11mm x 16mm x 4.2mm
Area	52.6mm ²	120mm ² (2.25x larger)	176mm ² (3.4x larger)	256mm ² (5x larger)
Volume	196mm ³	480mm ³	992mm ³	739mm ³
Current Density, A/cm ³	127.3	52.1	26.2	33.8
TDK is x-times better		2.4	4.9	3.8
Current Density, A/cm ²	48.4	20.8	11.6	14.2
TDK is x-times better		2.3	4.2	3.4

Design Example: Altera Agilex SoM



New – TDK FS1606 / FS1003 or FS3303 for Agilex 5E



**FS1606
or
FS3303**

**Compact Power
Design**

TDK


**Altera Agilex™ 5E Reference
Design Platform by Arrow using
μPOL™ DC-DC**

- Minimum BOM and few external components

TDK **ALTERA** **ARROW**

Agilex is registered trademark of Altera

**TDK μPOL
Proven Power Design
Altera Agilex 5E**



[Pre-Registration for ordering](#)

Key TDK μ POL devices to Power the Altera Agilex

Device	Voltage	Current	Design Notes
FS1525	VID set: 0.8V default 0.7V to 0.9V in +/-10mV steps Fixed set: 0.75V, 0.78V, 0.8V	25A to 200A	FS1525 has PMBus to support Intel Quartus for SmartVID FS1525 Vout can be set <ul style="list-style-type: none"> • via PS (hardware pin / resistor) • Resistor divider • I2C/PMBus
FS1412	0.8V, 1.0V, 1.2V, 1.8V, 1.1V, 0.9V	6A to 12A	
FS1406/FS1606	0.8V, 1.0V, 1.2V, 1.8V, 1.1V, 0.9V	1A to 6A	
FS1003	0.6V to 5V	3A	
FS1404 / FS1604	3.3V	1A to 4A	
FS3303	0.4V to 3.3V	500mA to 3A	
Other System Power			
FS1006	3.3V	6A	For 10G to 40Gb Enet supplies 3.3V system supplies
FS1603	5.0V	3A	5V system supplies

TDK μ POL devices to Power the Altera Agilex

Agilex 5 Power Maps



FS1525-0600 x1 or x 2	0.8V default 0.7V to 0.9V VID via PMBus 25A - 50A	Intel Agilex 5 VCC, VCCP, VCCL_HPS rails, VCCPLLDIG*, VCC_IO_SDM VCC_ADC_SDM,
FS1606-0600 FS1406-0600	0.8V / 6A	VCCL_SDM, VCCPLLDIG_SDM* VCC_HSSI_L1, VCC_HSSI_R4
FS1606-0600 FS1406-0600	1.0V / 6A	VCCH_SDM, VCCERT_GTSL1B VCCERT_GTSL1C, VCCERT_GTSR4B VCCERT_GTSR4C
FS1606-0600 FS1406-0600 FS1406-1200	1.2V / 3A	VCCRCORE, VCCIO_PIO_3B_T VCCIO_PIO_3B_B, (USB - VDD12)
FS1606-0600 FS1406-0600 FS1406-1800	1.8V / 4A-6A	VCCPT, VCCPT_HVIO, VCCPLL1_HPS VCCPLL2_HPS, VCCIO_HPS, VCCIO_SDM VCCPLL_SDM, VCCADC, VCCFUSEWR_SDM VCCERT_GTSL1B, VCCERT_GTSL1C, VCCERT_GTSR4B, VCCERT_GTSR4C VCCIO_HVIO_6A, VCCIO_HVIO_6B, VCCIO_HVIO_6C, VCCBAT, HPS ETH - VDDIO FPGA ETH - VDDIO, USB HUB - VDDIO USB HUB - VDD18, HDMI - DVDD, HDMI_AVDD HDMI - PVDD, HDMI - PLVDD, HDMI - BGVDD
FS1604-3300 FS1404-3300	3.3V / 4A	VCCIO_HVIO_5A, VCCIO_HVIO_5B, VCCIO_HVIO_6D, ADC - VREF, HPS ETH - AVDD_3P3, FPGA ETH - AVDD_3P3, HDMI - MVDD, PLL - VDD_DIG, PLL - VDD_XTAL, PLL - VDDA, USB HUB - VDD33, USB PHY - VBAT, USB PHY - VDD33
FS1606-0600 FS1406-0600 FS1406-1100	1.1V / 4A-6A	VCCIO_PIO_2A_T, VCCIO_PIO_2A_B, VCCIO_PIO_3A_T VCCIO_PIO_3A_B, VCCIO_PIO_SDM, FPGA LPDDR4 - VDD2, HPS LPDDR4 - VDD2 FPGA LPDDR4 - VDDQ, HPS LPDDR4 - VDDQ
FS1606-0600 FS1406-0600 FS1406-0900	0.9V / 1A FMC_ADJ	HPS ETH - DVDD_0P9 FPGA ETH - DVDD_0P9
FS1606-0600 FS1406-0600 FS1406-1200	1.2V / 6A	VCCIO_PIO_2B_T VCCIO_PIO_2B_B

All 12Vin Devices

check
Intel PSG
Early Power
Estimator (EPE)
for
VCC / VCCP
rail consumption

E-Series Device Group A: VID 0.70V to 0.90V
E-Series Device Group B:
VCC fixed 0.75V, 0.78V, 0.8V

Note: FS1406-0600
(FS1606 telemetry option)
alternative for voltage divider
for Vout from 0.6V to 1.8V;
Otherwise voltage FS1406-xxxx
suggested for best accuracy.

Additional power rails for
Agilex tiles with QFSP ports
(i.e. 3.3V rails)

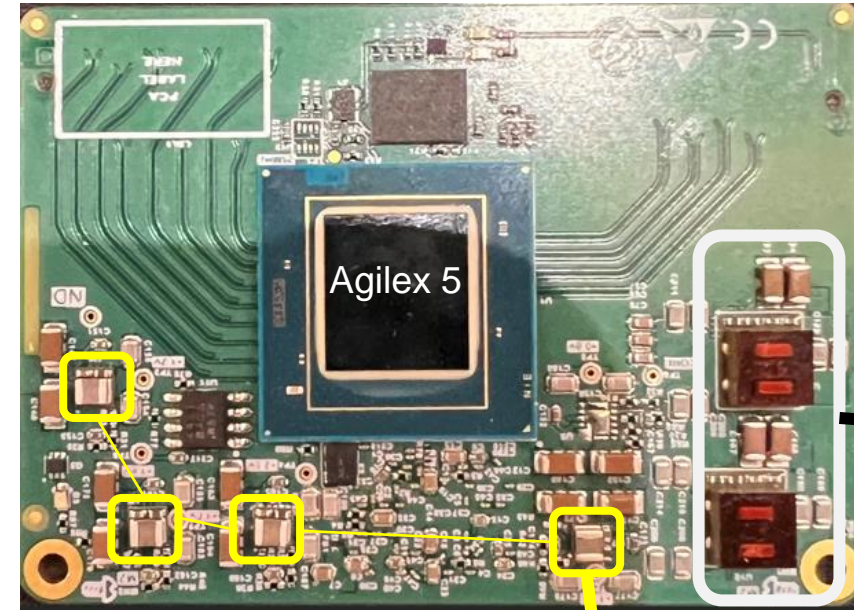
Ethernet MAC options:
10Mbps, 100Mbps
1Gbps / 2.5Gbps

FS1404-3300 3.3V / 4A 10W QFSP
FS1604-3300

FS1404-3300 3.3V / 4A 10W QFSP
FS1604-3300

FS1403-5000 5.0V / 3A System
Voltage 5.0V
USB, ADC, Sensor
(Cruvi)

FS1406-0600 1.1V / 6A LP-DDR4
FS1406-1100



FS1525

FS1406

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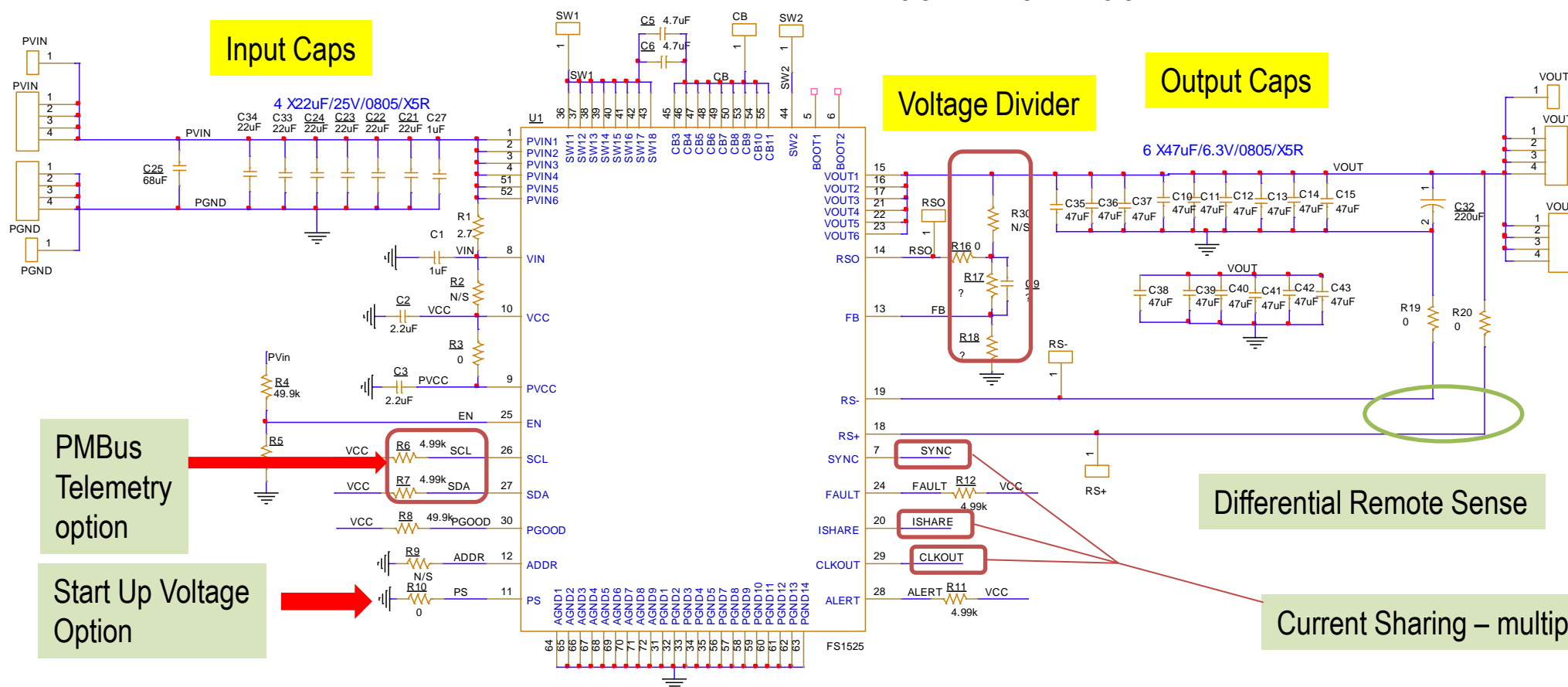


Vcore rail for Agilex 5 – Using the FS1525

FS1525 – 25A Design – Ease of Design



6.8mm x 7.6mm x 3.8mm



TDK μ POL devices to Power the Altera Agilex

Agilex 5 – VCC, VCCP voltage rail 25A

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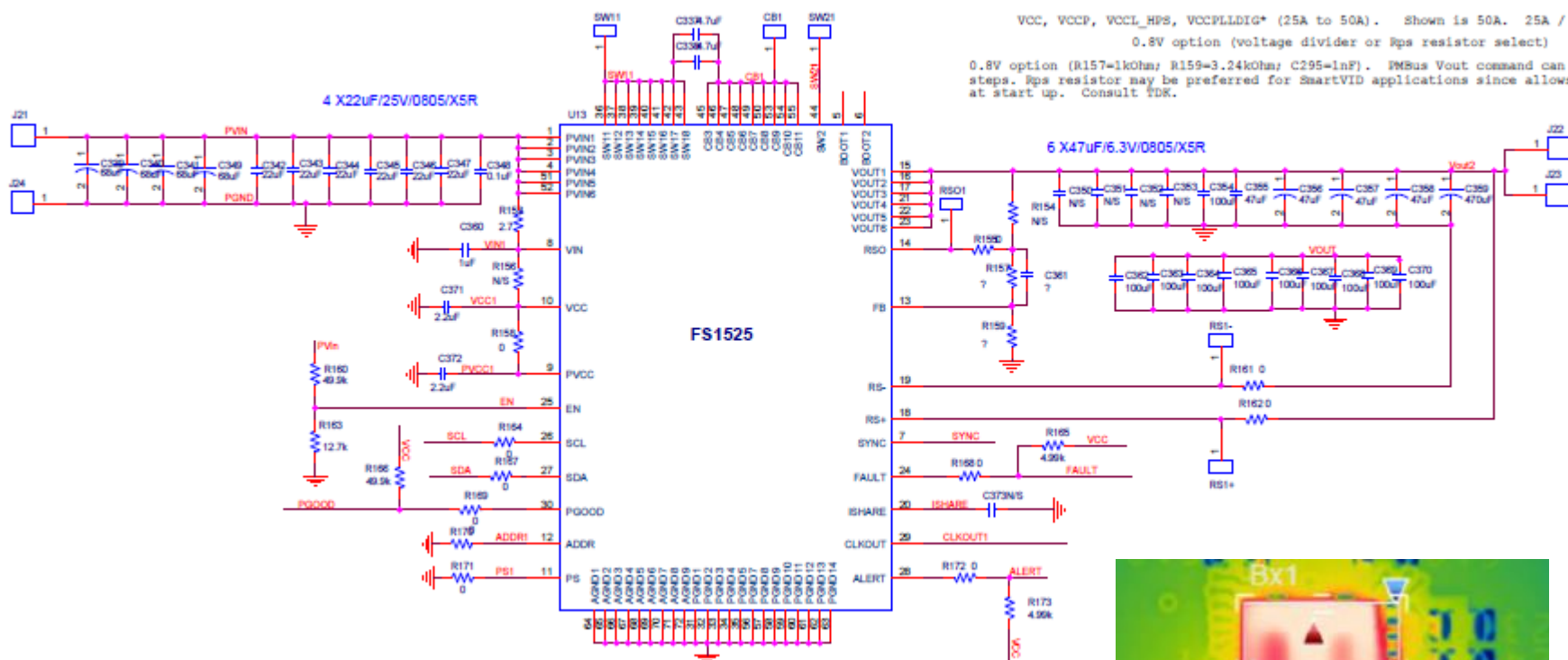
FS1525-0600
x1 or x 2

0.8V default
0.7V to 0.9V VID
via PMBus
25A - 50A

Intel Agilex 5

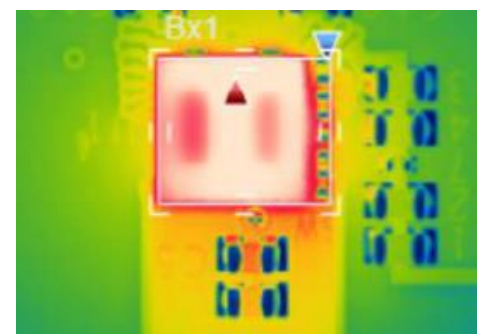
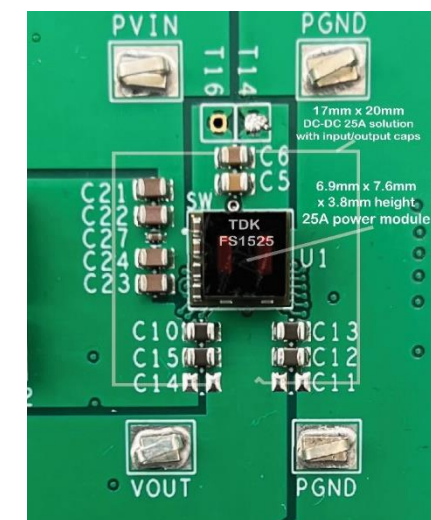
VCC, VCCP, VCCL_HPS rails,
VCCPLLDIG*, VCC_IO_SDM
VCC_ADC_SDM,

TDK micro-POL Power Solution for Intel Agilex 5



25A

















17mm x 20mm



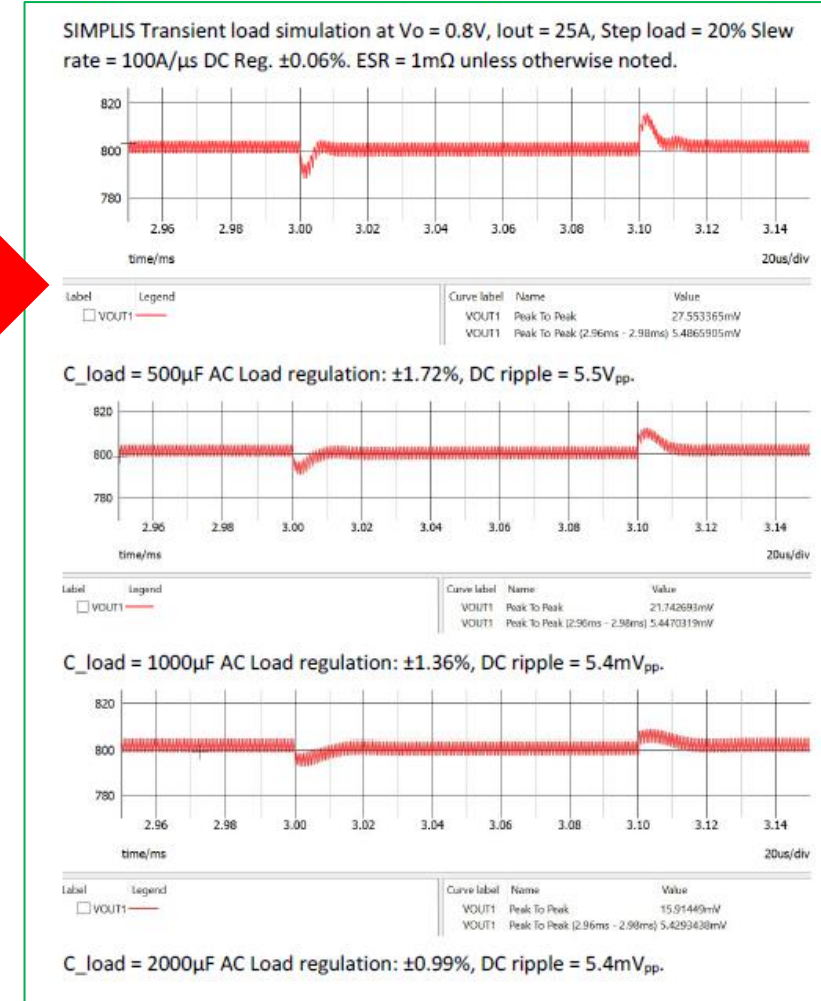
PVin=12V, Vo= 0.8V,
Fsw=625 kHz,
Io=25A, no airflow.
+42C rise from room temp

TDK – Altera Agilex 5 – Simplis Design Library

Agilex 5 – SIM Library SIMPLIS

Voltage rail name	Nom Vin	Max Iin	DC ripple	DC reg	AC reg	Load step	Slew rate	TDK μ POL	SIMPLIS model	Transient response plot
VCC, VCCP, VCCL_HPS, VCCPLLDIG*, VCC_IO_SDM, VCC_ADC_SDM	0.70V	25A				20%	100A/ μ s	FS1525-0600	 0V7 25A 20pc 100A μ s SIM.zip	 Plot 0V7 25A 20pc 100A μ s SIM.pdf
	0.80V								 0V8 25A 20pc 100A μ s SIM.zip	 Plot 0V8 25A 20pc 100A μ s SIM.pdf
	0.90V								 0V9 25A 20pc 100A μ s SIM.zip	 Plot 0V9 25A 20pc 100A μ s SIM.pdf
VCCL_SDM, VCC_HSSI_L1, VCC_HSSI_R4	0.8V	12A			$\pm 3\%$	25%	10A/ μ s	FS1412-0600	 0V8 12A 25pc 10A μ s SIM.zip	 Plot 0V8 12A 25pc 10A μ s SIM.pdf
VCCPLLDIG_SDM *									 0V8 12A 25pc 10A μ s SIM.zip	 Plot 0V8 12A 25pc 10A μ s SIM.pdf
VCCL_SDM, VCC_HSSI_L1, VCC_HSSI_R4	0.8V	6A			$\pm 3\%$	25%	10A/ μ s	FS1406-0800	 0V8 6A 25pc 10A μ s SIM.zip	 Plot 0V8 6A 25pc 10A μ s SIM.pdf
VCCPLLDIG_SDM *									 0V8 6A 25pc 10A μ s SIM.zip	 Plot 0V8 6A 25pc 10A μ s SIM.pdf
VCCH_SDM, VCCERT_GTSL1B, VCCERT_GTSL1C, VCCERT_GTSR4B, VCCERT_GTSR4C	1.0V	6A			$\pm 3\%$	100%	1A/ μ s	FS1406-1000	 1V0 6A 100pc 1A μ s SIM.zip	 Plot 1V0 6A 100pc 1A μ s SIM.pdf

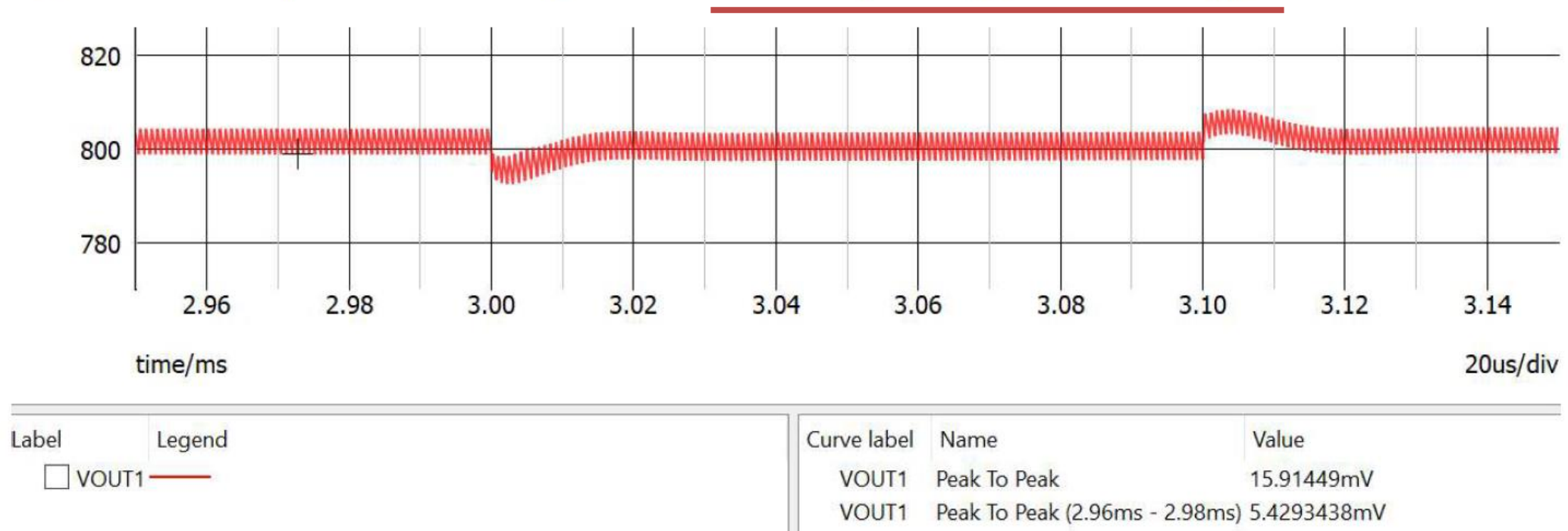
FS1525
Simplis
performance
guidelines
data



Design Example: VCC/VCCP (Vcore) of Altera Agilex 5

FS1525 – 25A / 0.8V. 20% step load. 100A/usec.

$C_{load} = 1000\mu\text{F}$ AC Load regulation: $\pm 1.36\%$, DC ripple = 5.4mV_{pp} .



Design Example: VCC/VCCP (Vcore) of Altera Agilex 5

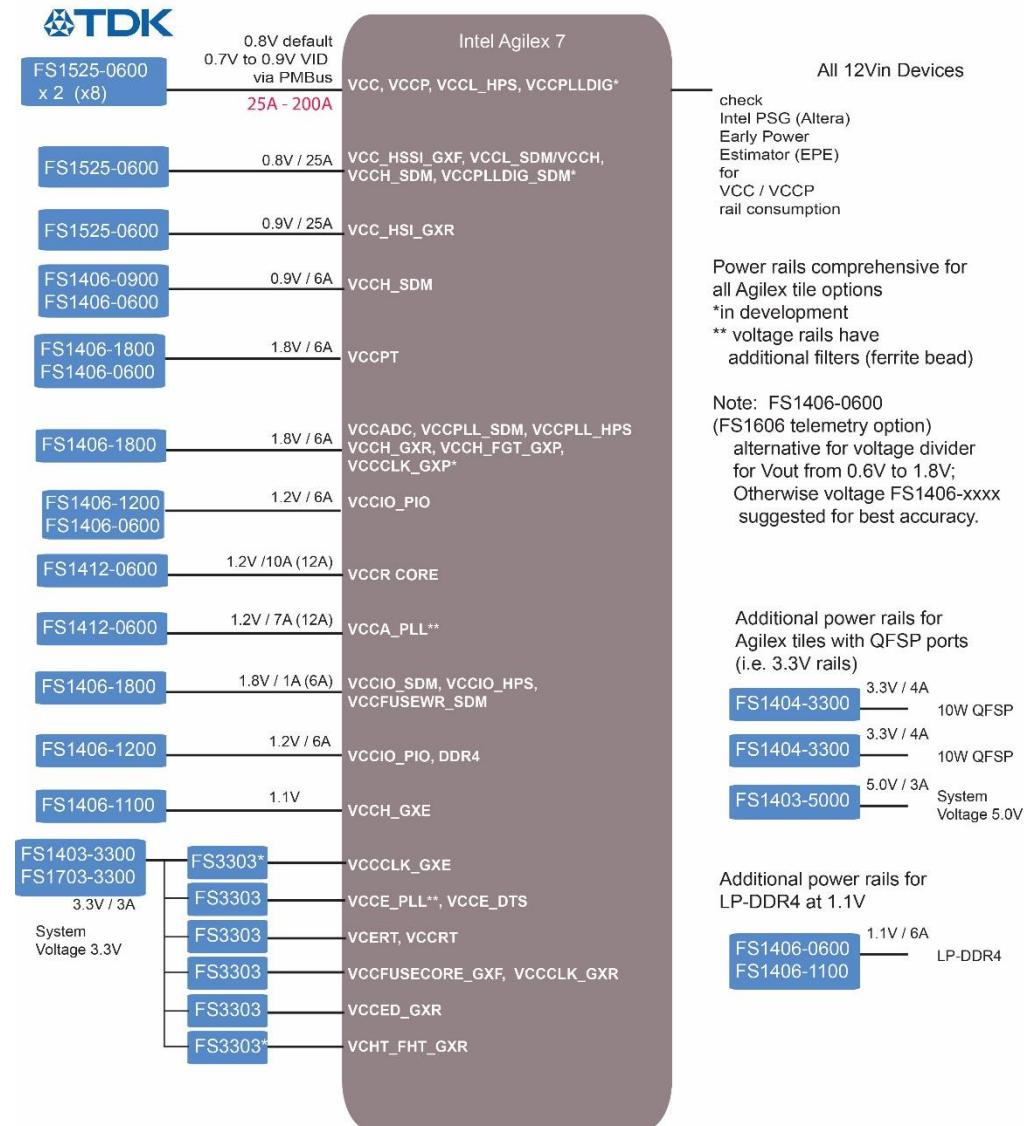
FS1525 – 25A / 0.8V. 20% step load. 100A/usec.

Part reference	Qty	Value	Description
C1,C48	2	1μF	0603/25V/X7R
C27,C40	2	1μF	0402/25V/X5R
C2,C3,C50,C51	4	2.2μF	0402/10V/X7R
C5,C6,C33,C34	4	4.7μF	0805/16V/X7R
C97,C*	2	330μF	1210/2.5V/X6S
C10,C13,C127,C130	4	47μF	0805/6.3V/X5R
C110,C111,C112	3	100μF	0805/4V/X6S
C107,C108,C109	3	47μF	0603/2.5V/X6S
C113,C126,C41	3	10μF	0402/6.3V/X5R
C21,C22,C23,C24,C37,C38,C39,C101	8	22μF	0805/25V/X5R
C35,C95	2	68μF	25V,poscap
C32,C93,C96	3	470μF	SP-CAP

TDK μ POL devices to Power the Altera Agilex

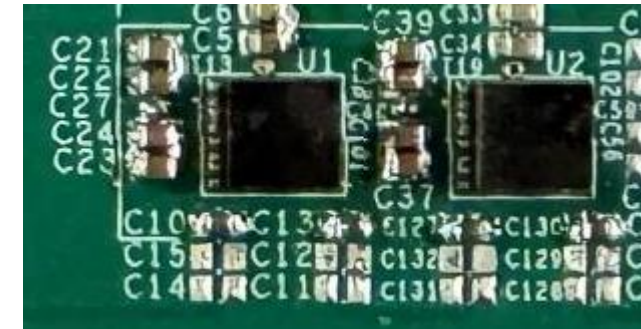
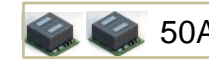
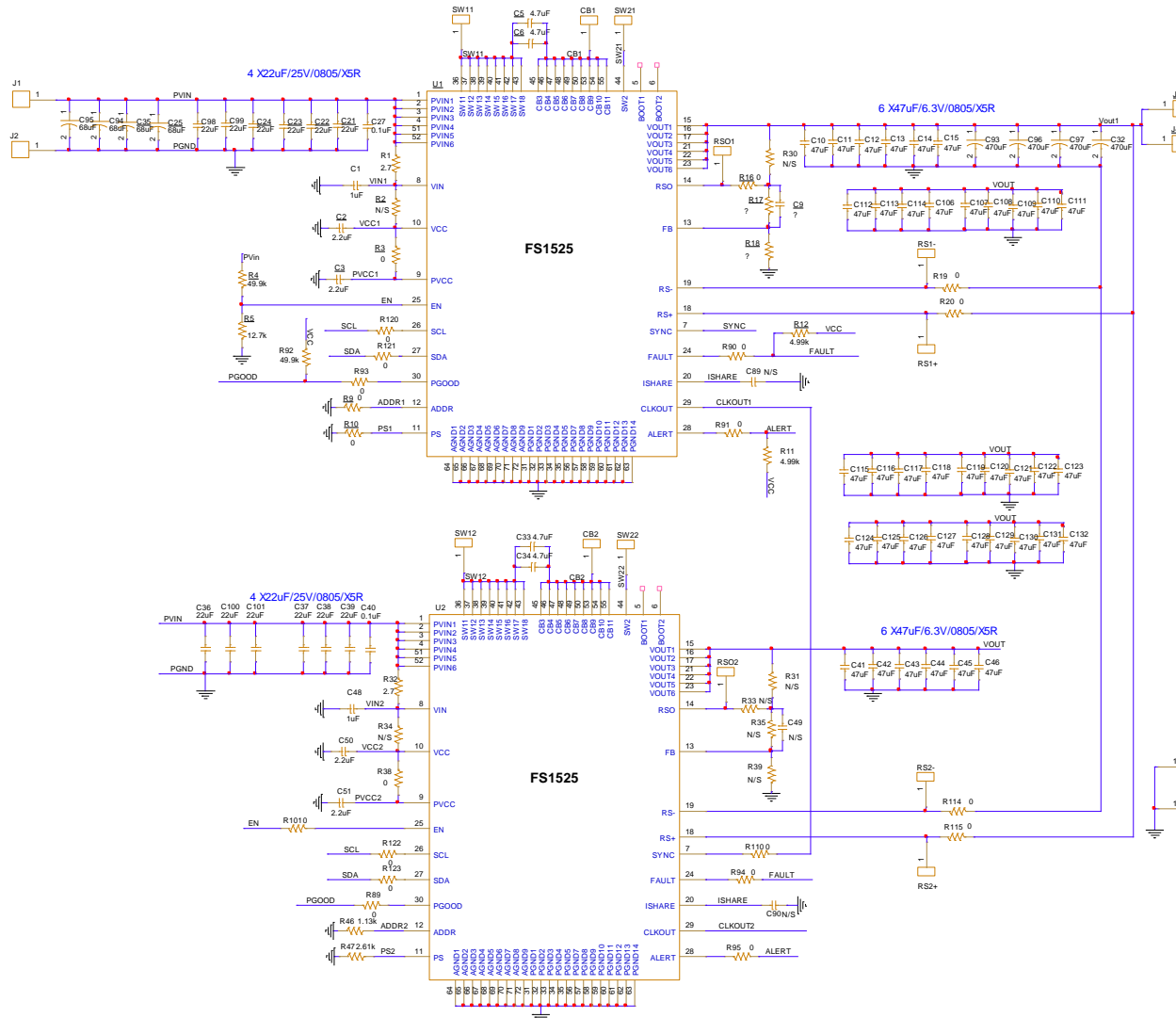
Agilex 7, 9

Power Maps



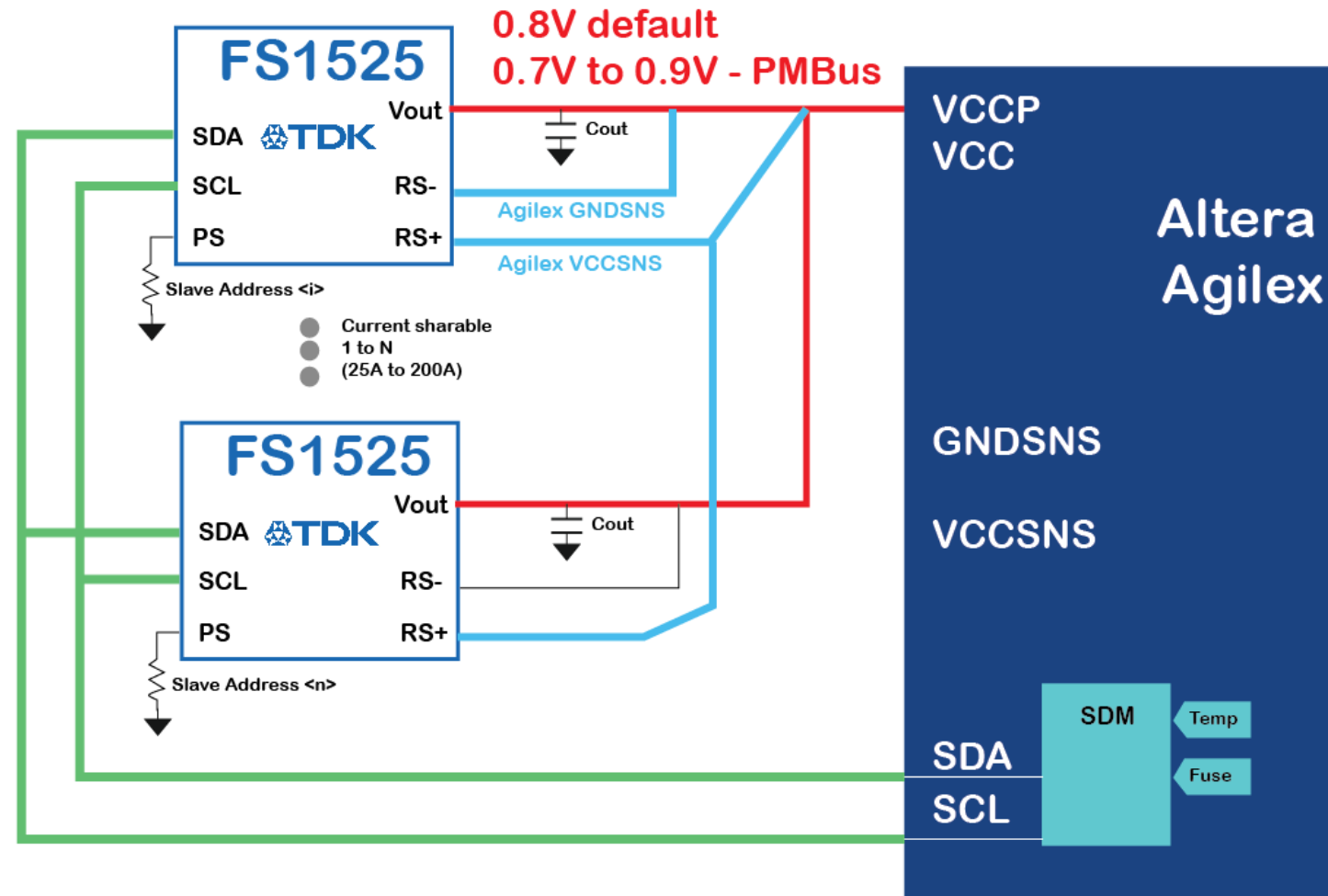
TDK μ POL devices to Power the Altera Agilex Agilex 5 – VCC, VCCP voltage rail 50A

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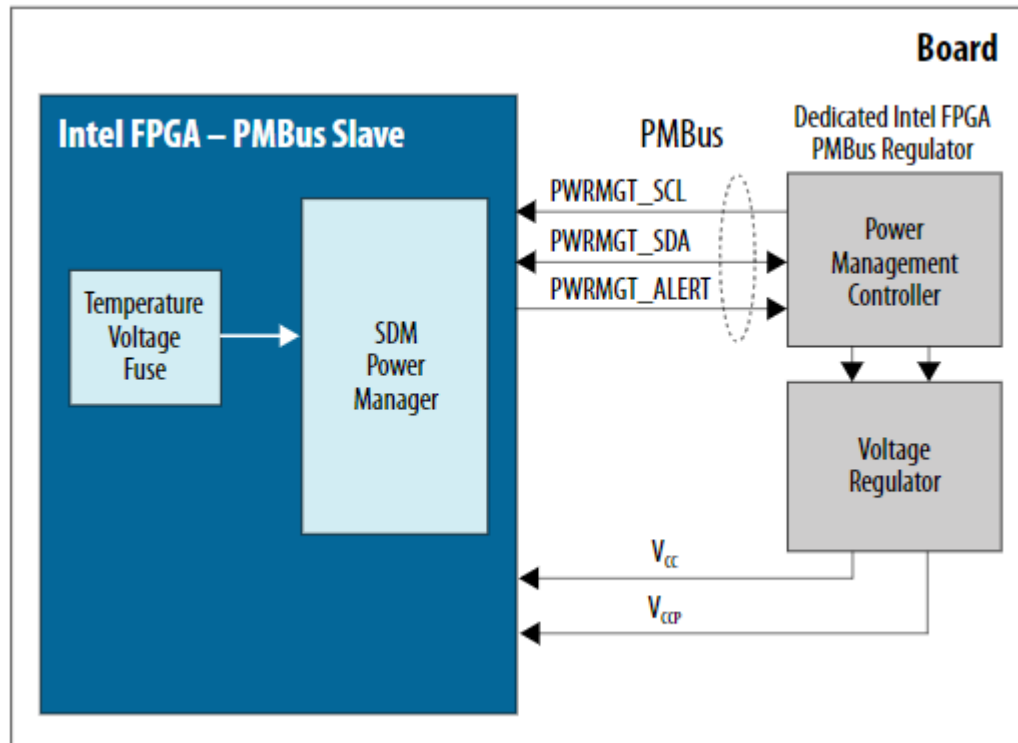
FS1525 – Using it for Agilex SmartVID

- Vcore Rail has two modes: Fixed or SmartVID
VCCP, VCC
 - SmartVID: 0.8V default. 0.7V to 0.9V +/-10mV steps
 - Fixed: 0.75V, 0.78V, 0.8V
- FS1525 can be used for either SmartVID or Fixed modes
- Altera uses PMBus to communicate to Slave Power Devices to set the VID voltages.
- Each FS1525 has a unique hardware address to be addressed by the Agilex SDM via Intel Quartus Software
- **Design Configuration Tips for Quartus for FS1525 use case:**
 - 1) Slave mode selected
 - 2) Linear mode selected
 - 3) Assign the slave hardware address for each FS1525
 - 4) FS1525 does not work in PAGE mode
 - 5) Each FS1525 must be addressed and programmed separately (Group mode is not available)



Supported Commands for the PMBus Slave Mode FS1525 to Agilex

Command Name	Command Code	Default	PMBus Transaction Type	Number of Bytes
CLEAR_FAULTS	03h	—	Send byte	0
VOUT_MODE	20h	40h	Read byte	1
VOUT_COMMAND	21h	—	Read word	2
STATUS_BYTE	78h	00h	Read byte	1



FS1525 Quick PMBus Command Sets

Register	Name
40	I2C-base(6:0)
41	PMBus_base(6:0)
42	Operation[7:0]
43	On_off_config[7:0]
4C	Vout_command_lower[7:0]
4D	Vout_command_upper[7:0]

FS1525 also has
Full telemetry command
sets

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Other voltage rail for Agilex 5 – Using TDK μ POL

Other voltage rails for Agilex 5 Power Design

FS1606-0600
FS1406-0600

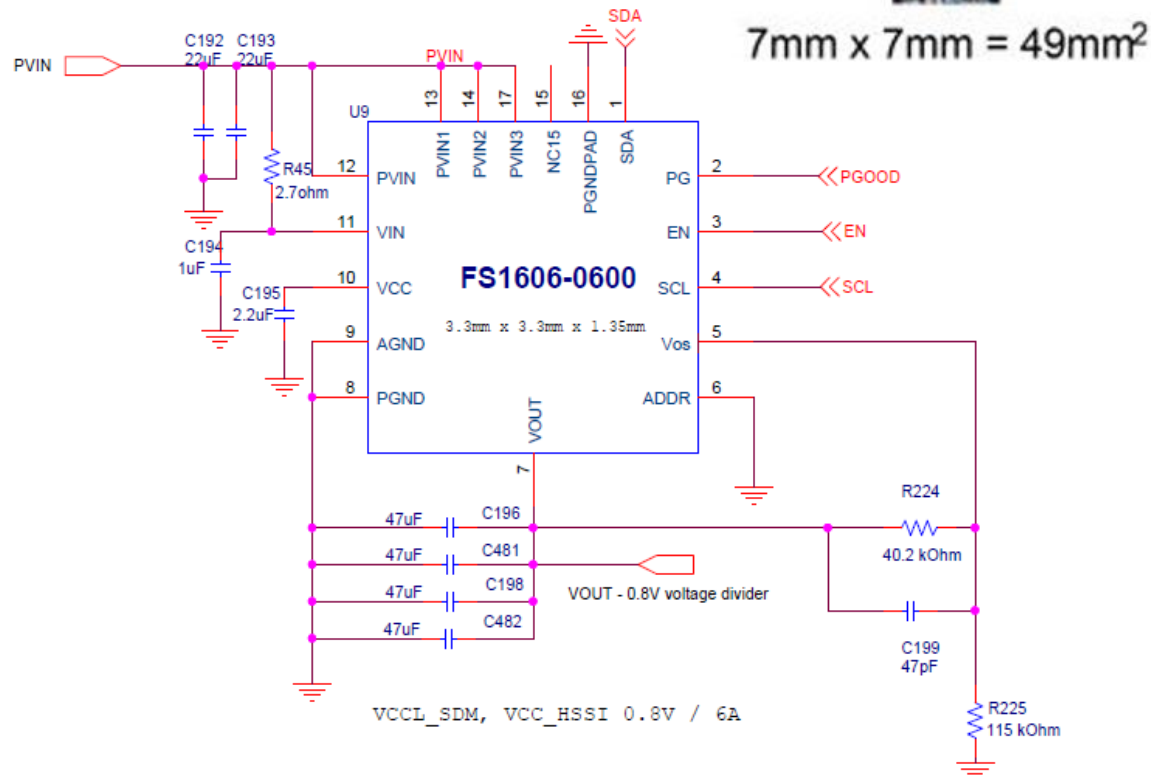
1.0V / 6A

VCCH_SDM, VCCERT_GTSL1B
VCCERT_GTSL1C, VCCERT_GTSR4B
VCCERT_GTSR4C

DC-DC Total Solution

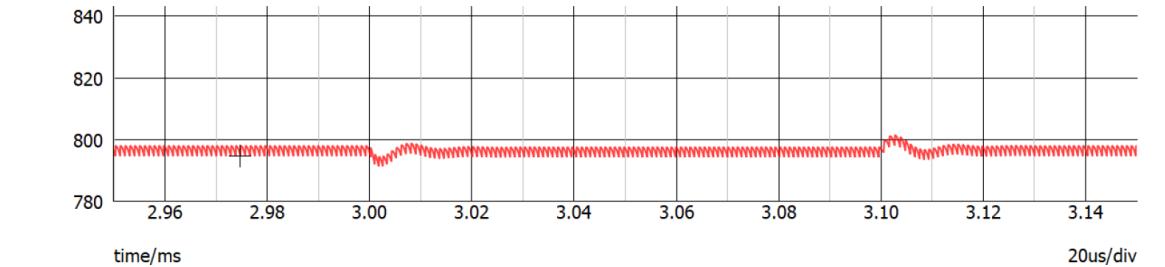


7mm x 7mm = 49mm²

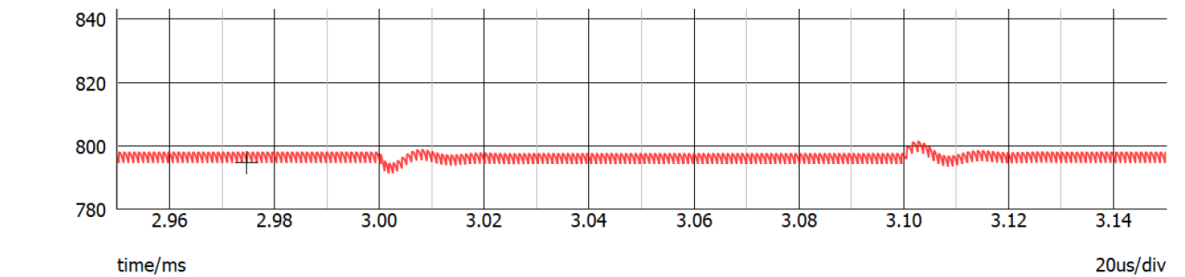


Transient load at $V_o = 0.8V$, $I_{out} = 6A$, Step load = 25% Slew rate = $10A/\mu s$

$C_{load} = 100\mu F$ AC Load regulation: $\pm 1.23\%$, DC ripple = $5.4mV_{pp}$.



Label	Legend	Curve label	Name	Value
Vout		Vout	Peak To Peak	10.091143mV
		Vout	Peak To Peak (2.96ms - 2.98ms)	3.3081897mV



Label	Legend	Curve label	Name	Value
Vout		Vout	Peak To Peak	10.091143mV
		Vout	Peak To Peak (2.96ms - 2.98ms)	3.3081897mV

$C_{load} = 500\mu F$ AC Load regulation: $\pm 0.63\%$, DC ripple = $3.3mV_{pp}$.

Other voltage rails for Agilex 5 Power Design

FS1606-0600
FS1406-0600

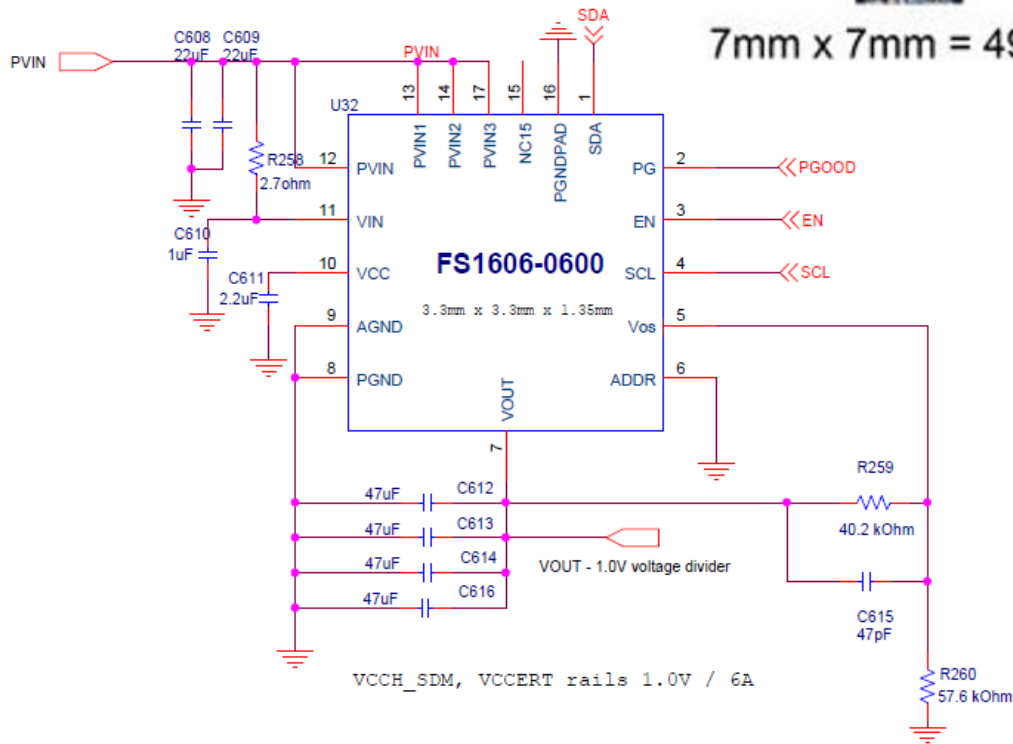
1.0V / 6A

VCCH_SDM, VCCERT_GTSL1B
VCCERT_GTSL1C, VCCERT_GTSR4B
VCCERT_GTSR4C

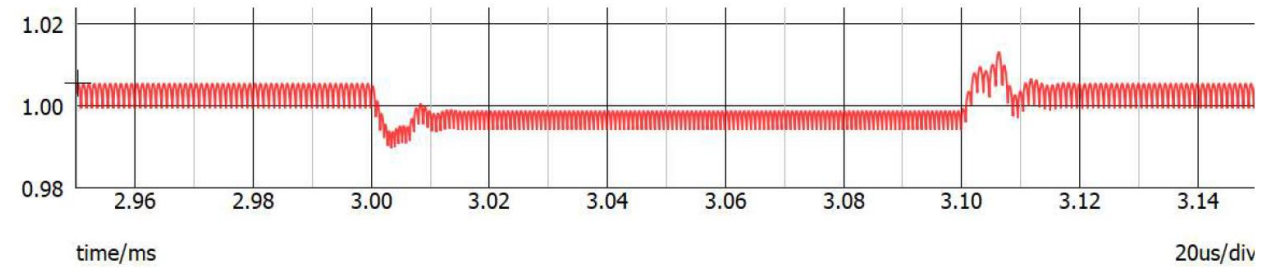
DC-DC Total Solution



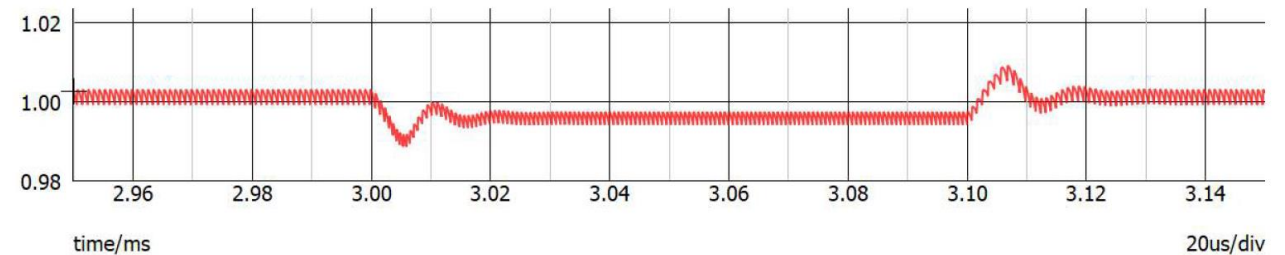
7mm x 7mm = 49mm²



Transient load at $V_o = 1.0V$, $I_{out} = 6A$,
Step load = 100% Slew rate = $1A/\mu s$

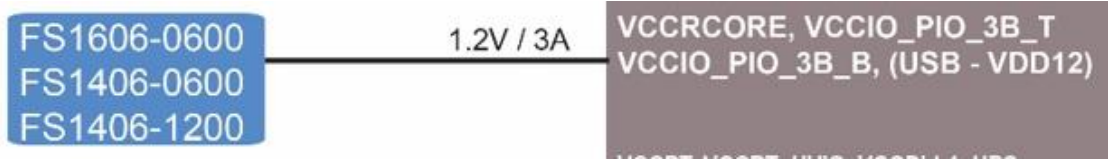


$C_{load} = 100\mu F$ AC Load regulation: $\pm 1.18\%$, DC ripple = $6.1mV_{pp}$.

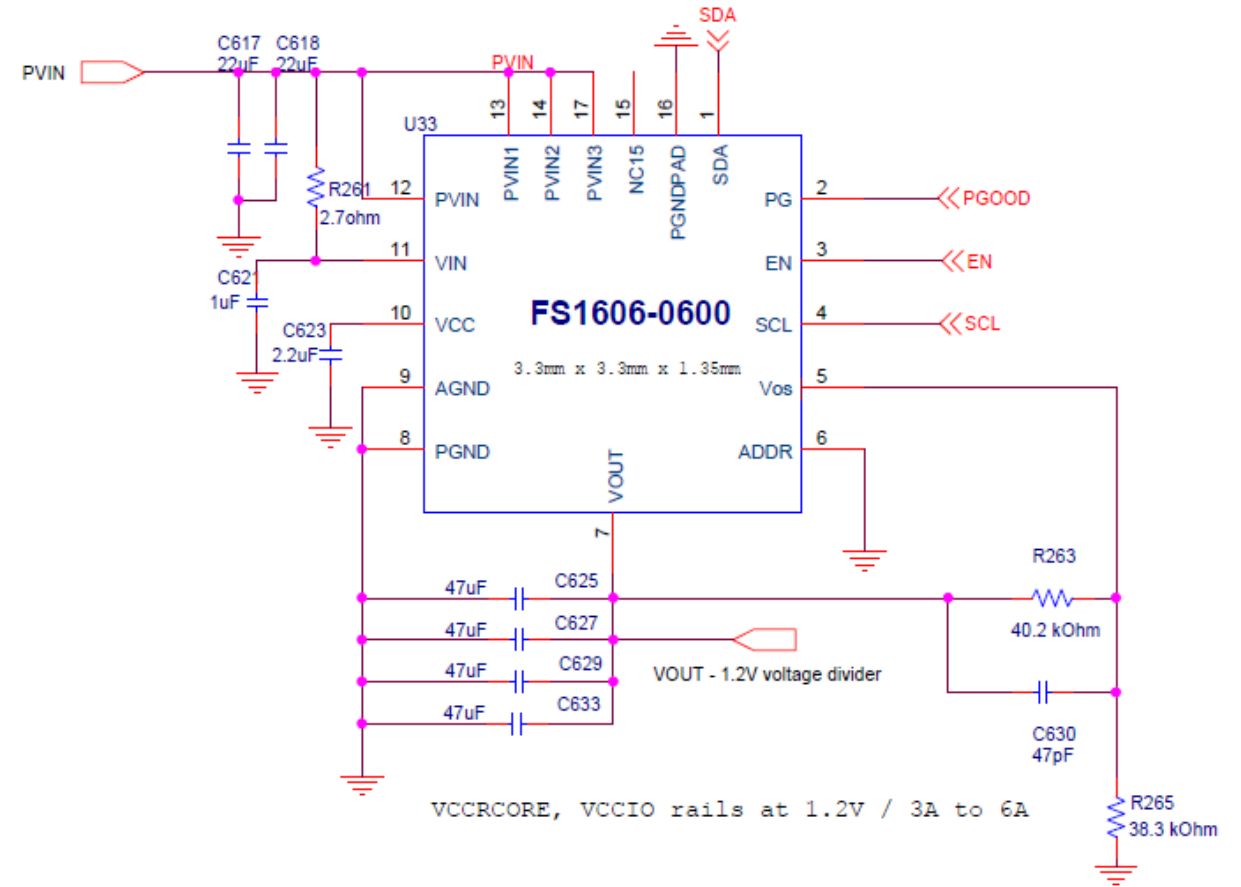


$C_{load} = 500\mu F$ AC Load regulation: $\pm 1.03\%$, DC ripple = $3.8mV_{pp}$.

Other voltage rails for Agilex 5 Power Design

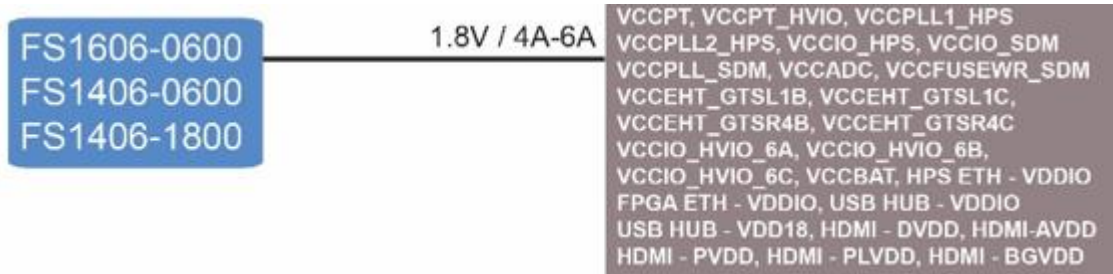


DC-DC Total Solution


$$7\text{mm} \times 7\text{mm} = 49\text{mm}^2$$


Other voltage rails for Agilex 5 Power Design

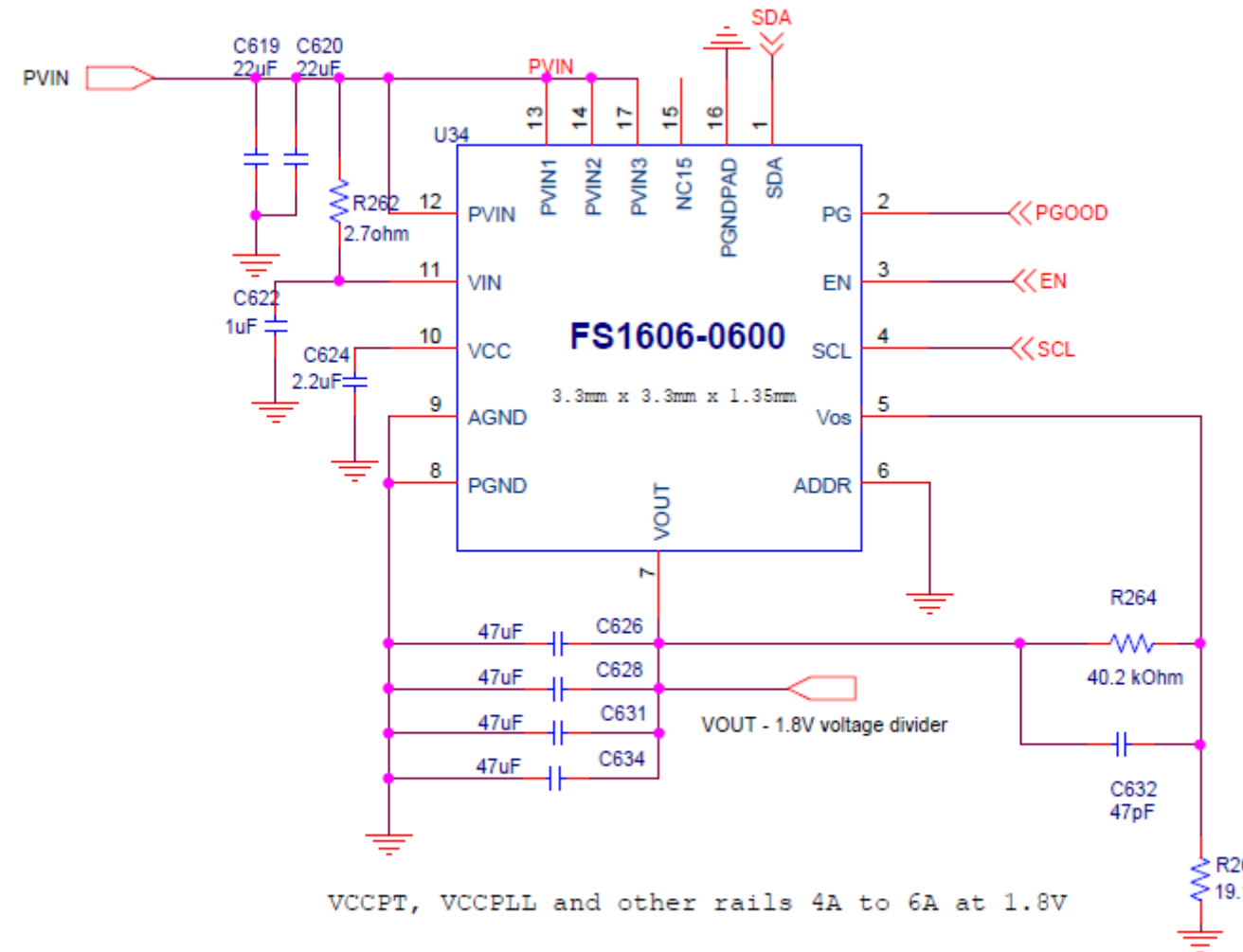
Attracting Tomorrow



DC-DC Total Solution



7mm x 7mm = 49mm²



Other voltage rails for Agilex 5 Power Design

Attracting Tomorrow



FS1604-3300
FS1404-3300

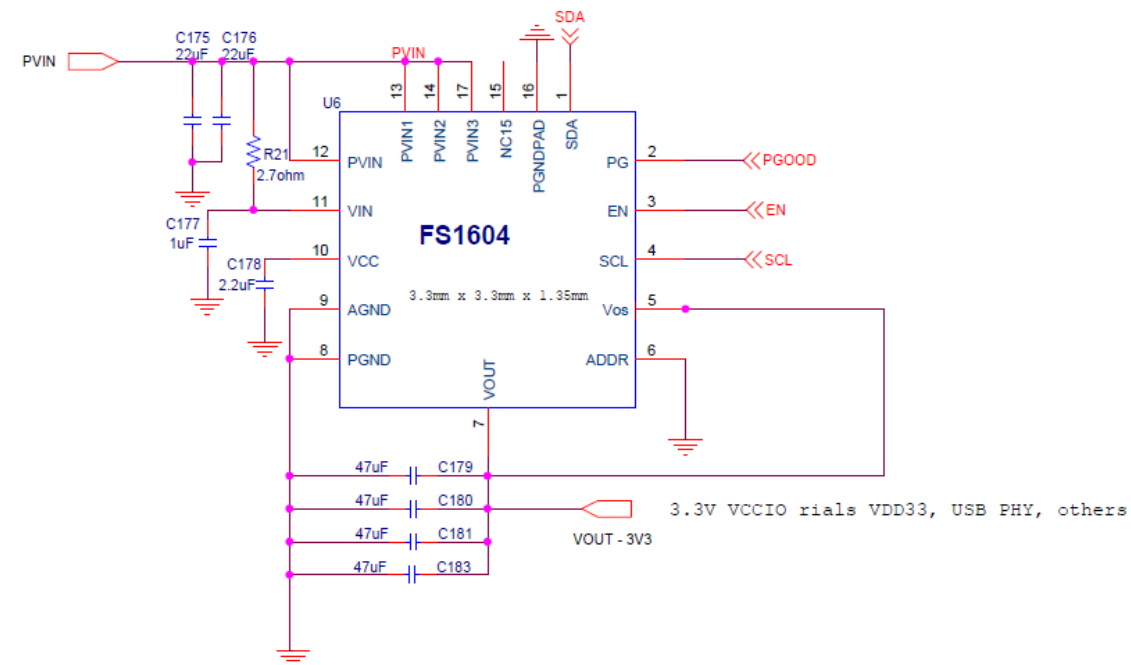
3.3V / 4A

VCCIO_HVIO_5A, VCCIO_HVIO_5B, VCCIO_HVIO_6D,
ADC - VREFPA, HPS ETH - AVDD_3P3, FPGA ETH - AVDD_3P3,
HDMI - MVDD, PLL - VDD_DIG, PLL - VDD_XTAL, PLL - VDDA,
USB HUB - VDD33, USB PHY - VBAT, USB PHY - VDD33

DC-DC Total Solution



7mm x 7mm = 49mm²



Other voltage rails for Agilex 5 Power Design

Attracting Tomorrow



FS1604-3300
FS1404-3300

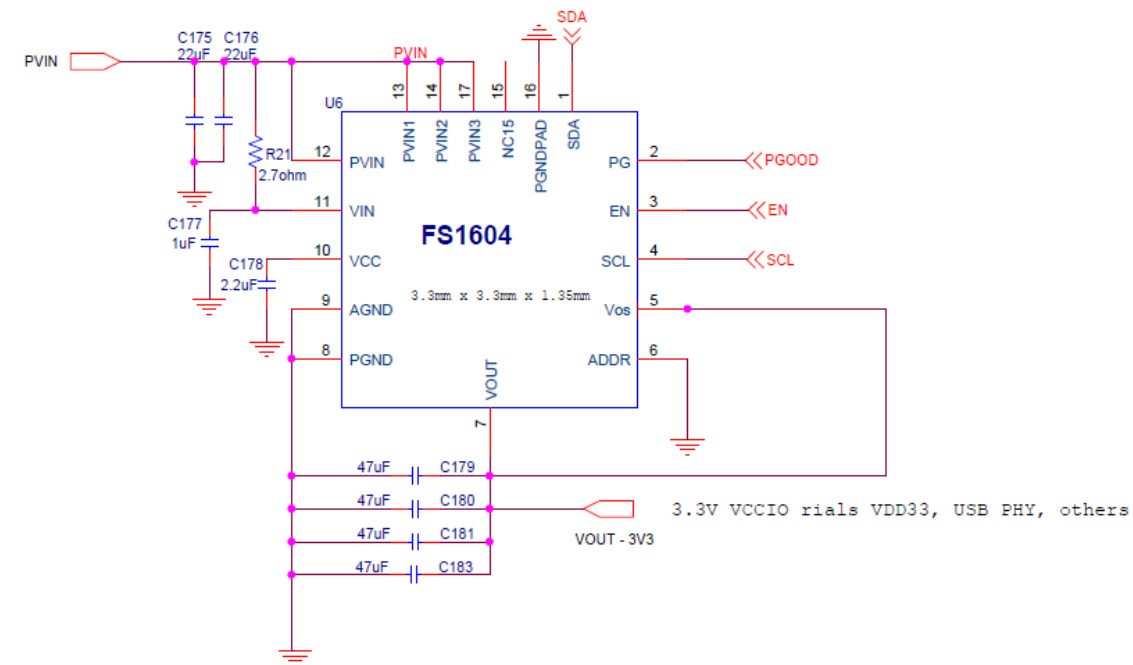
3.3V / 4A

VCCIO_HVIO_5A, VCCIO_HVIO_5B, VCCIO_HVIO_6D,
ADC - VREFPA, HPS ETH - AVDD_3P3, FPGA ETH - AVDD_3P3,
HDMI - MVDD, PLL - VDD_DIG, PLL - VDD_XTAL, PLL - VDDA,
USB HUB - VDD33, USB PHY - VBAT, USB PHY - VDD33

DC-DC Total Solution



7mm x 7mm = 49mm²



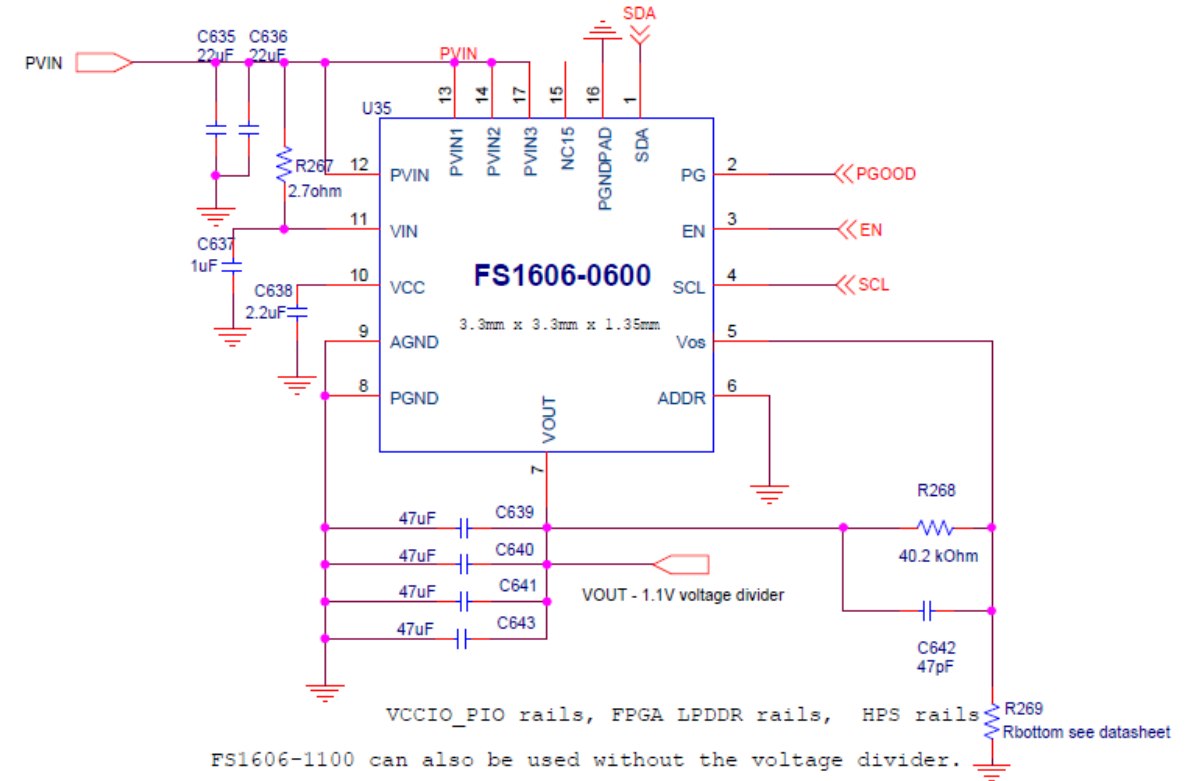
Other voltage rails for Agilex 5 Power Design



DC-DC Total Solution



7mm x 7mm = 49mm²



Attracting Tomorrow

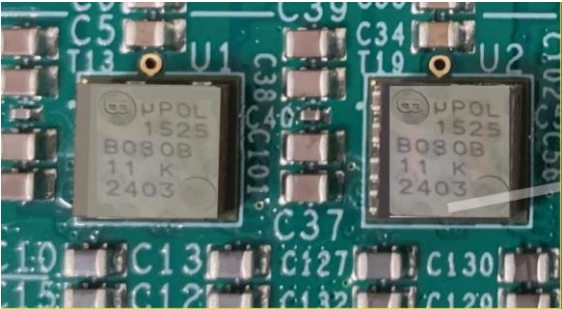
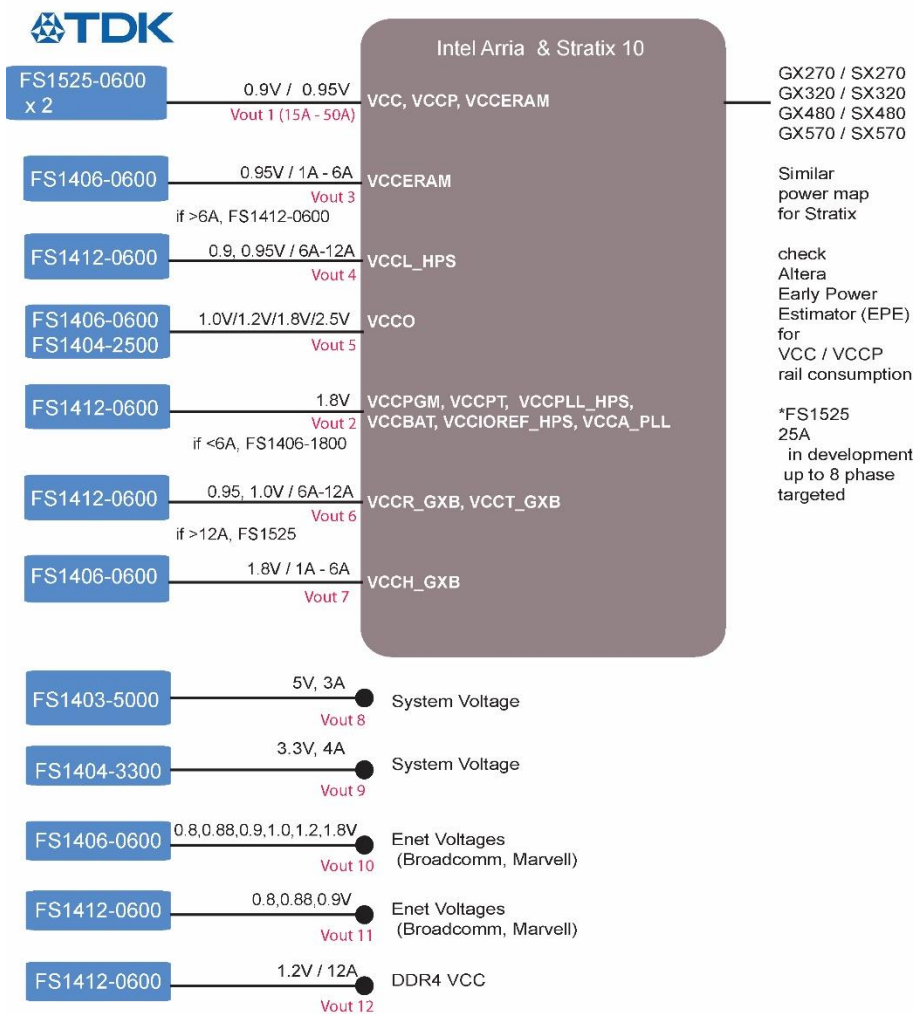


TDK μ POL:

Other Altera FPGA powered by TDK μ POL

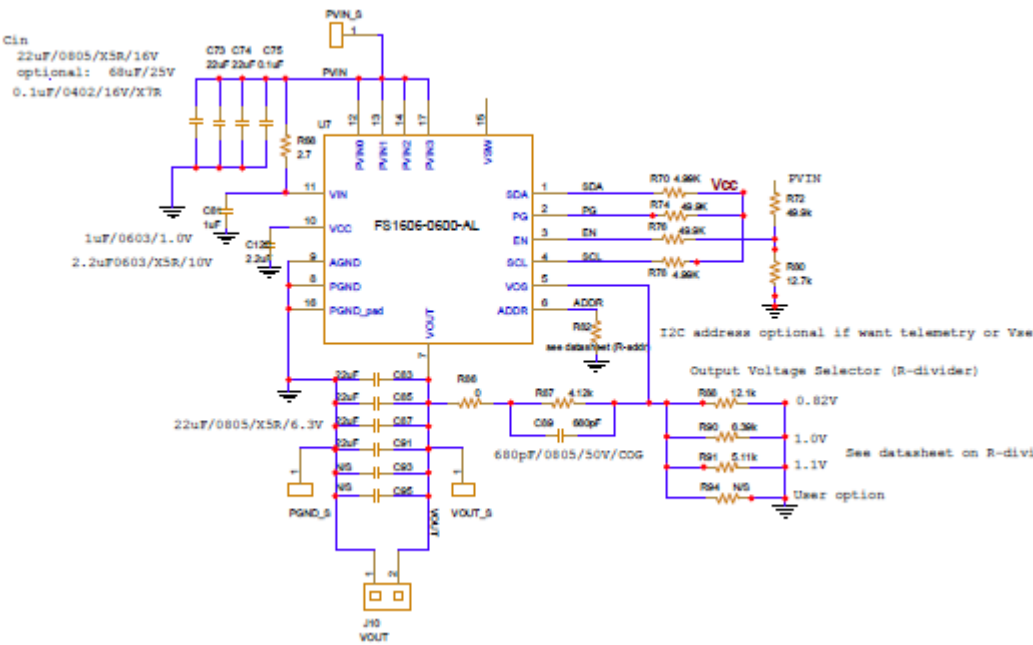
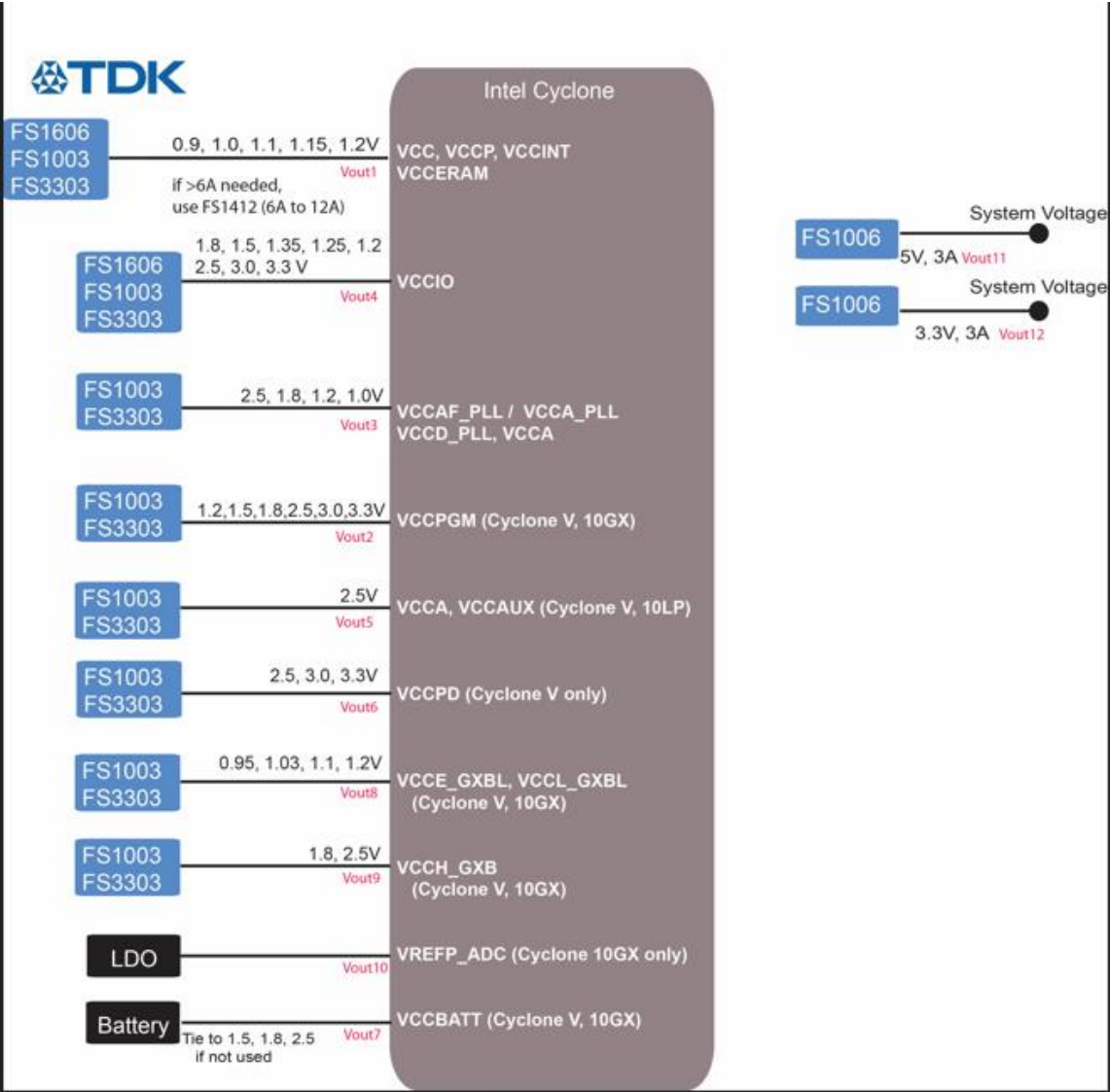
Stratix, Arria 10, Cyclone, Max10

TDK μ POL: Altera Stratix and Arria 10



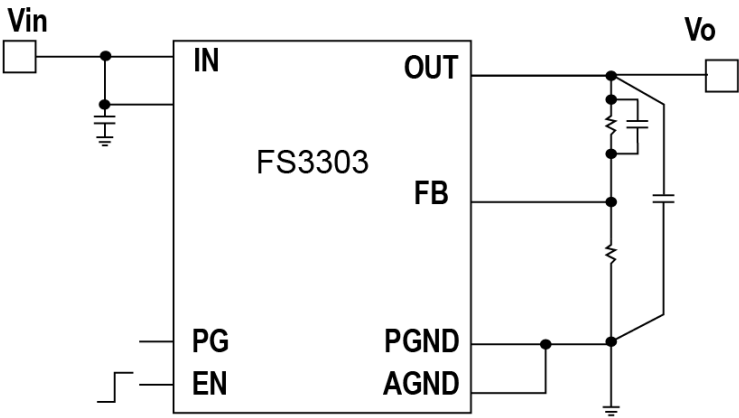
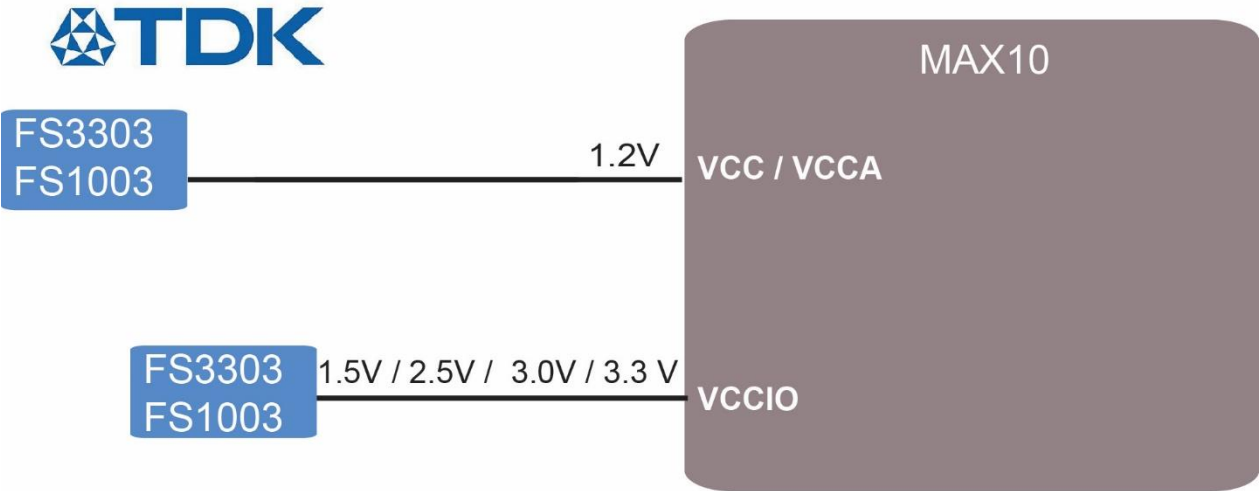
Shown 25A to 50A Vcore

FS1525 scalable for
Stratix and Arria 10
from 25A to 200A



Designs Available for 12Vin and 5Vin

		cyclone V	cyclone 10 LP	cyclone 10 GX
1	VCC, VCCINT, VCCP, VCCERAM	1.1, 1.15	1.0, 1.2	0.9
2	VCCPGM	1.8, 2.5, 3.0, 3.3	N/A	1.2, 1.5, 1.8
3	VCCAF_PLL, VCCA_PLL, VCCD_PLL	2.5	1.2, 1.0	1.8
4	VCCIO *	3.3, 3.0	3.3, 3.0	3.0, 2.5
		2.5, 1.8, 1.5, 1.35, 1.25, 1.2	2.5, 1.8, 1.5, 1.35, 1.25, 1.2	1.8, 1.5, 1.35, 1.25, 1.2
5	VCCA, VCCAUX	2.5	2.5	N/A
6	VCCPD	2.5, 3.0, 3.3	N/A	N/A
7	VCCBATT	BATT or 2.5V (not used)	N/A	Batt: 1.8, 1.2; connect to 1.5/1.8 if not used
10	VREFP_ADC	N/A	N/A	1.25 LDO
8	VCCE_GXBL, VCCL_GXBL	1.1, 1.2	N/A	1.03, 0.95
9	VCCH_GXBL	2.5	N/A	1.8



Attracting Tomorrow



TDK μ POL: FPGA/SoC power libraries on QSPICE and Simplis

FPGA / SoC Power Design Library (Coming Soon)

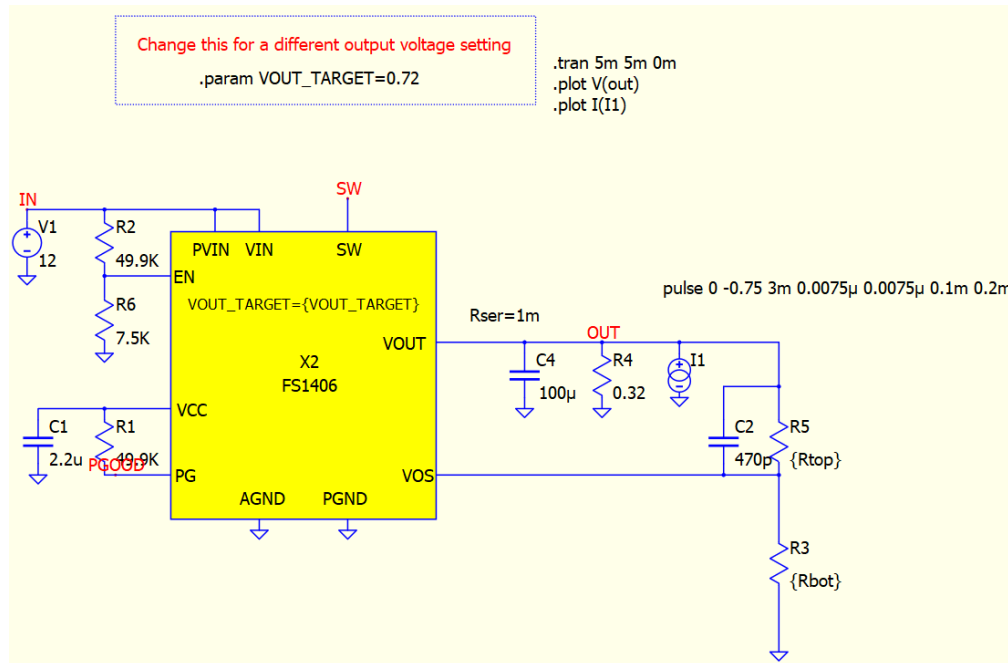
(click manufacturer for details)

- Xilinx
- Broadcom
- NXP
- Intel - FPGA
- Intel
- Microchip
- Marvell



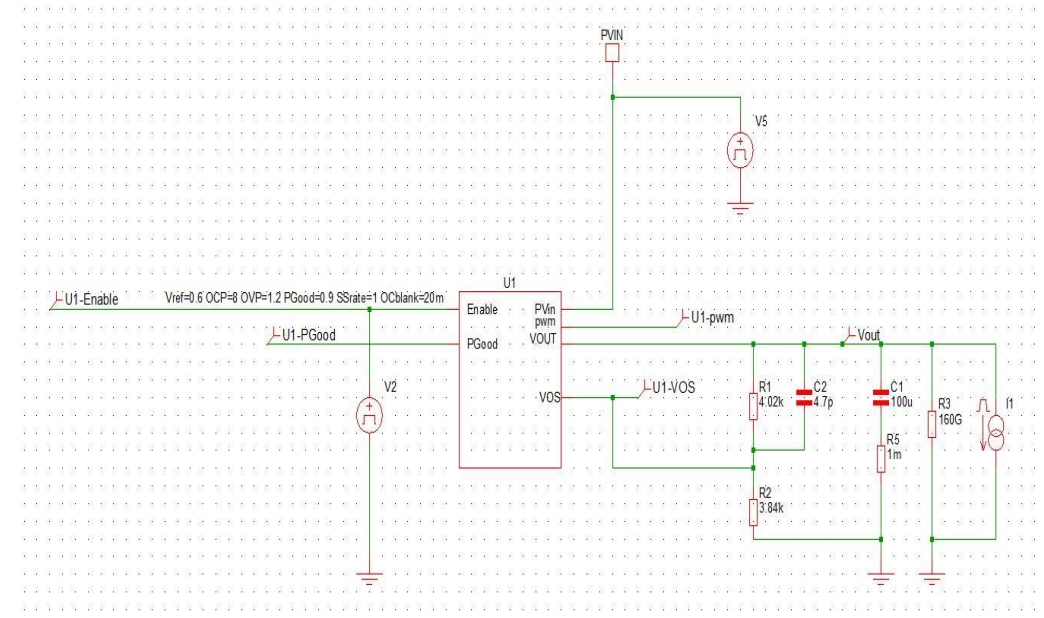
Power Tree / Map	Schematic/ BoM	Reference Design (DSN)	Power Design Guideline	QSPICE Models	Simplis Models
PDF	PDF	DSN (Cadence) schematic file in DSN format	PDF (Design Summary)	Zip File (FPGA power table with PDN power models by rail)	Zip File (FPGA power table with PDN power models by rail)

QSPICE



- ❑ New free circuit simulation software
- ❑ Runs much faster than LTSpice
- ❑ New models constantly being uploaded

SIMPLIS













- ❑ Powerful simulation software.
- ❑ Runs much faster than LTSpice
- ❑ Helps to analyze effect of parasitics












Available TDK μ POL Power Design Libraries: QSPICE and Simplis (as of August 2024)

www.us.tdk.com/POL

QSPICE Libraries

-  10 – 40W Power Strip DCDC Board QSPICE FS160x Rev. 1
-  Kintex Ultrascaleplus sim table Rev 1 QSpice
-  Avant-E Sims Table Rev 1 QSPICE
-  Versal Edge SIM Library Dbase QSPICE 1
-  Zynq US LoCost Zu1-Zu2-Zu3 sim table QSPICE
-  Artix 7 sim table rev2.0 QSPICE
-  Intel Arria 10 sim table rev0.2 QSPICE
-  Agilex 7 SIM Library QSPICE
-  Artix UltraScale sim table rev1.0 QSPICE
-  Intel Agilex 5 - sim table rev0.2 QSPICE

Simplis Libraries

-  Agilex 5 SIM Library SIMPLIS
-  Agilex 7 SIM Library SIMPLIS
-  Arria 10 SIM Library SIMPLIS
-  Artix UltraScale sim table rev1.0 SIMPLIS
-  Avant-E Sims Table SIMPLIS
-  Kintex UltraScaleplus sim table SIMPLIS
-  Spartan 7 sim table SIMPLIS
-  Versal Edge SIM Library Dbase SIMPLIS
-  Zynq US LoCost Zu1-Zu2-Zu3 sim table SIMPLIS
-  Zynq US+ Zu02-Zu04 sim table SIMPLIS
-  Zynq Zu5-Zu19 sim table SIMPLIS



Availability:

Qspice:

FS140x
FS160x

Simplis

FS140x
FS1412
FS1525 (single phase)

Locations of Design collateral support

Other Design Collaterals



Package Design Guidelines



Symbols Schematic Layout 3D



Package Reel Info POL



www.tdk.com