

Title: TEI0185 - System Overview

A4 Number: TEI0185
P001

Rev. 02

Date: 2023-11-15 Copyright: Trenz Electronic GmbH

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Filename: System Overview.SchDoc

| REV | Description | |
|-----|--|----|
| -01 | Initial revision | VT |
| -02 | 1. Change J29 power connector 2. Added clock signal 25MHz HPS_OSC_CLK1 to HPS_IOA_12 3. Added series resistor R394 to HPS_OSC_CLK1 4. Changed resistors value R169 , R172 , R179 , R190 33R to 100R 5. DIPSW1 connected from HPS_IO12 to HPS_IO2 | |

A

A

B

B

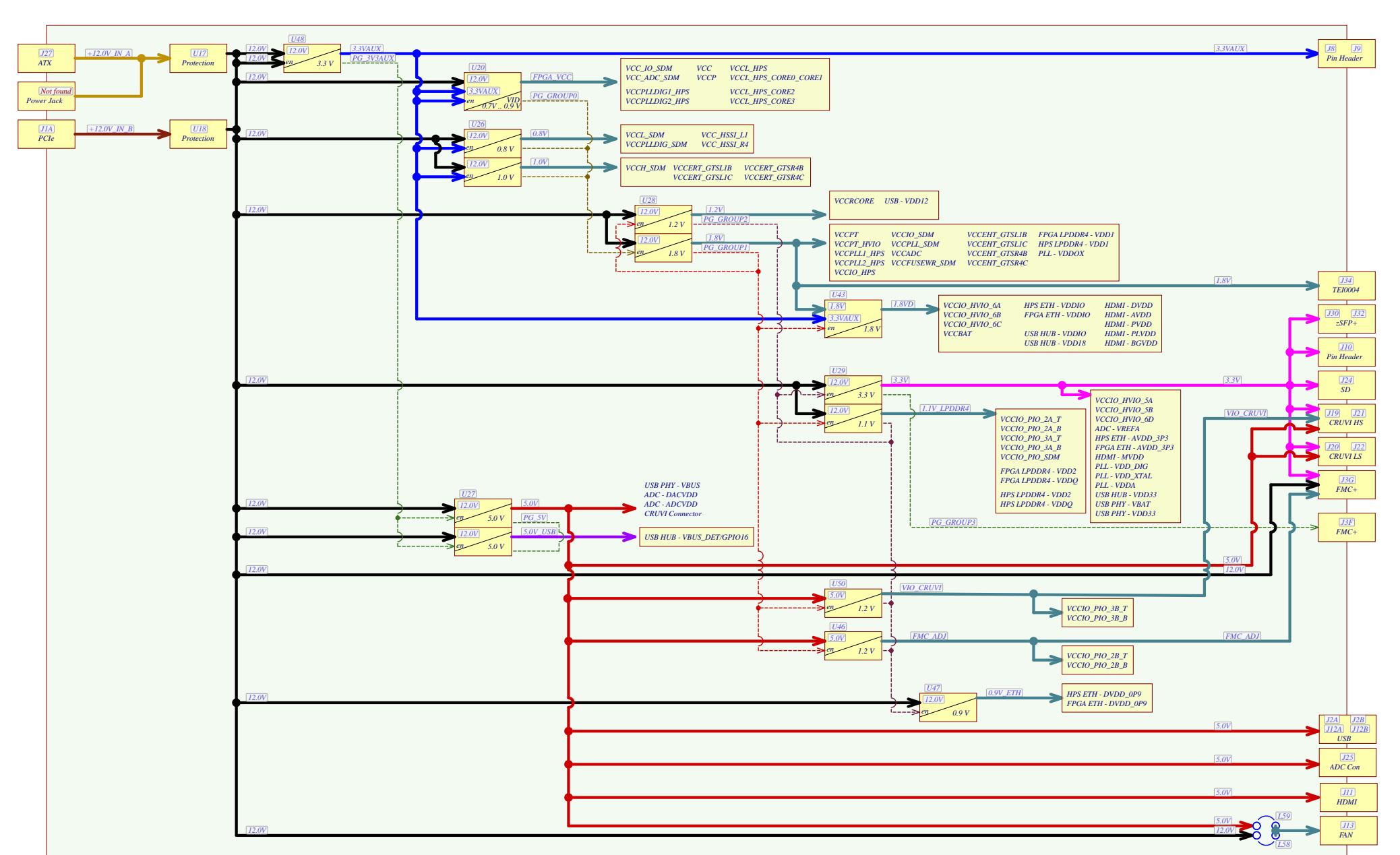
C

C

D

D

| | | | |
|-----------------------------------|----------------------------------|------|--------------|
| | Title: TE0185 - Revision Changes | | |
| A4 | Number: TE0185 P001 | Rev. | 02 |
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| Filename: Revision Changes.SchDoc | | | |



[12.0V]
Net name
Power bus
Control signal
PL_DCIN
0.9V
Power converter

| VID: | | | | | |
|--------|--------------|-------------|--------------|--------------------|--|
| Series | Device Group | Speed grade | Power Option | FPGA_VCC | |
| E | A | 1 | V | 0.70 V .. 0.90 V * | |
| | | 2 | E | | |
| | | 2 | V | | |
| | B | 3 | V | | |
| | | 4 | S | 0.8 V | |
| | | 5 | S | 0.78 V | |
| | | 6 | L | 0.75 V | |
| | | 6 | S | 0.75 V | |

*: The typical value is based on SmartVID programmed value.

Title: TEI0185 - Power Diagram

A3 Nummer: TEI0185 P001

Rev. 02

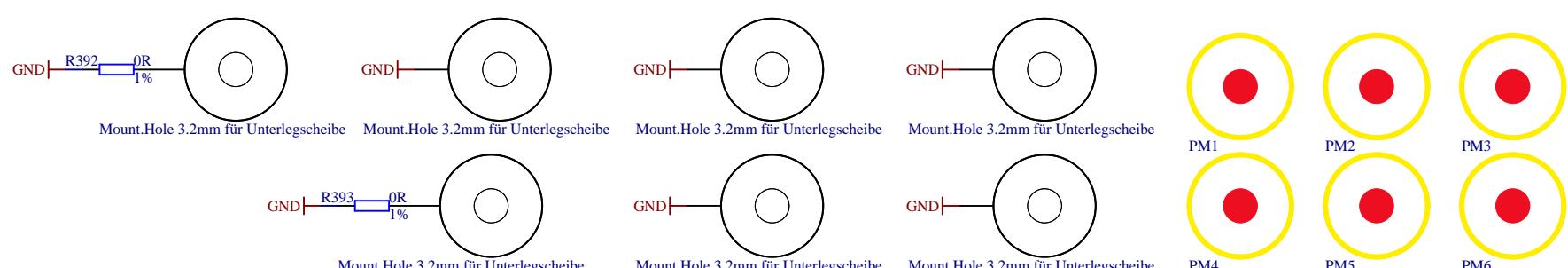
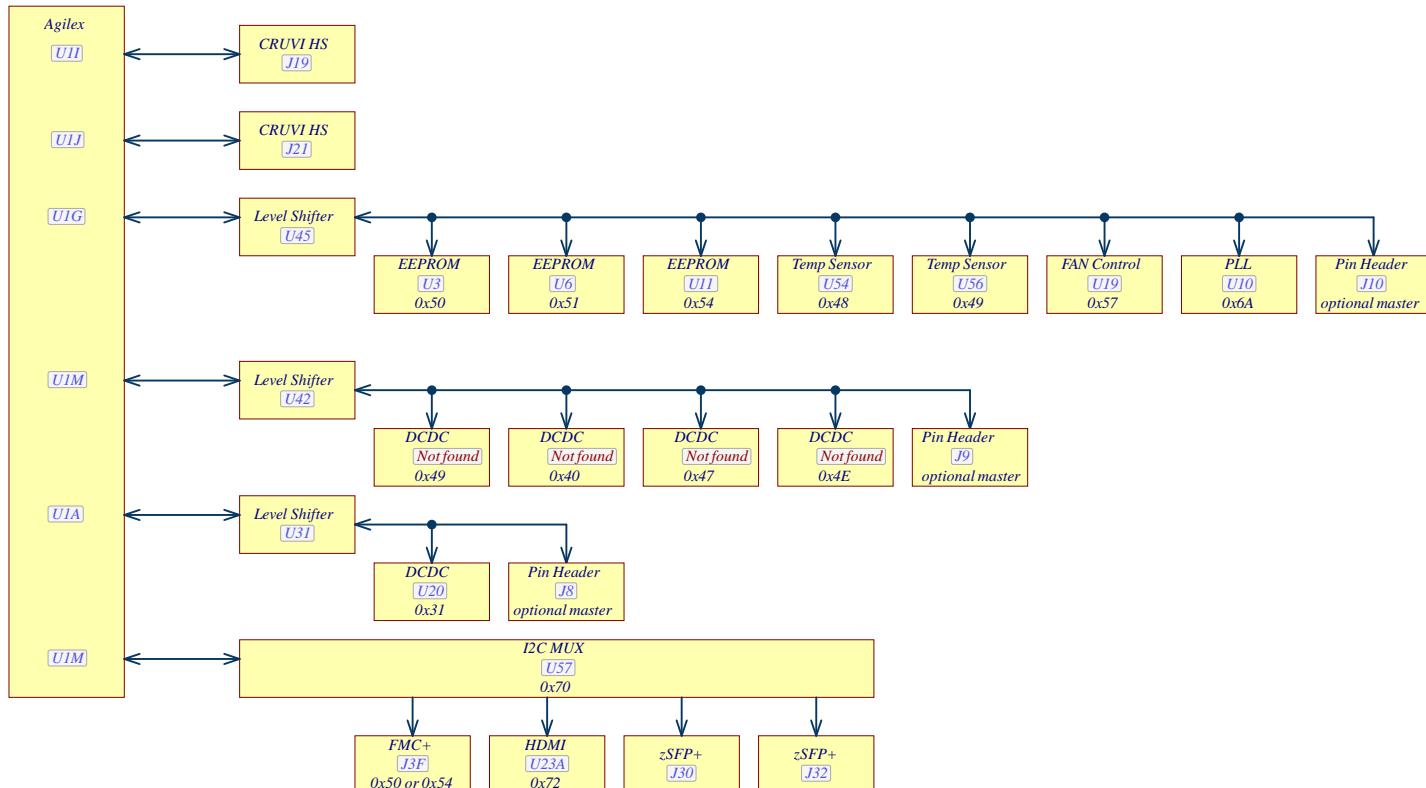
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Filename: Power_Diagram.SchDoc

1 2 3 4

I2C Structure:



CE Logo on Top Overlay

CE-TOPOVERLAY
RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY
WEEE

WEEE Logo on Top Overlay

WEEE-TOPOVERLAY
Serial1
Serial

Serialnumber 6,3 x 6,3mm

Design drawn by: VT

Checked by:

Assembly variant: P001

Created by:

Modified by:

Modified at: 2023-09-20

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1 2 3 4

A

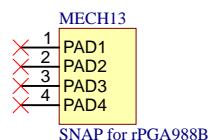
A

B

B

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C



SNAP for rPGA988B

D

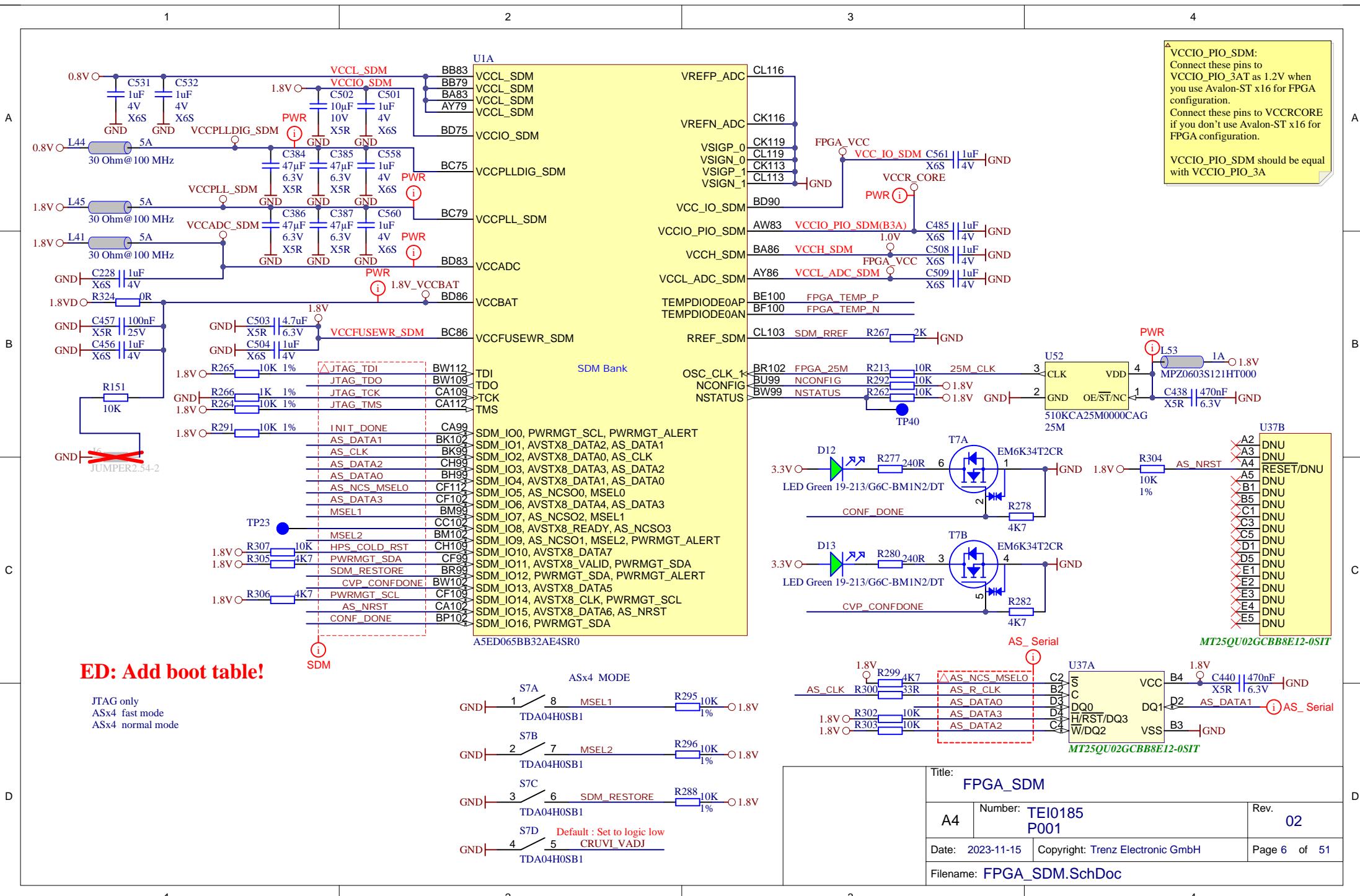
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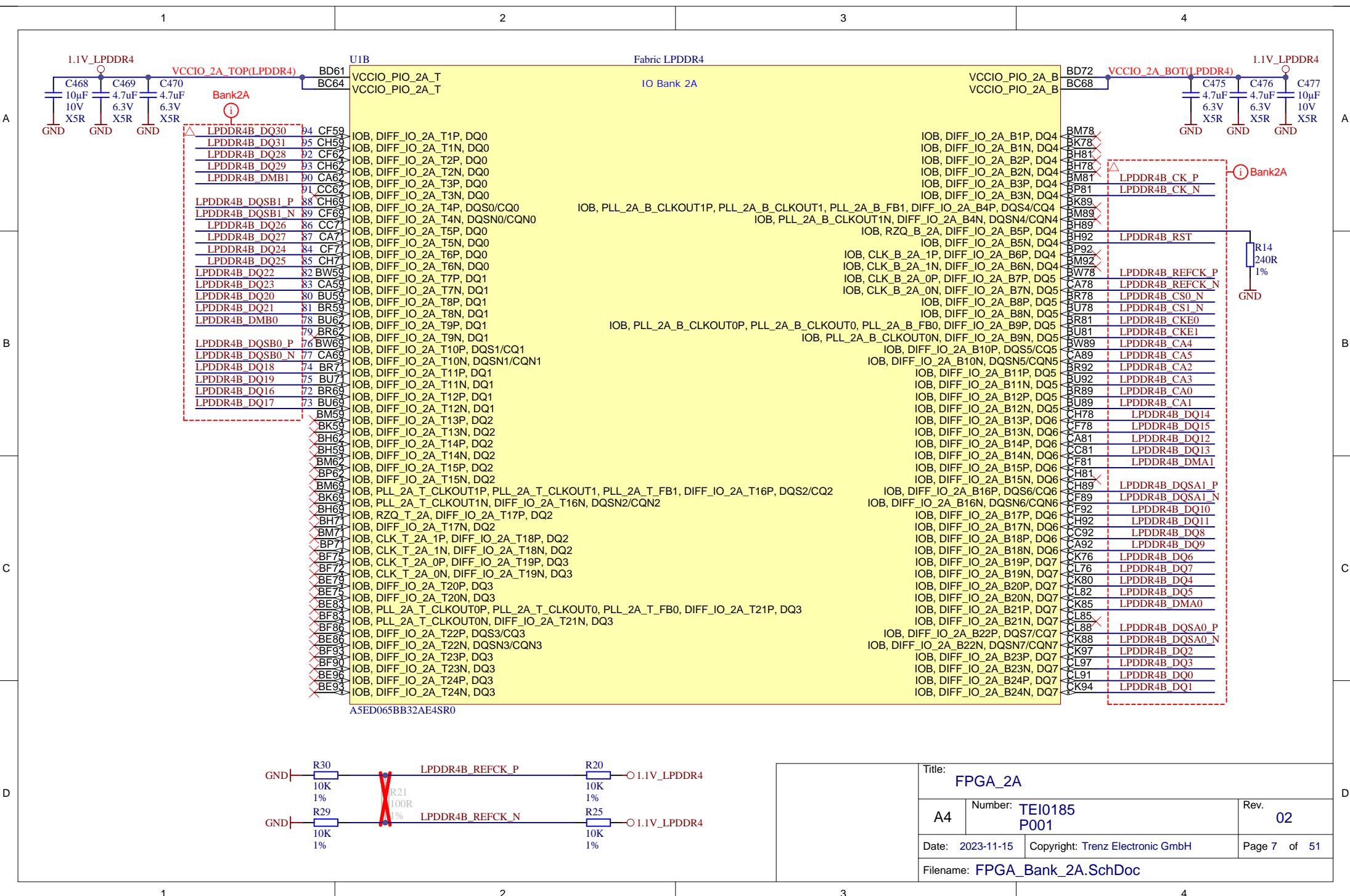
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FPGAA4 | Number: TEI0185
P001Rev.
02

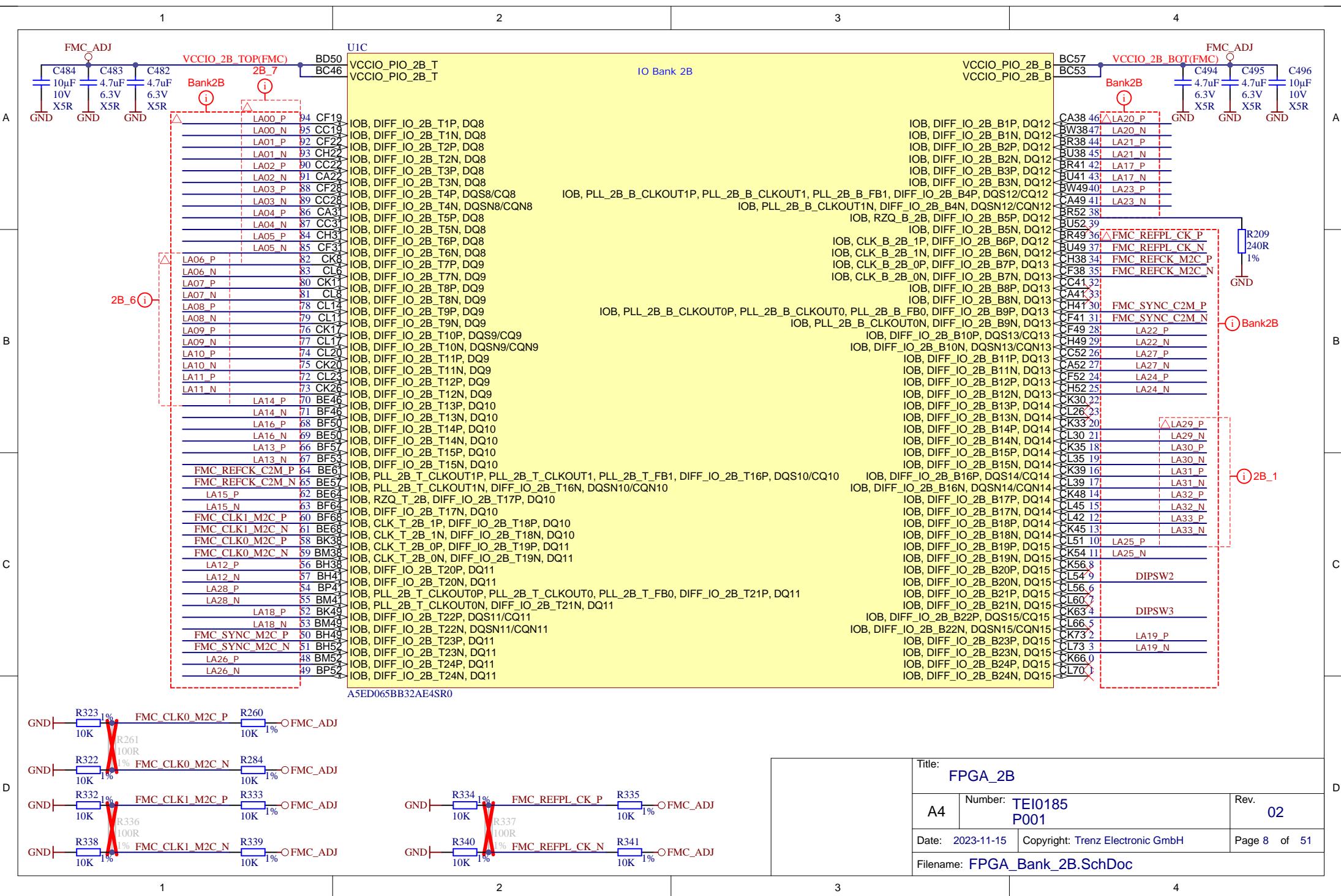
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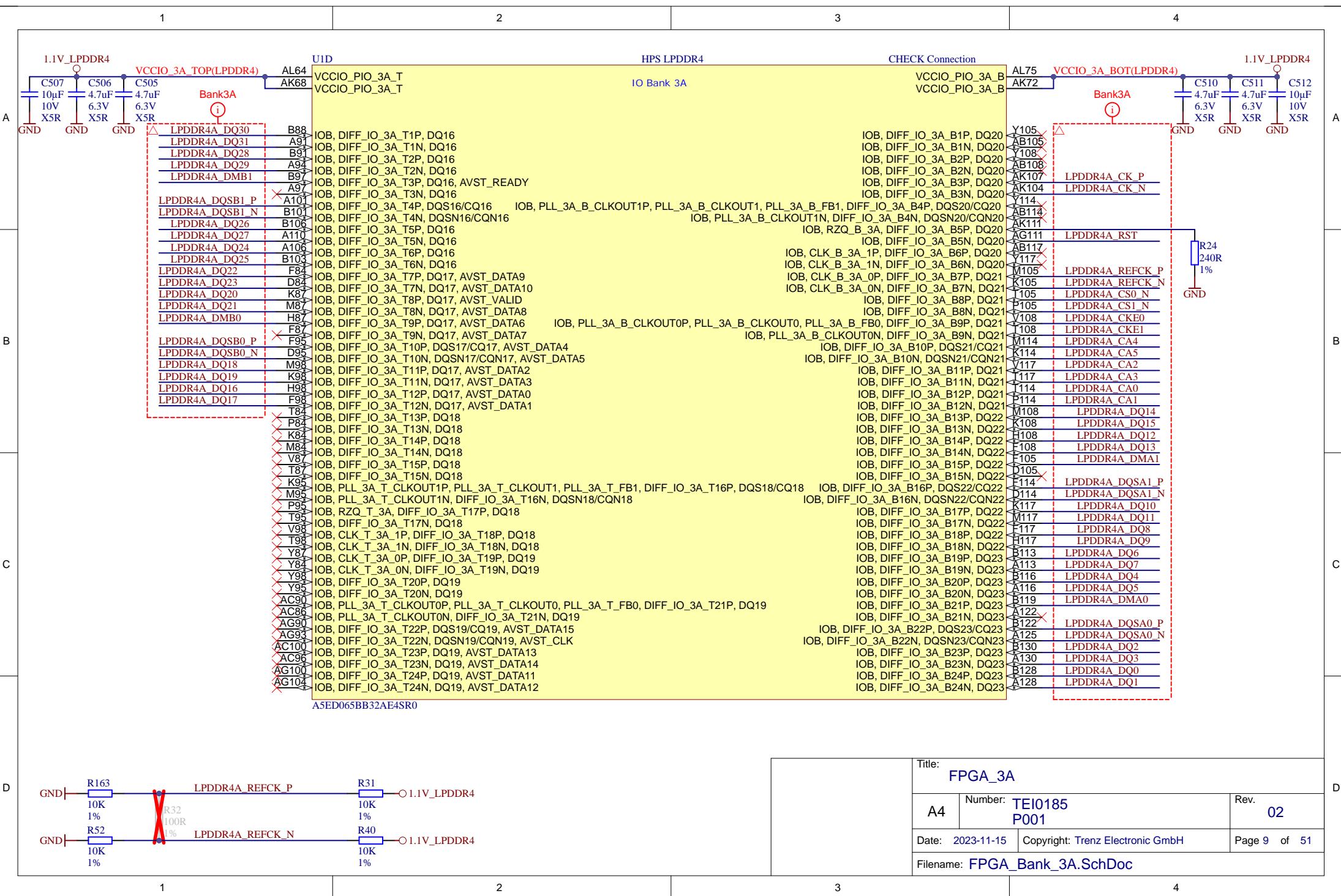
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Filename: FPGA.SchDoc







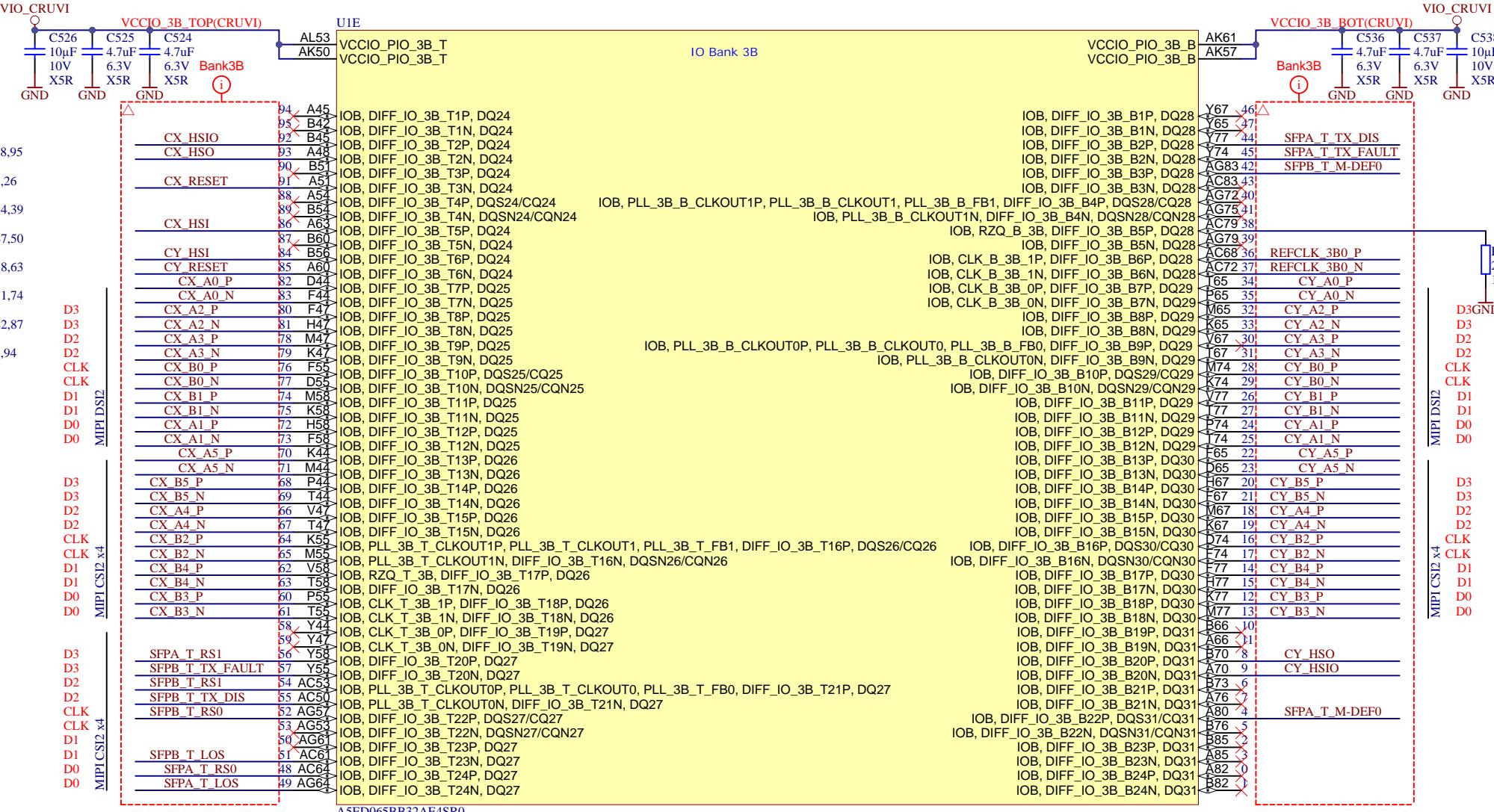


1

2

3

4



| Title: FPGA_3B | | Rev. 02 |
|--------------------------------------|----------------------------------|----------------|
| A4 | Number: TEI0185 P001 | |
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| Filename: FPGA_Bank_3B.SchDoc | | |

1

2

3

4

1.8VIO

HPS

(i)

U1G

| | | |
|--------------|-------|--|
| HPS_OSC_CLK | W135 | HPS_IOA_1, GPIO0_IO0, SPIM0_SS1_N, SPIM0_CLK, UART0_CTS_N, NAND_ADQ0, SDMMC_DATA0, USB0_CLK, EMAC0_PPS0, TRACE_D10 |
| DIPSW1 | U135 | HPS_IOA_2, GPIO0_IO1, SPIM1_SS1_N, SPIM0_MOSI, UART0_RTS_N, NAND_ADQ1, SDMMC_DATA1, USB0_STP, EMAC0_PPSTRIG0, TRACE_D9 |
| UART0_TX | W134 | HPS_IOA_3, GPIO0_IO2, SPIM0_SS0_N, UART0_RX, I2C1_SDA, NAND_WE_N, SDMMC_CLK, USB0_DIR, EMAC1_PPS1, TRACE_D8 |
| UART0_RX | AK115 | HPS_IOA_4, GPIO0_IO3, SPIM0_SS0_N, UART0_RX, I2C1_SCL, NAND_NE_N, USB0_DATA0, EMAC1_PPSTRIG1, TRACE_D7 |
| I2CO_SDA | U133 | HPS_IOA_5, GPIO0_IO4, SPIM0_CLK, UART1_CTS_N, I2C0_SDA, NAND_WP_N, SDMMC_WRITE_PROTECT, USB0_DATA1, EMAC2_PPS2, TRACE_D6 |
| I2CO_SCL | AL120 | HPS_IOA_6, GPIO0_IO5, SPIM0_MOSI, UART1_RTS_N, I2C0_SCL, NAND_ADQ2, SDMMC_DATA2, USB0_NXT, EMAC2_PPSTRIG2, TRACE_D5 |
| GPIO_LED0 | R134 | HPS_IOA_7, GPIO0_IO6, SPIM0_SS0_N, MDIO2_MDIO, MDUART1_RX, I2C_EMAC2_SDA, NAND_ADQ3, SDMMC_DATA3, USB0_DATA2, TRACE_D4 |
| GPIO_LED1 | AG115 | HPS_IOA_8, GPIO0_IO7, SPIM0_SS0_N, MDIO2_MDC, UART1_RX, I2C_EMAC2_SCL, NAND_CLE, SDMMC_CMD, USB0_DATA3, TRACE_D15 |
| PB0 | N135 | HPS_IOA_9, GPIO0_IO8, SPIM1_CLK, SPI1_SS0_N, MDIO1_MDC, I2C_EMAC1_SDA, NAND_ADQ4, SDMMC_DATA4, USB0_DATA4, I3C1_SDA, TRACE_D14 |
| PBI | AK120 | HPS_IOA_10, GPIO0_IO9, SPIM1_MOSI, SPI1_SS0_N, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ5, SDMMC_DATA5, USB0_DATA5, I3C1_SCL, TRACE_D13 |
| DIPSW0 | N134 | HPS_IOA_11, GPIO0_IO10, SPIM1_MISO, SPI1_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, USB0_DATA6, I3C0_SDA, TRACE_D12 |
| HPS_OSC_CLK1 | T134 | HPS_IOA_12, GPIO0_IO11, SPIM1_SS0_N, SPI1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, USB0_DATA7, I3C0_SCL, TRACE_D11 |
| USB_CLK | P135 | HPS_IOA_13, GPIO0_IO12, NAND_ALE, SDMMC_PU_PD_DATA2, USB1_CLK, EMAC0_TX_CLK, TRACE_D10 |
| USB_STP | L135 | HPS_IOA_14, GPIO0_IO13, NAND_CE_N, USB1_STP, EMAC0_TX_CTL, TRACE_D9 |
| USB_DIR | J135 | HPS_IOA_15, GPIO0_IO14, NAND_CE_N, USB1_DIR, EMAC0_RX_CLK, TRACE_D8 |
| USB_DATA0 | AD135 | HPS_IOA_16, GPIO0_IO15, NAND_DQS, SDMMC_DATA_STROBE, USB1_DATA0, EMAC0_RX_CTL, TRACE_D7 |
| USB_DATA1 | M132 | HPS_IOA_17, GPIO0_IO16, I3C1_SDA, NAND_ADQ8, USB1_DATA1, EMAC0_TXD0, TRACE_D6 |
| USB_NXT | AD133 | HPS_IOA_18, GPIO0_IO17, I3C1_SCL, NAND_ADQ9, USB1_NXT, EMAC0_TxD1, TRACE_D5 |
| USB_DATA2 | K132 | HPS_IOA_19, GPIO0_IO18, I3C0_SDA, NAND_ADQ10, USB1_DATA2, EMAC0_RXD0, TRACE_D4 |
| USB_DATA3 | AG129 | HPS_IOA_20, GPIO0_IO19, SPIM1_SS1_N, I3C0_SCL, NAND_ADQ11, USB1_DATA3, EMAC0_RXD1, TRACE_CLK |
| USB_DATA4 | J132 | HPS_IOA_21, GPIO0_IO20, SPIM1_CLK, SPI1_SS0_N, UART0_CTS_N, I2C1_SDA, NAND_ADQ12, USB1_DATA4, EMAC0_RXD2, TRACE_D0 |
| USB_DATA5 | AG120 | HPS_IOA_22, GPIO0_IO21, SPIM1_MOSI, SPI1_SS0_N, UART0_RTS_N, I2C1_SCL, NAND_ADQ13, USB1_DATA5, EMAC0_RXD3, TRACE_D1 |
| USB_DATA6 | G134 | HPS_IOA_23, GPIO0_IO22, SPIM1_MISO, SPI1_SS0_N, UART0_RX, I2C0_SDA, NAND_ADQ14, USB1_DATA6, EMAC0_RXD2, TRACE_D2 |
| USB_DATA7 | G135 | HPS_IOA_24, GPIO0_IO23, SPIM1_SS0_N, SPI1_MISO, UART0_RX, I2C0_SCL, NAND_ADQ15, USB1_DATA7, EMAC0_RXD3, TRACE_D3 |

A5ED065BB32AE4SR0

U1H

| | | | | | | |
|-----------|------|------|---------|-----------|--|--|
| SD_RDATA0 | R8 | 0R1% | SD_DAT0 | E135 | HPS_IoB_1, GPIO1_IO0, SPIM1_CLK, UART0_CTS_N, EMAC0_PPS0, NAND_ADQ0, SDMMC_DATA0, EMAC1_TX_CLK, TRACE_D10 | |
| SD_RDATA1 | R360 | 0R1% | SD_DAT1 | F132 | HPS_IoB_2, GPIO1_IO1, SPIM1_MOSI, UART0_RTS_N, EMAC0_PPSTRIG0, NAND_ADQ1, SDMMC_DATA1, EMAC1_TX_CTL, TRACE_D9 | |
| SD_RCLK | R361 | 0R1% | SD_CLK | D132 | HPS_IoB_3, GPIO1_IO2, SPIM1_MISO, UART0_RX, I2C0_SDA, NAND_WE_N, SDMMC_CLK, EMAC1_RX_CLK, TRACE_D8 | |
| | | | X | AG123 | HPS_IoB_4, GPIO1_IO3, SPIM1_SS0_N, UART0_RX, I2C0_SCL, NAND_NE_N, EMAC1_RX_CTL, TRACE_D7 | |
| SD_RDATA2 | R362 | 0R1% | USB_RST | B134 | HPS_IoB_5, GPIO1_IO4, SPIM1_SS1_N, SPI1_SS0_N, UART1_CTS_N, EMAC2_PPS2, NAND_WP_N, SDMMC_WRITE_PROTECT, I3C1_SDA, EMAC1_TxD0, TRACE_D6 | |
| SD_RDATA3 | R363 | 0R1% | SD_DAT2 | AA132 | HPS_IoB_6, GPIO1_IO5, SPI1_SS0_N, SPI1_SS1_N, EMAC2_PPSTRIG2, NAND_ADQ2, SDMMC_DATA2, I3C1_SCL, EMAC1_TxD1, TRACE_D5 | |
| SD_RCMD | R364 | 0R1% | SD_DAT3 | V127 | HPS_IoB_7, GPIO1_IO6, SPI1_SS0_N, UART1_RX, I2C1_SDA, NAND_ADQ3, SDMMC_DATA3, I3C0_SDA, EMAC1_RXD0, TRACE_D4 | |
| | | | X | SD_CMD | AB132 | HPS_IoB_8, GPIO1_IO7, SPI1_MISO, SPI1_SS0_N, UART1_RX, I2C1_SCL, NAND_CLE, SDMMC_CMD, I3C0_SCL, EMAC1_RXD1, TRACE_D15 |
| | | | | ETH_MDI0 | T124 | HPS_IoB_9, GPIO1_IO8, JTAG_TCK, SPI0_CLK, MDIO2_MDIO, I2C_EMAC2_SDA, NAND_ADQ4, SDMMC_DATA4, EMAC1_TxD2, TRACE_D14 |
| | | | | ETH_MDC | Y132 | HPS_IoB_10, GPIO1_IO9, JTAG_TCK, SPI0_CLK, MDIO2_MDC, I2C_EMAC2_SCL, NAND_ADQ5, SDMMC_DATA5, EMAC1_TxD3, TRACE_D13 |
| | | | | ETH_RST | T125 | HPS_IoB_11, GPIO1_IO10, JTAG_TDO, SPI0_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ6, SDMMC_DATA6, EMAC1_RXD2, TRACE_D12 |
| | | | | SD_DETECT | P124 | HPS_IoB_12, GPIO1_IO11, JTAG_TDI, SPI0_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ7, SDMMC_DATA7, EMAC1_RXD3, TRACE_D11 |
| | | | | ETH_TXCK | M127 | HPS_IoB_13, GPIO1_IO12, I2C1_SDA, NAND_ALE, SDMMC_PU_PD_DATA2, EMAC2_TX_CLK, TRACE_D10 |
| | | | | ETH_RXCTL | K124 | HPS_IoB_14, GPIO1_IO13, I2C1_SCL, NAND_RB_N, SDMMC_PWR_ENA, EMAC2_RX_CTL, TRACE_D9 |
| | | | | ETH_RXCK | M124 | HPS_IoB_15, GPIO1_IO14, UART1_RX, NAND_CE_N, I3C1_SDA, EMAC2_RX_CLK, TRACE_D8 |
| | | | | ETH_TXDO | K124 | HPS_IoB_16, GPIO1_IO15, UART1_RX, NAND_DQS, SDMMC_DATA_STROBE, I3C1_SCL, EMAC2_RX_CTL, TRACE_D7 |
| | | | | ETH_RXD1 | Y127 | HPS_IoB_17, GPIO1_IO16, UART1_CTS_N, NAND_ADQ8, I3C0_SDA, EMAC2_RXD0, TRACE_D6 |
| | | | | ETH_RXD0 | H124 | HPS_IoB_18, GPIO1_IO17, SPI0_SS1_N, UART1_RTS_N, NAND_ADQ9, I3C0_SCL, EMAC2_TxD1, TRACE_D5 |
| | | | | ETH_RXD1 | AB124 | HPS_IoB_19, GPIO1_IO18, SPI0_MISO, MDIO1_MDIO, I2C_EMAC1_SDA, NAND_ADQ10, EMAC2_RXD0, TRACE_D4 |
| | | | | ETH_RXD2 | F127 | HPS_IoB_20, GPIO1_IO19, SPI0_SS0_N, MDIO1_MDC, I2C_EMAC1_SCL, NAND_ADQ11, EMAC2_RXD1, TRACE_CLK |
| | | | | ETH_RXD3 | Y127 | HPS_IoB_21, GPIO1_IO20, SPI0_SS0_N, SPI1_SS0_N, I2C_EMAC2_SDA, NAND_ADQ12, EMAC2_TxD2, TRACE_D0 |
| | | | | ETH_RXD2 | F124 | HPS_IoB_22, GPIO1_IO21, SPI0_MOSI, SPI1_SS0_N, I2C_EMAC2_SCL, NAND_ADQ13, EMAC2_TxD3, TRACE_D1 |
| | | | | ETH_RXD3 | D124 | HPS_IoB_23, GPIO1_IO22, SPI0_MISO, SPI1_SS0_N, MDIO0_MDIO, I2C_EMAC0_SDA, NAND_ADQ14, EMAC2_RXD2, TRACE_D2 |
| | | | | | | HPS_IoB_24, GPIO1_IO23, SPI0_SS0_N, SPI1_MISO, MDIO0_MDC, I2C_EMAC0_SCL, NAND_ADQ15, EMAC2_RXD3, TRACE_D3 |

A5ED065BB32AE4SR0

R394

10R

1%

R212

10R

1%

25M

CK

GND

2

CLK

VDD

4

1

GND

OE/ST/NC

2

1

PWR

i

L52

O 1.8V

C437

6.3V

X5R

1A

MPZ0603S121HT000

Title: FPGA_HPS
A4 Number: TEI0185 P001Rev. 02
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Filename: FPGA_Bank_HPS.SchDoc

A

A

B

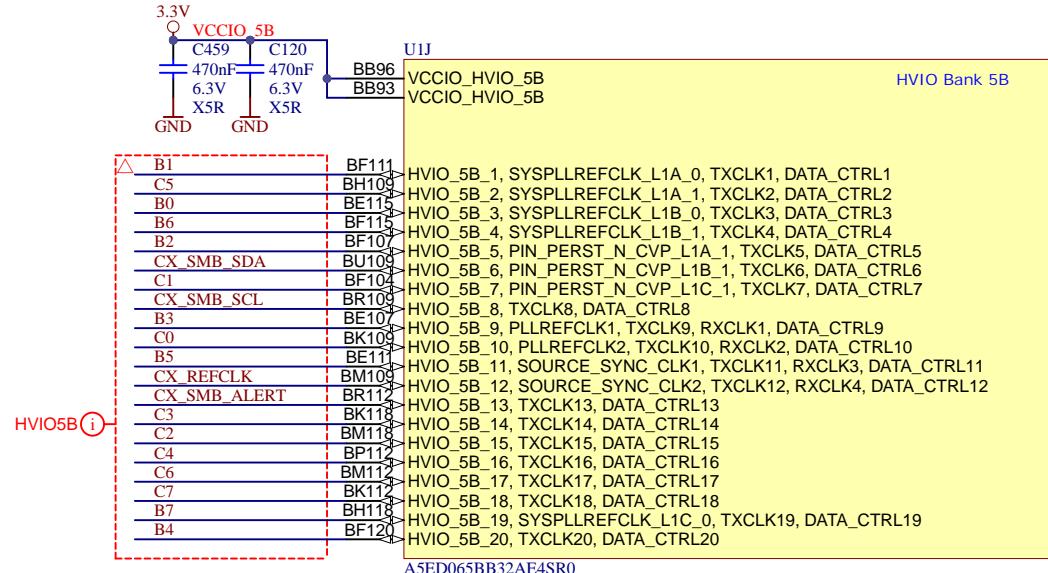
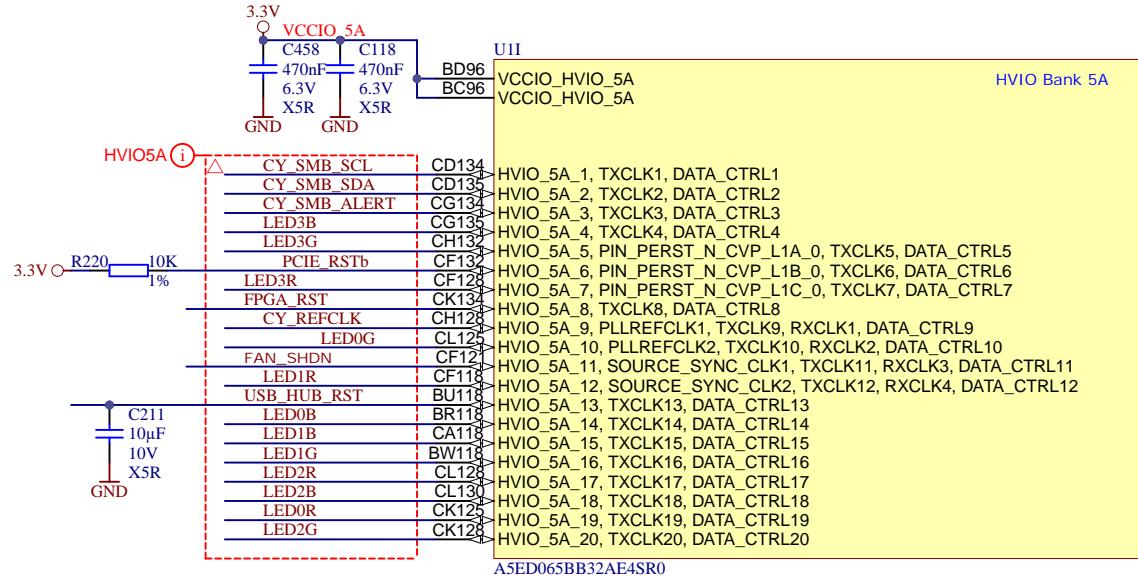
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C

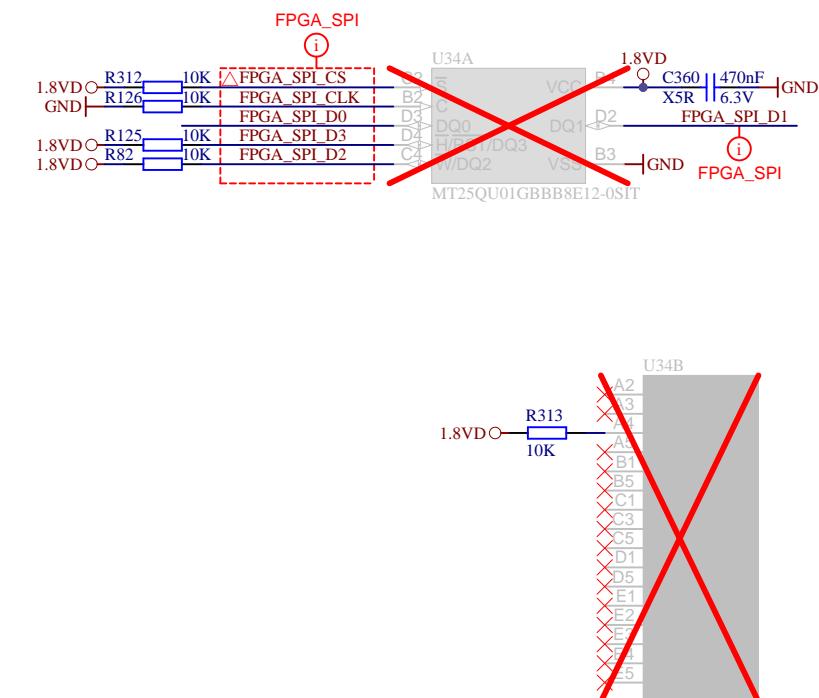
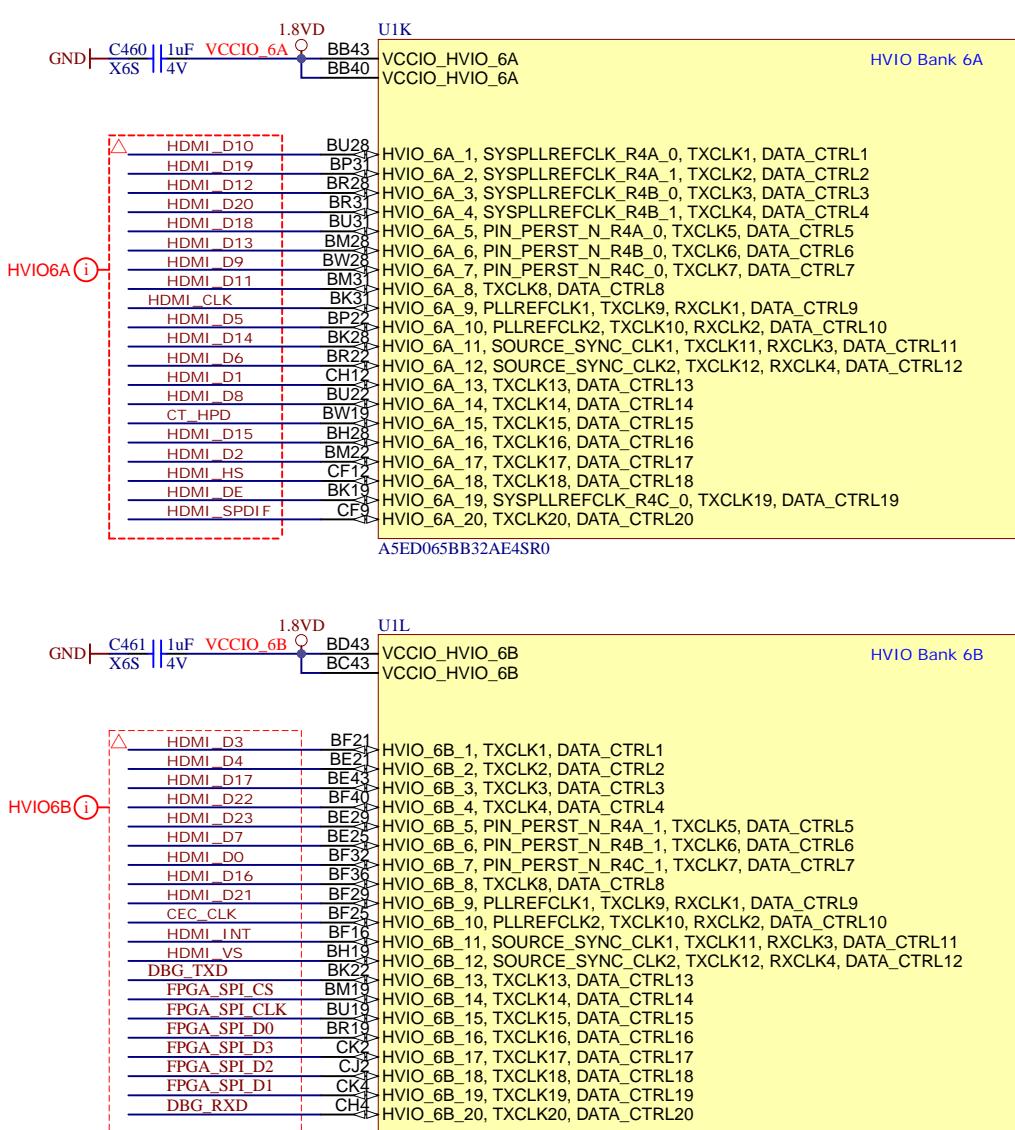
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D

D

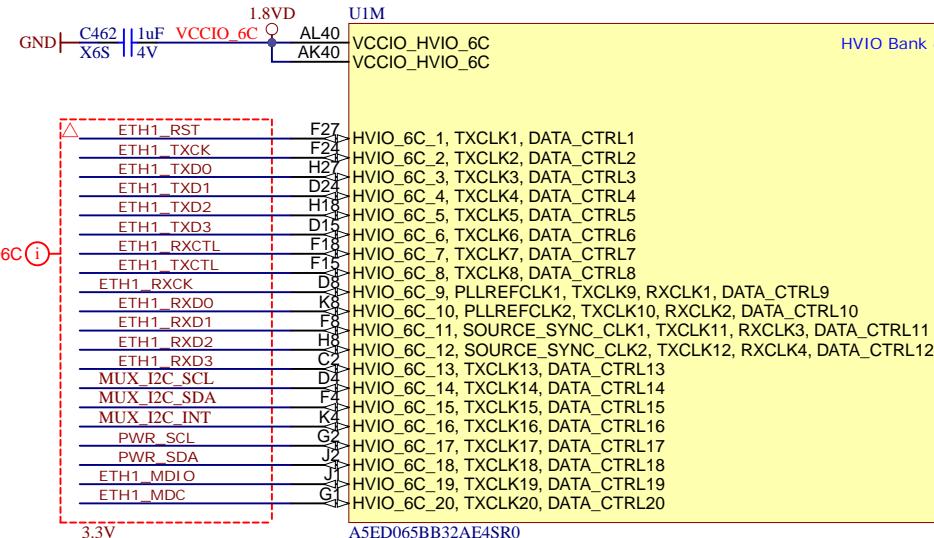


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| | | Title: FPGA_5A_5B | |
| A4 | Number: TEI0185 P001 | Rev. 02 | |
| Date: 2023-11-21 | Copyright: Trenz Electronic GmbH | Page 12 of 51 | |
| Filename: FPGA_Bank_HVIO_5A_5B.SchDoc | | | |

Title: **FPGA_6A_6B**A4 | Number: **TEI0185
P001**Rev. **02**Date: **2023-11-21** Copyright: **Trenz Electronic GmbH**Page **13** of **51**Filename: **FPGA_Bank_HVIO_6A_6B.SchDoc**

A

Hvio Bank 6C



B

Hvio Bank 6D

C

Title: FPGA_6C_6D

A4 | Number: TEI0185
P001

Rev. 02

Date: 2023-11-21 Copyright: Trenz Electronic GmbH

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Filename: FPGA_Bank_HVIO_6C_6D.SchDoc

A

A

B

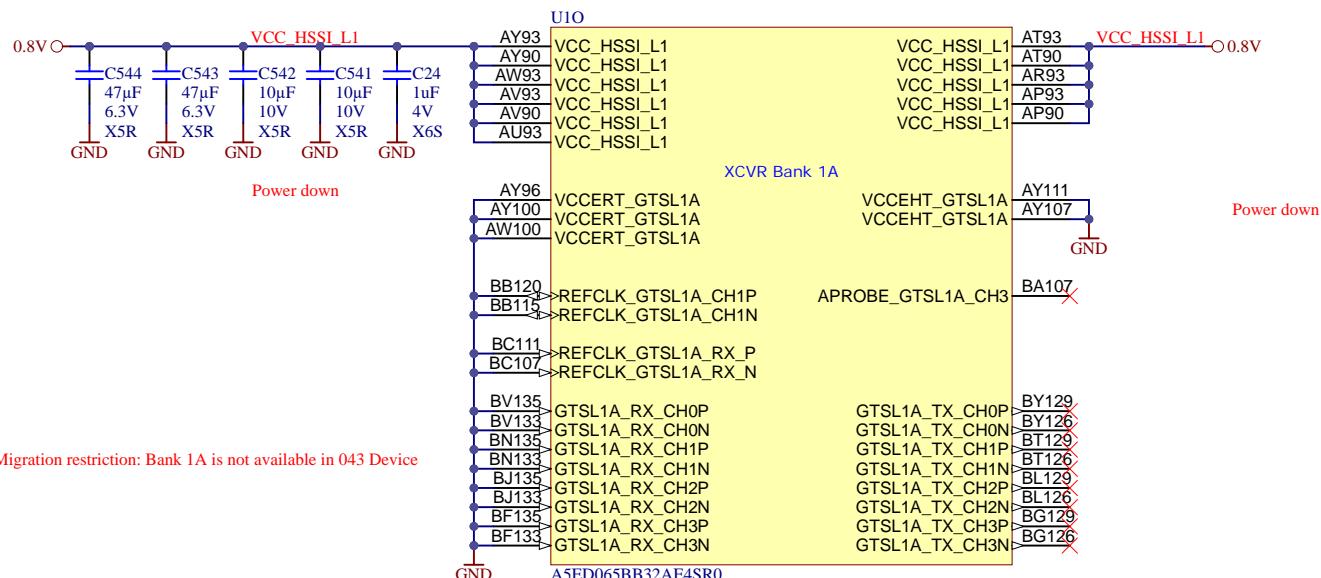
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C

C

D

D



Title: **FPGA_1A**

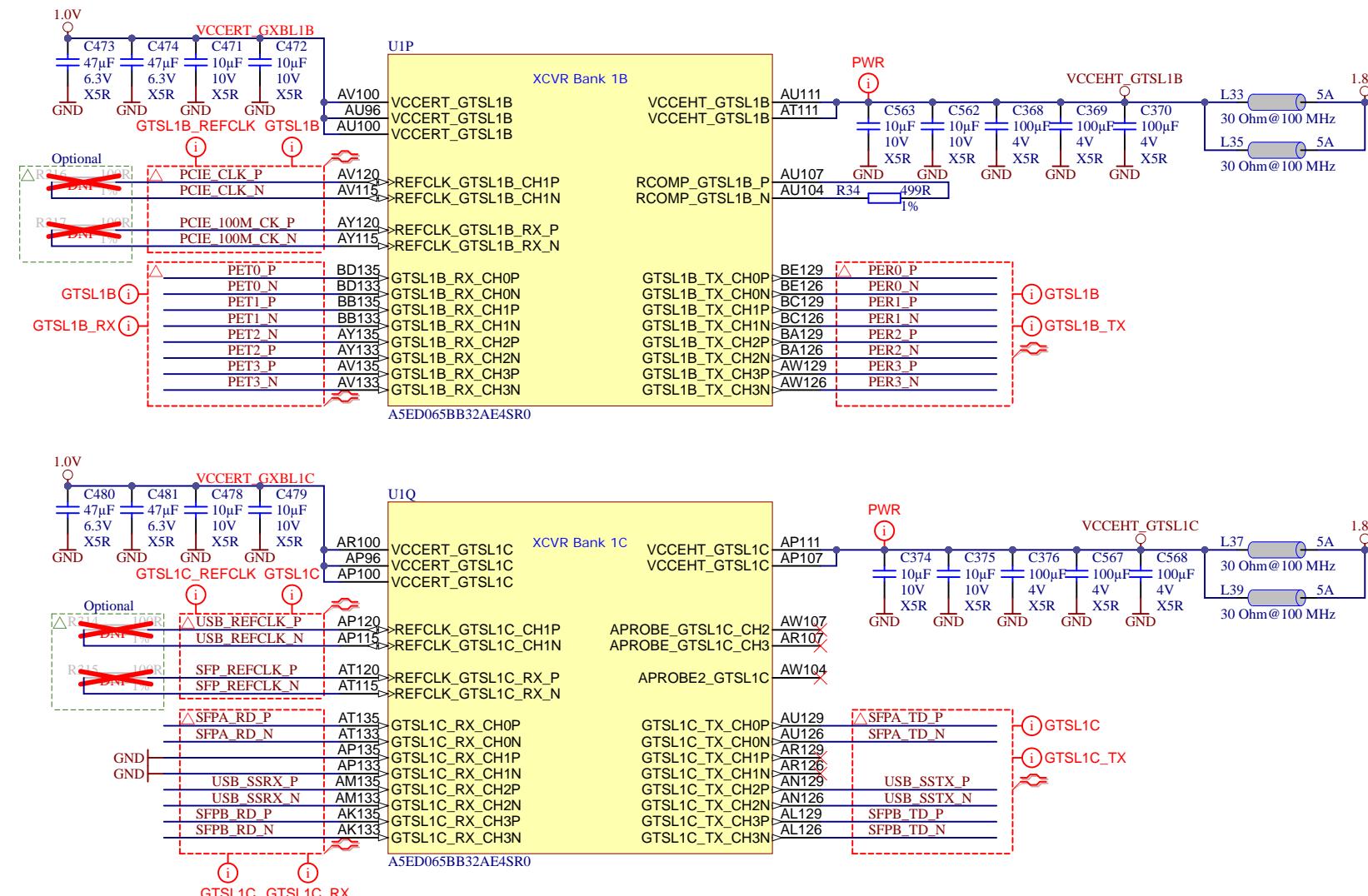
A4 Number: **TEI0185
P001**

Rev. **02**

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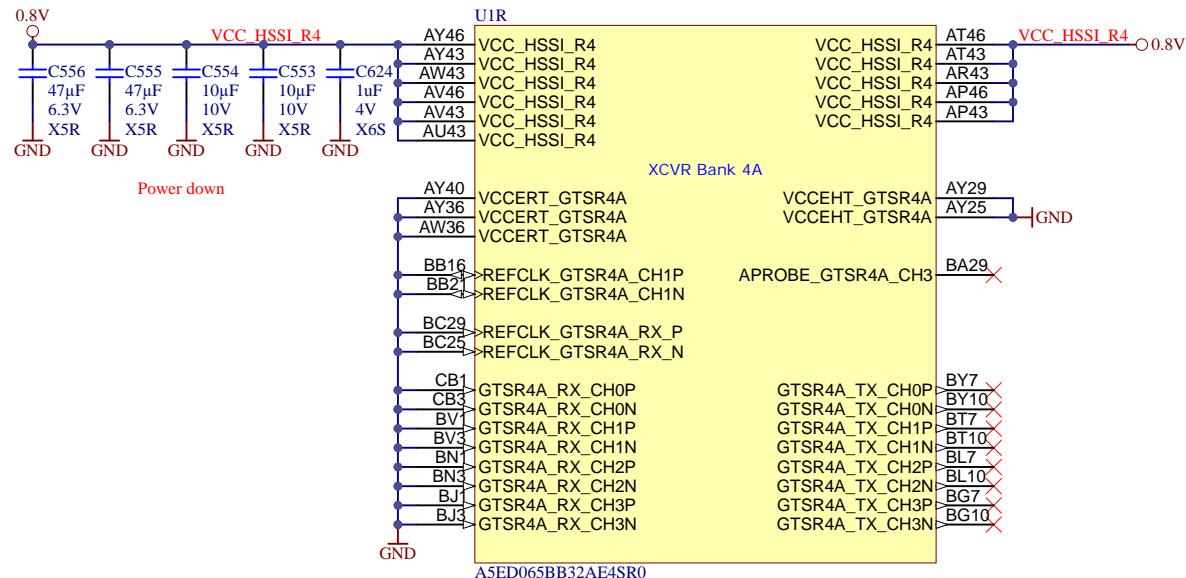
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|---|---|----------------|--------------|
| | Title: FPGA_1B_1C | | |
| A4 | Number: TEI0185 P001 | Rev. 02 | |
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| Filename: FPGA_XCVR_1B_1C.SchDoc | | | |

A

A



B

B

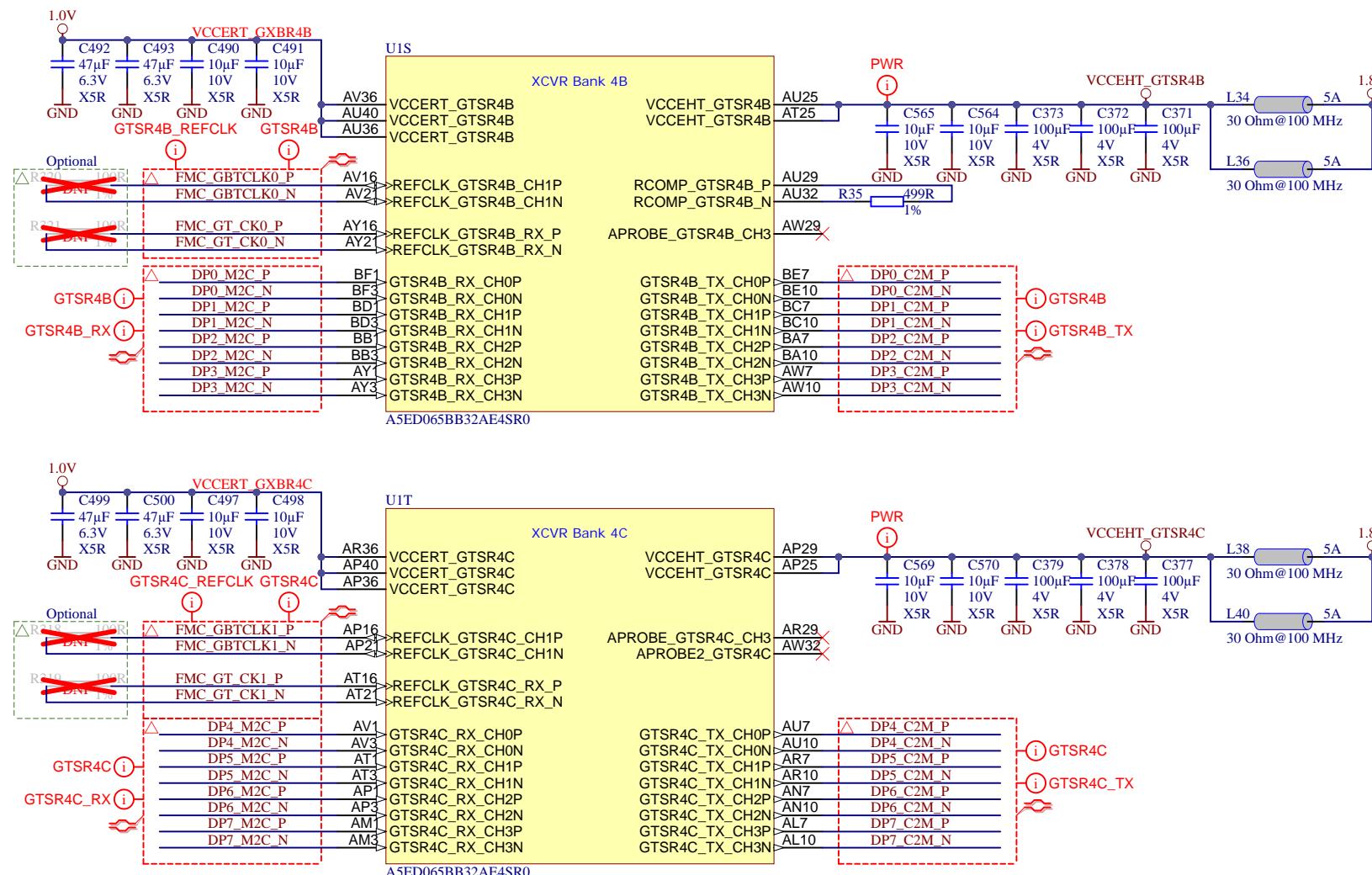
C

C

D

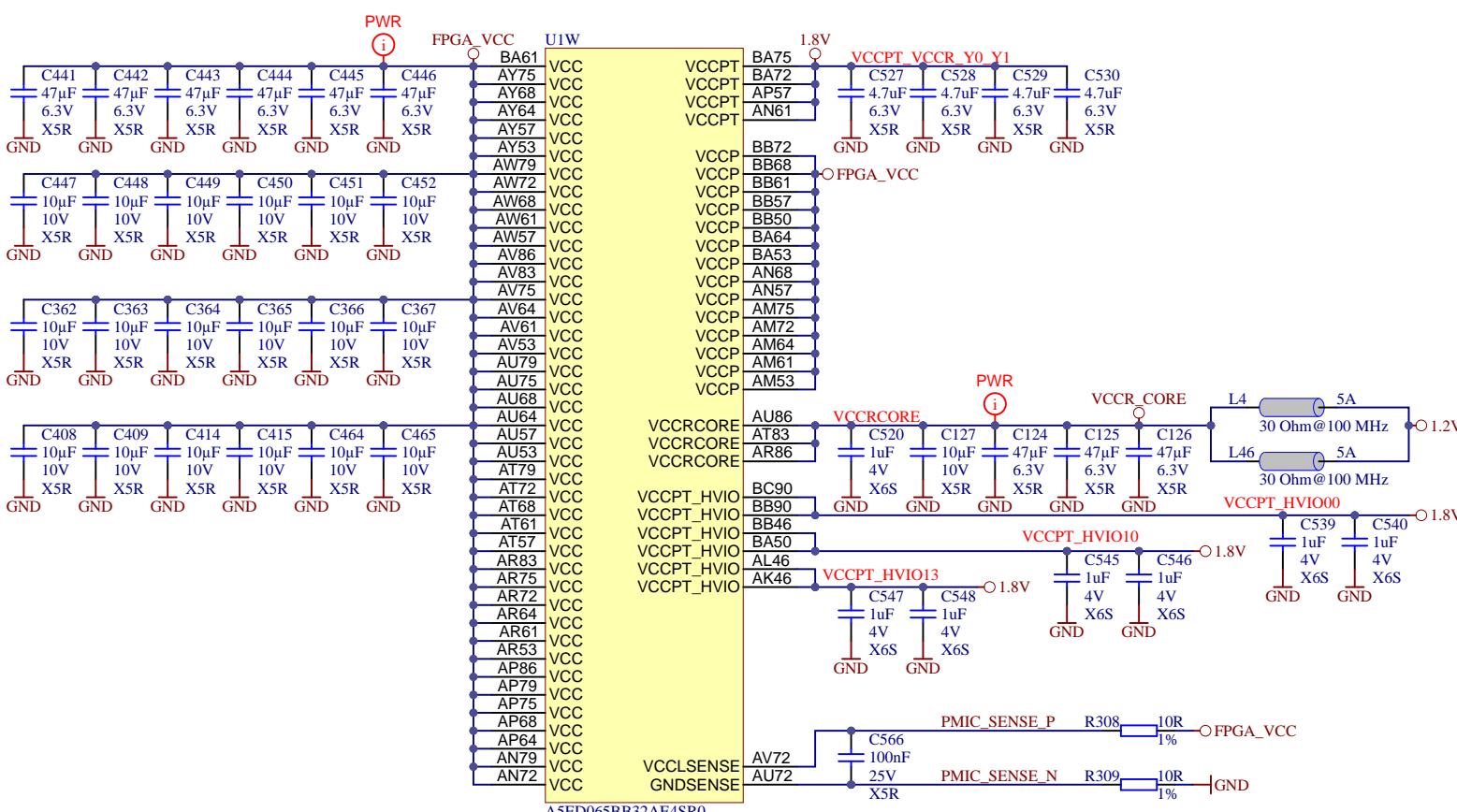
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| | | |
|--------------------------------------|---|-----------------------------|
| Title: FPGA_4A | | |
| A4 | Number: TEI0185 P001 | Rev. 02 |
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|---|---|-----------------------------|
| | Title: FPGA_4B_4C | |
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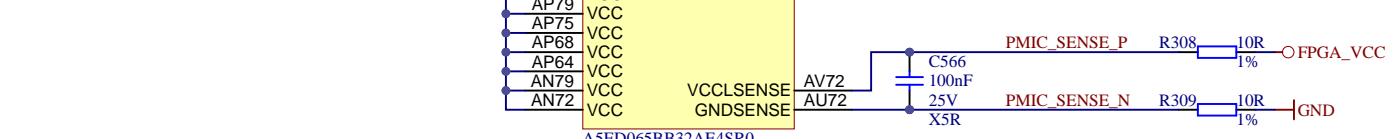
A



B

| U1V | |
|-------|------|
| AA1 | BD16 |
| AB4 | NC |
| AB8 | NC |
| AB15 | NC |
| AB18 | NC |
| AB24 | NC |
| AB27 | NC |
| AC36 | NC |
| AC43 | NC |
| AC46 | NC |
| AD1 | NC |
| AD2 | NC |
| AE4 | NC |
| AF2 | NC |
| AG13 | NC |
| AG21 | NC |
| AG29 | NC |
| AG36 | NC |
| AG40 | NC |
| AH4 | NC |
| AH8 | NC |
| AJ1 | NC |
| AJ2 | NC |
| AK16 | NC |
| AK21 | NC |
| AK25 | NC |
| AK32 | NC |
| AL16 | NC |
| AL25 | NC |
| AL29 | NC |
| AL32 | NC |
| AL104 | NC |
| AL107 | NC |
| AM16 | NC |
| AM43 | NC |
| AM46 | NC |
| AM50 | NC |
| AN25 | NC |
| AN29 | NC |
| AN50 | NC |
| AN107 | NC |
| AN111 | NC |
| AP50 | NC |
| AP53 | NC |
| AR50 | NC |
| AT50 | NC |
| AU50 | NC |
| AV50 | NC |
| AW50 | NC |
| AY50 | NC |
| | Y34 |
| | Y37 |

C



Title: FPGA_Power

A4 Number: TEI0185
P001

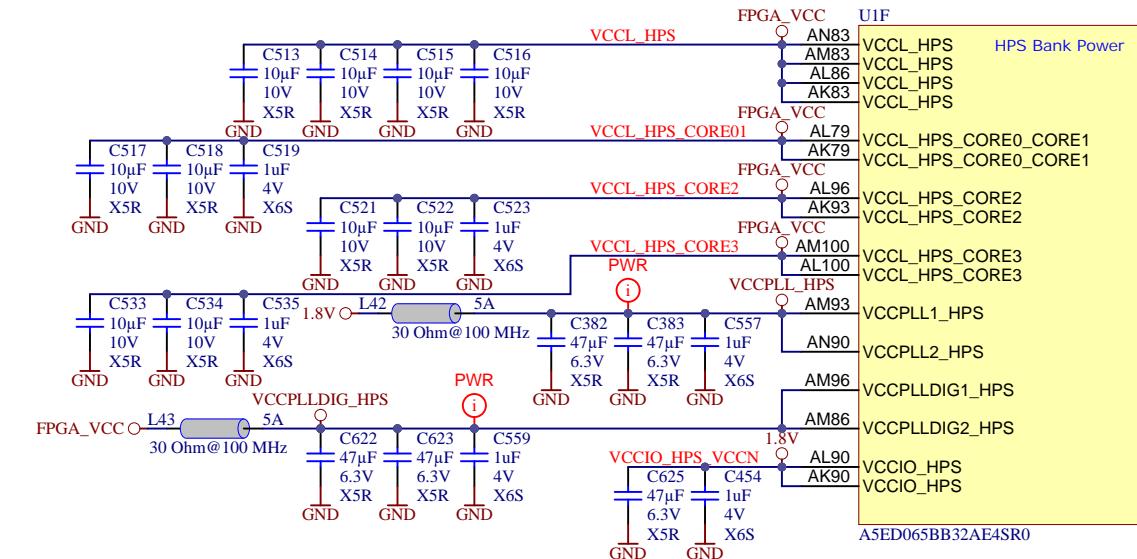
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Filename: FPGA_PWR.SchDoc

A



B

| U1U | |
|-------|-------|
| AL43 | DNU |
| AL57 | DNU |
| AL68 | DNU |
| AL115 | DNU |
| AM36 | DNU |
| AM40 | DNU |
| AM120 | DNU |
| AR32 | DNU |
| AR104 | DNU |
| BA32 | DNU |
| BA104 | DNU |
| BC36 | DNU |
| AN83 | BC40 |
| AM83 | BC100 |
| AL86 | BD36 |
| AK83 | BD53 |
| AL79 | BD64 |
| AK93 | BD100 |
| AL96 | BD120 |
| AM100 | CK101 |
| AL100 | CK103 |
| AM93 | CL101 |
| AN90 | CL106 |

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C

D

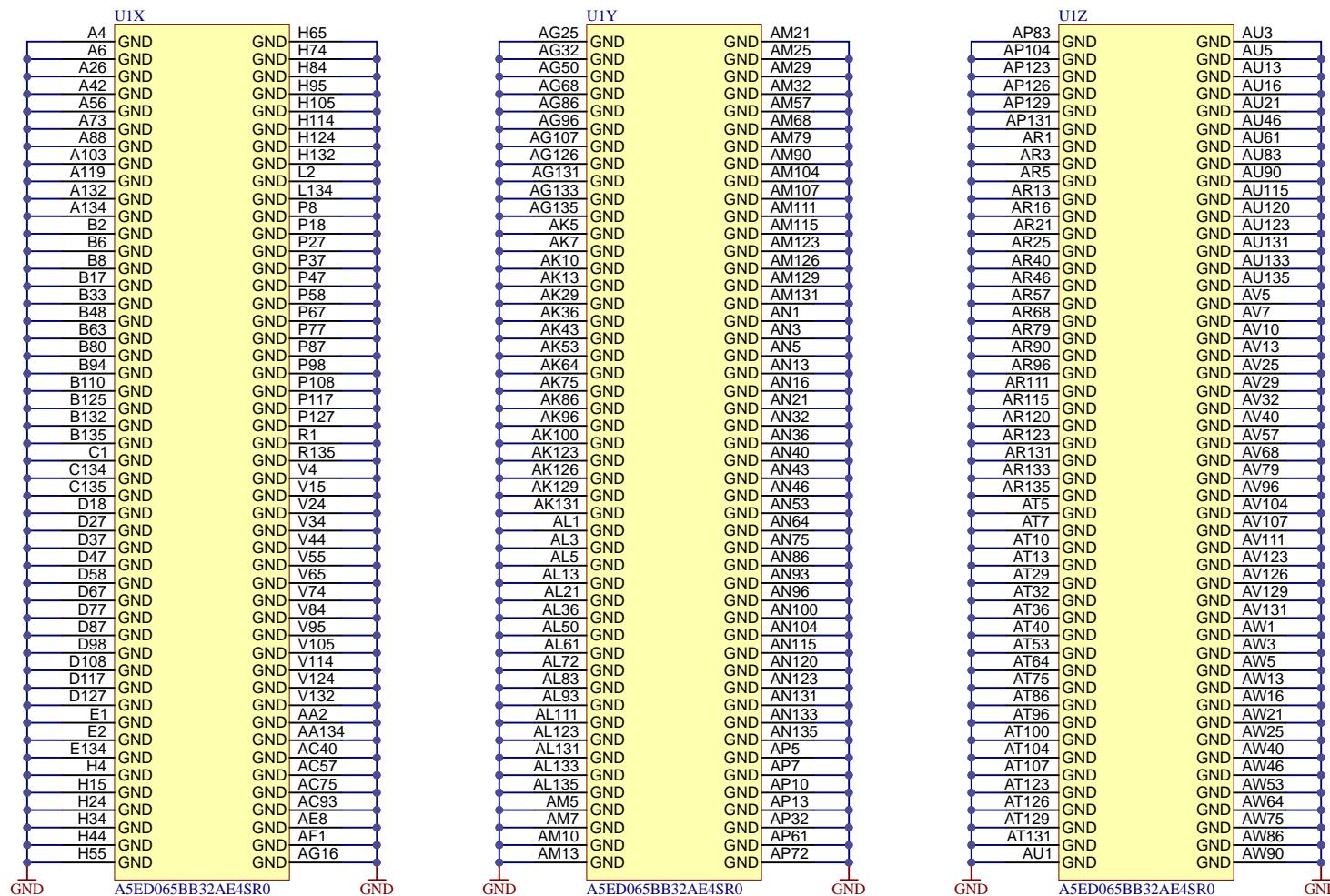
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 A4 Number: **TEI0185**
P001

Rev. **02**

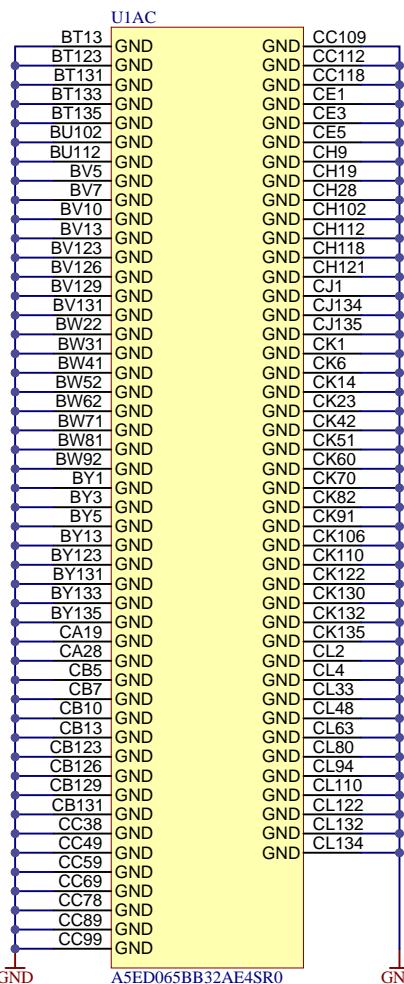
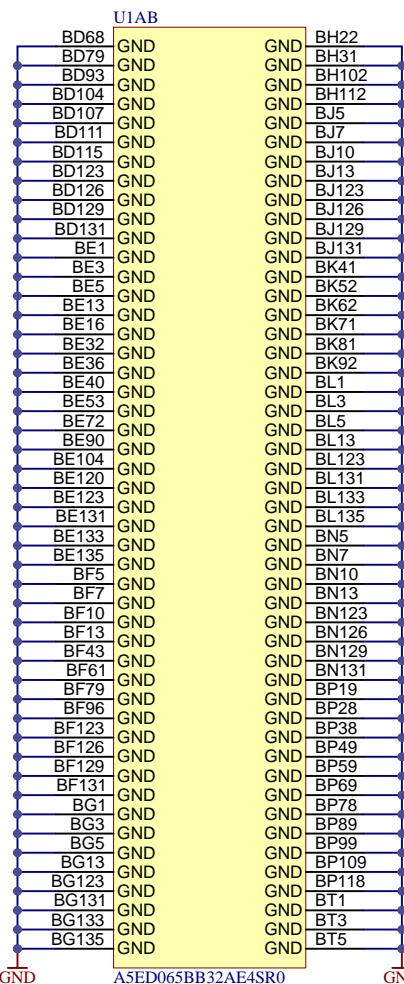
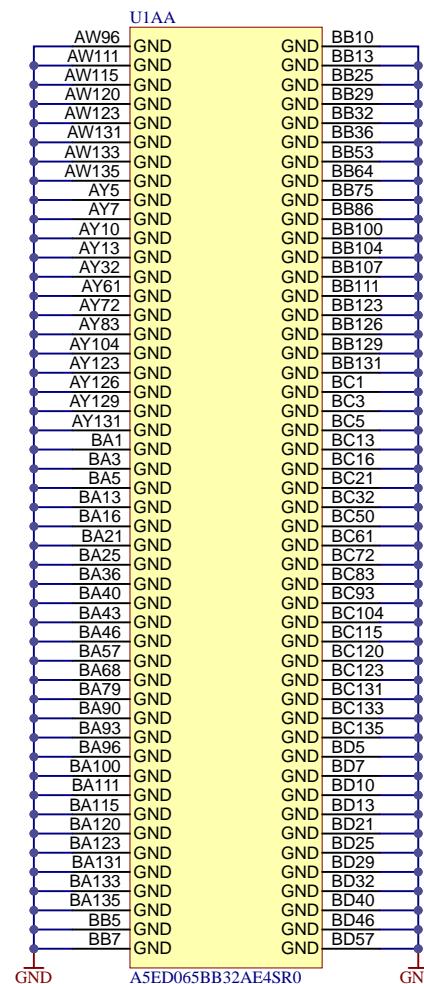
Date: **2023-11-15** Copyright: **Trenz Electronic GmbH**

Page **20** of **51**

Filename: **FPGA_PWR2.SchDoc**

Title: **FPGA_GND**A4 | Number: **TEI0185
P001**Rev. **02**Date: **2023-11-15** Copyright: **Trenz Electronic GmbH**Page **21** of **51**Filename: **FPGA_GND_1.SchDoc**

A



A

A

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D

Title: FPGA_GND

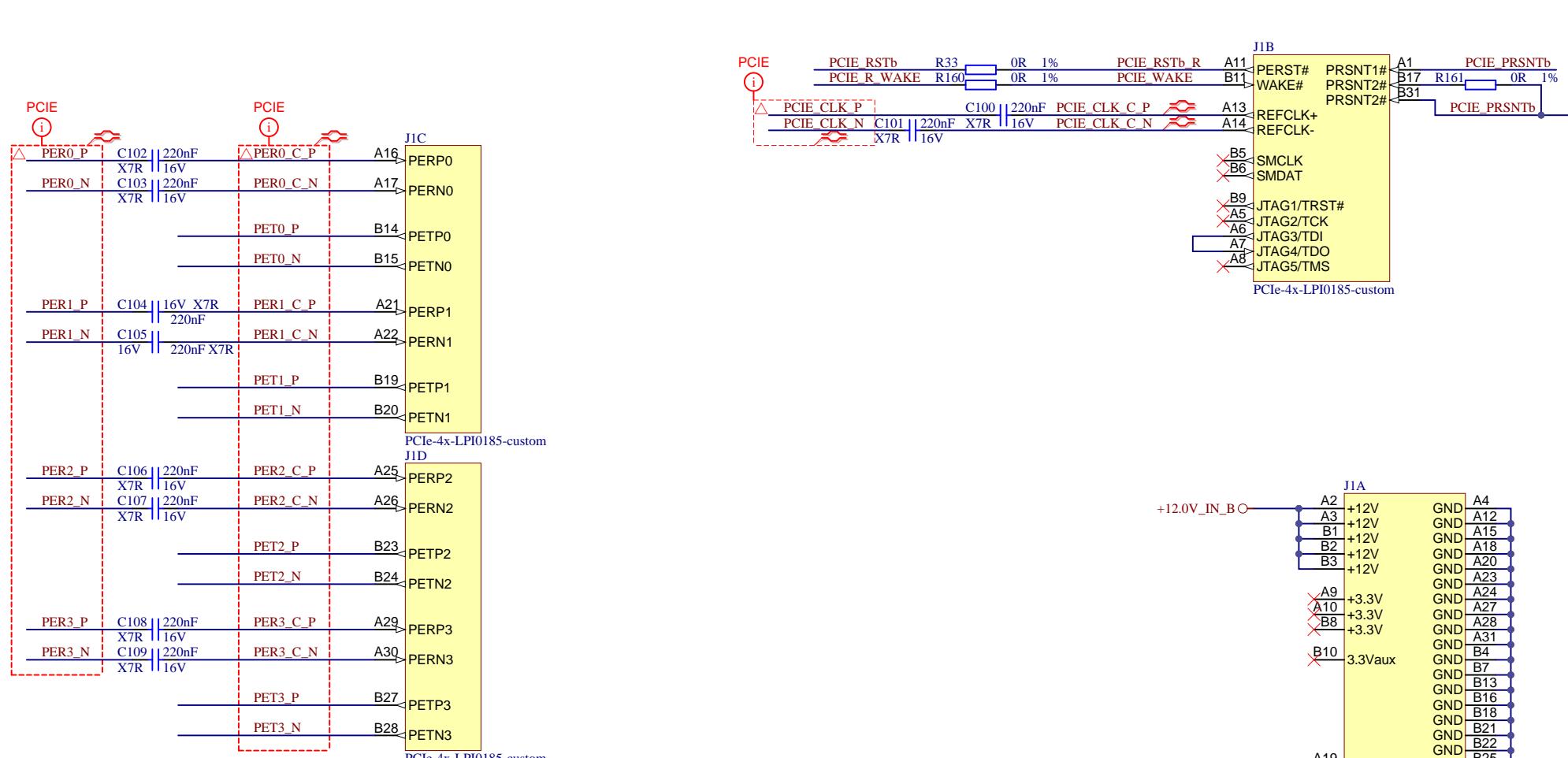
A4 Number: TEI0185
P001

Rev. 02

Date: 2023-11-15 Copyright: Trenz Electronic GmbH

Page 22 of 51

Filename: FPGA_GND_2.SchDoc



| | | | |
|-----------------------------------|----------------------------------|-----------------------|--|
| | | Title: PCIE x4 | |
| A4 | Number: TEI0185 P001 | Rev. 02 | |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | Page 23 of 51 | |
| Filename: PCIE_CONN.SchDoc | | | |

1

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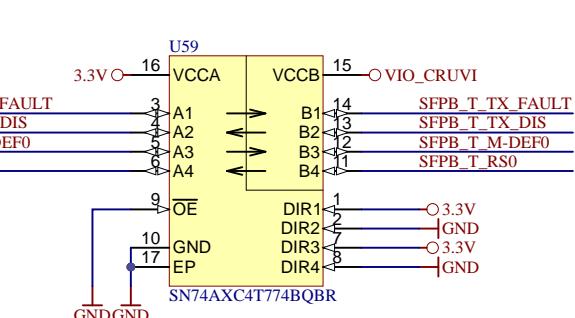
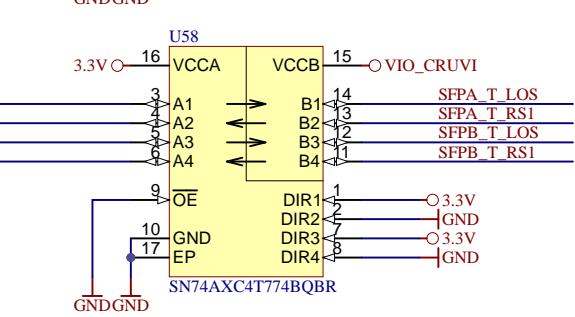
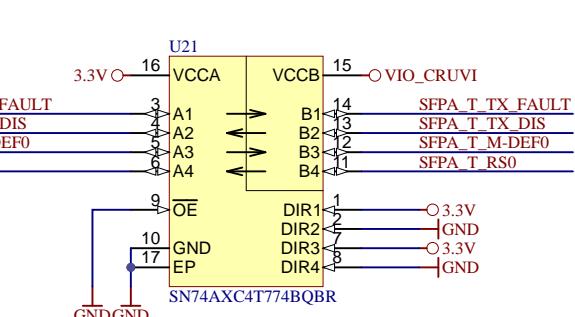
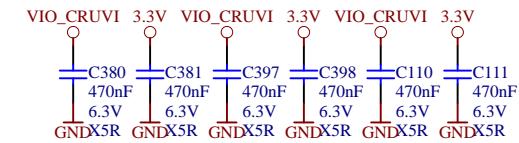
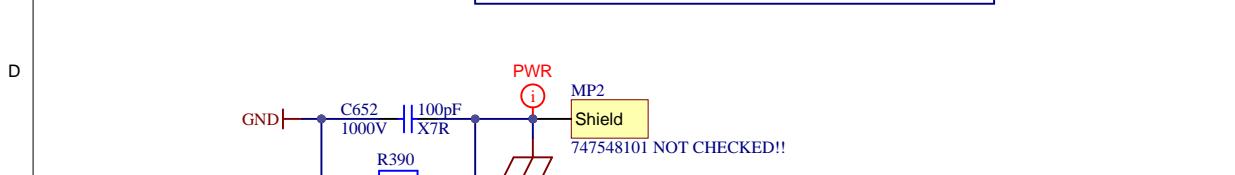
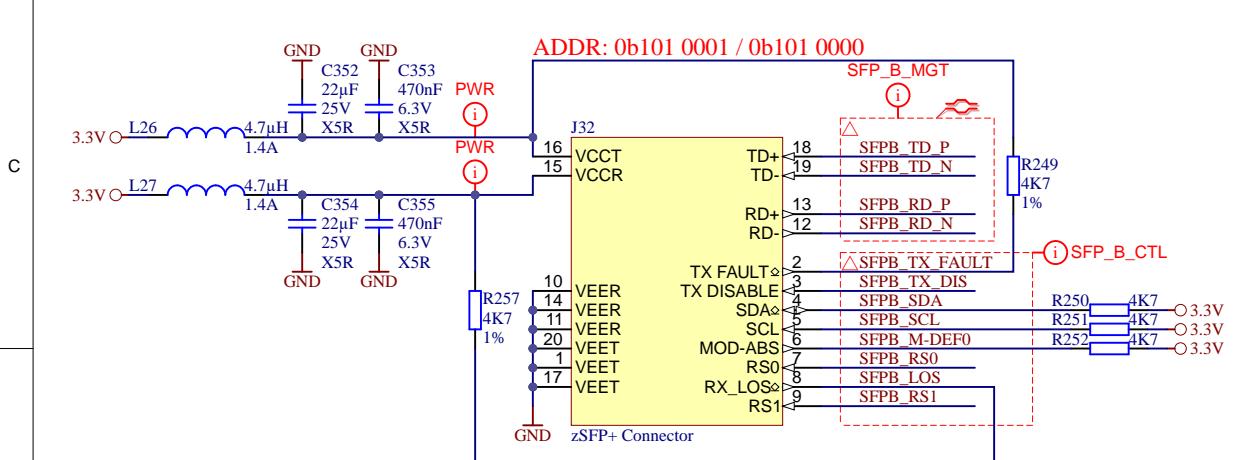
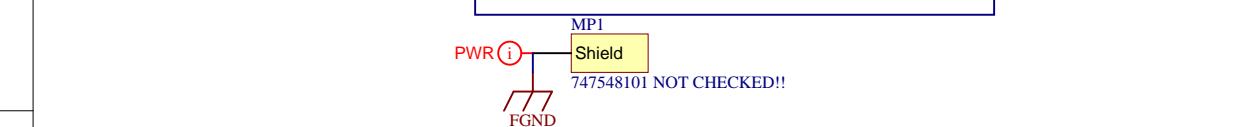
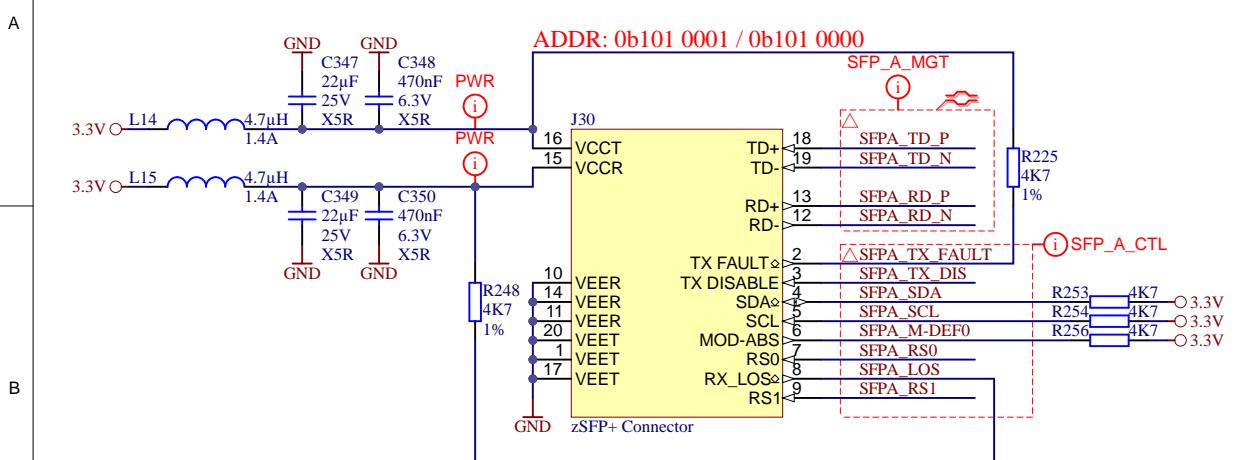
4

1

2

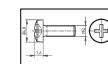
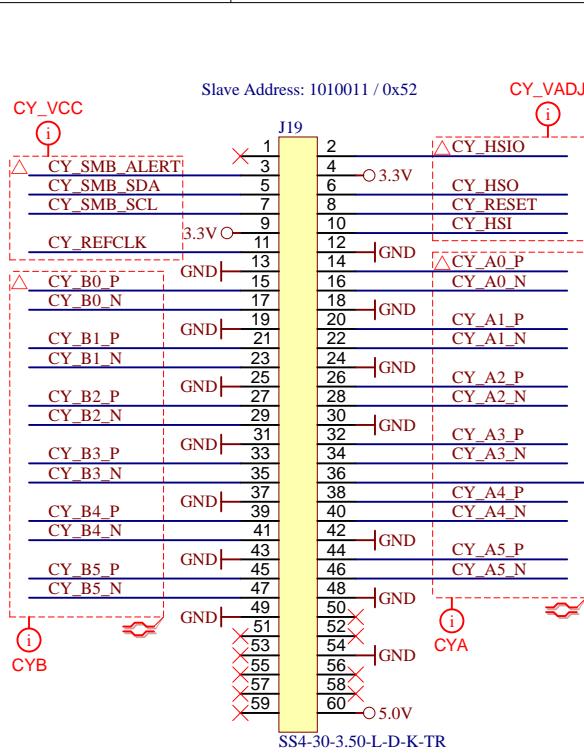
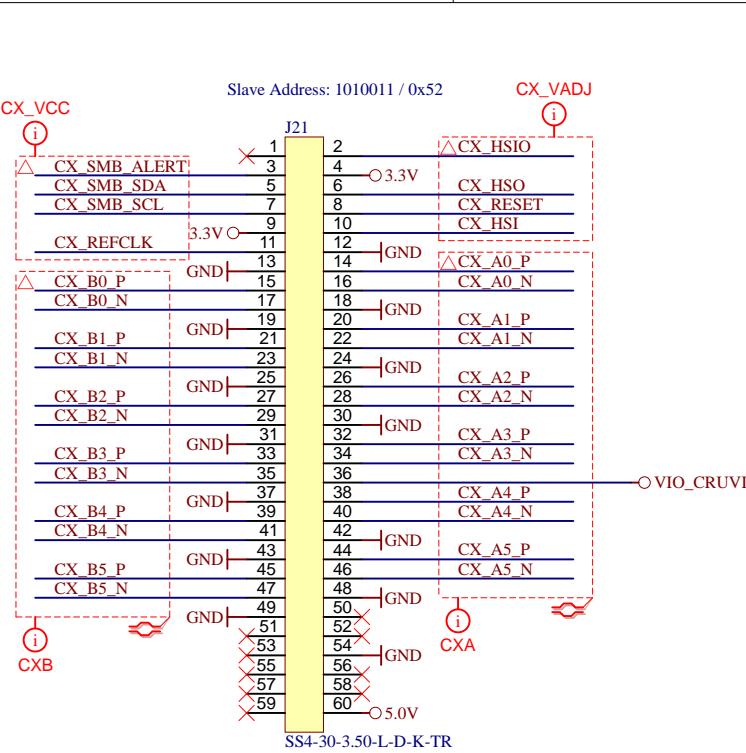
3

4



Title: zSFP+ **Rev.:** 02

| | |
|------------------------|----------------------------------|
| A4 | Number: TEI0185 P001 |
| Date: 2023-11-16 | Copyright: Trenz Electronic GmbH |
| Filename: zSFP+.SchDoc | Page 24 of 51 |



Screw M2x6



Steel Spacer M2 5mm SMD



Steel Spacer M2.5mm SMD



S-480-1135-GB



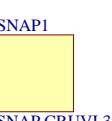
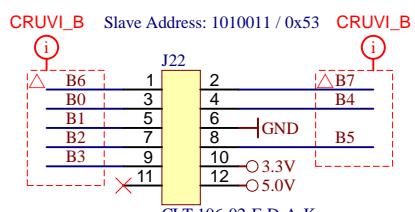
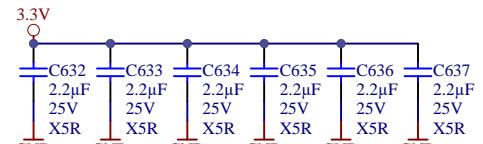
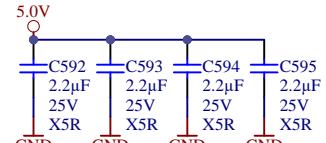
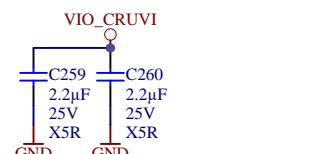
ANSWER



□

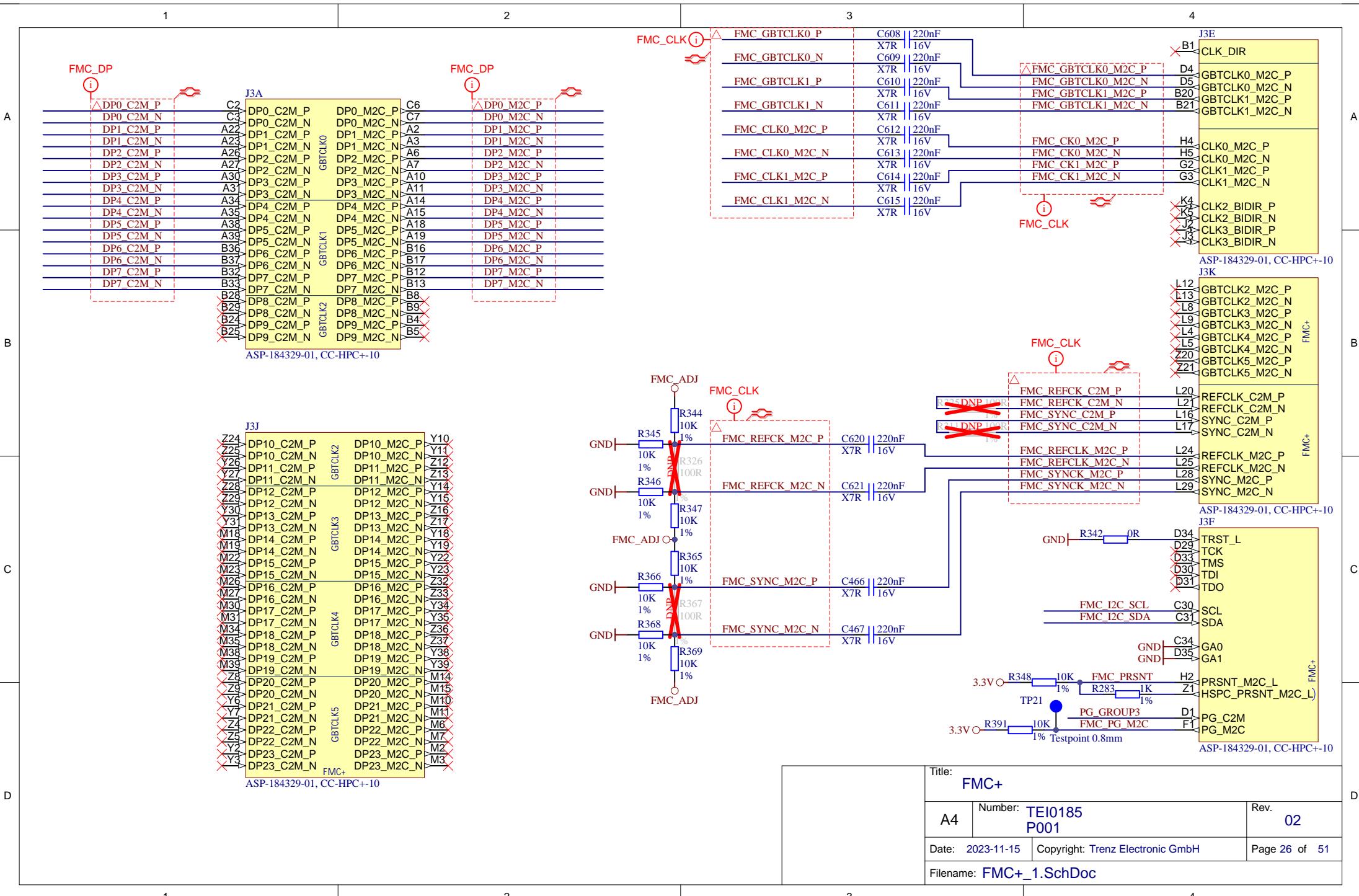


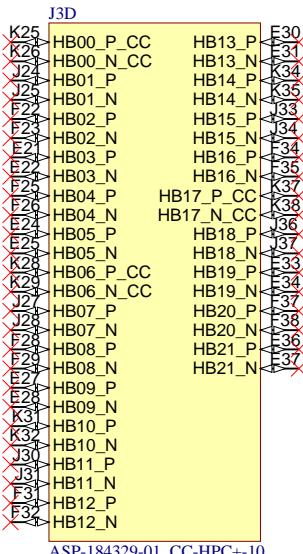
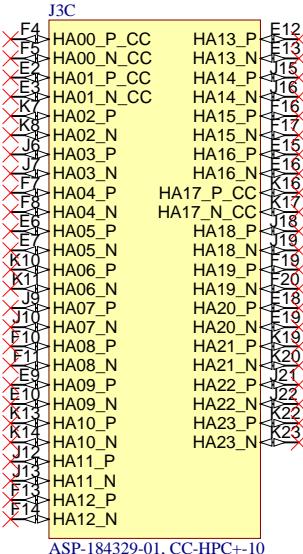
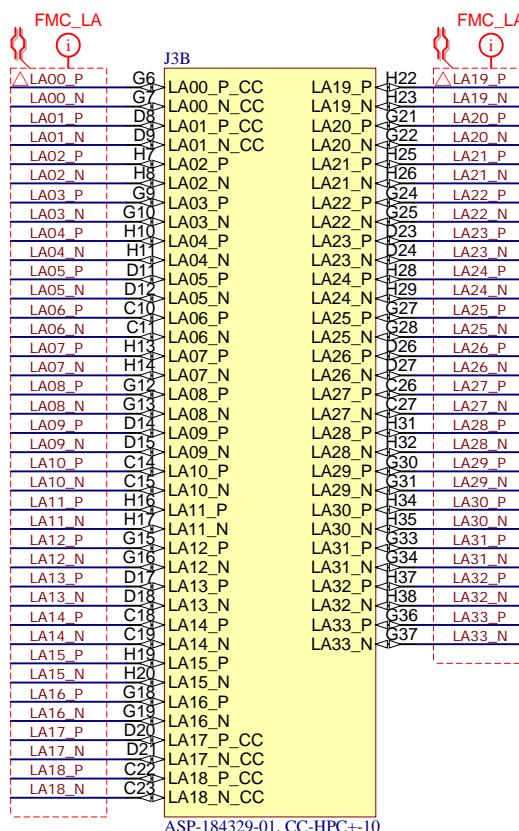
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Title: CPH 411

| CRUVI | | |
|------------------------|----------------------------------|--------------|
| A4 | Number: TEI0185 P001 | Rev. 02 |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | Page 25 of 5 |
| Filename: CRUVI.SchDoc | | |





| | | | |
|--------------------------------|----------------------------------|--------------------|---------------|
| | | Title: FMC+ | |
| A4 | Number: TEI0185 P001 | Rev. 02 | |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | | Page 27 of 51 |
| Filename: FMC+_2.SchDoc | | | |

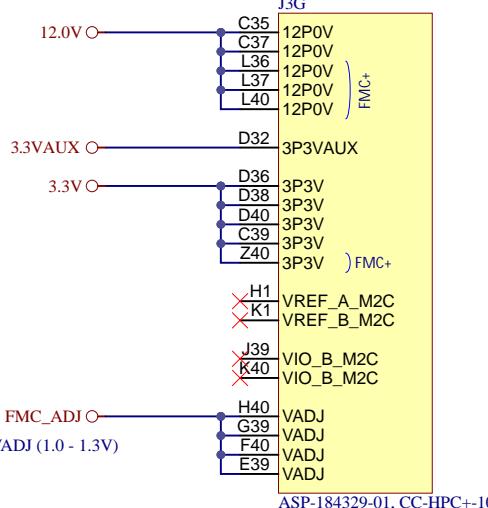
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2

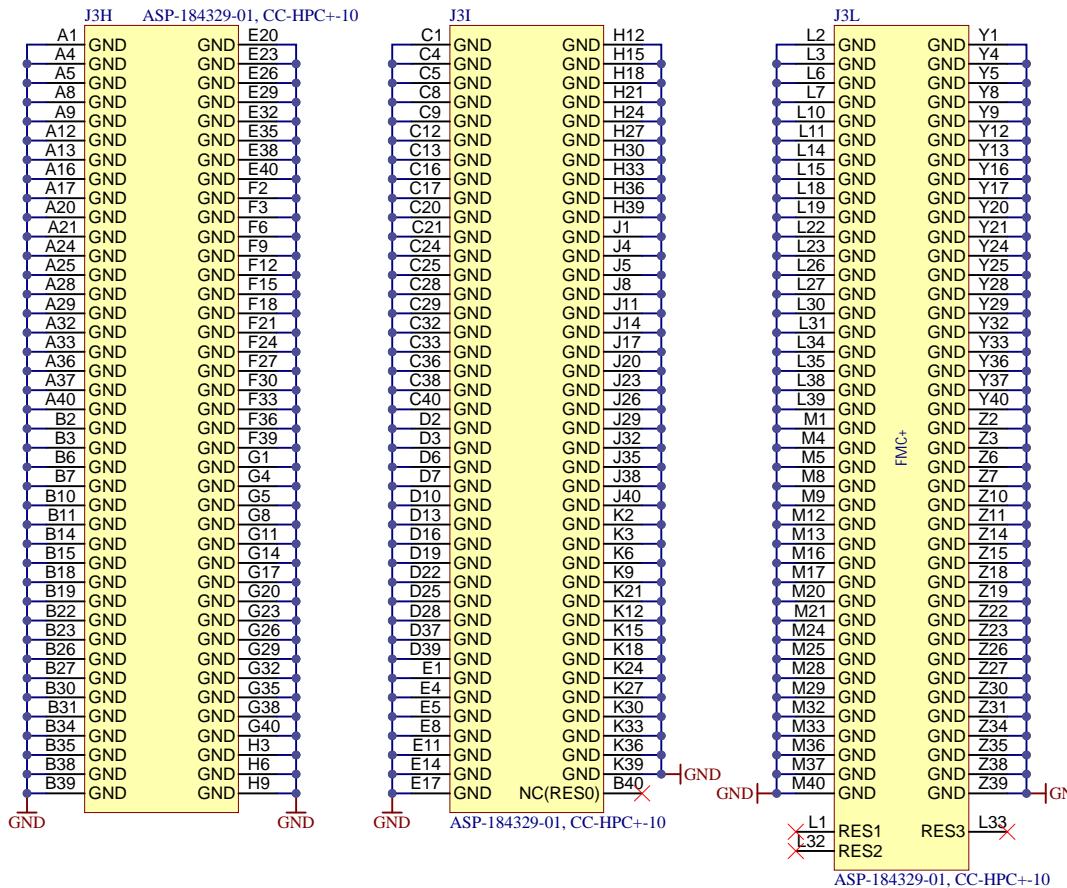
3

4

A



B



C

| | | | |
|----------------------------------|----------------------------------|--------------------|--|
| | | Title: FMC+ | |
| A4 | Number: TEI0185 P001 | Rev. 02 | |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | Page 28 of 51 | |
| Filename: FMC+_PWR.SchDoc | | | |

1

2

3

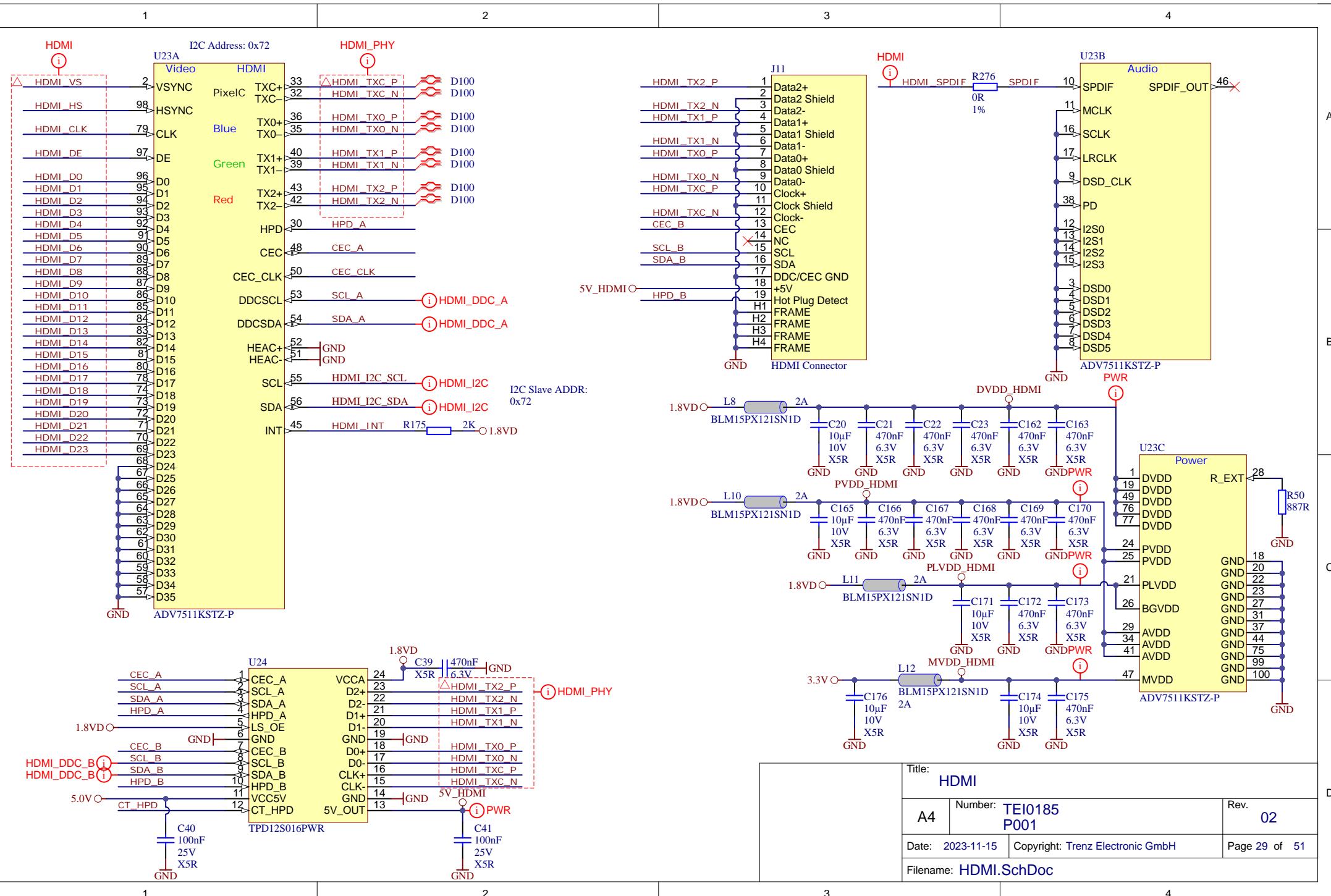
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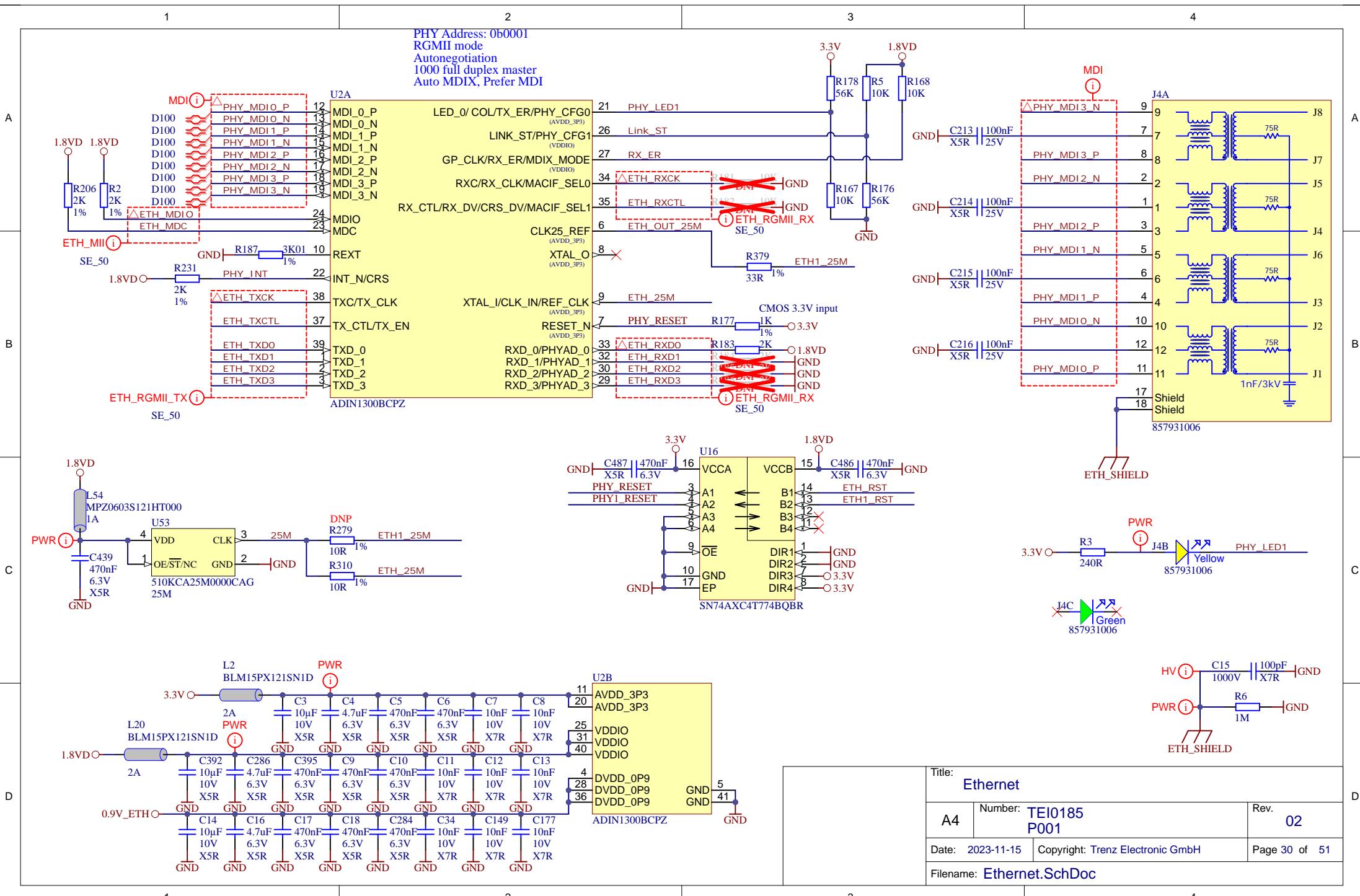
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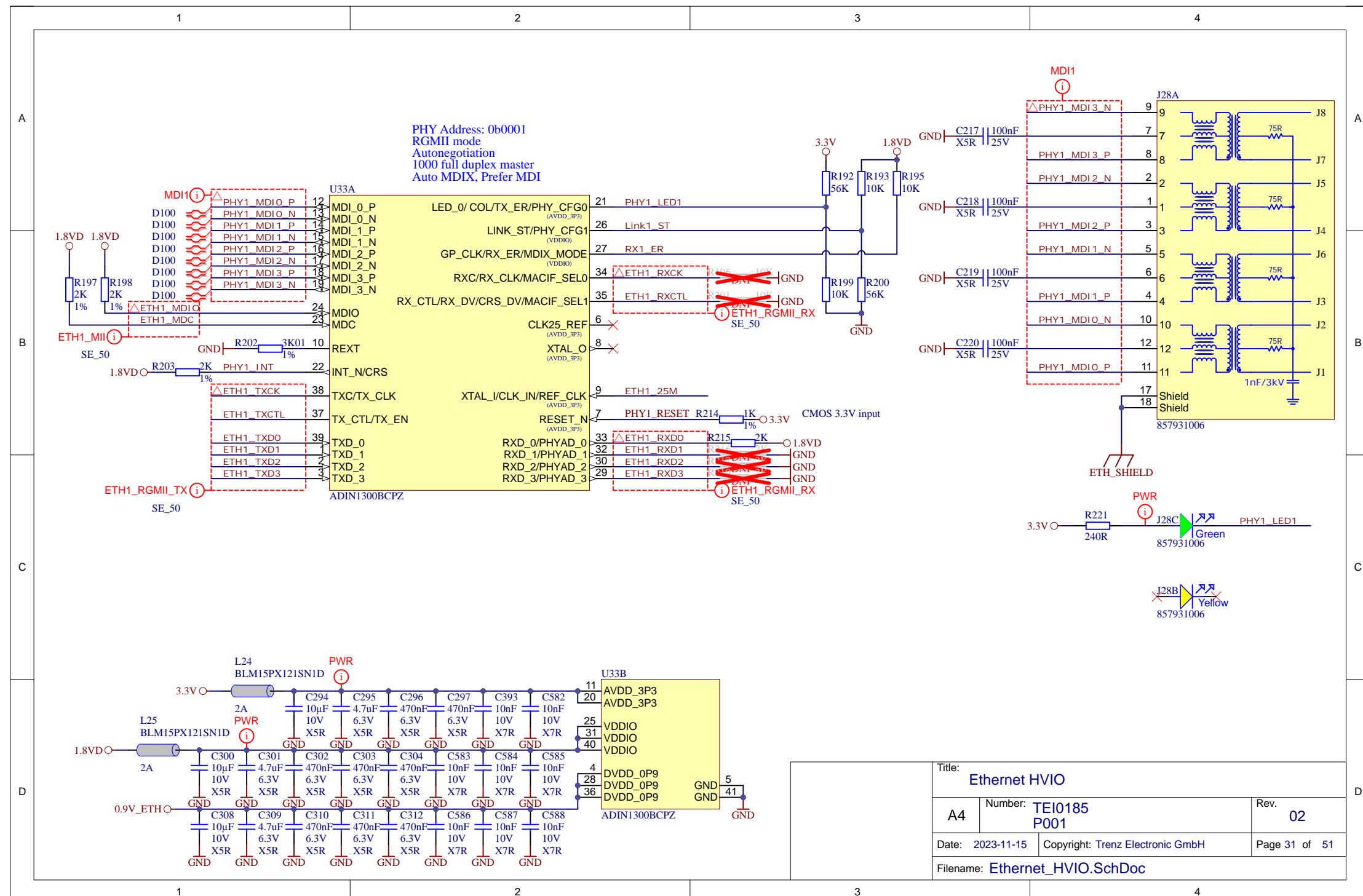
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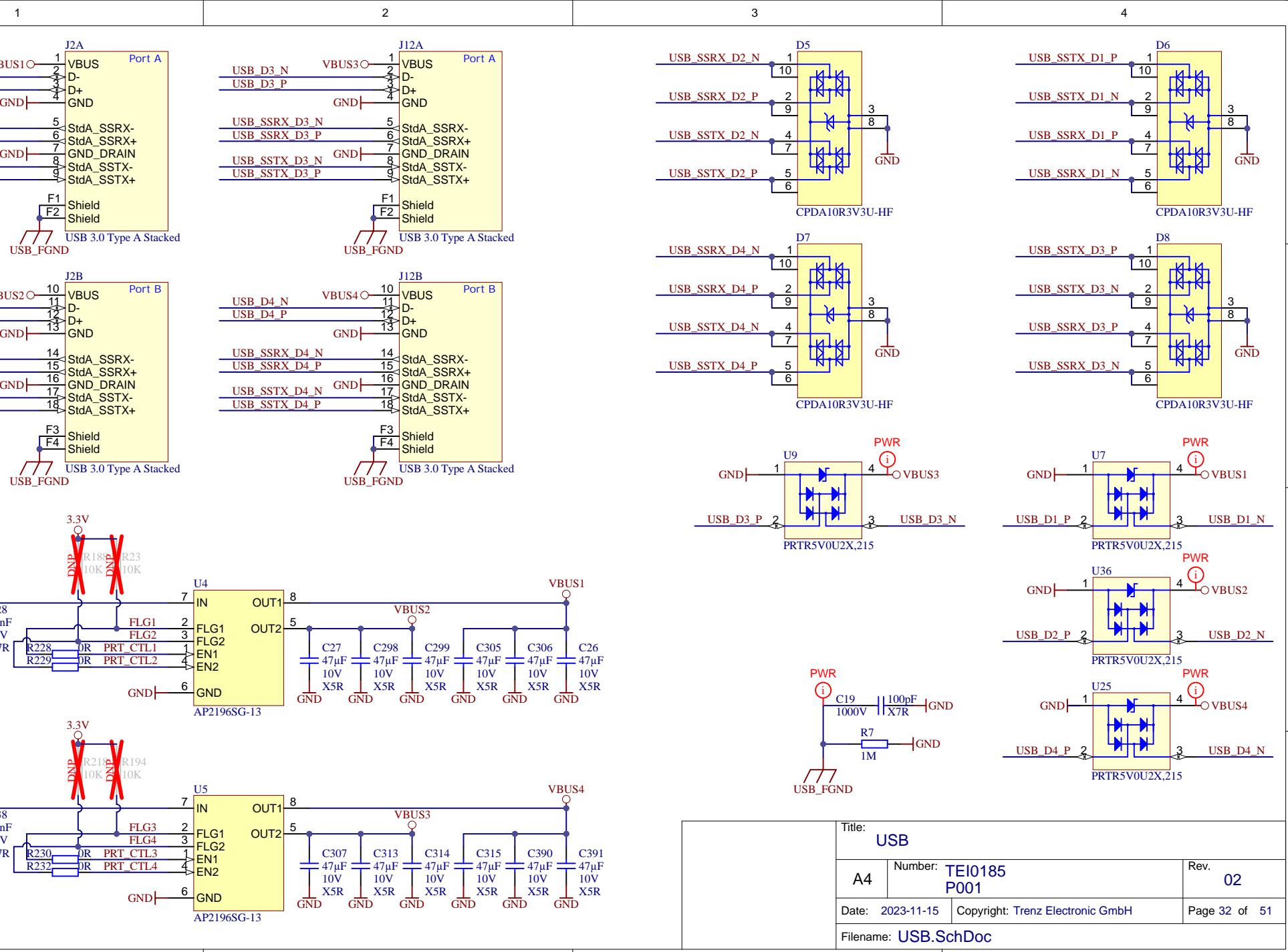
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D





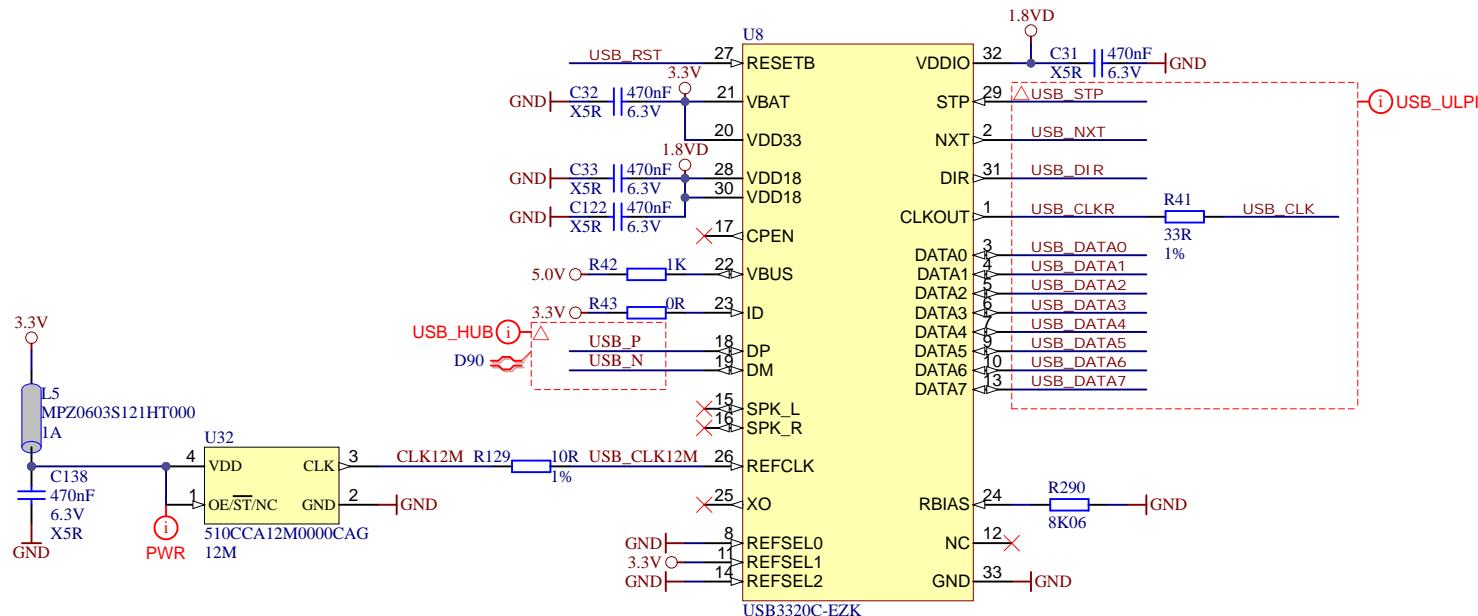




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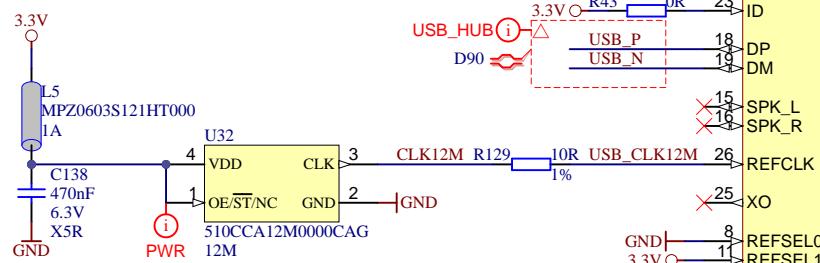
A

VBAT, VDD33, and VDD18 can be applied in any order.
 The VDD18 supply must be turned on and stable before
 the VDDIO supply is applied. This does not apply in
 cases where the VDD18 and VDDIO are tied together.



B

B



C

C

D

D

Title:
USB-PHY

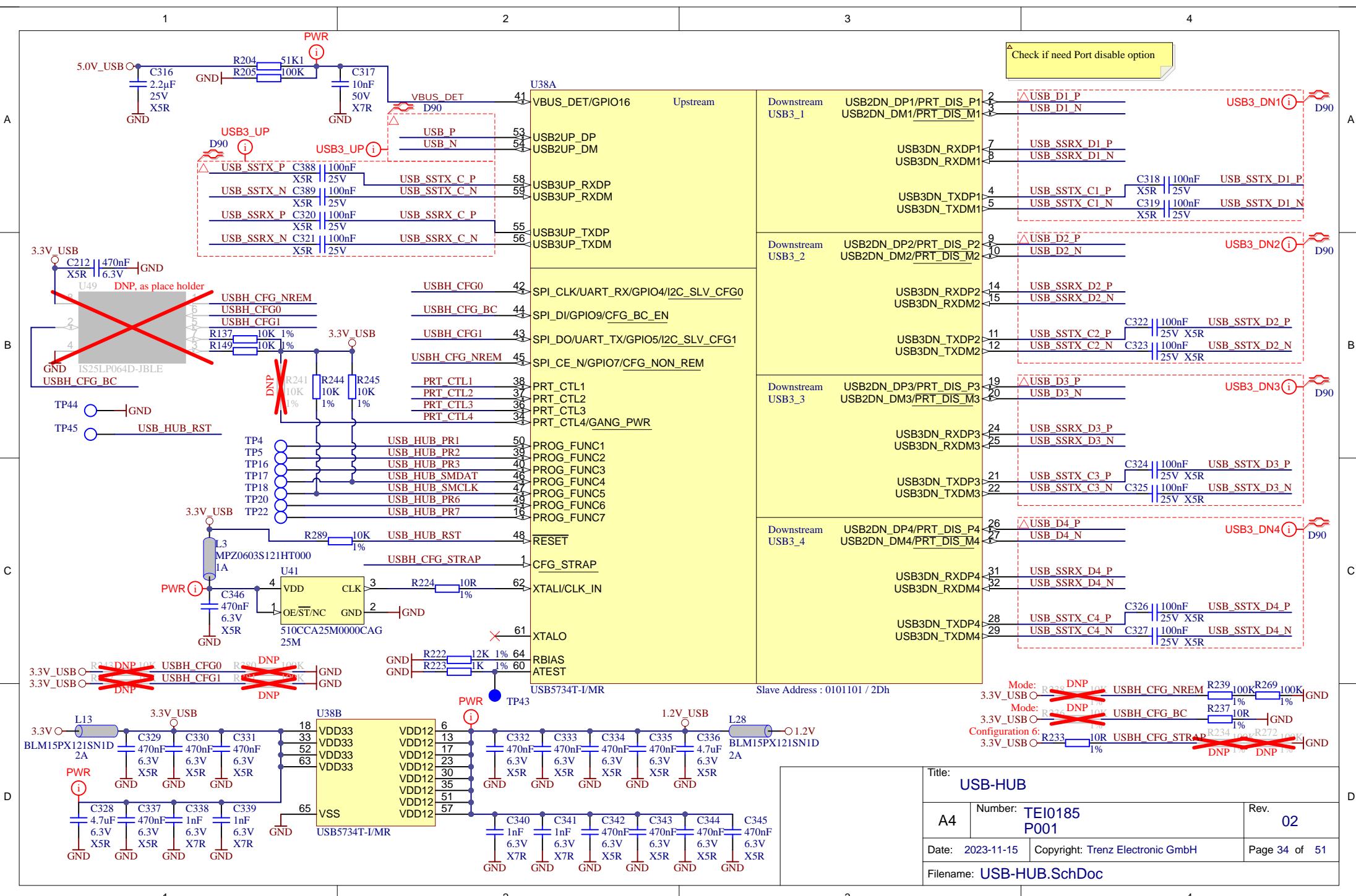
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P001**

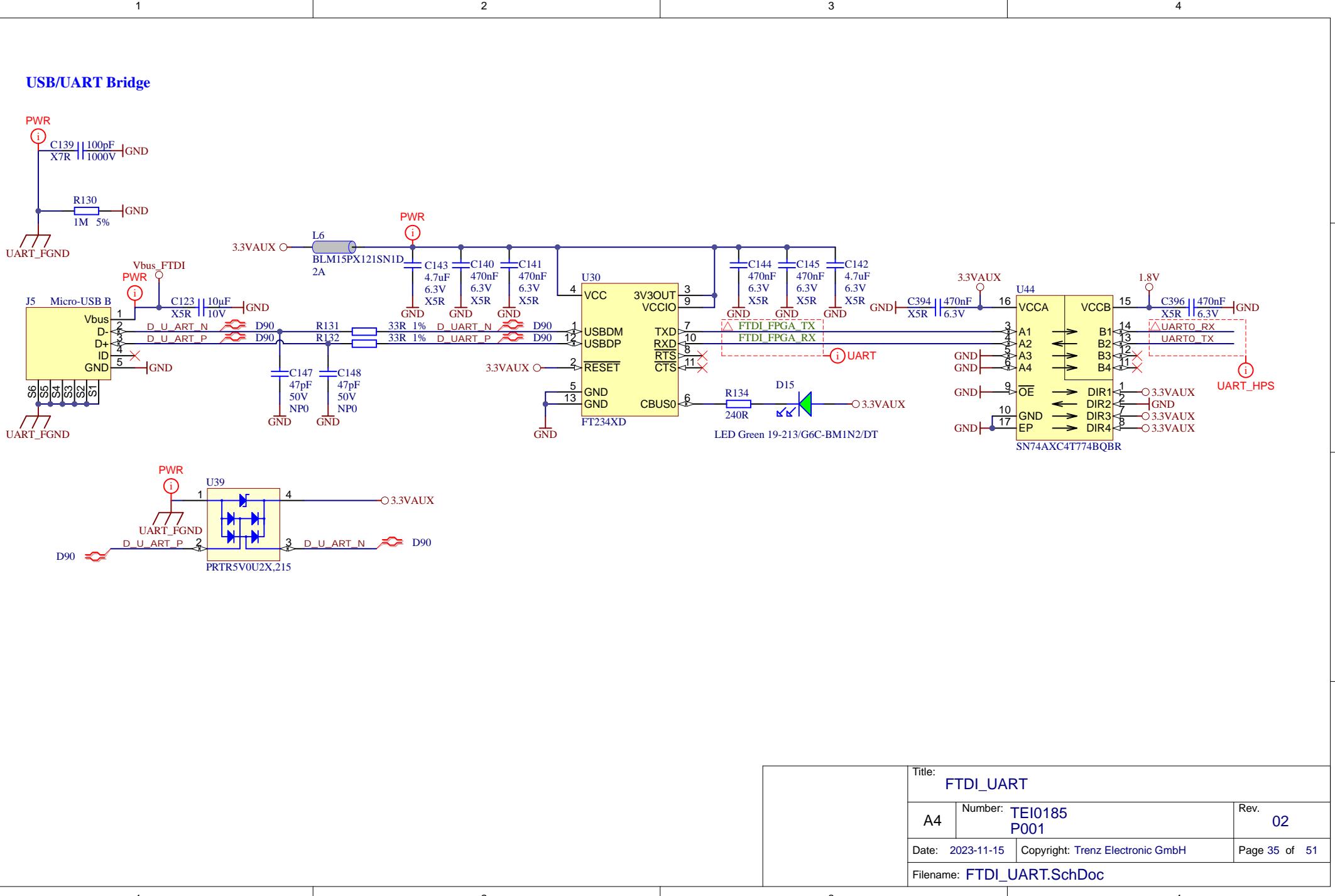
Rev.
02

Date: 2023-11-15 Copyright: Trenz Electronic GmbH

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Filename: **USB-PHY.SchDoc**





A

A

B

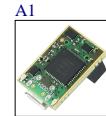
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C

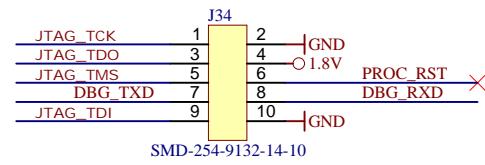
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D

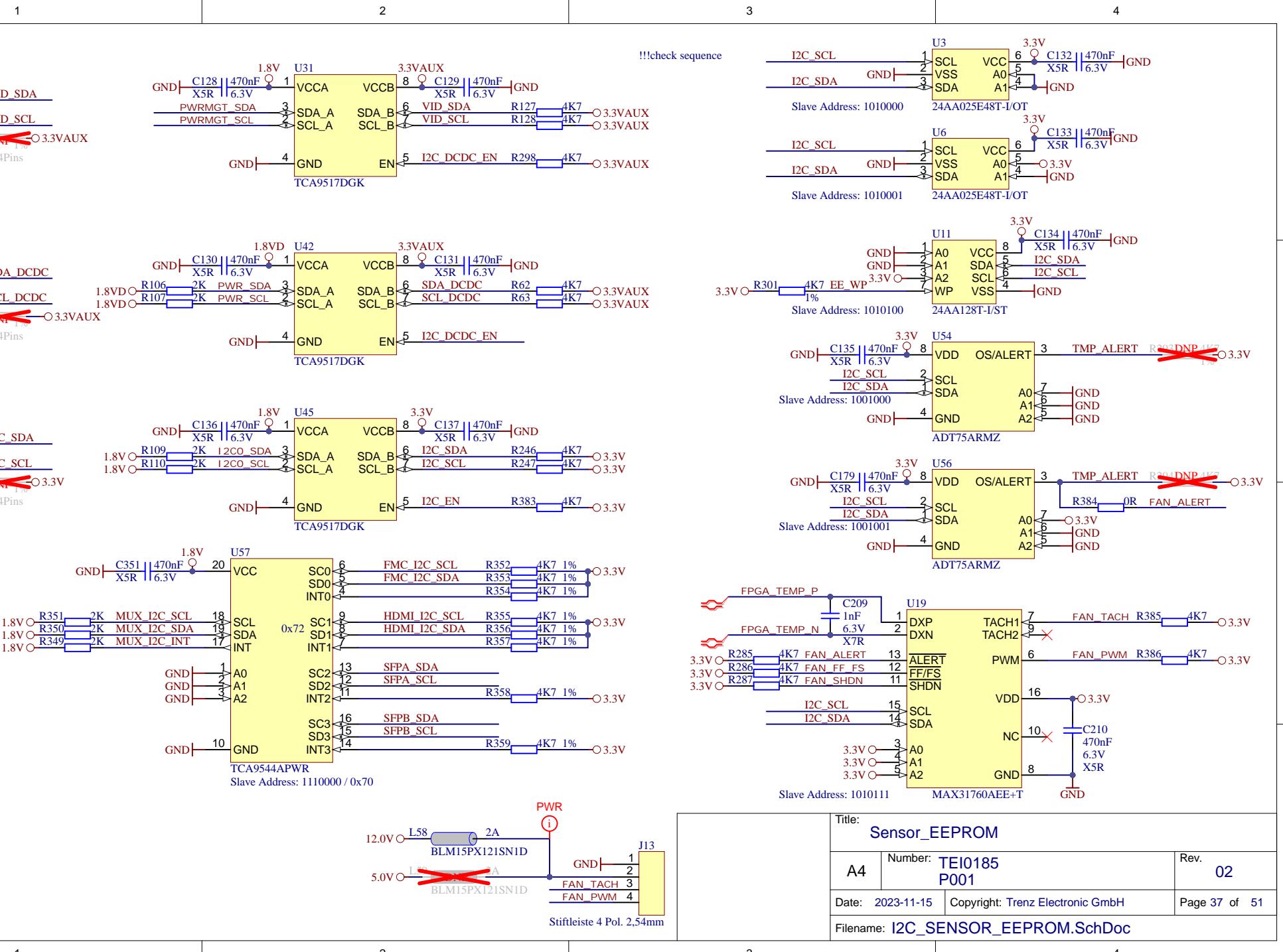
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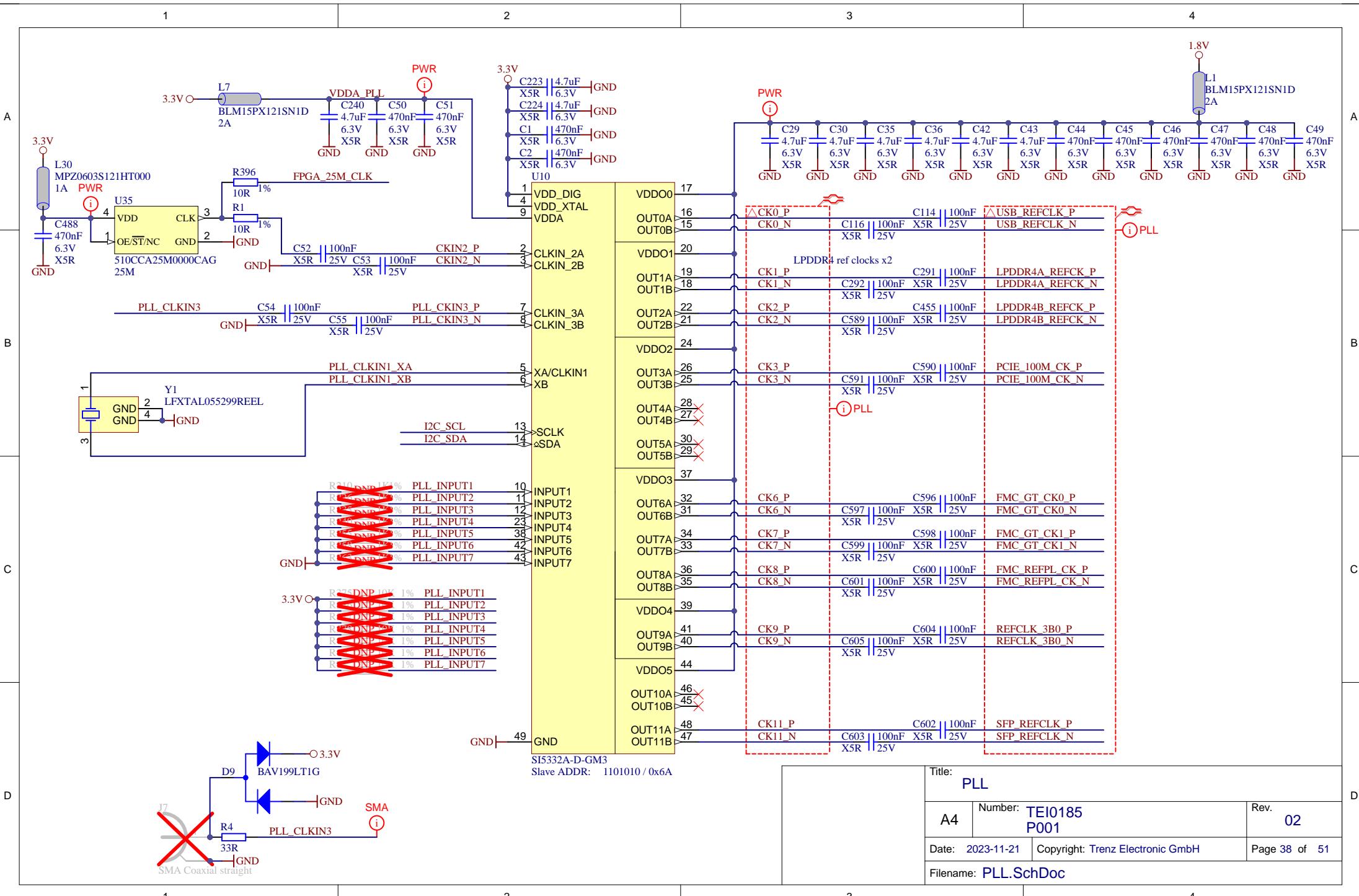


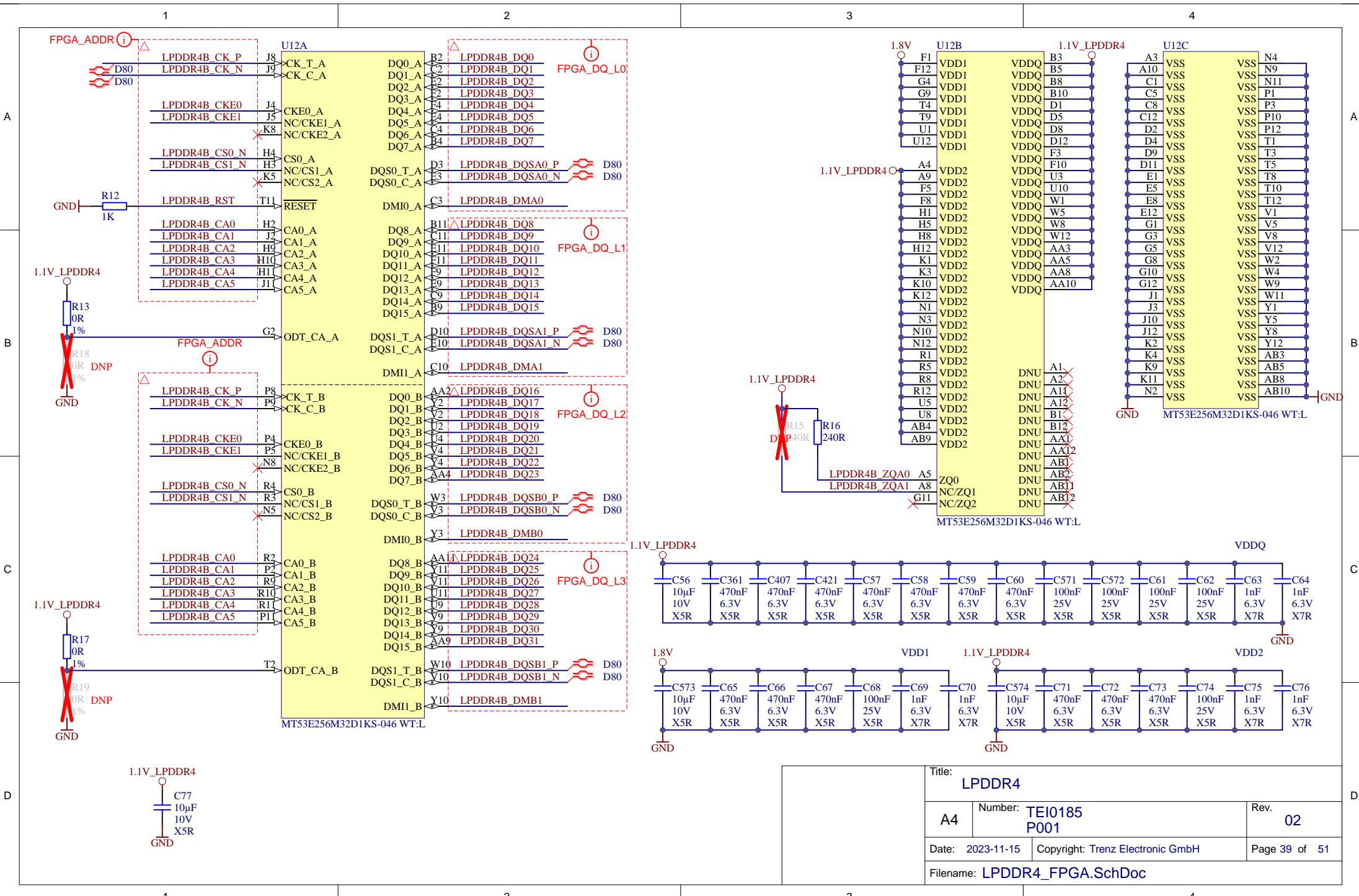
TEI0004 ARROW USB Programmer2

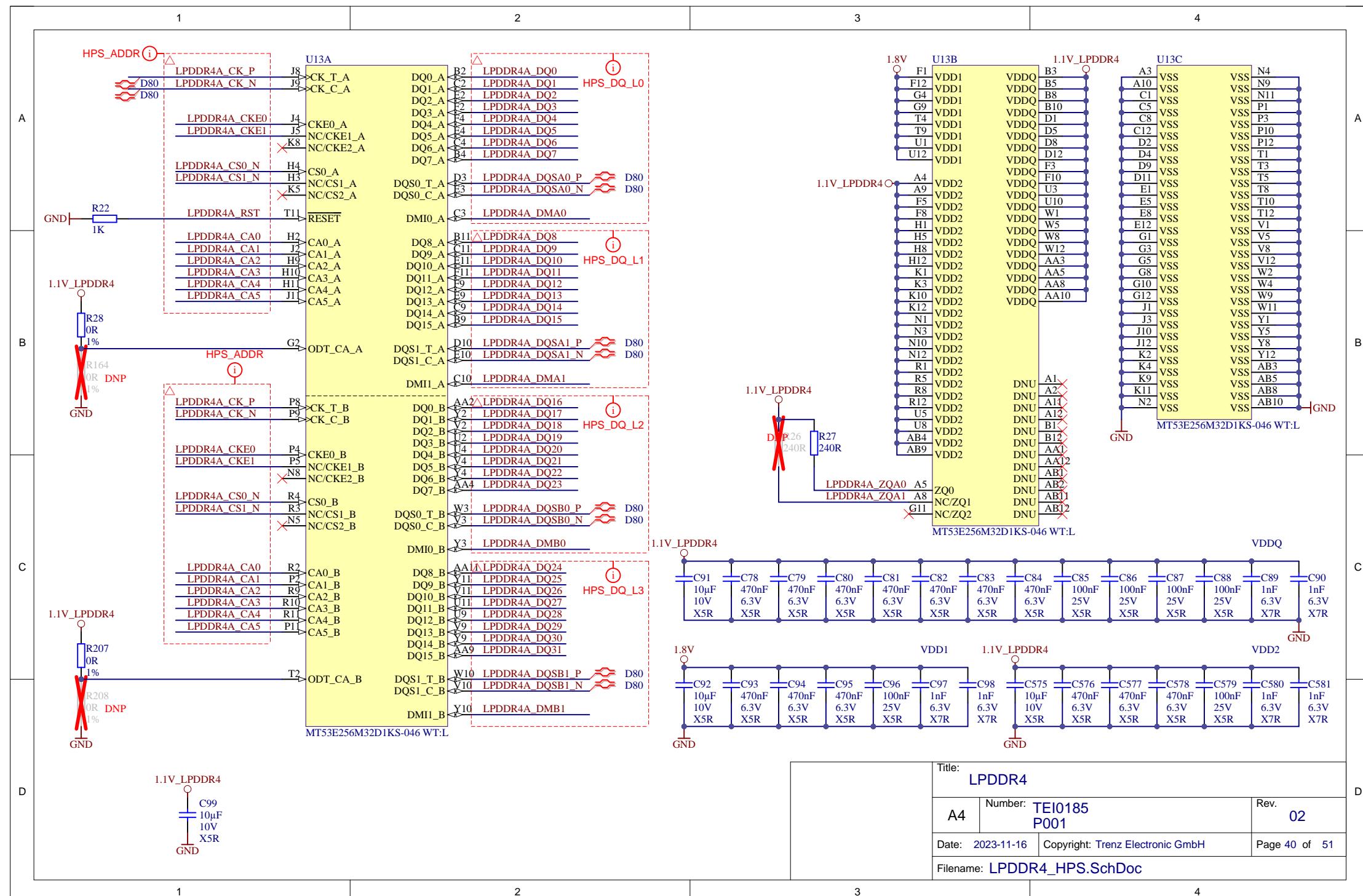


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| | | Title: FTDI_JTAG | |
| A4 | Number: TEI0185 P001 | Rev. 02 | |
| Date: 2023-11-15 Copyright: Trenz Electronic GmbH | | Page 36 of 51 | |
| Filename: FTDI_JTAG.SchDoc | | | |









1

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A

A

B

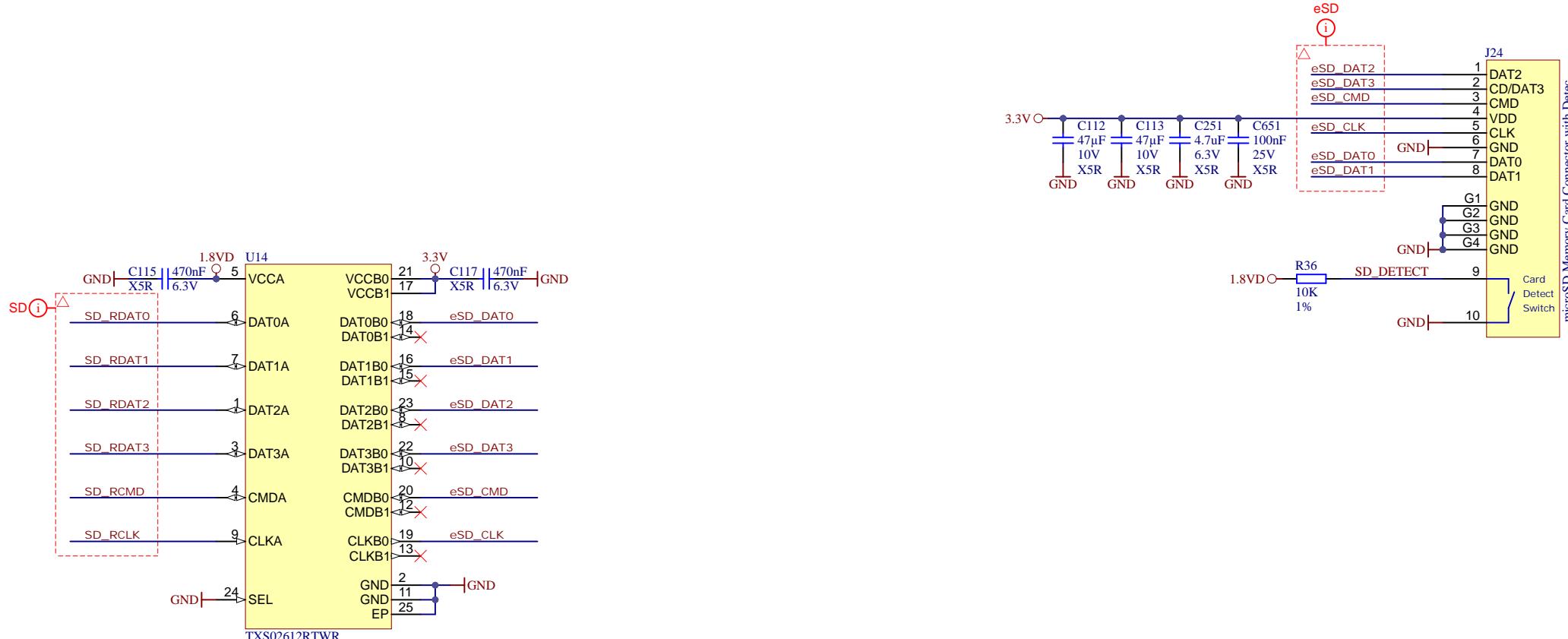
B

C

C

D

D



| | | | |
|---------------------|----------------------------------|---------------|--|
| | | Title: SD | |
| A4 | Number: TEI0185 P001 | Rev. 02 | |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | Page 41 of 51 | |
| Filename: SD.schdoc | | | |

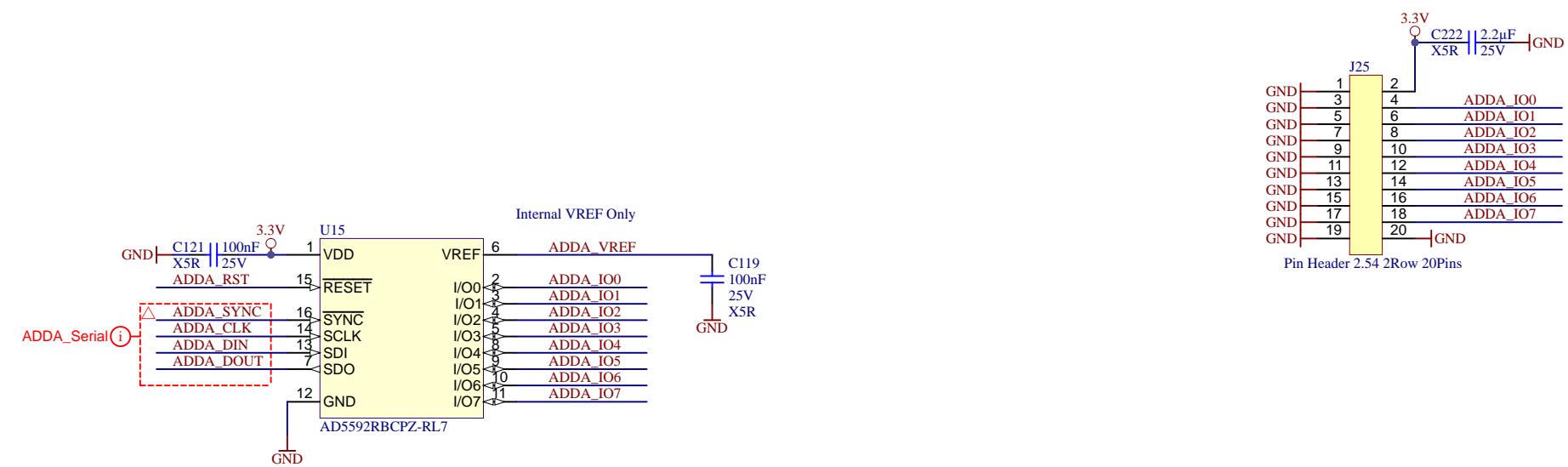
1

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D

Title: ADC - DAC

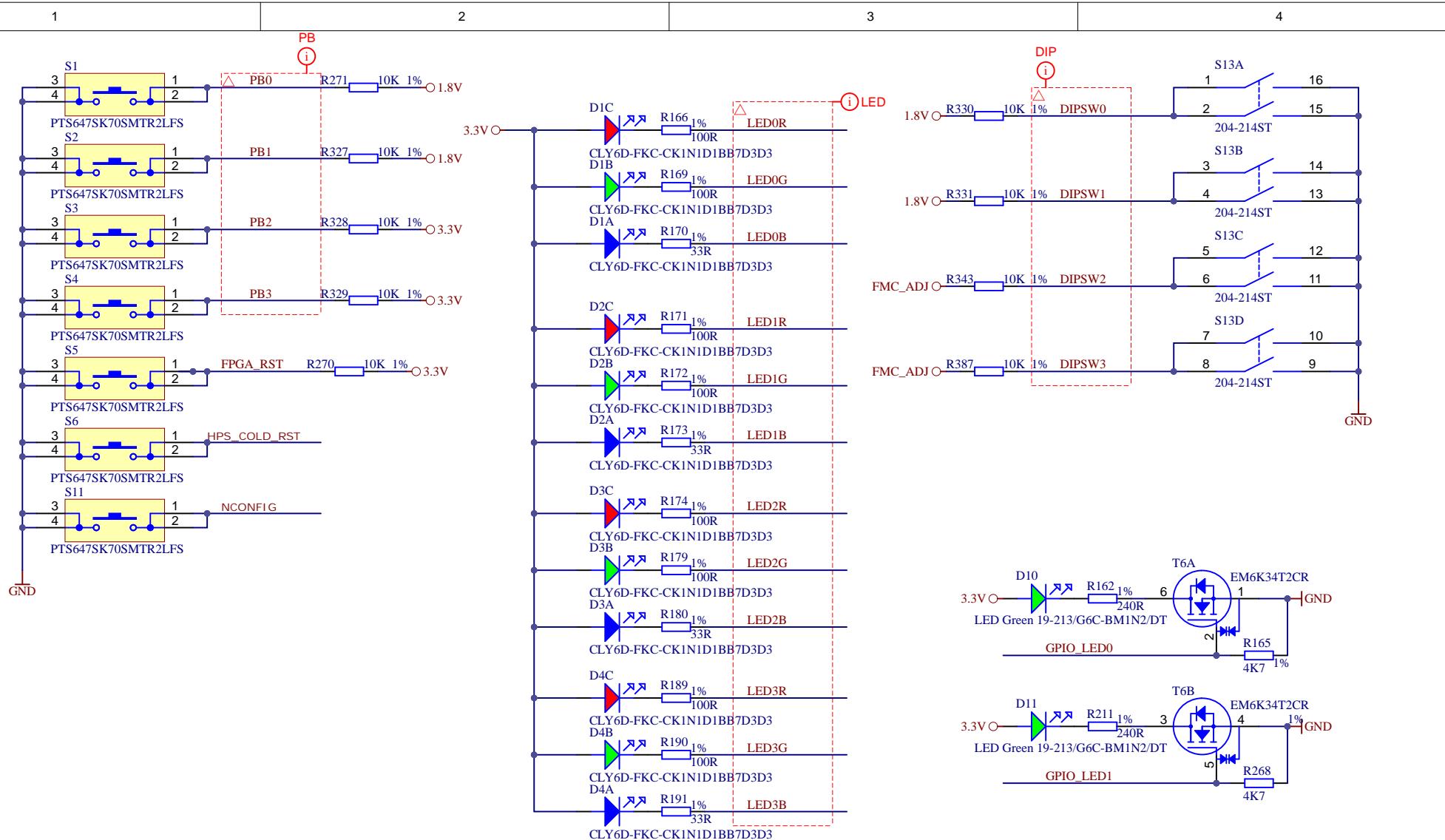
A4 Number: TEI0185
P001

Rev. 02

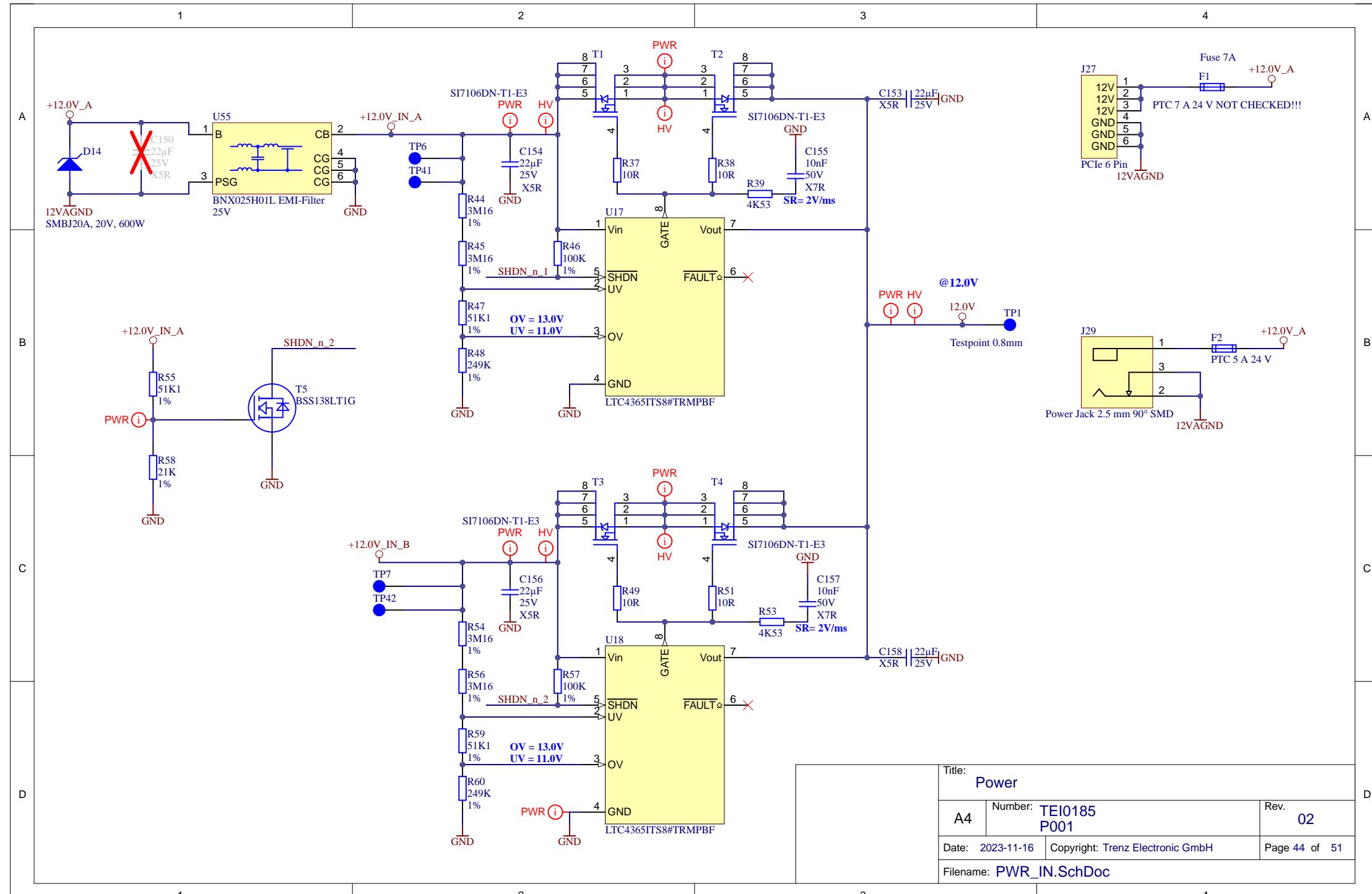
Date: 2023-11-15 Copyright: Trenz Electronic GmbH

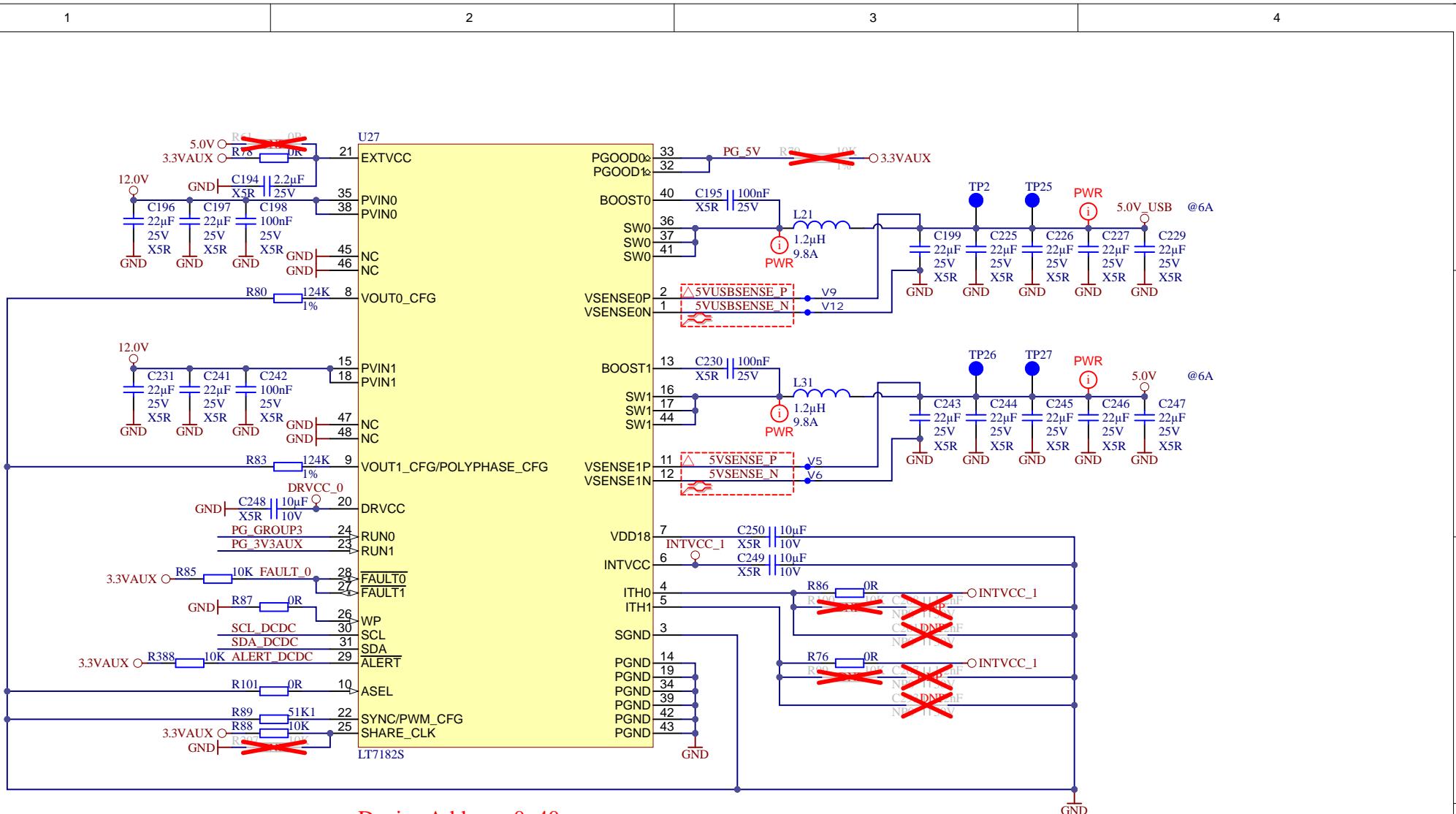
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Filename: ADC.SchDoc



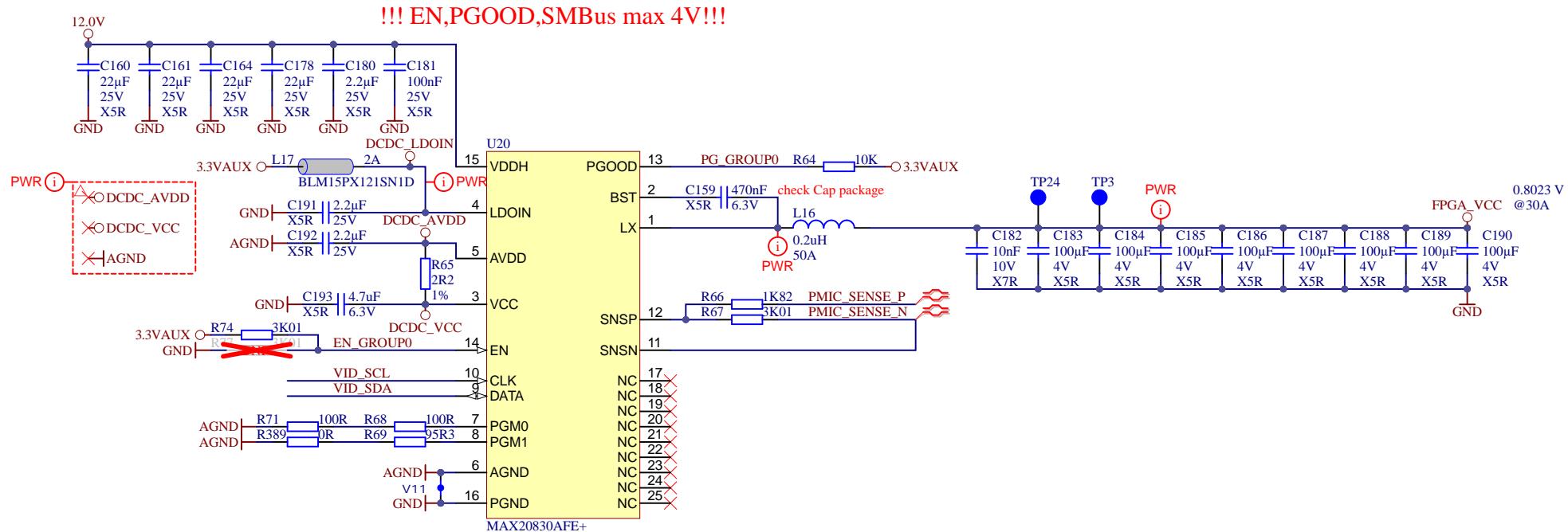
| Title: Misc | | Rev. 02 |
|-----------------------|----------------------------------|---------------|
| A4 | Number: TEI0185 P001 | |
| Date: 2023-12-14 | Copyright: Trenz Electronic GmbH | Page 43 of 51 |
| Filename: MISC.SchDoc | | |





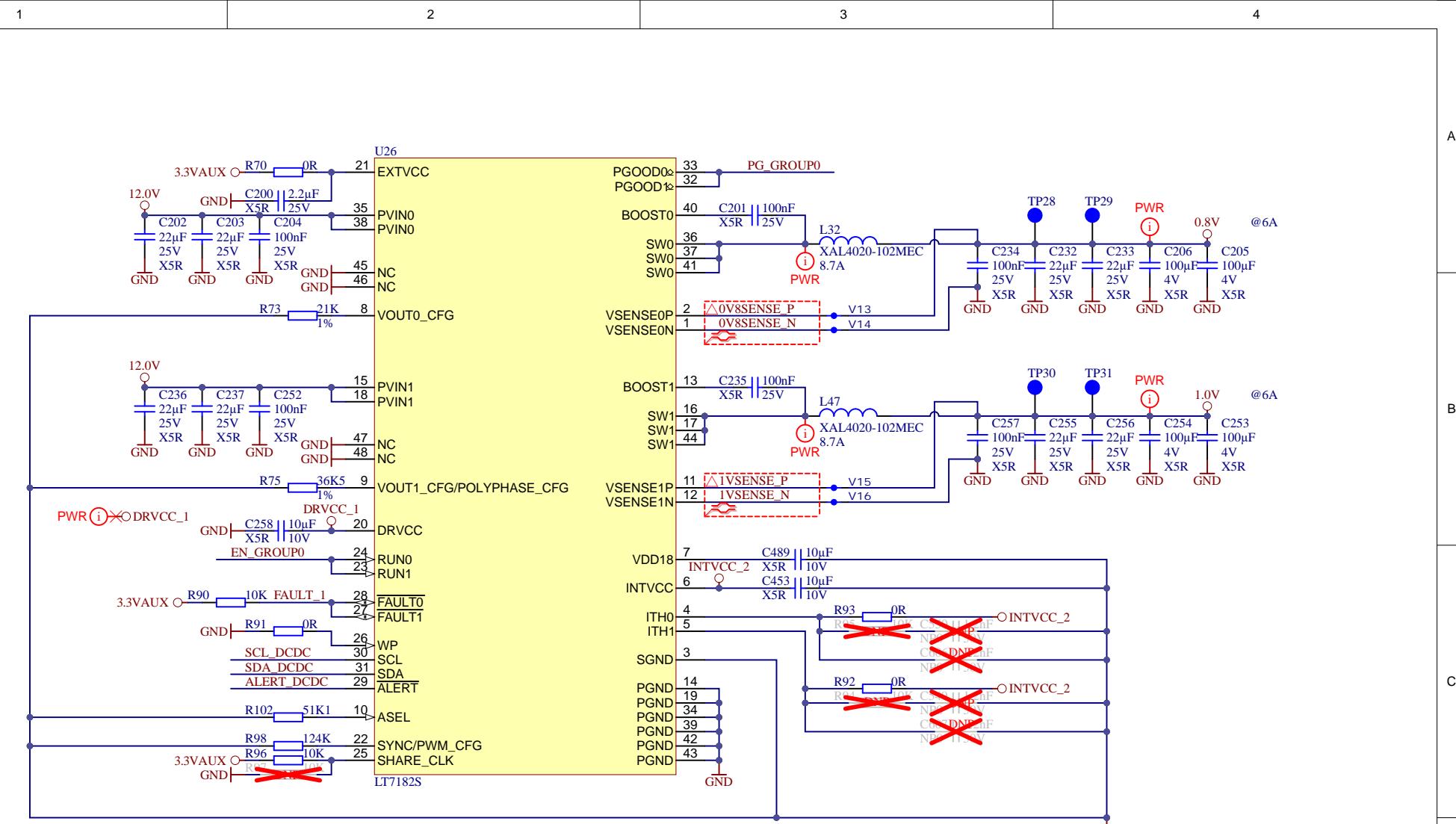
Device Address: 0x40
PWM Frequency: 2MHz
PWM Mode: Forced Continuous Mode
PWM Phase: 0°/180°

| Title: Power | |
|------------------------|----------------------------------|
| A4 | Number: TEI0185 P001 |
| Rev. 02 | |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH |
| Page 45 of 51 | |
| Filename: PWR_1.SchDoc | |



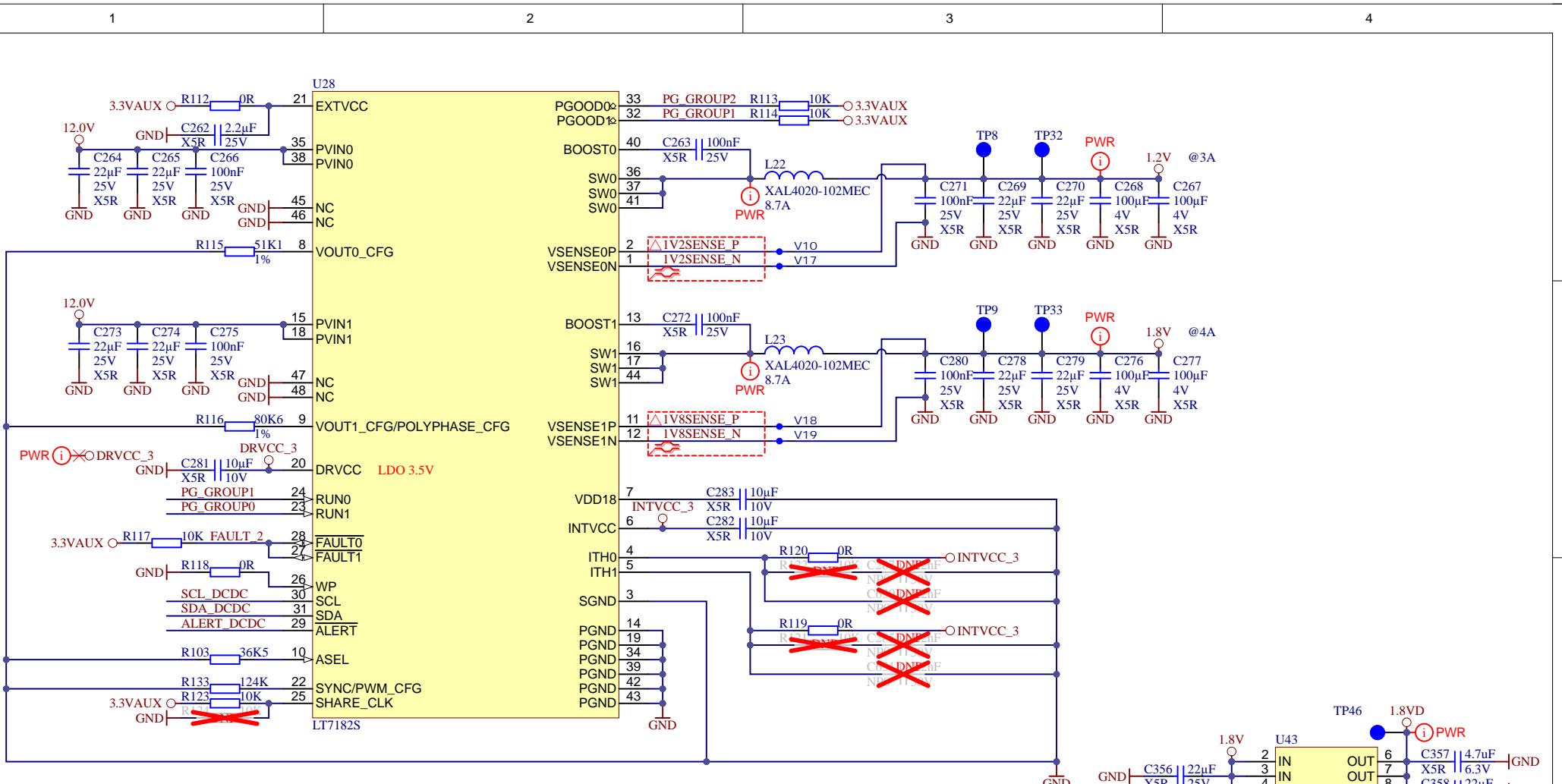
I2C ADDRESS: 0X31h
POCP=38A
FSW=500kHz
Scenario A

| | | |
|-------------------------------|---|-----------------------------|
| Title: Power | | |
| A4 | Number: TEI0185 P001 | Rev. 02 |
| Date: 2023-12-14 | Copyright: Trenz Electronic GmbH | Page 46 of 51 |
| Filename: PWR_2.SchDoc | | |



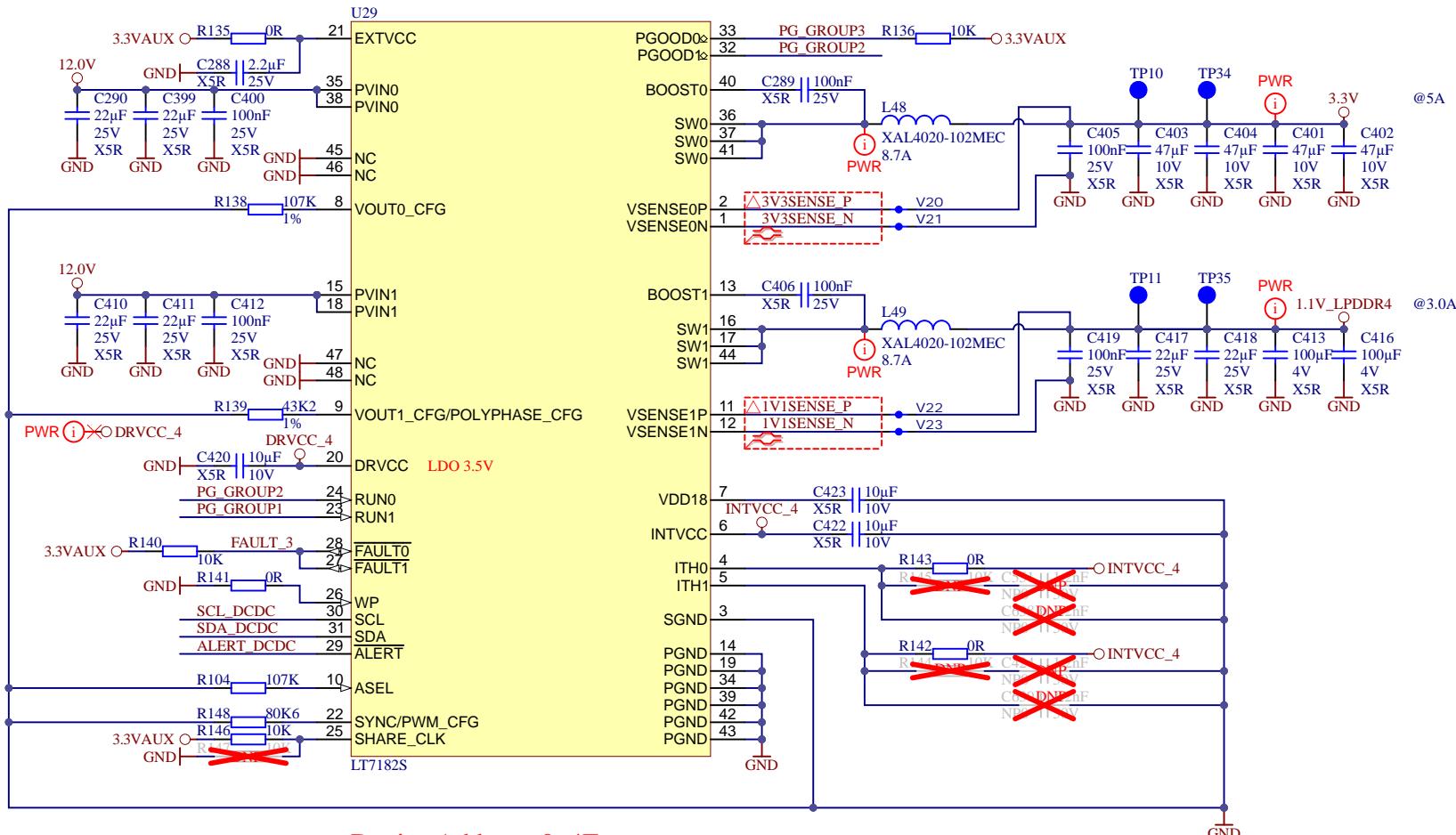
Device Address: 0x49
 PWM Frequency: 500kHz
 PWM Mode: Forced Continuous Mode
 PWM Phase: 0°/180°

| | | Title: Power | |
|------------------------|----------------------|----------------------------------|---------------|
| A4 | Number: TEI0185 P001 | | Rev. 02 |
| Date: 2023-11-15 | | Copyright: Trenz Electronic GmbH | Page 47 of 51 |
| Filename: PWR_3.SchDoc | | | |



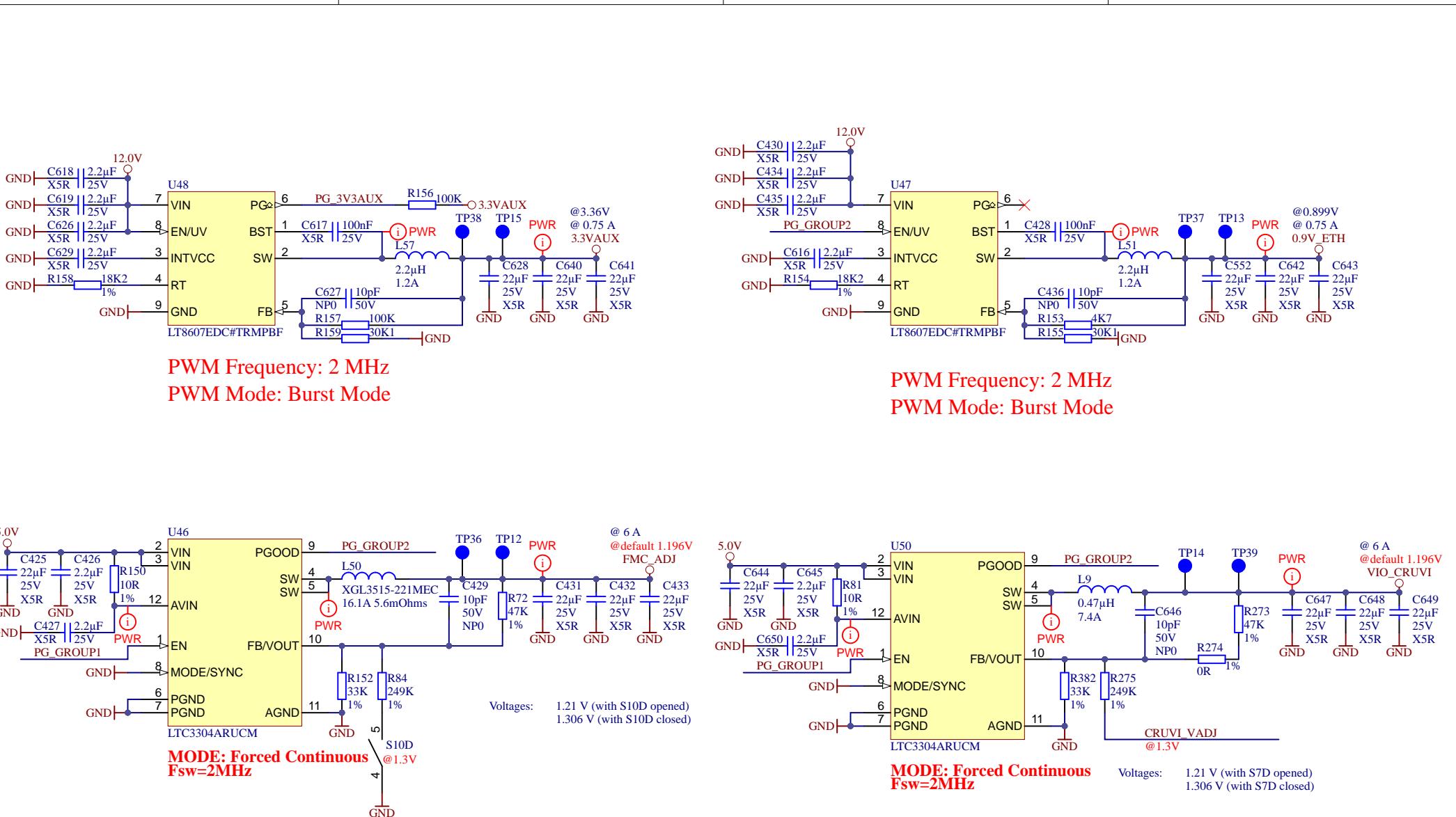
Device Address: 0x47
 PWM Frequency: 500kHz
 PWM Mode: Forced Continuous Mode
 PWM Phase: 0°/180°

| Title: Power | | |
|------------------------|----------------------------------|---------------|
| A4 | Number: TEI0185 P001 | Rev. 02 |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | Page 48 of 51 |
| Filename: PWR_4.SchDoc | | |



| | | | |
|------------------------|----------------------------------|--------------|---------------|
| | | Title: Power | |
| A4 | Number: TEI0185 P001 | | Rev. 02 |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | | Page 49 of 51 |
| Filename: PWR_5.SchDoc | | | |

1 2 3 4



| Title: Power | | |
|------------------------|----------------------------------|---------------|
| A4 | Number: TEI0185 P001 | Rev. 02 |
| Date: 2023-11-15 | Copyright: Trenz Electronic GmbH | Page 50 of 51 |
| Filename: PWR_6.SchDoc | | |

1 2 3 4