AXE5-Eagle User Guide

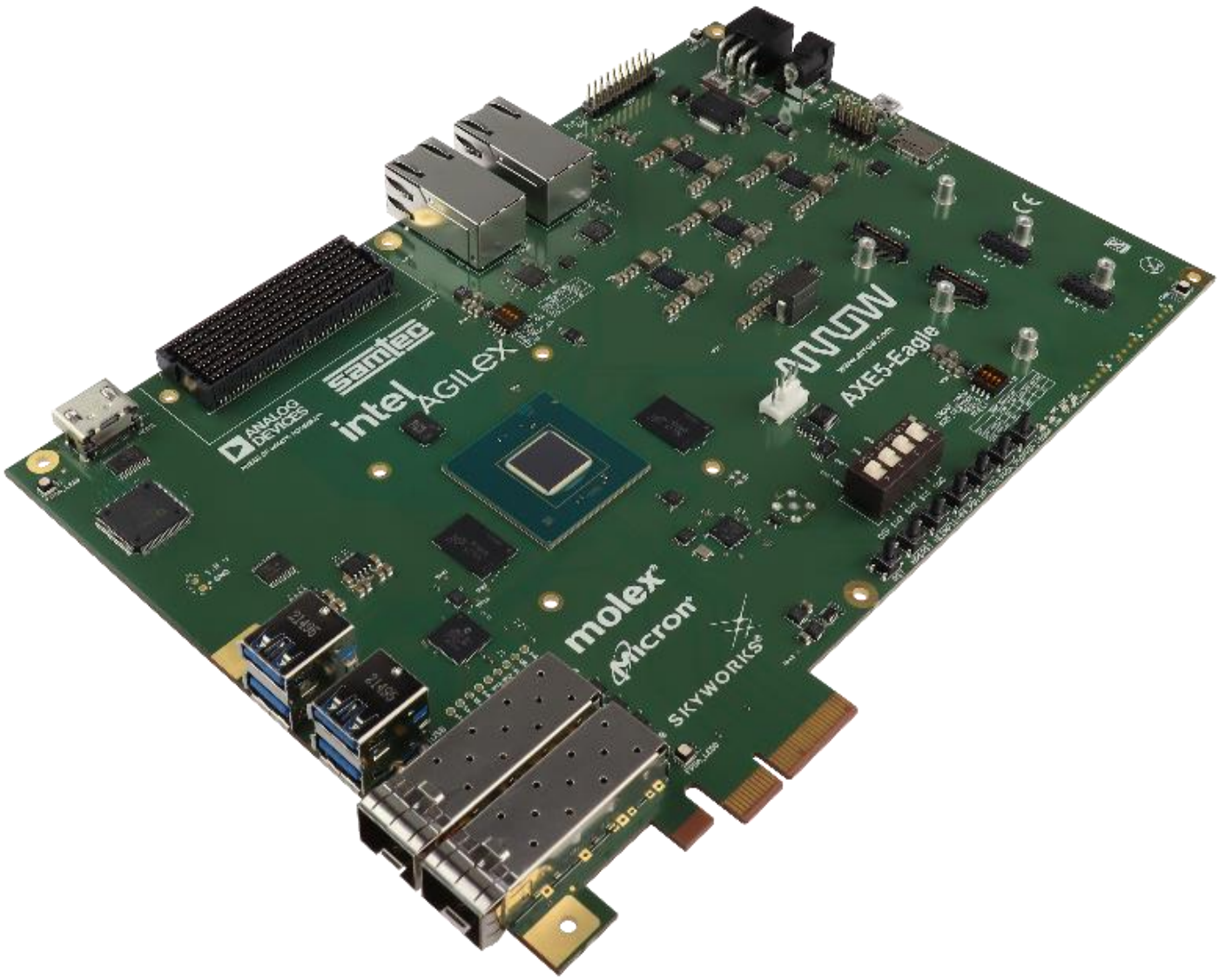

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Table of Contents

Table of figures

Chapter 1 - AXE5-Eagle Development Kit

1.1 About Arrow AXE5-Eagle Development Kit

The AXE5-Eagle Development Kit is a general-purpose, full-featured board in PCIe form factor delivering a development platform for evaluating the features of the Intel Agilex® 5 SoC FPGA. It supports various connector interfaces for transceivers, FPGA, and Hard Processor System (HPS) workloads providing a complete design environment to speed up the development.

The evaluation board is based on Intel Agilex® 5 E-Series SoC FPGA which provides power-efficient performance and smaller form factors for midrange FPGA applications. This series is manufactured using Intel 7 technology and offers advanced features such as a second-generation Intel® Hyperflex™ FPGA architecture, high-speed transceivers support up to 28.1 Gbps (17 Gbps is available on the development board), PCIe 4.0, and a processor system consisting of dual Arm Cortex-A76 cores and dual Arm Cortex-A55 cores. The capabilities and cutting-edge functionality of Intel Agilex® 5 are suitable for a broad range of applications that require high performance, lower power consumption, smaller form factor, and lower logic densities.

The AXE5-Eagle board is equipped with HPS-enabled hardware features, LPDDR4 memory, 2 Time-Sensitive Networking (TSN) capable 10/100/1000 Mbps Ethernet ports, 2 ports SFP+ cage for up to 16 Gbps, PCIe 4.0 x4 edge connector, 4 ports USB 3.1 Gen1, FMC+ connector, HDMI 1.4, microSD card, flash memory, CRUVI HS and LS interfaces.

The AXE5-Eagle Development Kit contains all the tools needed to use the board in conjunction with a computer that runs a 64-bit Linux or Microsoft Windows 10, Windows 11, or later operating system.

1.2 Useful Links

A set of useful links that can be used to get relevant information about the AXE5-Eagle development kit or the Agilex 5 FPGA and FPGA SoC.

- AXE5-Eagle at Arrow Shop
- Intel Agilex 5 Webpage
- AXE5-Eagle Wiki Page

1.3 Getting Help

To get help for this development kit, contact us at fpga_support@arrow.com

1.4 Documentation Guidelines

The meaning of the icon in this User Guide as follow:

This icon signposts warnings and important items that must be taken care of and needs to be aware of when operating the AXE5-Eagle Development Kit.

Chapter 2 - Introduction to the AXE5-Eagle Board

2.1 Layout and Components

Figure 1 and Figure 2 show the top and the bottom view of the board. It depicts the layout of the board and indicates the location of the various connectors and key components.

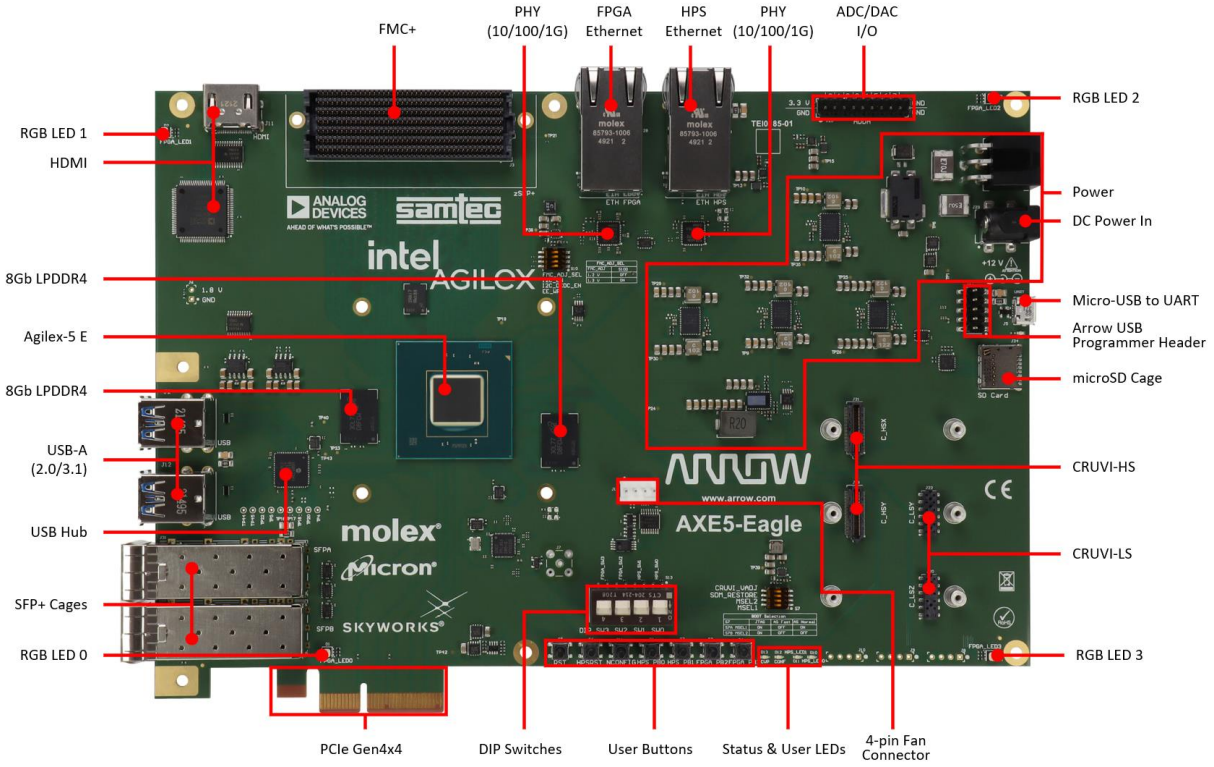

Figure 1 – AXE5-Eagle Board (top view)

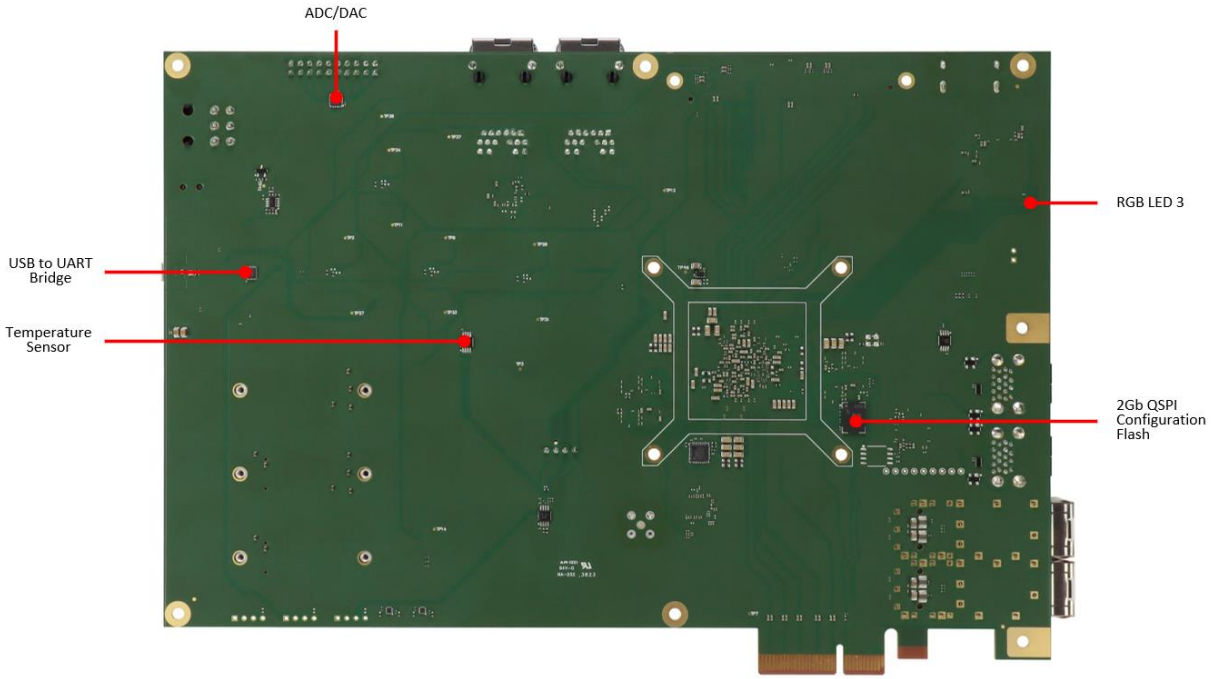

Figure 2 – AXE5-Eagle Board (bottom view)

2.2 Block Diagram

Figure 3 represents the block diagram of the board. All the connections are established through the Agilex SoC FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

A complete set of schematics and other board relevant files are available at Trenz Electronic.

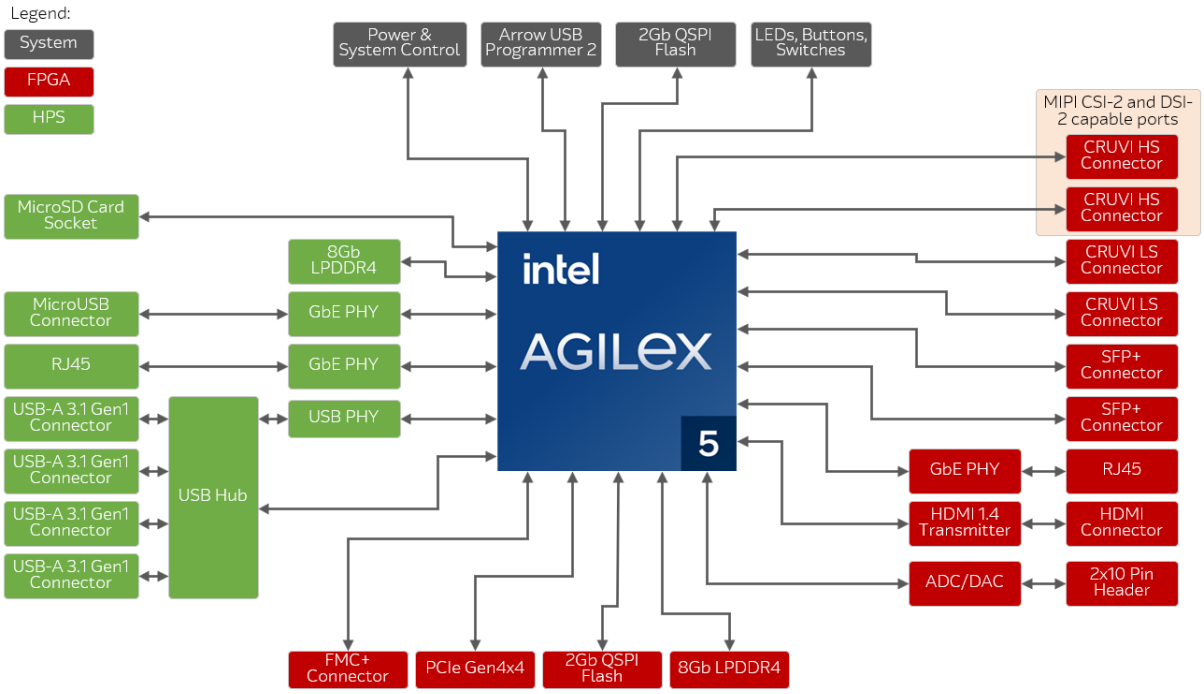

Figure 3 – AXE5-Eagle Block Diagram

2.3 Board Features

The following features are available on the AXE5-Eagle board:

System

FPGA Device:

- Intel Agilex® 5 E-Series SoC FPGA device:
    - A5ED065BB32AE4SR0 (Engineering Silicon)
    - A5ED043BB32AE4S (Production FPGA)

Features of the SoC FPGAs on the AXE5-Eagle Board:

Resources	Device	
	A5ED065B ('ES' version)	A5ED043B
Logic Elements (kLE)	656	434
Logic core architecture:	Second generation Intel Hyperflex™ FPGA architecture	
M20K Memory (Mb)	31.46	20.51
18x19 Multipliers	1,692	1,128
LVDS data rate	1.6 Gbps	
MIPI D-PHY data rate	2.5 Gbps	
Processor	• Dual core Arm Cortex-A76 up to 1.4 GHz • Dual core Arm Cortex-A55 up to 1.25 GHz	
Cache size	Shared: 2 MB L3 Cortex-A76: 64 KB L1, 256 KB L2 Cortex-A55: 32 KB L1, 128 KB L2	
Transceiver data rate	17.16 Gbps	
Process technology:	Intel 7	
Package	1591-pin VPBGA	

Board Management System:

- Power Monitor
- Temperature Monitor
- Fan Control
- Configurable Clock Source

FPGA Configuration and Debug

- 10-pin header for USB Blaster Programmer – JTAG mode
- 2 Gbit QSPI Flash – AS x4 Configuration scheme
- Partial reconfiguration support
- Support for Configuration via Protocol (CvP) through the PCI Express interface

FPGA Side

Memory Devices

- 8 Gbit 2133 MHz LPDDR4, 32 bits
- 2 Gbit QSPI Flash memory

- 2× 2 kbit serial MAC-Address EEPROMs
- 128 kbit EEPROM

Communication and Connectivity

- VITA 57.4 FMC+ Connector with 8 serial transceivers (8 RX and 8 TX)
- PCIe Gen4 x4 Edge connector
- 2× SFP+ connectors with up to 16 Gbps data rate
- 10/100/1000 Mbps Ethernet with TSN support via RJ45 connector
- HDMI 1.4 Transmitter with HDMI connector
- 2× CRUVI HS Connectors with MIPI D-PHY v2.5 interface
- 2× CRUVI LS Connectors
- 8-Channel, 12-Bit configurable ADC/DAC

HPS Side

Memory Devices

- 8 Gbit 2133 MHz LPDDR4, 32 bits
- microSD Card socket

Communication and Connectivity

- 10/100/1000 Mbps Ethernet with TSN support via RJ45 connector
- 4× USB-A 3.2 Gen1 Connectors
- USB to UART Bridge with Micro-USB Connector

Others

Buttons and Indicators

- 4× user RGB LEDs
- 2× green user LEDs
- 3× board status LEDs
- 7× push buttons
- 3× 4POS DIP switches

Power

- 2×3 PCIe auxiliary power input connector for PCIe add-in operation
- DC Jack power input connector for standalone operation
- Recommended external supply voltage range: +12.0 V, 6.25 A (nominal)
- Recommended I/O signal voltage ranges:
  - FMC+ interface: 0 to +1.3 V[1]
  - CRUVI HS interface: 0 to +1.3 V[1]
  - CRUVI LS interface: 0 to +3.3 V
  - ADC analog input: 0 to +2.5 V
  - ADC digital input: 0 to +3.3 V

[1] These values represent maximums. The VCCIO voltages are adjustable via DIP switches, thus their actual values might vary depending on the exact configuration.

Mechanical

- PCIe standard form factor (full height, 3/4 length)
- 165mm × 241 mm board size
- Air-cooled heatsink and optional fan

2.4 Ordering Information

This chapter provides information on the different versions of the development kit, including their corresponding ordering codes and the associated FPGA configurations.

Development Kit Version	Ordering Code	Core Device Part Number
ES version	AXE5-Eagle-ES	A5ED065BB32AE4SR0
Production (Q2 2025)	AXE5-Eagle	A5ED043BB32AE4S

2.5 Box Contents

The AXE5-Eagle Development Kit includes the following hardware:

- AXE5-Eagle development board
- 12VDC 40 W Power supply
- Arrow USB Programmer2
- Micro USB cable
- Passive Heatsink

Depending on the kit revision, additional components may need to be obtained. Please click on this link to review.

Chapter 3 - Development Board Setup

3.1 System Power

This development kit is designed to operate in two modes:

- **Standalone evaluation mode**
  In standalone evaluation mode, the board must be powered by the provided power supply connected to the power barrel connector J29 of the board.

- **PCIe add-in card mode**
  When operating the card as a PCIe endpoint in a PCIe-Compliant System, the board can be powered in two ways:

  - **Powered by the PCIe slot:** when the board is inserted into a PCI Express slot on a motherboard, it can be sourced entirely from the host. It eliminates the need for additional external power connections, relying solely on the power supply provided by the PCIe slot.

  - **ATX Power Supply:** insert the card into an available PCIe slot and connect a 2×3 pin PCIe power cable from the ATX Power Supply System to the power connector J27 of the board respectively. This power supply provides the entire power to the board without the need to obtain power from the PCIe slot. The J27 connector may not be populated on the board.

The power source selection occurs automatically on the AXE5-Eagle board. The external power connections, J27 and J29, take precedence over the PCIe power source without the need for user intervention or manual switching.

For detailed information about the AXE5-Eagle power system, see the Power Distribution System section.

Caution: Please note that the J27 and J29 input power supplies on the board are not electrically isolated from one another. It is crucial to operate the board using only one external power connection mode at a time. Using both simultaneously can result in unstable performance and may cause irreversible damage to the development kit, power supplies and even the surrounding environment.

Note: Before the AXE5-Eagle board is powered through the PCIe slot, ensure that the host PCIe system is able to deliver a minimum of 75W on the 12V power rail. If this requirement is not met, the board should be powered using the ATX Power Supply System.

3.2 DIP Switch Settings

There are switches on the AXE5-eagle development kit that affect the basic functionality of the board. These switches offer the ability to modify configurations and peripheral accesses and adjust circuit settings.

Before utilizing the kit, it is essential to review and verify the switch configurations. If it is necessary, configure them appropriately to align with the specific design requirements. The default setting is to have all switches in the low logic level position.

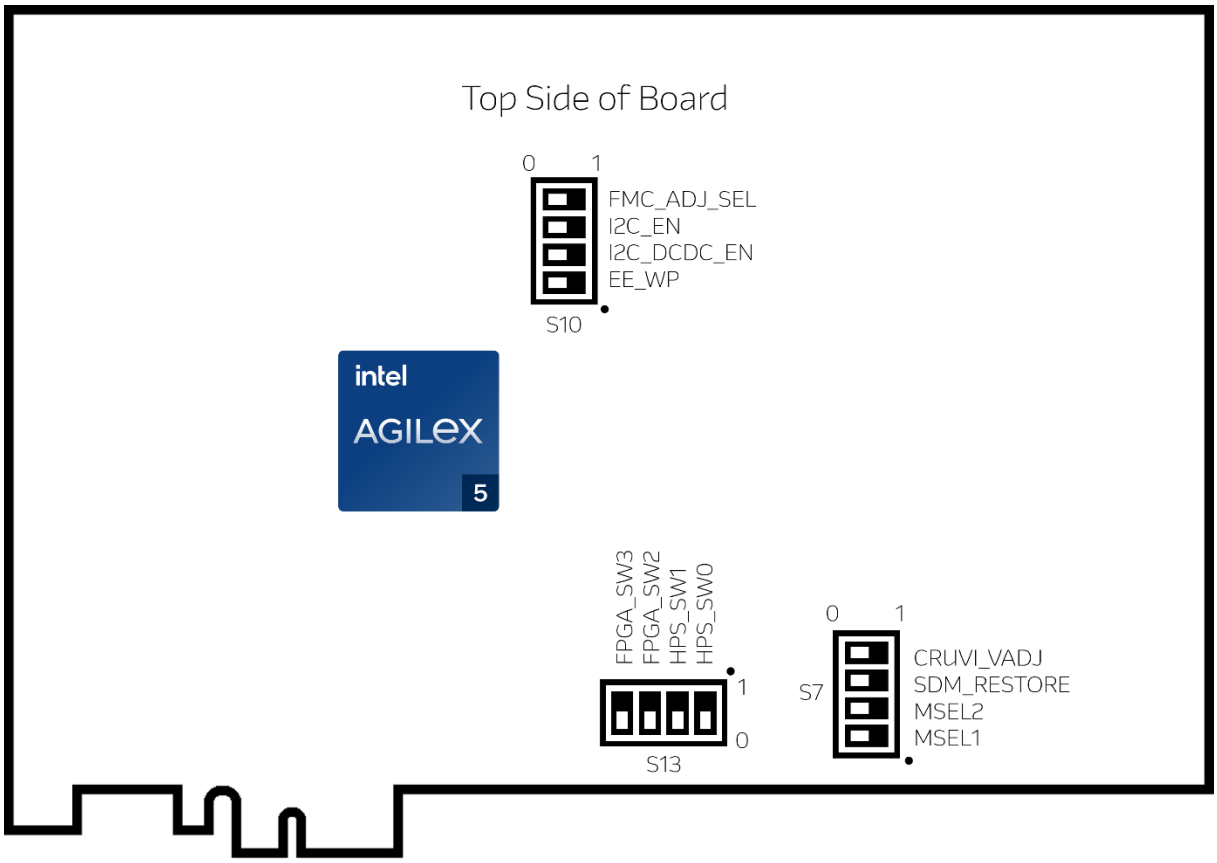

Figure 4 – Switch Locations

S7 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	MSEL1	Configuration scheme setting • MSEL [2], MSEL [1] = [0,0] QSPI AS Fast mode • MSEL [2], MSEL [1] = [0,1] QSPI AS Normal mode • MSEL [2], MSEL [1] = [1,0] Not supported mode • MSEL [2], MSEL [1] = [1,1] JTAG only mode MSEL [0] is tied to V_{CC}	0
2	MSEL2		0

Continued on the next page

Switch	Board Label	Function	Default Position
3	SDM_RESTORE	Direct to Factory input when RSU is used. • OFF: Load Application Image • ON: Load Factory Image	OFF
4	CRUVI_VADJ	IO Voltage select for CRUVI-HS Interfaces • ON: VIO_CRUVI = 1.3 V • OFF: VIO_CRUVI = 1.2 V	OFF

S10 DIP Switch Settings

Switch	Board Label	Function	Default Position
1	EE_WP	Write-Protect of EEPROM memory • ON: Read/Write operations are enabled • OFF: Only Read operations are enabled	OFF
2	I2C_DCDC_EN	Enable I^2C communication with the Power Supply System • ON: Disable • OFF: Enable	OFF
3	I2C_EN	Enable I^2C communication with the System Control's components • ON: Disable • OFF: Enable	OFF
4	FMC_ADJ_SEL	IO Voltage select for FMC+ Interface • ON: FMC_ADJ = 1.3 V • OFF: FMC_ADJ = 1.2 V	OFF

S13 DIP Switch Settings

The S13 DIP switch is a user-configurable input, allowing for various static variable inputs to be defined by the user for custom application configurations.

Switch	Board Label	FPGA Pin No.	Function	I/O Std	Default Position
1	HPS_SW0	PIN_N134	HPS user input	1.8-V LVCMOS	OFF
2	HPS_SW1	PIN_U135	HPS user input	1.8-V LVCMOS	OFF
3	FPGA_SW2	PIN_CL54	FPGA user input	Adjustable*	OFF
4	FPGA_SW3	PIN_CK63	FPGA user input	Adjustable*	OFF

** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on FMC_ADJ setting.*

Note: Without proper anti-static handling, you can damage the board.

3.3 Board Status Elements

The Arrow AXE5-Eagle development kit has overall 6 user-controlled LEDs and 3 board-specific status LEDs that indicate the status of the board. The following figure shows the status LED areas of the board.

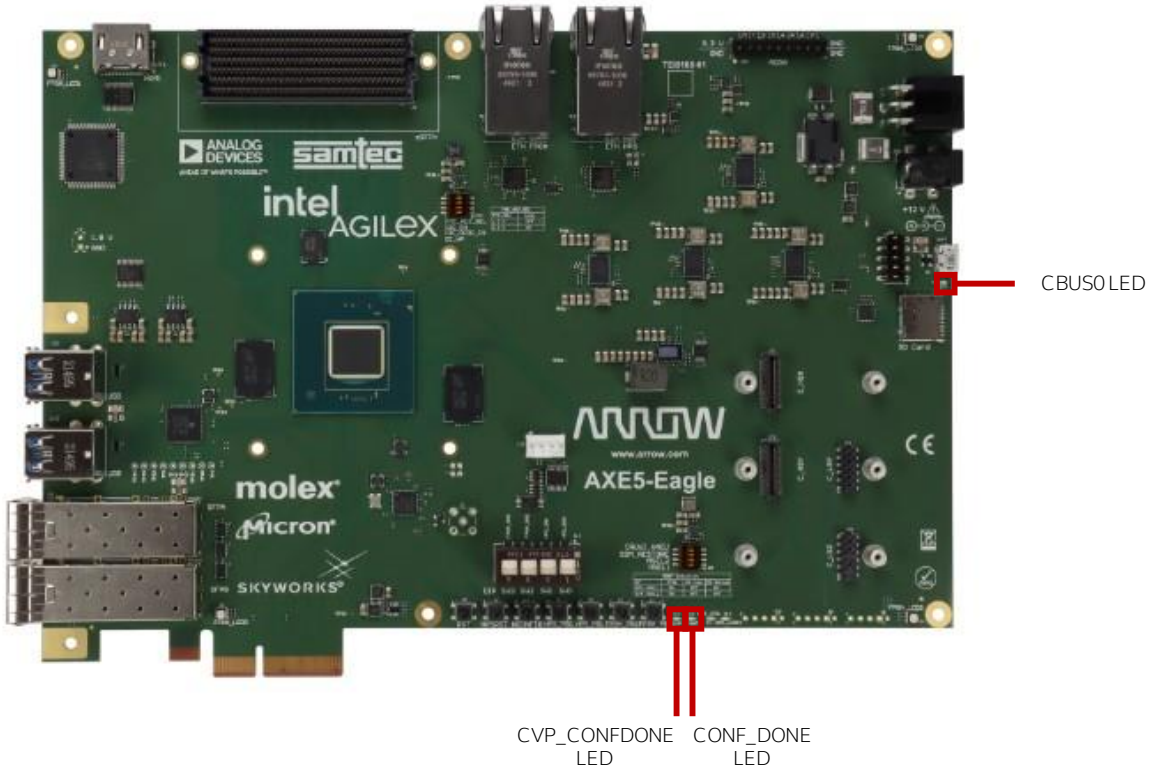

Figure 5 – Position of Indication LEDs

The following table defines the status LEDs. For user-controlled LED details, see User-defined LEDs section.

Board Reference	LED Name	Colour	Description
D12	CONF_DONE	Green	On when configuration data was loaded to Agilex 5 device without error
D13	CVP_CONFDONE	Green	On when Agilex 5 is fully configured via CvP initialization mode
D15	CBUS0	Green	Configurable pin of USB to UART bridge

Chapter 4 - Connections and Peripherals of the AXE5-Eagle Development Kit

4.1 Clock Circuitry

On the AXE5-Eagle board, the Intel Agilex 5 receives clock signals from multiple clock sources to ensure that the correct clock signal is directly available for different applications and interfaces.

The devkit contains two type of clock circuits:

- **On-Board Clock Circuits**
  This includes constant value oscillators and a preprogrammed, user-programmable PLL*, that are integrated into the board and provide all local clock signals for the operation of the AXE5-Eagle board including reference clocks for LPDDR4 memory interfaces, SFP+, FPGA SDM, fabric, and the HPS core.
  **The programming of the PLL is not the focus of this document. For detailed information regarding Si5332A PLL programming, we recommend visiting the manufacturer's website, where datasheets and other related documents are available.*

- **Off-Board Clock I/Os**
  The development board has optional input and output clocks which can be driven onto the board. These clock I/Os can be any preferred frequencies and different I/O standards according to the FPGA device's specification.

The clock system can be seen in Figure 6. For detailed clock connections, refer to the schematic.

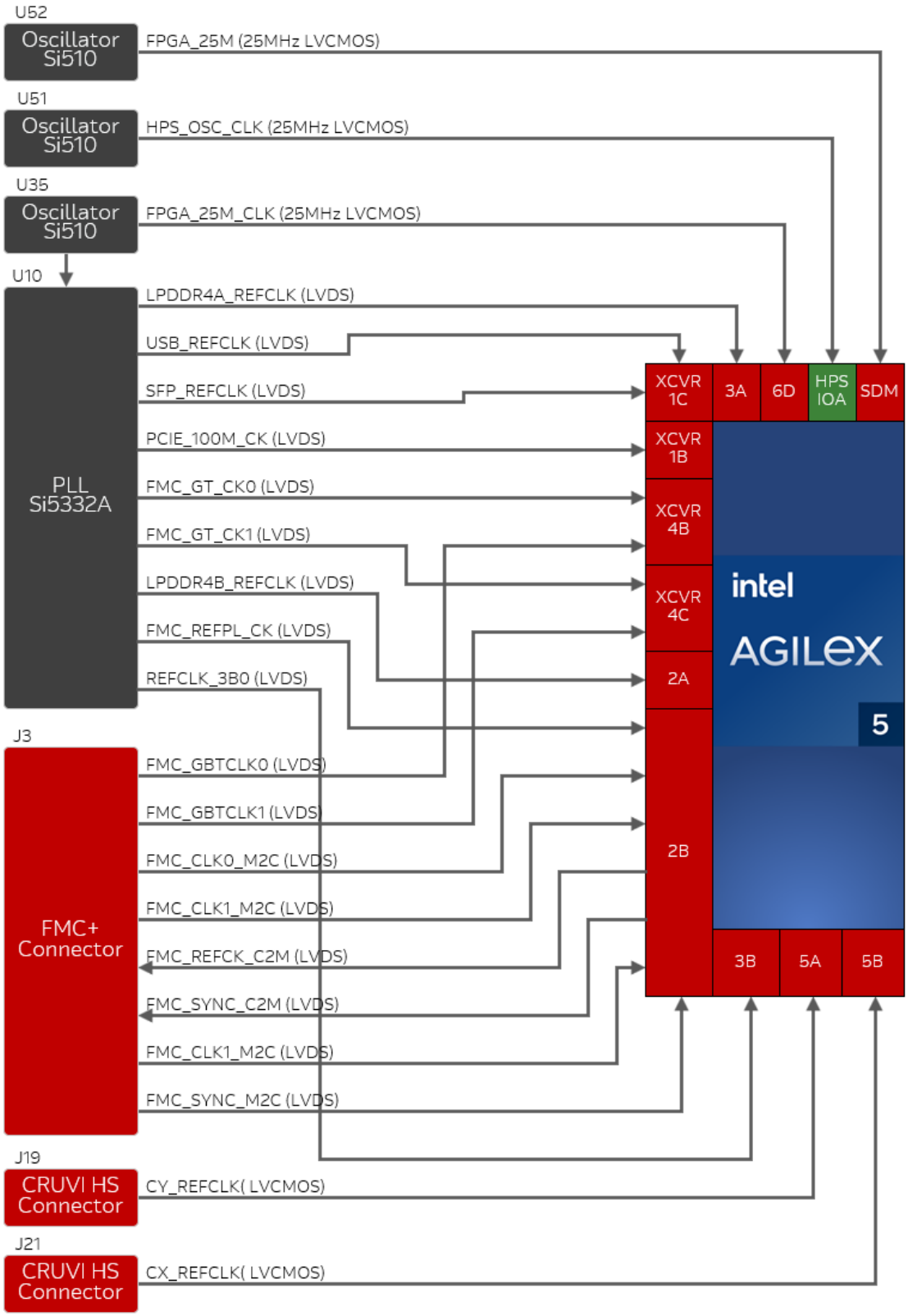

Figure 6 – Simplified Clock Connection Diagram

On-Board Clock Inputs

Board Reference	FPGA Pin No.	Clock Freq. (MHz)	Description	I/O Std
FPGA_25M	PIN_BR102	25	25 MHz clock for SDM	1.8-V LVCMOS
FPGA_25M_CLK	PIN_A23	25	25 MHz clock for FPGA Fabric	3.3-V LVCMOS
HPS_OSC_CLK	PIN_T132	25	25 MHz clock for HPS	1.8-V LVCMOS
FMC_GT_CK0_P	PIN_AY16	156.25	FMC+ GT clocks	CML
FMC_GT_CK0_N	PIN_AY21			
FMC_GT_CK1_P	PIN_AT16	156.25		CML
FMC_GT_CK1_N	PIN_AT21			
FMC_REFPL_CK_P	PIN_BR49	156.25	FMC+ reference clock for FPGA fabric	Adjustable*
FMC_REFPL_CK_N	PIN_BU49			
LPDDR4A_REFCK_P	PIN_M105	200	HPS LPDDR4 reference clock	1.1V True Differential Signaling
LPDDR4A_REFCK_N	PIN_K105			
LPDDR4B_REFCK_P	PIN_BW78	200	FPGA LPDDR4 reference clock	1.1V True Differential Signaling
LPDDR4B_REFCK_N	PIN_CA78			
PCIE_100M_CK_P	PIN_AY120	100	On board PCIe reference clock	CML
PCIE_100M_CK_N	PIN_AY115			
REFCLK_3B0_P	PIN_AC68	25	FPGA fabric reference clock	Adjustable**
REFCLK_3B0_N	PIN_AC72			
SFP_REFCLK_P	PIN_AT120	156.25	SFP+ reference clock	CML
SFP_REFCLK_N	PIN_AT115			
USB_REFCLK_P	PIN_AP120	100	USB 3.1 reference clock	CML
USB_REFCLK_N	PIN_AP115			

** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on FMC_ADJ setting.*
*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on CRUVI_ADJ.*
Note: For True Differential Signaling, Input Termination must be set to "differential".

Off-Board Clock I/Os

For detailed pinout information regarding off-board clock I/Os, please refer to the section associated with the respective connector.

4.2 I²C Structure

The I²C is a two-wire serial communication protocol that allows multiple devices to communicate with each other over a common bus.

The Intel Agilex 5 device use the I²C for reading and writing to the various components on the board and have option to utilize it as the I²C host for accessing the devices, adjusting clock frequencies, obtaining board status data or accessing EEPROM memory.

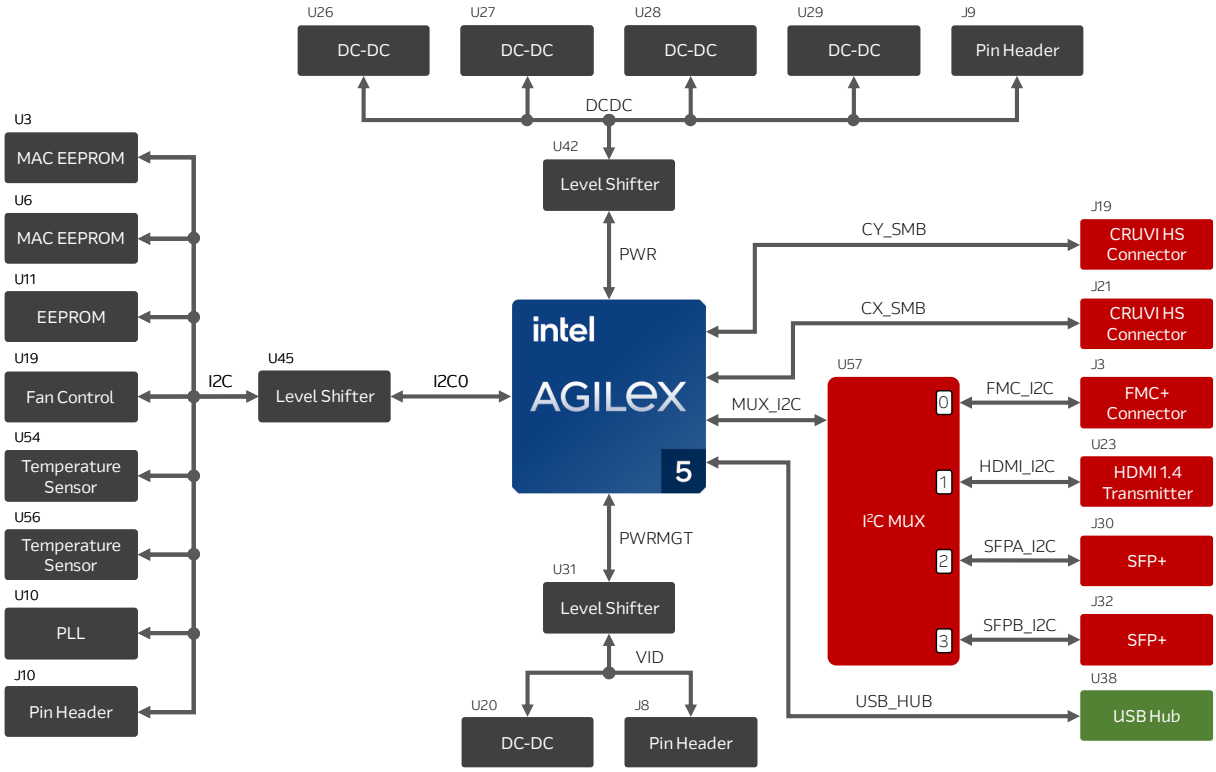

Figure 7 – I²C Block Diagram

I²C Device Address Table

All I²C addresses are in 7-bit format.

Bus	Address	Device Part Number	Device Label	Device Name
PWR	0x49	LT7182S	U26	DC to DC Converter
	0x40	LT7182S	U27	DC to DC Converter
	0x47	LT7182S	U28	DC to DC Converter
	0x4E	LT7182S	U29	DC to DC Converter
	-	-	J9	Pin Header
PWRMGT	0x31	MAX20830	U20	DC to DC Converter
	-	-	J8	Pin Header
I2C0	0x50	24AA025E48	U3	MAC EEPROM
	0x51	24AA025E48	U6	MAC EEPROM
	0x54	24AA128	U11	EEPROM
	0x57	MAX31760	U19	Fan Control
	0x48	ADT75	U54	Temperature Sensor
	0x49	ADT75	U56	Temperature Sensor
	0x6A	SI5332A	U10	PLL
	-	-	J10	Pin Header
MUX_I2C	0x70	TCA9544A	U57	I²C MUX
	-	-	J3	FMC+ Connector
	0x72	ADV7511	U23	HDMI Transmitter
	0x50[2]	-	J30	SFP+ Connector
	0x50[2]	-	J32	SFP+ Connector
USB_HUB	0x2D	USB5734	U38	USB Hub
CY_SMB	-	-	J19	CRUVI HS Connector
CX_SMB	-	-	J21	CRUVI HS Connector

4.2.1 Power and System Control

The I²C bus forms the essential interface for board management. This management system is divided into two parts:

- The PWR and the PWRMGT I²C bus lines provide access to the power system thereby enabling control of the power supply and taking advantage of the SmartVID* capability of Agilex 5. The SmartVID* technology enables dynamic power consumption control during the FPGA operation without compromising system stability or reliability. This feature contributes to the efficiency and energy saving of FPGAs in various application areas. The Intel FPGA documentation provides detailed information on setting up and using SmartVID*.

  * Installed Group B devices do not support SmartVID. Feature is reserved for the future.

[2] Default SFP+ I²C address, it may differ depending on the exact device.

- The I2C0 bus line enables access to various board management functions such as MAC and user EEPROMs, temperature sensors fan control, and PLL clock system.

  Devices connected to the I2C0 bus line:

  - 2× **MAC Address EEPROMs:** 24AA025E48T from Microchip, which is a serial pre-programmed EEPROM memory. It only contains its own unique number to give individual identification and Internet addressing;
  - **User EEPROM:** 24AA128T from Microchip, which is a serial EEPROM for custom application-related configuration data;
  - **Fan Controller:** in accordance with data measured by various temperature sensors, supervising and regulating the fan speed to prevent the FPGA device and the board from overheating;
  - **PLL:** provides clock to the FPGA and other board components;
  - 2× **Temperature sensors**: these devices function is to measure and monitor the board temperature;

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
I2C0_SDA	PIN_U134	Bidir	Serial Data Line of I2C0	1.8-V LVCMOS
I2C0_SCL	PIN_AL120	Bidir	Serial Clock Line of I2C0	1.8-V LVCMOS
PWR_SDA	PIN_J2	Bidir	Serial Data Line of PWR	1.8-V LVCMOS
PWR_SCL	PIN_G2	Bidir	Serial Clock Line of PWR	1.8-V LVCMOS
PWRMGT_SDA	PIN_CF99	Bidir	Serial Data Line of PWRMGT	1.8-V LVCMOS
PWRMGT_SCL	PIN_CF109	Bidir	Serial Clock Line of PWRMGT	1.8-V LVCMOS

4.2.2 I²C MUX and FPGA Peripherals

The I²C bus also provides access to managing interfaces of various FPGA peripherals. These peripherals are the USB Hub, CRUVI HS and FMC+ connectors, HDMI and SFP+ transmitters. All excepted CRUVI HS connectors and USB Hub are accessed through a common I²C MUX device, which needs to be configured and set separately before communicating with peripherals.

To select a channel, do an I2C write with the value in the channel select column to the MUX TCA9544 (U57) at I2C address 0x70.

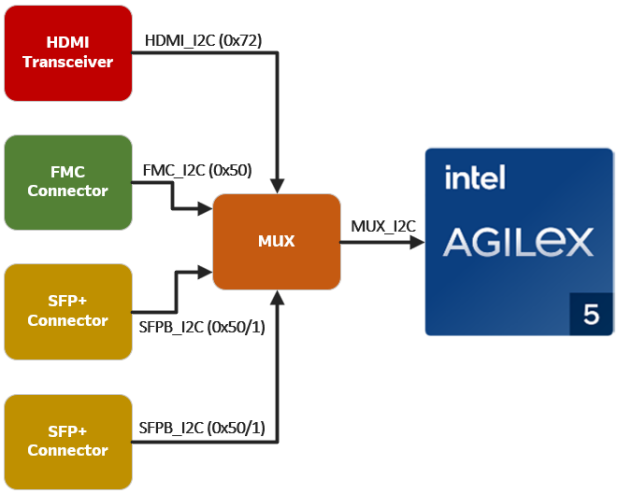

Figure 8 – I2C MUX Connections

I2C MUX Channel Assignment

Channel	Channel Select	Device Label	I2C Address	Device Name
0	0x04	J3	0x50	FMC+ Connector
1	0x05	U23	0x72	HDMI Transmitter
2	0x06	J30	0x50	SFP+ Connector
3	0x07	J32	0x50	SFP+ Connector

FPGA Pin Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
MUX_I2C_SDA	PIN_F4	Bidir	Serial Data Line	1.8-V LVCMOS
MUX_I2C_SCL	PIN_D4	Bidir	Serial Clock Line	1.8-V LVCMOS
MUX_I2C_INT	PIN_K4	Input	Peripheral Interrupts	1.8-V LVCMOS

For further connections of the interfaces, please refer to the section about the specific interface.

Note: Please be advised that the I^2C MUX address (0x70) is persistently present on MUX_I2C and on all I^2C buses connected to it. Consequently, users are advised to avoid using this address assignment for any connected devices on FMC+ or SFP+ connectors.

4.3 Peripherals Connected to the Agilex 5 SoC FPGA

The Agilex 5 SoC FPGA connects to various peripherals for both the FPGA and HPS parts. The versatile peripheral integration offers a flexible platform and ensures efficient and seamless system operation with the SoC FPGA, resulting in faster and smoother development cycles.

4.3.1 Configuration

There are multiple types of configuration methods supported by AXE5-Eagle:

- **JTAG Configuration:** configuration using JTAG ports. JTAG configuration scheme allows you to directly configure the device core through JTAG pins (TDI, TDO, TMS and TCK pins). The Quartus Prime software automatically generates a .sof that can be downloaded to the Agilex 5 with a download cable through the Quartus Prime Programmer. The AXE5-Eagle board uses an integrated Arrow USB Programmer2 to perform configuration of the FPGA for JTAG configuration.

- **Active Serial Configuration from QSPI flash:** configuration using external flash. Before configuration, you need to program the configuration data .jic into the configuration flash memory which provides non-volatile storage for the bit stream. The information is retained within flash memory even if the AXE5-Eagle is turned off. When the board is powered on, the configuration data in the flash memory is automatically loaded into the Agilex 5 FPGA.

- **Configuration via Protocol through PCI Express**: it is an advanced and powerful method for FPGA configuration. This configuration scheme leverages the high-speed PCIe interface to efficiently update the configuration bitstream of the FPGA, offering seamless adaptability in real-time applications.

For detailed information about how to configure the Agilex 5, please refer to Chapter 7.

4.3.1.1 JTAG Chain Configuration

The JTAG Chain Configuration is controlled by an Arrow USB Programmer2 module which is a development tool for Intel FPGAs and supported by Intel Quartus Prime. For connection to the AXE5-Eagle board, there is used the standard JTAG header. The following diagram illustrates its connection.

For the detailed operation of this module, please refer to the related Technical Reference Manual.

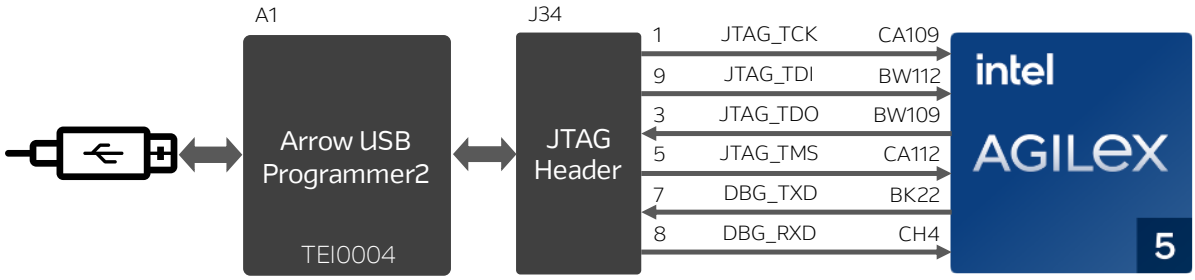

Figure 9 –JTAG Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
JTAG_TCK	PIN_CA109	Input	Test Interface Clock	1.8-V LVCMOS
JTAG_TDI	PIN_BW112	Input	Test Data In	1.8-V LVCMOS
JTAG_TDO	PIN_BW109	Output	Test Data Out	1.8-V LVCMOS
JTAG_TMS	PIN_CA112	Input	Test Mode Select	1.8-V LVCMOS
DBG_TXD	PIN_BK22	Output	Additional UART TX	1.8-V LVCMOS
DBG_RXD	PIN_CH4	Input	Additional UART RX	1.8-V LVCMOS

4.3.1.2 QSPI Configuration Flash Memory

The AXE5-Eagle board is integrated with a 2 Gbit of QSPI flash memory that can be used for user data and programming non-volatile storage. The configuration bitstream is downloaded into the configuration device which automatically loads the configuration data into the Agilex 5 when the board is powered on. The Secure Device Manager (SDM) in Agilex 5 SoC FPGA is responsible for the entire AS mode process and interface.

Device memory capacity not consumed storing configuration data can be used as general-purpose non-volatile memory, which with its operation of up to 166 MHz is perfect for program and data storage. Several interfaces available with Nios V embedded processors allow you to access the serial configuration device as a memory module connected to your embedded system.

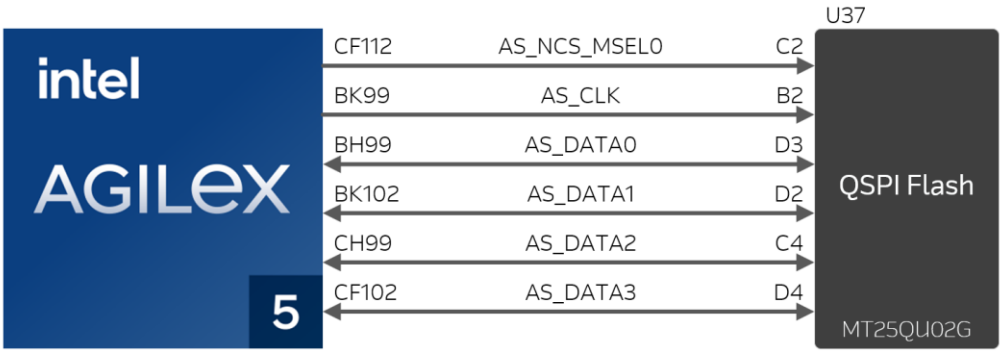

Figure 10 – Configuration Flash Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
AS_NCS_MSEL0	PIN_CF112	Output	Dual purpose I/O, **MSEL[0]** during power-up, **Chip Select** after determining the configuration scheme	1.8-V LVCMOS
AS_CLK	PIN_BK99	Output	Clock	1.8-V LVCMOS
AS_DATA0	PIN_BH99	Bidir	Data [0]	1.8-V LVCMOS
AS_DATA1	PIN_BK102	Bidir	Data [1]	1.8-V LVCMOS
AS_DATA2	PIN_CH99	Bidir	Data [2]	1.8-V LVCMOS
AS_DATA3	PIN_CF102	Bidir	Data [3]	1.8-V LVCMOS

4.3.2 Memory Interfaces

The AXE5-Eagle development board supports an array of volatile and non-volatile interface options. From high-speed DDR memory to large-capacity flash memory, it provides adaptable solutions in various applications by addressing a broad spectrum of memory integration.

4.3.2.1 LPDDR4 memory

The AXE5-Eagle board supports single-chip LPDDR4 with 8 Gbit density, operating at a speed of 2133 MHz, for both the FPGA and the HPS parts. Below are the connections and pinning of the LPDDR4 used in the AXE5-Eagle.

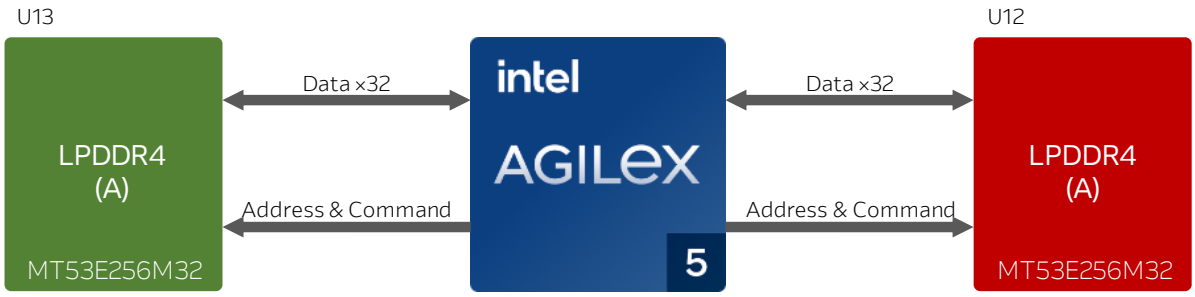

Figure 11 – LPDDR4 Connections

LPDDR4 (A) – HPS Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
LPDDR4A_CK_P	PIN_AK107	Output	Differential clock	1.1-V LVSTL
LPDDR4A_CK_N	PIN_AK104			
LPDDR4A_CKE0	PIN_V108	Output	Clock enable	1.1-V LVSTL
LPDDR4A_CKE1	PIN_T108	Output	Clock enable	1.1-V LVSTL
LPDDR4A_CS0_N	PIN_T105	Output	Chip select	1.1-V LVSTL
LPDDR4A_CS1_N	PIN_P105	Output	Chip select	1.1-V LVSTL
LPDDR4A_RST	PIN_AG111	Output	Reset	1.1-V LVSTL
LPDDR4A_CA0	PIN_T114	Output	Command/Address	1.1-V LVSTL
LPDDR4A_CA1	PIN_P114	Output	Command/Address	1.1-V LVSTL
LPDDR4A_CA2	PIN_V117	Output	Command/Address	1.1-V LVSTL
LPDDR4A_CA3	PIN_T117	Output	Command/Address	1.1-V LVSTL
LPDDR4A_CA4	PIN_M114	Output	Command/Address	1.1-V LVSTL
LPDDR4A_CA5	PIN_K114	Output	Command/Address	1.1-V LVSTL
LPDDR4A_DQ0	PIN_B128	Bidir	Data [0]	1.1-V LVSTL
LPDDR4A_DQ1	PIN_A128	Bidir	Data [1]	1.1-V LVSTL
LPDDR4A_DQ2	PIN_B130	Bidir	Data [2]	1.1-V LVSTL
LPDDR4A_DQ3	PIN_A130	Bidir	Data [3]	1.1-V LVSTL
LPDDR4A_DQ4	PIN_B116	Bidir	Data [4]	1.1-V LVSTL
LPDDR4A_DQ5	PIN_A116	Bidir	Data [5]	1.1-V LVSTL

Continued on the next page

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
LPDDR4A_DQ6	PIN_B113	Bidir	Data [6]	1.1-V LVSTL
LPDDR4A_DQ7	PIN_A113	Bidir	Data [7]	1.1-V LVSTL
LPDDR4A_DQ8	PIN_F117	Bidir	Data [8]	1.1-V LVSTL
LPDDR4A_DQ9	PIN_H117	Bidir	Data [9]	1.1-V LVSTL
LPDDR4A_DQ10	PIN_K117	Bidir	Data [10]	1.1-V LVSTL
LPDDR4A_DQ11	PIN_M117	Bidir	Data [11]	1.1-V LVSTL
LPDDR4A_DQ12	PIN_H108	Bidir	Data [12]	1.1-V LVSTL
LPDDR4A_DQ13	PIN_F108	Bidir	Data [13]	1.1-V LVSTL
LPDDR4A_DQ14	PIN_M108	Bidir	Data [14]	1.1-V LVSTL
LPDDR4A_DQ15	PIN_K108	Bidir	Data [15]	1.1-V LVSTL
LPDDR4A_DQ16	PIN_H98	Bidir	Data [16]	1.1-V LVSTL
LPDDR4A_DQ17	PIN_F98	Bidir	Data [17]	1.1-V LVSTL
LPDDR4A_DQ18	PIN_M98	Bidir	Data [18]	1.1-V LVSTL
LPDDR4A_DQ19	PIN_K98	Bidir	Data [19]	1.1-V LVSTL
LPDDR4A_DQ20	PIN_K87	Bidir	Data [20]	1.1-V LVSTL
LPDDR4A_DQ21	PIN_M87	Bidir	Data [21]	1.1-V LVSTL
LPDDR4A_DQ22	PIN_F84	Bidir	Data [22]	1.1-V LVSTL
LPDDR4A_DQ23	PIN_D84	Bidir	Data [23]	1.1-V LVSTL
LPDDR4A_DQ24	PIN_A106	Bidir	Data [24]	1.1-V LVSTL
LPDDR4A_DQ25	PIN_B103	Bidir	Data [25]	1.1-V LVSTL
LPDDR4A_DQ26	PIN_B106	Bidir	Data [26]	1.1-V LVSTL
LPDDR4A_DQ27	PIN_A110	Bidir	Data [27]	1.1-V LVSTL
LPDDR4A_DQ28	PIN_B81	Bidir	Data [28]	1.1-V LVSTL
LPDDR4A_DQ29	**PIN_A94**	**Bidir**	**Data [29]**	
LPDDR4A_DQ30	PIN_B88	Bidir	Data [30]	1.1-V LVSTL
LPDDR4A_DQ31	PIN_A91	Bidir	Data [31]	1.1-V LVSTL
LPDDR4A_DQSA0_P	PIN_B122	Bidir	Data strobe	1.1-V LVSTL
LPDDR4A_DQSA0_N	PIN_A125			
LPDDR4A_DQSA1_P	PIN_F114	Bidir	Data strobe	1.1-V LVSTL
LPDDR4A_DQSA1_N	PIN_D114			
LPDDR4A_DQSB0_P	PIN_F95	Bidir	Data strobe	1.1-V LVSTL
LPDDR4A_DQSB0_N	PIN_D95			
LPDDR4A_DQSB1_P	PIN_A101	Bidir	Data strobe	1.1-V LVSTL
LPDDR4A_DQSB1_N	PIN_B101			
LPDDR4A_DMA0	PIN_B119	Bidir	Data mask/Data bus inversion	1.1-V LVSTL
LPDDR4A_DMA1	PIN_F105	Bidir	Data mask/Data bus inversion	1.1-V LVSTL
LPDDR4A_DMB0	PIN_H87	Bidir	Data mask/Data bus inversion	1.1-V LVSTL
LPDDR4A_DMB1	PIN_B97	Bidir	Data mask/Data bus inversion	1.1-V LVSTL

LPDDR4 (B) – FPGA Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
LPDDR4B_CK_P	PIN_BM81	Output	Differential clock	1.1-V LVSTL
LPDDR4B_CK_N	PIN_BP81			
LPDDR4B_CKE0	PIN_BR81	Output	Clock enable	1.1-V LVSTL
LPDDR4B_CKE1	PIN_BU81	Output	Clock enable	1.1-V LVSTL
LPDDR4B_CS0_N	PIN_BR78	Output	Chip select	1.1-V LVSTL
LPDDR4B_CS1_N	PIN_BU78	Output	Chip select	1.1-V LVSTL
LPDDR4B_RST	PIN_BH92	Output	Reset	1.1-V LVSTL
LPDDR4B_CA0	PIN_BR89	Output	Command/Address	1.1-V LVSTL
LPDDR4B_CA1	PIN_BU89	Output	Command/Address	1.1-V LVSTL
LPDDR4B_CA2	PIN_BR92	Output	Command/Address	1.1-V LVSTL
LPDDR4B_CA3	PIN_BU92	Output	Command/Address	1.1-V LVSTL
LPDDR4B_CA4	PIN_BW89	Output	Command/Address	1.1-V LVSTL
LPDDR4B_CA5	PIN_CA89	Output	Command/Address	1.1-V LVSTL
LPDDR4B_DQ0	PIN_CL91	Bidir	Data [0]	1.1-V LVSTL
LPDDR4B_DQ1	PIN_CK94	Bidir	Data [1]	1.1-V LVSTL
LPDDR4B_DQ2	PIN_CK97	Bidir	Data [2]	1.1-V LVSTL
LPDDR4B_DQ3	PIN_CL97	Bidir	Data [3]	1.1-V LVSTL
LPDDR4B_DQ4	PIN_CK80	Bidir	Data [4]	1.1-V LVSTL
LPDDR4B_DQ5	PIN_CL82	Bidir	Data [5]	1.1-V LVSTL
LPDDR4B_DQ6	PIN_CK76	Bidir	Data [6]	1.1-V LVSTL
LPDDR4B_DQ7	PIN_CL76	Bidir	Data [7]	1.1-V LVSTL
LPDDR4B_DQ8	PIN_CC92	Bidir	Data [8]	1.1-V LVSTL
LPDDR4B_DQ9	PIN_CA92	Bidir	Data [9]	1.1-V LVSTL
LPDDR4B_DQ10	PIN_CF92	Bidir	Data [10]	1.1-V LVSTL
LPDDR4B_DQ11	PIN_CH92	Bidir	Data [11]	1.1-V LVSTL
LPDDR4B_DQ12	**PIN_CA81**	**Bidir**	**Data [12]**	**1.1-V LVSTL**
LPDDR4B_DQ13	PIN_CC81	Bidir	Data [13]	1.1-V LVSTL
LPDDR4B_DQ14	PIN_CH78	Bidir	Data [14]	1.1-V LVSTL
LPDDR4B_DQ15	PIN_CF78	Bidir	Data [15]	1.1-V LVSTL
LPDDR4B_DQ16	PIN_BR69	Bidir	Data [16]	1.1-V LVSTL
LPDDR4B_DQ17	PIN_BU69	Bidir	Data [17]	1.1-V LVSTL
LPDDR4B_DQ18	PIN_BR71	Bidir	Data [18]	1.1-V LVSTL
LPDDR4B_DQ19	PIN_BU71	Bidir	Data [19]	1.1-V LVSTL
LPDDR4B_DQ20	PIN_BU59	Bidir	Data [20]	1.1-V LVSTL
LPDDR4B_DQ21	PIN_BR59	Bidir	Data [21]	1.1-V LVSTL
LPDDR4B_DQ22	PIN_BW59	Bidir	Data [22]	1.1-V LVSTL
LPDDR4B_DQ23	PIN_CA59	Bidir	Data [23]	1.1-V LVSTL
LPDDR4B_DQ24	PIN_CF71	Bidir	Data [24]	1.1-V LVSTL
LPDDR4B_DQ25	PIN_CH71	Bidir	Data [25]	1.1-V LVSTL
LPDDR4B_DQ26	PIN_CC71	Bidir	Data [26]	1.1-V LVSTL
LPDDR4B_DQ27	PIN_CA71	Bidir	Data [27]	1.1-V LVSTL
LPDDR4B_DQ28	PIN_CF62	Bidir	Data [28]	1.1-V LVSTL

Continued on the next page

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
LPDDR4B_DQ29	PIN_CH62	Bidir	Data [29]	1.1-V LVSTL
LPDDR4B_DQ30	PIN_CF59	Bidir	Data [30]	1.1-V LVSTL
LPDDR4B_DQ31	PIN_CH59	Bidir	Data [31]	1.1-V LVSTL
LPDDR4B_DQSA0_P	PIN_CL88	Bidir	Data strobe	1.1-V LVSTL
LPDDR4B_DQSA0_N	PIN_CK88			
LPDDR4B_DQSA1_P	PIN_CH89	Bidir	Data strobe	1.1-V LVSTL
LPDDR4B_DQSA1_N	PIN_CF89			
LPDDR4B_DQSB0_P	PIN_BW69	Bidir	Data strobe	1.1-V LVSTL
LPDDR4B_DQSB0_N	PIN_CA69			
LPDDR4B_DQSB1_P	PIN_CH69	Bidir	Data strobe	1.1-V LVSTL
LPDDR4B_DQSB1_N	PIN_CF69			
LPDDR4B_DMA0	PIN_CK85	Bidir	Data mask/Data bus inversion	1.1-V LVSTL
LPDDR4B_DMA1	PIN_CF81	Bidir	Data mask/Data bus inversion	1.1-V LVSTL
LPDDR4B_DMB0	PIN_BU62	Bidir	Data mask/Data bus inversion	1.1-V LVSTL
LPDDR4B_DMB1	PIN_CA62	Bidir	Data mask/Data bus inversion	1.1-V LVSTL

4.3.2.2 MicroSD Card

The AXE5-Eagle board features a microSD card interface with x4 data lanes, primarily designed to function as an external storage solution for the HPS. The SD card can also be utilized for booting purposes, allowing for firmware execution directly from the card. Additionally, the SD card socket is equipped with a Card Detect pin, facilitating automatic detection of card insertion or removal, enhancing system responsiveness and user convenience.

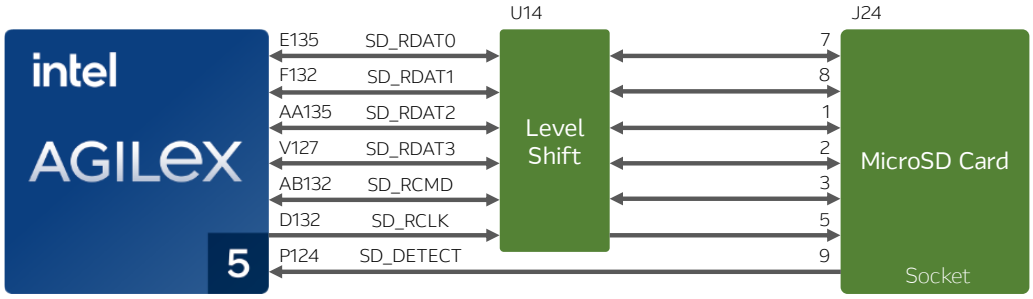

Figure 12 – MicroSD Card Socket Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
SD_RDAT0	PIN_E135	Bidir	Data line [0]	1.8-V LVCMOS
SD_RDAT1	PIN_F132	Bidir	Data line [1]	1.8-V LVCMOS
SD_RDAT2	PIN_AA135	Bidir	Data line [2]	1.8-V LVCMOS
SD_RDAT3	PIN_V127	Bidir	Data line [3]	1.8-V LVCMOS
SD_RCMD	PIN_AB132	Bidir	Command line	1.8-V LVCMOS
SD_RCLK	PIN_D132	Output	SD Clock	1.8-V LVCMOS
SD_DETECT	PIN_P124	Input	Card detect pin	1.8-V LVCMOS

4.3.3 Data Communication Interfaces

The AXE5-Eagle development board offers various data communication interfaces, including Ethernet, SFP+, USB 3.1, HDMI, and PCIe, ensuring high-level integration in an extensive range of applications. From high-speed data transfer with Ethernet and PCIe to multimedia capabilities with HDMI, this board provides adaptable solutions tailored to diverse requirements.

4.3.3.1 10/100/1000 Ethernet PHY

The development kit is equipped with two independent, standard RJ45-connected Gigabit Ethernet ports using an external Analog Devices ADIN1300 PHY chip and HPS Ethernet MAC function with integrated Time-Sensitive Networking support. The ADIN1300 chip is a low-power Ethernet transceiver with low latency primarily designed for industrial Ethernet applications.

The MAC-to-PHY interface is configured to an RGMII interface connections with MDIO interface as management.

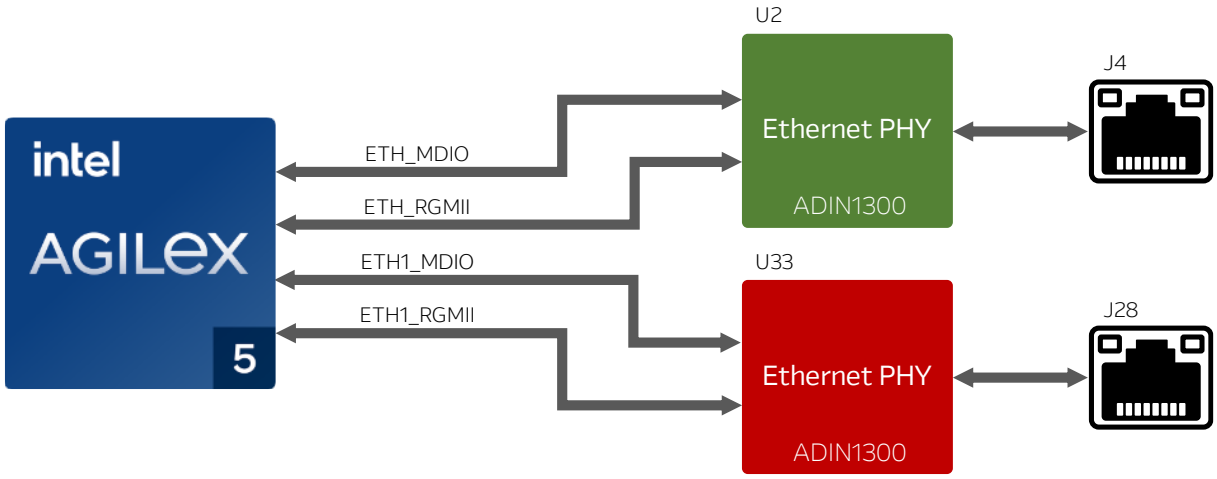

Figure 13 – Connection between the Agilex 5 and Ethernet PHYs

Ethernet PHY connected to the HPS

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
ETH_MDIO	PIN_T127	Bidir	Management Data	1.8-V LVCMOS
ETH_MDC	PIN_Y132	Output	Management Clock	1.8-V LVCMOS
ETH_TXCK	PIN_M127	Output	Transmit Clock	1.8-V LVCMOS
ETH_TXCTL	PIN_K127	Output	Transmit Control Signal	1.8-V LVCMOS
ETH_TXD0	PIN_K124	Output	Transmit data [0]	1.8-V LVCMOS
ETH_TXD1	PIN_Y127	Output	Transmit data [1]	1.8-V LVCMOS
ETH_TXD2	PIN_F127	Output	Transmit data [2]	1.8-V LVCMOS
ETH_TXD3	PIN_Y124	Output	Transmit data [3]	1.8-V LVCMOS
ETH_RXCK	PIN_M124	Input	Receive Clock	1.8-V LVCMOS
ETH_RXCTL	PIN_AB127	Input	Receive Control Signal	1.8-V LVCMOS
ETH_RXD0	PIN_H127	Input	Receive data [0]	1.8-V LVCMOS
ETH_RXD1	PIN_AB124	Input	Receive data [1]	1.8-V LVCMOS
ETH_RXD2	PIN_F124	Input	Receive data [2]	1.8-V LVCMOS
ETH_RXD3	PIN_D124	Input	Receive data [3]	1.8-V LVCMOS
ETH_RST	PIN_T124	Output	PHY Reset	1.8-V LVCMOS

Ethernet PHY connected to the FPGA Fabric

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
ETH1_MDIO	PIN_J1	Bidir	Management Data	1.8-V LVCMOS
ETH1_MDC	PIN_G1	Output	Management Clock	1.8-V LVCMOS
ETH1_TXCK	PIN_F24	Output	Transmit Clock	1.8-V LVCMOS
ETH1_TXCTL	PIN_F15	Output	Transmit Control Signal	1.8-V LVCMOS
ETH1_TXD0	PIN_H27	Output	Transmit data [0]	1.8-V LVCMOS
ETH1_TXD1	PIN_D24	Output	Transmit data [1]	1.8-V LVCMOS
ETH1_TXD2	PIN_H18	Output	Transmit data [2]	1.8-V LVCMOS
ETH1_TXD3	PIN_D15	Output	Transmit data [3]	1.8-V LVCMOS
ETH1_RXCK	PIN_F8	Input	Receive Clock	1.8-V LVCMOS
ETH1_RXCTL	PIN_F18	Input	Receive Control Signal	1.8-V LVCMOS
ETH1_RXD0	PIN_K8	Input	Receive data [0]	1.8-V LVCMOS
ETH1_RXD1	PIN_D8	Input	Receive data [1]	1.8-V LVCMOS
ETH1_RXD2	PIN_H8	Input	Receive data [2]	1.8-V LVCMOS
ETH1_RXD3	PIN_C2	Input	Receive data [3]	1.8-V LVCMOS
ETH1_RST	PIN_F27	Output	PHY Reset	1.8-V LVCMOS

4.3.3.2 SFP+ Interfaces

The development kit supports two independent SFP+ connectors that connect to the Intel Agilex 5's transceivers. Each port is capable of operation at a speed of up to 16 Gbps. These modules take in serial data from Agilex 5 device and transform them into optical signals. The board includes cage assemblies for the SFP+ connectors.

Figure 14 shows the connection diagram between SFP+ and Intel Agilex 5.

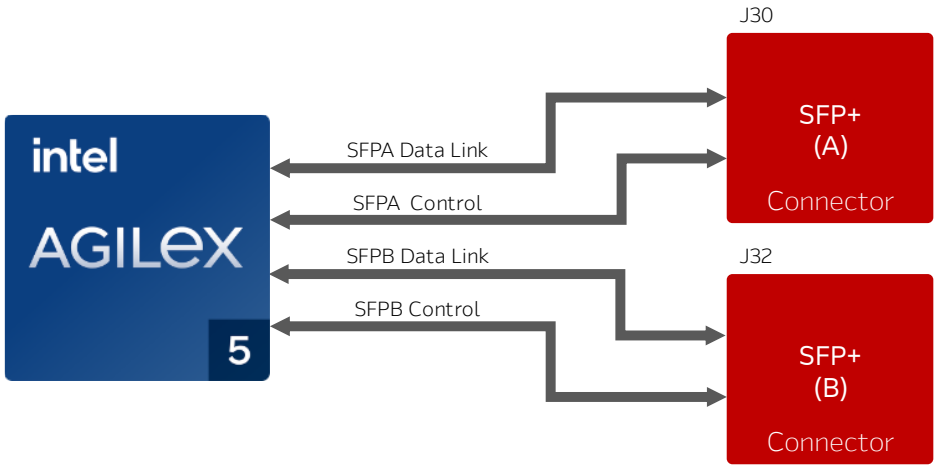

Figure 14 – SFP+ Connection

SFPA Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
SFPA_TD_P	PIN_AU129	Output	Transmitter data	High Speed Differential I/O
SFPA_TD_N	PIN_AU126			
SFPA_RD_P	PIN_AT135	Input	Receiver data	High Speed Differential I/O
SFPA_RD_N	PIN_AT133			
SFPA_TX_FAULT	PIN_Y74	Input	Transmitter fault	Adjustable**
SFPA_TX_DIS	PIN_Y77	Output	Transmitter output disable	Adjustable**
SFPA_MDEF0	PIN_A80	Input	Module definition signal	Adjustable**
SFPA_RS0	PIN_AC64	Output	Rate select 0	Adjustable**
SFPA_RS1	PIN_Y58	Output	Rate select 1	Adjustable**
SFPA_LOS	PIN_AG64	Input	Signal loss indicator	Adjustable**
SFPA_SDA / MUX_I2C_SDA	PIN_F4	Bidir	Serial Data Line	1.8-V LVCMOS
SFPA_SCL / MUX_I2C_SCL	PIN_D4	Bidir	Serial Clock Line	1.8-V LVCMOS

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on CRUVI_ADJ.*

SFPB Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
SFPB_TD_P	PIN_AL129	Output	Transmitter data	High Speed Differential I/O
SFPB_TD_N	PIN_AL126			
SFPB_RD_P	PIN_AK135	Input	Receiver data	High Speed Differential I/O
SFPB_RD_N	PIN_AK133			
SFPB_TX_FAULT	PIN_Y55	Input	Transmitter fault	Adjustable**
SFPB_TX_DIS	PIN_AC50	Output	Transmitter output disable	Adjustable**
SFPB_MDEF0	PIN_AG83	Input	Module definition signal	Adjustable**
SFPB_RS0	PIN_AG57	Output	Rate select 0	Adjustable**
SFPB_RS1	PIN_AC53	Output	Rate select 1	Adjustable**
SFPB_LOS	PIN_AC61	Input	Signal loss indicator	Adjustable**
SFPB_SDA / MUX_I2C_SDA	PIN_F4	Bidir	Serial Data Line	1.8-V LVCMOS
SFPB_SCL / MUX_I2C_SCL	PIN_D4	Bidir	Serial Clock Line	1.8-V LVCMOS

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on CRUVI_ADJ.*

For detailed information about the I²C connection, please refer to the I²C Structure section.

4.3.3.3 HDMI Transmitter

The development board provides High Performance HDMI Transmitter via the Analog Devices ADV7511 which incorporates HDMI v1.4 features, including 3D video support, and 225 MHz supports all video formats up to 1080p. The ADV7511 is controlled via a serial I²C bus interface, which is connected to the Agilex 5 SoC FPGA through the I2C MUX device. Additionally, the HDMI interface supports single-wire SPDIF (Sony/Philips Digital Interface Format) audio transmission up to 192 kHz sampling rate.

Detailed information on using ADV7511 HDMI Transmitter is available on the manufacturer's website.

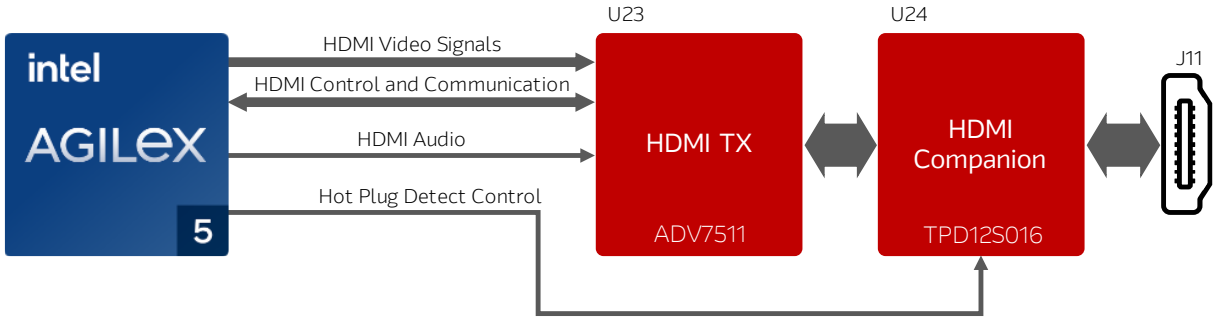

Figure 15 – HDMI Transmitter Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
HDMI_VS	PIN_BH19	Output	Vertical Synchronization	1.8-V LVCMOS
HDMI_HS	PIN_CF12	Output	Horizontal Synchronization	1.8-V LVCMOS
HDMI_CLK	PIN_BK31	Output	Video Pixel Clock	1.8-V LVCMOS
HDMI_DE	PIN_BK19	Output	Data Enable Signal for Digital Video	1.8-V LVCMOS
HDMI_D0	PIN_BF32	Output	Video Data bus [0]	1.8-V LVCMOS
HDMI_D1	PIN_CH12	Output	Video Data bus [1]	1.8-V LVCMOS
HDMI_D2	PIN_BM22	Output	Video Data bus [2]	1.8-V LVCMOS
HDMI_D3	PIN_BF21	Output	Video Data bus [3]	1.8-V LVCMOS
HDMI_D4	PIN_BE21	Output	Video Data bus [4]	1.8-V LVCMOS
HDMI_D5	PIN_BP22	Output	Video Data bus [5]	1.8-V LVCMOS
HDMI_D6	PIN_BR22	Output	Video Data bus [6]	1.8-V LVCMOS
HDMI_D7	PIN_BE25	Output	Video Data bus [7]	1.8-V LVCMOS
HDMI_D8	PIN_BU22	Output	Video Data bus [8]	1.8-V LVCMOS
HDMI_D9	PIN_BW28	Output	Video Data bus [9]	1.8-V LVCMOS
HDMI_D10	PIN_BU28	Output	Video Data bus [10]	1.8-V LVCMOS
HDMI_D11	PIN_BM31	Output	Video Data bus [11]	1.8-V LVCMOS
HDMI_D12	PIN_BR28	Output	Video Data bus [12]	1.8-V LVCMOS
HDMI_D13	PIN_BM28	Output	Video Data bus [13]	1.8-V LVCMOS
HDMI_D14	PIN_BK28	Output	Video Data bus [14]	1.8-V LVCMOS
HDMI_D15	PIN_BH28	Output	Video Data bus [15]	1.8-V LVCMOS
HDMI_D16	PIN_BF36	Output	Video Data bus [16]	1.8-V LVCMOS
HDMI_D17	PIN_BE43	Output	Video Data bus [17]	1.8-V LVCMOS
HDMI_D18	PIN_BU31	Output	Video Data bus [18]	1.8-V LVCMOS
HDMI_D19	PIN_BP31	Output	Video Data bus [19]	1.8-V LVCMOS
HDMI_D20	PIN_BR31	Output	Video Data bus [20]	1.8-V LVCMOS
HDMI_D21	PIN_BF29	Output	Video Data bus [21]	1.8-V LVCMOS
HDMI_D22	PIN_BF40	Output	Video Data bus [22]	1.8-V LVCMOS
HDMI_D23	PIN_BE29	Output	Video Data bus [23]	1.8-V LVCMOS
HDMI_INT	PIN_BF16	Input	Interrupt signal	1.8-V LVCMOS
HDMI_SPDIF	PIN_CF9	Output	SPDIF Audio signal	1.8-V LVCMOS
MUX_I2C_SDA	PIN_F4	Bidir	Serial Data Line	1.8-V LVCMOS
MUX_I2C_SCL	PIN_D4	Bidir	Serial Clock Line	1.8-V LVCMOS
CEC_CLK	PIN_BF25	Output	CEC Clock	1.8-V LVCMOS
CT_HPD	PIN_BW19	Output	Hot Plug Detect Control	1.8-V LVCMOS

For detailed information about the I²C connection, please refer to the I²C Structure section.

4.3.3.4 PCI Express Gen4

The AXE5-Eagle Development Kit provides PCIe-compliant multi-lane edge connectivity through the integrated transceivers and PCIe hard IP block of the Intel Agilex 5 SoC FPGA. Integration of the PCI Express hard IP block within the Agilex 5 device empowers users to deploy an efficient, high-speed protocol, all while optimizing logic resources for the logic application.

The PCI Express edge connector supports varying connection speeds:

- 2.5 Gbps/lane for a maximum of 10 Gbps full-duplex (Gen1);
- 5.0 Gbps/lane for a maximum of 20 Gbps full-duplex (Gen2);
- 8.0 Gbps/lane for a maximum of 32 Gbps full-duplex (Gen3);
- 16.0 Gbps/lane for a maximum of 64 Gbps full-duplex (Gen4);

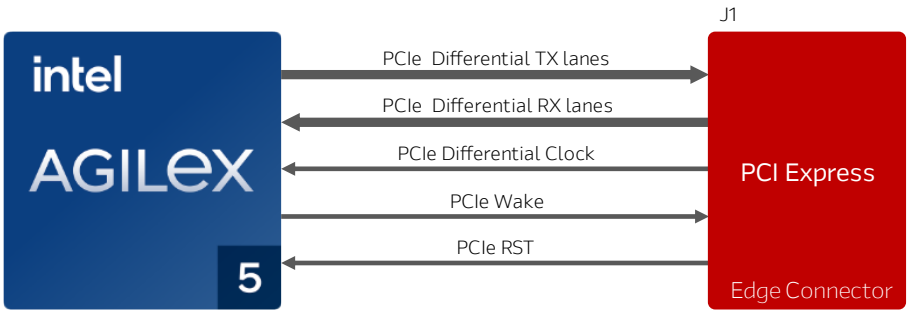

Figure 16 – PCIe Edge Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
PER0_P	PIN_BE129	Output	Transmit lane [0]	High Speed Differential I/O
PER0_N	PIN_BE126			
PER1_P	PIN_BC129	Output	Transmit lane [1]	High Speed Differential I/O
PER1_N	PIN_BC126			
PER2_P	PIN_BA129	Output	Transmit lane [2]	High Speed Differential I/O
PER2_N	PIN_BA126			
PER3_P	PIN_AW129	Output	Transmit lane [3]	High Speed Differential I/O
PER3_N	PIN_AW126			
PET0_P	PIN_BD135	Input	Receive lane [0]	High Speed Differential I/O
PET0_N	PIN_BD133			
PET1_P	PIN_BB135	Input	Receive lane [1]	High Speed Differential I/O
PET1_N	PIN_BB133			
PET2_P*	PIN_AY135	Input	Receive lane [2]	High Speed Differential I/O
PET2_N*	PIN_AY133			
PET3_P	PIN_AV135	Input	Receive lane [3]	High Speed Differential I/O
PET3_N	PIN_AV133			
PCIE_CLK_P	PIN_AV120	Input	100 MHz PCIe reference clock	CML
PCIE_CLK_N	PIN_AV115			
PCIE_RSTb	PIN_CF132	Input	Reset	3.3-V LVCMOS
PCIE_R_WAKE	PIN_D34	Output	Wake signal	3.3-V LVCMOS

** P and N are reversed in the Schematics, but Quartus wants to see them this way. The PCIe IP can handle the polarity reversal*

4.3.3.5 USB 3.1 Gen1

The AXE5-Eagle board features a Microchip's USB5734 USB Hub that offers a total of four USB-A connectivity options. This USB Hub is fully compliant with the USB 3.1 Gen1 specification and supports High Speed, Full Speed and Low-Speed USB signalling. This hub enables parallel operation of both USB 2.0 and SuperSpeed data transfer, ensuring optimal performance for a wide range of devices.

The USB 2.0 controller within the HPS is interfaced with a USB PHY via ULPI, establishing a connection to the upstream port of the USB Hub. Simultaneously, the communication on the high-speed data lines of the USB 3.1 Gen1 is ensured by the FPGA transceivers.

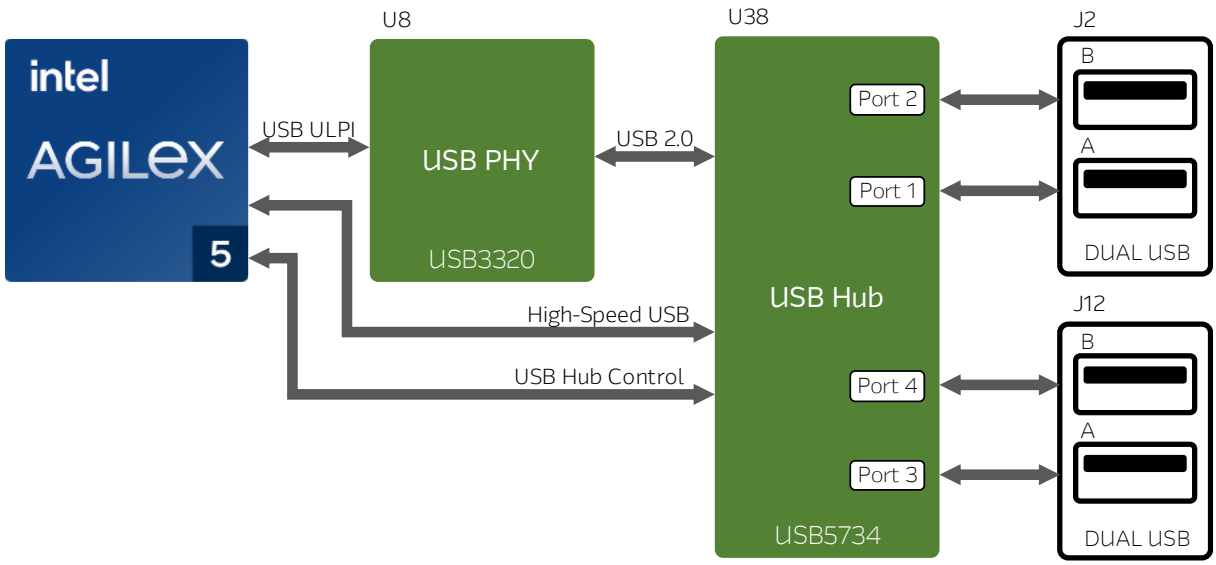

Figure 17 – USB Connection of Agilex 5 SoC FPGA

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
USB_CLK	PIN_P132	Bidir	ULPI Clock	1.8-V LVCMOS
USB_STP	PIN_L135	Output	ULPI STP signal	1.8-V LVCMOS
USB_DIR	PIN_J135	Input	Direction of ULPI	1.8-V LVCMOS
USB_NXT	PIN_AD134	Input	ULPI NXT signal	1.8-V LVCMOS
USB_DATA0	PIN_AD135	Bidir	ULPI data bus [0]	1.8-V LVCMOS
USB_DATA1	PIN_M132	Bidir	ULPI data bus [1]	1.8-V LVCMOS
USB_DATA2	PIN_K132	Bidir	ULPI data bus [2]	1.8-V LVCMOS
USB_DATA3	PIN_AG129	Bidir	ULPI data bus [3]	1.8-V LVCMOS
USB_DATA4	PIN_J134	Bidir	ULPI data bus [4]	1.8-V LVCMOS
USB_DATA5	PIN_AG120	Bidir	ULPI data bus [5]	1.8-V LVCMOS
USB_DATA6	PIN_G134	Bidir	ULPI data bus [6]	1.8-V LVCMOS
USB_DATA7	PIN_G135	Bidir	ULPI data bus [7]	1.8-V LVCMOS

Continued on the next page

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
USB_RST	PIN_B134	Output	USB PHY Reset	1.8-V LVCMOS
USB_SSTX_P	PIN_AN129	Output	USB 3.1 Gen 1 SuperSpeed transmit data	High Speed Differential I/O
USB_SSTX_N	PIN_AN126			
USB_SSRX_P	PIN_AM135	Input	USB 3.1 Gen 1 SuperSpeed receive data	High Speed Differential I/O
USB_SSRX_N	PIN_AM133			
USBH_CFG0	PIN_A35	Output	I²C Slave 0 Configuration Strap	3.3-V LVCMOS
USBH_CFG1	PIN_A33	Output	I²C Slave 1 Configuration Strap	3.3-V LVCMOS
USB_HUB_SMDAT	PIN_B23	Bidir	SMBus/I²C data	3.3-V LVCMOS
USB_HUB_SMCLK	PIN_B26	Bidir	SMBus/I²C clock	3.3-V LVCMOS
USB_HUB_RST	PIN_BU118	Output	USB Hub reset	3.3-V LVCMOS

4.3.3.6 USB to UART Bridge

Besides the USB 3.1 Gen1 interfaces, the AXE5-Eagle board uses an additional FT234XD chip to perform UART communication over USB. The FTDI chip converts signals from USB 2.0 to a standard serial interface, which is routed to the HPS UART0 module.

The USB to UART Bridge communicates over the micro-USB connector labelled as J5.

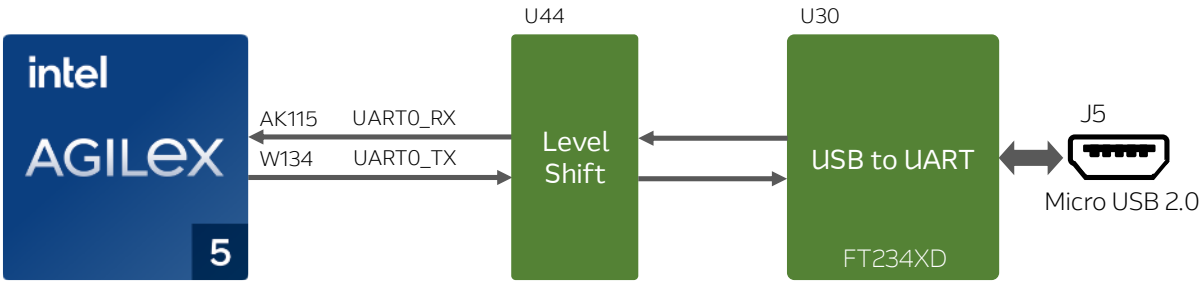

Figure 18 – FTDI Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
UART0_RX	PIN_AK115	Input	Receiving Asynchronous Data Input	1.8-V LVCMOS
UART0_TX	PIN_W134	Output	Transmit Asynchronous Data Output	1.8-V LVCMOS

4.3.4 Expansion Connectors

The AXE5-Eagle development kit features expansion options with support for various mezzanine cards, including FMC+, CRUVI HS, and CRUVI LS connectors. This flexibility allows users to easily integrate additional peripherals, functionalities, and customize the development environment to their specific needs.

4.3.4.1 FPGA Mezzanine Card Plus Interface (FMC+)

The AXE5-Eagle development board supports the latest standard VITA 57.4 FMC+ specification. It features a subset implementation of the high pin count at the J3 High Serial Pin Connector (HSPC), specifically designed to expand FPGA I/Os capabilities.

The 560-pin FMC+ connector provides connectivity for:

- 68 single-ended or 34 differential user-defined signals
- 8 transceivers differential pairs with 17.16 Gbps data date (8 TX and 8 RX)
- 2 transceivers differential clocks
- 2 differential Mezzanine to Carrier clocks
- 1 differential reference clock (1 Mezzanine to Carrier and 1 Carrier to Mezzanine)
- 1 differential sync clock (1 Mezzanine to Carrier and 1 Carrier to Mezzanine)

The AXE5-Eagle board provides 12 V, 3.3 V and FMC_ADJ power through FMC+ port. The power control of the VADJ_FMC power rail is managed by the U46 DCDC regulator. This rail powers the VADJ pins of J3 connector, as well as the 2B I/O Bank of Agilex 5 SoC FPGA. The FPGA I/O standards of the FMC+ ports can be adjusted by configuring a switch position. The valid values of the VADJ_FMC rail is 1.2 V or 1.3 V which can be adjusted via the S10 DIP switch on the AXE5-Eagle board. For detailed setting, please refer to Switch Settings section.

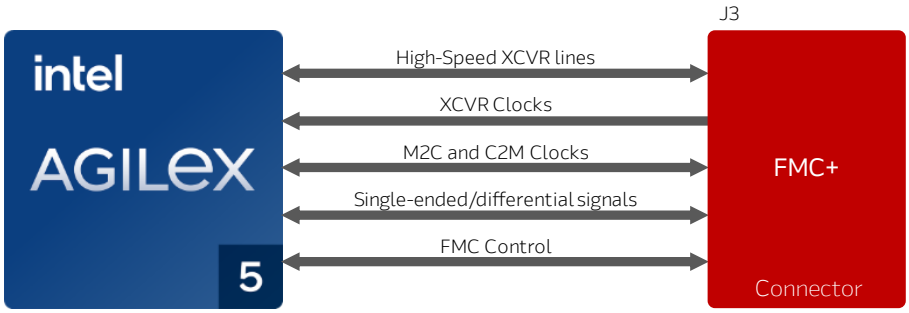

Figure 19 – FMC+ Connection on AXE5-Eagle Board

FMC+ Clock Interface

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
FMC_GBTCLK0_P	PIN_AV16	D4	Input	Mezzanine to Carrier seria clock	CML
FMC_GBTCLK0_N	PIN_AV21	D5			
FMC_GBTCLK1_P	PIN_AP16	B20	Input	Mezzanine to Carrier serial clock	CML
FMC_GBTCLK1_N	PIN_AP21	B21			
FMC_CLK0_M2C_P	PIN_BK38	H4	Input	Mezzanine to Carrier FPGA fabric clock	Adjustable*
FMC_CLK0_M2C_N	PIN_BM38	H5			
FMC_CLK1_M2C_P	PIN_BF68	G2	Input	Mezzanine to Carrier FPGA fabric clock	Adjustable*
FMC_CLK1_M2C_N	PIN_BE68	G3			
FMC_REFCK_C2M_P	PIN_BE61	L20	Output	Carrier to Mezzanine reference clock	Adjustable*
FMC_REFCK_C2M_N	PIN_BE57	L21			
FMC_SYNC_C2M_P	PIN_CH41	L16	Output	Carrier to Mezzanine sync clock	Adjustable*
FMC_SYNC_C2M_N	PIN_CF41	L17			
FMC_REFCK_M2C_P	PIN_CH38	L24	Input	Mezzanine to Carrier reference clock	Adjustable*
FMC_REFCK_M2C_N	PIN_CF38	L25			
FMC_SYNC_M2C_P	PIN_BH49	L28	Input	Mezzanine to Carrier sync clock	Adjustable*
FMC_SYNC_M2C_N	PIN_BH52	L29			

** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on FMC_ADJ setting.*

FMC+ XCVR Channels

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
DP0_C2M_P	PIN_BE7	C2	Output	Carrier to Mezzanine transmit data pair[0]	High Speed Differential I/O
DP0_C2M_N	PIN_BE10	C3			
DP1_C2M_P	PIN_BC7	A22	Output	Carrier to Mezzanine transmit data pair[1]	High Speed Differential I/O
DP1_C2M_N	PIN_BC10	A23			
DP2_C2M_P	PIN_BA7	A26	Output	Carrier to Mezzanine transmit data pair[2]	High Speed Differential I/O
DP2_C2M_N	PIN_BA10	A27			
DP3_C2M_P	PIN_AW7	A30	Output	Carrier to Mezzanine transmit data pair[3]	High Speed Differential I/O
DP3_C2M_N	PIN_AW10	A31			
DP4_C2M_P	PIN_AU7	A34	Output	Carrier to Mezzanine transmit data pair[4]	High Speed Differential I/O
DP4_C2M_N	PIN_AU10	A35			
DP5_C2M_P	PIN_AR7	A38	Output	Carrier to Mezzanine transmit data pair[5]	High Speed Differential I/O
DP5_C2M_N	PIN_AR10	A39			
DP6_C2M_P	PIN_AN7	B36	Output	Carrier to Mezzanine transmit data pair[6]	High Speed Differential I/O
DP6_C2M_N	PIN_AN10	B37			
DP7_C2M_P	PIN_AL7	B32	Output	Carrier to Mezzanine transmit data pair[7]	High Speed Differential I/O
DP7_C2M_N	PIN_AL10	B33			
DP0_M2C_P	PIN_BF1	C6	Input	Mezzanine to Carrier receiver data pair[0]	High Speed Differential I/O
DP0_M2C_N	PIN_BF3	C7			
DP1_M2C_P	PIN_BD1	A2	Input	Mezzanine to Carrier receiver data pair[1]	High Speed Differential I/O
DP1_M2C_N	PIN_BD3	A3			
DP2_M2C_P	PIN_BB1	A6	Input	Mezzanine to Carrier receiver data pair[2]	High Speed Differential I/O
DP2_M2C_N	PIN_BB3	A7			
DP3_M2C_P	PIN_AY1	A10	Input	Mezzanine to Carrier receiver data pair[3]	High Speed Differential I/O
DP3_M2C_N	PIN_AY3	A11			
DP4_M2C_P	PIN_AV1	A14	Input	Mezzanine to Carrier receiver data pair[4]	High Speed Differential I/O
DP4_M2C_N	PIN_AV3	A15			
DP5_M2C_P	PIN_AT1	A18	Input	Mezzanine to Carrier receiver data pair[5]	High Speed Differential I/O
DP5_M2C_N	PIN_AT3	A19			
DP6_M2C_P	PIN_AP1	B16	Input	Mezzanine to Carrier receiver data pair[6]	High Speed Differential I/O
DP6_M2C_N	PIN_AP3	B17			
DP7_M2C_P	PIN_AM1	B12	Input	Mezzanine to Carrier receiver data pair[7]	High Speed Differential I/O
DP7_M2C_N	PIN_AM3	B13			

FMC+ Single-ended/differential signals

Mixing differential and single-ended signals on LA00 through LA33 must follow the restrictions in table 19 of the Agilex 5 General-Purpose I/O User Guide.

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
LA00_P	PIN_CF19	G6	Bidir	FMC+ LA bank data[0]_p	Adjustable*
LA00_N	PIN_CC19	G7	Bidir	FMC+ LA bank data[0]_n	Adjustable*
LA01_P	PIN_CF22	D8	Bidir	FMC+ LA bank data[1]_p	Adjustable*
LA01_N	PIN_CH22	D9	Bidir	FMC+ LA bank data[1]_n	Adjustable*
LA02_P	PIN_CC22	H7	Bidir	FMC+ LA bank data[2]_p	Adjustable
LA02_N	PIN_CA22	H8	Bidir	FMC+ LA bank data[2]_n	Adjustable*
LA03_P	PIN_CF28	G9	Bidir	FMC+ LA bank data[3]_p	Adjustable*
LA03_N	PIN_CC28	G10	Bidir	FMC+ LA bank data[3]_n	Adjustable*
LA04_P	PIN_CA31	H10	Bidir	FMC+ LA bank data[4]_p	Adjustable*
LA04_N	PIN_CC31	H11	Bidir	FMC+ LA bank data[4]_n	Adjustable*
LA05_P	PIN_CH31	D11	Bidir	FMC+ LA bank data[5]_p	Adjustable*
LA05_N	PIN_CF31	D12	Bidir	FMC+ LA bank data[5]_n	Adjustable*
LA06_P	PIN_CK8	C10	Bidir	FMC+ LA bank data[6]_p	Adjustable*
LA06_N	PIN_CL6	C11	Bidir	FMC+ LA bank data[6]_n	Adjustable*
LA07_P	PIN_CK11	H13	Bidir	FMC+ LA bank data[7]_p	Adjustable*
LA07_N	PIN_CL8	H14	Bidir	FMC+ LA bank data[7]_n	Adjustable*
LA08_P	PIN_CL14	G12	Bidir	FMC+ LA bank data[8]_p	Adjustable*
LA08_N	PIN_CL11	G13	Bidir	FMC+ LA bank data[8]_n	Adjustable*
LA09_P	PIN_CK17	D14	Bidir	FMC+ LA bank data[9]_p	Adjustable*
LA09_N	PIN_CL17	D15	Bidir	FMC+ LA bank data[9]_n	Adjustable*
LA10_P	PIN_CL20	C14	Bidir	FMC+ LA bank data[10]_p	Adjustable*
LA10_N	PIN_CK20	C15	Bidir	FMC+ LA bank data[10]_n	Adjustable*
LA11_P	PIN_CL23	H16	Bidir	FMC+ LA bank data[11]_p	Adjustable*
LA11_N	PIN_CK26	H17	Bidir	FMC+ LA bank data[11]_n	Adjustable*
LA12_P	PIN_BH38	G15	Bidir	FMC+ LA bank data[12]_p	Adjustable*
LA12_N	PIN_BH41	G16	Bidir	FMC+ LA bank data[12]_n	Adjustable*
LA13_P	PIN_BF57	D17	Bidir	FMC+ LA bank data[13]_p	Adjustable*
LA13_N	PIN_BF53	D18	Bidir	FMC+ LA bank data[13]_n	Adjustable*
LA14_P	PIN_BE46	C18	Bidir	FMC+ LA bank data[14]_p	Adjustable*
LA14_N	PIN_BF46	C19	Bidir	FMC+ LA bank data[14]_n	Adjustable*
LA15_P	PIN_BE64	H19	Bidir	FMC+ LA bank data[15]_p	Adjustable*
LA15_N	PIN_BF64	H20	Bidir	FMC+ LA bank data[15]_n	Adjustable*
LA16_P	PIN_BF50	G18	Bidir	FMC+ LA bank data[16]_p	Adjustable*
LA16_N	PIN_BE50	G19	Bidir	FMC+ LA bank data[16]_n	Adjustable*
LA17_P	PIN_BR41	D20	Bidir	FMC+ LA bank data[17]_p	Adjustable*
LA17_N	PIN_BU41	D21	Bidir	FMC+ LA bank data[17]_n	Adjustable*
LA18_P	PIN_BK49	C22	Bidir	FMC+ LA bank data[18]_p	Adjustable*
LA18_N	PIN_BM49	C23	Bidir	FMC+ LA bank data[18]_n	Adjustable*
LA19_P	PIN_CK73	H22	Bidir	FMC+ LA bank data[19]_p	Adjustable*
LA19_N	PIN_CL73	H23	Bidir	FMC+ LA bank data[19]_n	Adjustable*

Continued on the next page

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
LA20_P	PIN_CA38	G21	Bidir	FMC+ LA bank data[20]_p	Adjustable*
LA20_N	PIN_BW38	G22	Bidir	FMC+ LA bank data[20]_n	Adjustable*
LA21_P	PIN_BR38	H25	Bidir	FMC+ LA bank data[21]_p	Adjustable*
LA21_N	PIN_BU38	H26	Bidir	FMC+ LA bank data[21]_n	Adjustable*
LA22_P	PIN_CF49	G24	Bidir	FMC+ LA bank data[22]_p	Adjustable*
LA22_N	PIN_CH49	G25	Bidir	FMC+ LA bank data[22]_n	Adjustable*
LA23_P	PIN_BW49	D23	Bidir	FMC+ LA bank data[23]_p	Adjustable*
LA23_N	PIN_CA49	D24	Bidir	FMC+ LA bank data[23]_n	Adjustable*
LA24_P	PIN_CF52	H28	Bidir	FMC+ LA bank data[24]_p	Adjustable*
LA24_N	PIN_CH52	H29	Bidir	FMC+ LA bank data[24]_n	Adjustable*
LA25_P	PIN_CL51	G27	Bidir	FMC+ LA bank data[25]_p	Adjustable*
LA25_N	PIN_CK54	G28	Bidir	FMC+ LA bank data[25]_n	Adjustable*
LA26_P	PIN_BM52	D26	Bidir	FMC+ LA bank data[26]_p	Adjustable*
LA26_N	PIN_BP52	D27	Bidir	FMC+ LA bank data[26]_n	Adjustable*
LA27_P	PIN_CC52	C26	Bidir	FMC+ LA bank data[27]_p	Adjustable*
LA27_N	PIN_CA52	C27	Bidir	FMC+ LA bank data[27]_n	Adjustable*
LA28_P	PIN_BP41	H31	Bidir	FMC+ LA bank data[28]_p	Adjustable*
LA28_N	PIN_BM41	H32	Bidir	FMC+ LA bank data[28]_n	Adjustable*
LA29_P	PIN_CK33	G30	Bidir	FMC+ LA bank data[29]_p	Adjustable*
LA29_N	PIN_CL30	G31	Bidir	FMC+ LA bank data[29]_n	Adjustable*
LA30_P	PIN_CK35	H34	Bidir	FMC+ LA bank data[30]_p	Adjustable*
LA30_N	PIN_CL35	H35	Bidir	FMC+ LA bank data[30]_n	Adjustable*
LA31_P	PIN_CK39	G33	Bidir	FMC+ LA bank data[31]_p	Adjustable*
LA31_N	PIN_CL39	G34	Bidir	FMC+ LA bank data[31]_n	Adjustable*
LA32_P	PIN_CK48	H37	Bidir	FMC+ LA bank data[32]_p	Adjustable*
LA32_N	PIN_CL45	H38	Bidir	FMC+ LA bank data[32]_n	Adjustable*
LA33_P	PIN_CL42	G36	Bidir	FMC+ LA bank data[33]_p	Adjustable*
LA33_N	PIN_CK45	G37	Bidir	FMC+ LA bank data[33]_n	Adjustable*

** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on FMC_ADJ setting.*

FMC+ Control and Management

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
MUX_I2C_SDA	PIN_F4	C31	Bidir	Serial Data Line	1.8-V LVCMOS
MUX_I2C_SCL	PIN_D4	C30	Bidir	Serial Clock Line	1.8-V LVCMOS
FMC_PRSNT	PIN_B39	H2	Input	FMC card presence indicator	3.3-V LVCMOS
PG_GROUP3	-	D1	-	Power Good from Carrier to Mezzanine	3.3-V LVCMOS

For detailed information about the I²C connection, please refer to the I²C Structure section.

4.3.4.2 CRUVI High-Speed Connectors

The AXE5-Eagle board features two CRUVI HS connectors. CRUVI is an open ecosystem, low-pin-count interface solution that enables the integration of a wide range of peripherals into the system, accommodating both high-speed signalling and support for low-speed device interfaces at the same time. CRUVI HS allows the connection of high-speed interfaces such as Gigabit Ethernet, camera, and other types of multimedia peripherals.

The AXE5-Eagle board provides 5.0 V, 3.3 V and VIO_CRUVI power through CRUVI HS port. The power control of the VIO_CRUVI power rail is managed by the U50 DCDC regulator. This rail powers the VADJ pins of J19 and J21 connectors, as well as the 3B I/O Bank of Agilex 5 SoC FPGA. The FPGA I/O standards of the CRUVI HS ports can be adjusted by configuring a switch position. The valid values of the VIO_CRUVI rail is 1.2 V or 1.3 V which can be adjusted via the S7 DIP switch on the AXE5-Eagle board. For detailed setting, please refer to Switch Settings section.

For custom add-on cards with CRUVI HS interface, the recommended counterpart for the connector is **ST4-30-1.50-L-D-P** from Samtec.

For hardware module mounting, use M2x6mm pan head Philips drive screw.

Below is the connection diagram and pinning information.

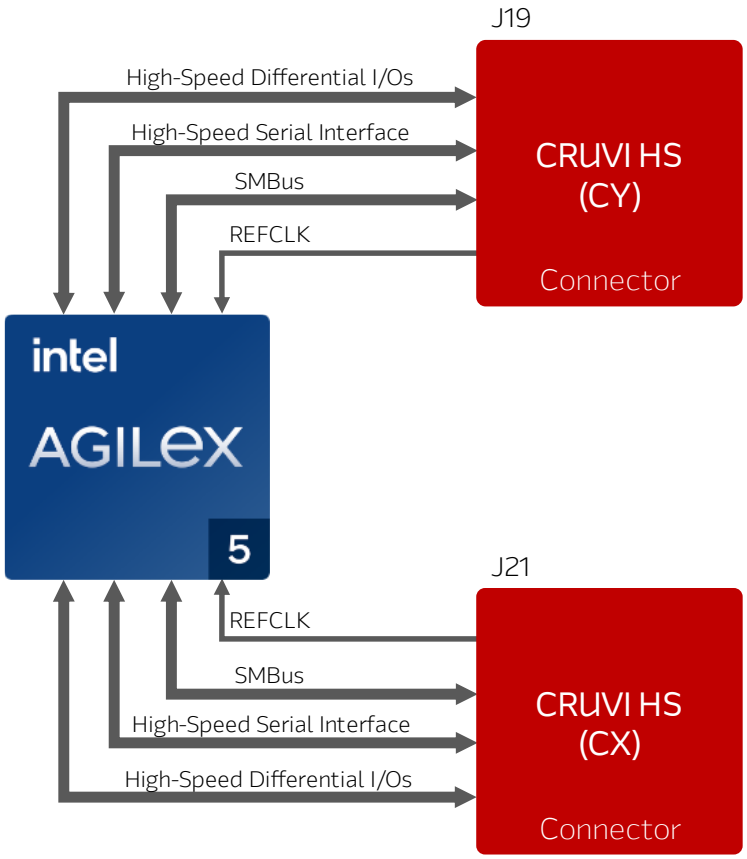

Figure 20 – CRUVI HS Connections

CRUVI HS CY Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CY_A0_P	PIN_T65	14	Bidir	HS Differential Data A[0]_p	Adjustable**
CY_A0_N	PIN_P65	16	Bidir	HS Differential Data A[0]_n	Adjustable**
CY_A1_P	PIN_P74	20	Bidir	HS Differential Data A[1]_p	Adjustable**
CY_A1_N	PIN_T74	22	Bidir	HS Differential Data A[1]_n	Adjustable**
CY_A2_P	PIN_M65	26	Bidir	HS Differential Data A[2]_p	Adjustable**
CY_A2_N	PIN_K65	28	Bidir	HS Differential Data A[2]_n	Adjustable**
CY_A3_P	PIN_V67	32	Bidir	HS Differential Data A[3]_p	Adjustable**
CY_A3_N	PIN_T67	34	Bidir	HS Differential Data A[3]_n	Adjustable**
CY_A4_P	PIN_M67	38	Bidir	HS Differential Data A[4]_p	Adjustable**
CY_A4_N	PIN_K67	40	Bidir	HS Differential Data A[4]_n	Adjustable**
CY_A5_P	PIN_F65	44	Bidir	HS Differential Data A[5]_p	Adjustable**
CY_A5_N	PIN_D65	46	Bidir	HS Differential Data A[5]_n	Adjustable**
CY_B0_P	PIN_M74	15	Bidir	HS Differential Data B[0]_p	Adjustable**
CY_B0_N	PIN_K74	17	Bidir	HS Differential Data B[0]_n	Adjustable**
CY_B1_P	PIN_V77	21	Bidir	HS Differential Data B[1]_p	Adjustable**
CY_B1_N	PIN_T77	23	Bidir	HS Differential Data B[1]_n	Adjustable**
CY_B2_P	PIN_D74	27	Bidir	HS Differential Data B[2]_p	Adjustable**
CY_B2_N	PIN_F74	29	Bidir	HS Differential Data B[2]_n	Adjustable**
CY_B3_P	PIN_K77	33	Bidir	HS Differential Data B[3]_p	Adjustable**
CY_B3_N	PIN_M77	35	Bidir	HS Differential Data B[3]_n	Adjustable**
CY_B4_P	PIN_F77	39	Bidir	HS Differential Data B[4]_p	Adjustable**
CY_B4_N	PIN_H77	41	Bidir	HS Differential Data B[4]_n	Adjustable**
CY_B5_P	PIN_H67	45	Bidir	HS Differential Data B[5]_p	Adjustable**
CY_B5_N	PIN_F67	47	Bidir	HS Differential Data B[5]_n	Adjustable**
CY_HSI	PIN_B56	10	Input	HS Serial In	Adjustable**
CY_HSIO	PIN_A70	2	Bidir	HS Serial Data I/O	Adjustable**
CY_HSO	PIN_B70	6	Output	HS Serial Out	Adjustable**
CY_RESET	PIN_A60	8	Output	Serial Reset	Adjustable**
CY_SMB_ALERT	PIN_CG134	3	Input	SMBus interrupt signal	3.3-V LVCMOS
CY_SMB_SDA	PIN_CD135	5	Bidir	SMBus Data Line	3.3-V LVCMOS
CY_SMB_SCL	PIN_CD134	7	Bidir	SMBus Data Clock Line	3.3-V LVCMOS
CY_REFCLK	PIN_CH128	11	Input	Clock Input	3.3-V LVCMOS
5V	-	60	PWR	5V power to the connector	-
3.3V	-	4, 9	PWR	3.3V power to the connector	-
VIO_CRUVI	-	36	PWR	HS IO Bank voltage	-

Continued on the next page

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
GND	-	12, 13, 18, 19, 24, 25, 30, 31, 37, 42, 43, 48, 49, 54	PWR	Ground to the connector	-
n.c.	-	1, 50, 51, 52, 53, 55, 56, 57, 58, 59	-	Not connected	-

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on CRUVI_ADJ*

CRUVI HS CX Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CX_A0_P	PIN_D44	14	Bidir	HS Differential Data A[0]_p	Adjustable**
CX_A0_N	PIN_F44	16	Bidir	HS Differential Data A[0]_n	Adjustable**
CX_A1_P	PIN_H58	20	Bidir	HS Differential Data A[1]_p	Adjustable**
CX_A1_N	PIN_F58	22	Bidir	HS Differential Data A[1]_n	Adjustable**
CX_A2_P	PIN_F47	26	Bidir	HS Differential Data A[2]_p	Adjustable**
CX_A2_N	PIN_H47	28	Bidir	HS Differential Data A[2]_n	Adjustable**
CX_A3_P	PIN_M47	32	Bidir	HS Differential Data A[3]_p	Adjustable**
CX_A3_N	PIN_K47	34	Bidir	HS Differential Data A[3]_n	Adjustable**
CX_A4_P	PIN_V47	38	Bidir	HS Differential Data A[4]_p	Adjustable**
CX_A4_N	PIN_T48	40	Bidir	HS Differential Data A[4]_n	Adjustable**
CX_A5_P	PIN_K44	44	Bidir	HS Differential Data A[5]_p	Adjustable**
CX_A5_N	PIN_M44	46	Bidir	HS Differential Data A[5]_n	Adjustable**
CX_B0_P	PIN_F55	15	Bidir	HS Differential Data B[0]_p	Adjustable**
CX_B0_N	PIN_D55	17	Bidir	HS Differential Data B[0]_n	Adjustable**
CX_B1_P	PIN_M58	21	Bidir	HS Differential Data B[1]_p	Adjustable**
CX_B1_N	PIN_K58	23	Bidir	HS Differential Data B[1]_n	Adjustable**
CX_B2_P	PIN_K55	27	Bidir	HS Differential Data B[2]_p	Adjustable**
CX_B2_N	PIN_M55	29	Bidir	HS Differential Data B[2]_n	Adjustable**
CX_B3_P	PIN_P55	33	Bidir	HS Differential Data B[3]_p	Adjustable**
CX_B3_N	PIN_T55	35	Bidir	HS Differential Data B[3]_n	Adjustable**
CX_B4_P	PIN_V58	39	Bidir	HS Differential Data B[4]_p	Adjustable**
CX_B4_N	PIN_T58	41	Bidir	HS Differential Data B[4]_n	Adjustable**
CX_B5_P	PIN_P44	45	Bidir	HS Differential Data B[5]_p	Adjustable**
CX_B5_N	PIN_T44	47	Bidir	HS Differential Data B[5]_n	Adjustable**
CX_HSI	PIN_A63	10	Input	HS Serial In	Adjustable**
CX_HSIO	PIN_B45	2	Bidir	HS Serial Data I/O	Adjustable**
CX_HSO	PIN_A48	6	Output	HS Serial Out	Adjustable**
CX_RESET	PIN_A51	8	Output	Serial Reset	Adjustable**

Continued on the next page

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CX_SMB_ALERT	PIN_BR112	3	Input	SMBus interrupt signal	3.3-V LVCMOS
CX_SMB_SDA	PIN_BU109	5	Bidir	SMBus Data Line	3.3-V LVCMOS
CX_SMB_SCL	PIN_BR109	7	Bidir	SMBus Data Clock Line	3.3-V LVCMOS
CX_REFCLK	PIN_BM109	11	Input	Clock Input	3.3-V LVCMOS
5V	-	60	PWR	5V power to the connector	-
3.3V	-	4, 9	PWR	3.3V power to the connector	-
VIO_CRUVI	-	36	PWR	HS IO Bank voltage	-
GND	-	12, 13, 18, 19, 24, 25, 30, 31, 37, 42, 43, 48, 49, 54	PWR	Ground to the connector	-
n.c.	-	1, 50, 51, 52, 53, 55, 56, 57, 58, 59	-	Not connected	-

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on CRUVI_ADJ*

4.3.4.3 CRUVI Low-Speed Connectors

CRUVI LS is the low-speed version of the CRUVI ecosystem that provides a connection surface for the simple peripheral modules. It features a simple layout with standard pins for power, ground, and several digital I/O signals. It offers an array of ready-to-use modules for easy prototyping and extends functional capabilities. This compact interface simplifies the connection of sensors, communication devices, and other components.

Delivering power to the mezzanine board, the AXE5-Eagle board offers both 5.0 V and 3.3 V via the CRUVI LS port.

The AXE5-Eagle development board provides two CRUVI LS connection interfaces.

For custom add-on cards with CRUVI LS interface, the recommended counterpart for the connector is **TMMH-106-04-F-DV-A-M** from Samtec.

For hardware module mounting, use M2x6mm pan head Philips drive screw.

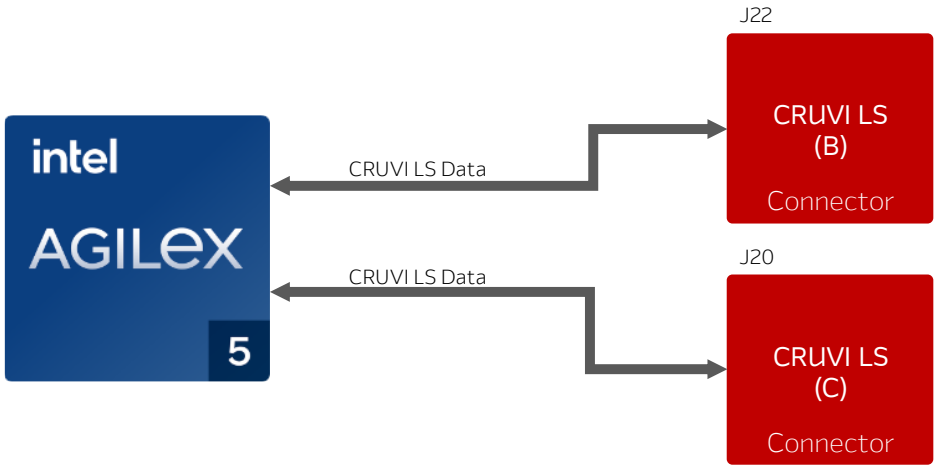

Figure 21 – CRUVI LS Connections

CRUVI LS B Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
B0	PIN_BE115	3	Bidir	CRUVI LS Data [0]	3.3-V LVCMOS
B1	PIN_BF111	5	Bidir	CRUVI LS Data [1]	3.3-V LVCMOS
B2	PIN_BF107	7	Bidir	CRUVI LS Data [2]	3.3-V LVCMOS
B3	PIN_BE107	9	Bidir	CRUVI LS Data [3]	3.3-V LVCMOS
B4	PIN_BF120	4	Bidir	CRUVI LS Data [4]	3.3-V LVCMOS
B5	PIN_BE111	8	Bidir	CRUVI LS Data [5]	3.3-V LVCMOS
B6	PIN_BF115	1	Bidir	CRUVI LS Data [6]	3.3-V LVCMOS
B7	PIN_BH118	2	Bidir	CRUVI LS Data [7]	3.3-V LVCMOS
5.0V	-	12	PWR	5V power to the connector	-
3.3V	-	10	PWR	3.3V power to the connector	-
GND	-	8	PWR	Ground to the connector	-
n.c.	-	11	-	Not connected	-

CRUVI LS C Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
C0	PIN_BK109	3	Bidir	CRUVI LS Data [0]	3.3-V LVCMOS
C1	PIN_BF104	5	Bidir	CRUVI LS Data [1]	3.3-V LVCMOS
C2	PIN_BM118	7	Bidir	CRUVI LS Data [2]	3.3-V LVCMOS
C3	PIN_BK118	9	Bidir	CRUVI LS Data [3]	3.3-V LVCMOS
C4	PIN_BP112	4	Bidir	CRUVI LS Data [4]	3.3-V LVCMOS
C5	PIN_BH109	8	Bidir	CRUVI LS Data [5]	3.3-V LVCMOS
C6	PIN_BM112	1	Bidir	CRUVI LS Data [6]	3.3-V LVCMOS
C7	PIN_BK112	2	Bidir	CRUVI LS Data [7]	3.3-V LVCMOS
5.0V	-	12	PWR	5V power to the connector	-
3.3V	-	10	PWR	3.3V power to the connector	-
GND	-	8	PWR	Ground to the connector	-
n.c.	-	11	-	Not connected	-

4.3.4.4 MIPI D-PHY

MIPI interface is a high-speed serial interface standard designed for efficient data transfer between components like cameras, displays, and sensors. The Intel Agilex 5 FPGA and SoCs support native MIPI IP D-PHY. The MIPI D-PHY implements MIPI transmit and receive interfaces, enabling the Camera Serial Interface (CSI-2) and the Display Serial Interface (DSI-2) at a data rate of 2.5 Gbps per lane.

The AXE5-Eagle board does not have standalone connection for MIPI interface, it is accessible through the CRUVI HS ports. For more information about CRUVI HS connections, please refer to the CRUVI High-Speed Connectors section.

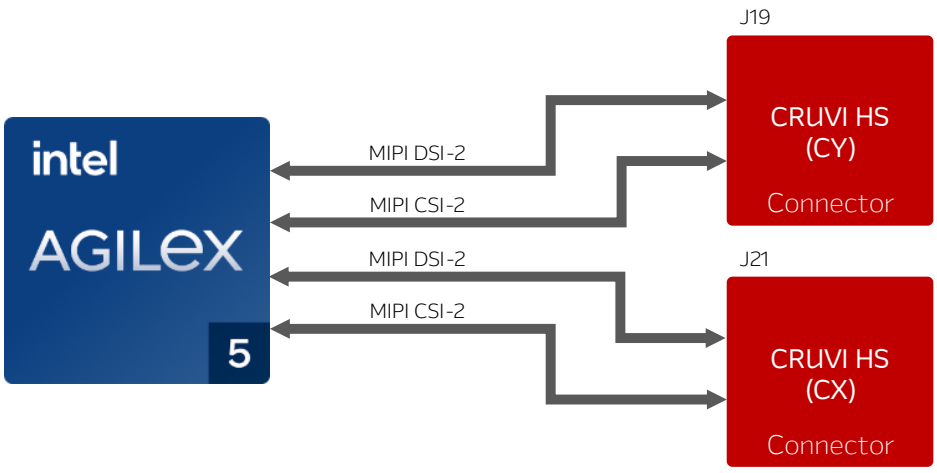

Figure 22 – MIPI D-PHY Connections

CRUVI HS CY Connection

MIPI	Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CSI-2	CY_B3_P	PIN_K77	33	Bidir	MIPI CSI-2 Data Lane [0]	Adjustable**
	CY_B3_N	PIN_M77	35			
	CY_B4_P	PIN_F77	39	Bidir	MIPI CSI-2 Data Lane [1]	Adjustable**
	CY_B4_N	PIN_H77	41			
	CY_A4_P	PIN_M67	38	Bidir	MIPI CSI-2 Data Lane [2]	Adjustable**
	CY_A4_N	PIN_K67	40			
	CY_B5_P	PIN_H67	45	Bidir	MIPI CSI-2 Data Lane [3]	Adjustable**
	CY_B5_N	PIN_F67	47			
	CY_B2_P	PIN_D74	27	Bidir	MIPI CSI-2 Clock Lane	Adjustable**
	CY_B2_N	PIN_F74	29			
DSI-2	CY_A1_P	PIN_P74	20	Bidir	MIPI DSI-2 Data Lane [0]	Adjustable**
	CY_A1_N	PIN_T74	22			
	CY_B1_P	PIN_V77	21	Bidir	MIPI DSI-2 Data Lane [1]	Adjustable**
	CY_B1_N	PIN_T77	23			
	CY_A3_P	PIN_V67	32	Bidir	MIPI DSI-2 Data Lane [2]	Adjustable**
	CY_A3_N	PIN_T67	34			
	CY_A2_P	PIN_M65	26	Bidir	MIPI DSI-2 Data Lane [3]	Adjustable**
	CY_A2_N	PIN_K65	28			
	CY_B0_P	PIN_M74	15	Bidir	MIPI DSI-2 Clock Lane	Adjustable**
	CY_B0_N	PIN_K74	17			

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on CRUVI_ADJ*

CRUVI HS CX Connection

MIPI	Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CSI-2	CX_B3_P	PIN_P55	33	Bidir	MIPI CSI-2 Data Lane [0]	Adjustable**
	CX_B3_N	PIN_T55	35			
	CX_B4_P	PIN_V58	39	Bidir	MIPI CSI-2 Data Lane [1]	Adjustable**
	CX_B4_N	PIN_T58	41			
	CX_A4_P	PIN_V47	38	Bidir	MIPI CSI-2 Data Lane [2]	Adjustable**
	CX_A4_N	PIN_T48	40			
	CX_B5_P	PIN_P44	45	Bidir	MIPI CSI-2 Data Lane [3]	Adjustable**
	CX_B5_N	PIN_T44	47			
	CX_B2_P	PIN_K55	27	Bidir	MIPI CSI-2 Clock Lane	Adjustable**
	CX_B2_N	PIN_M55	29			
DSI-2	CX_A1_P	PIN_H58	20	Bidir	MIPI DSI-2 Data Lane [0]	Adjustable**
	CX_A1_N	PIN_F58	22			
	CX_B1_P	PIN_M58	21	Bidir	MIPI DSI-2 Data Lane [1]	Adjustable**
	CX_B1_N	PIN_K58	23			
	CX_A3_P	PIN_M47	32	Bidir	MIPI DSI-2 Data Lane [2]	Adjustable**
	CX_A3_N	PIN_K47	34			
	CX_A2_P	PIN_F47	26	Bidir	MIPI DSI-2 Data Lane [3]	Adjustable**
	CX_A2_N	PIN_H47	28			
	CX_B0_P	PIN_F55	15	Bidir	MIPI DSI-2 Clock Lane	Adjustable**
	CX_B0_N	PIN_D55	17			

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on CRUVI_ADJ*

4.3.5 Miscellaneous Interfaces

The AXE5-Eagle development kit provides various miscellaneous interfaces, such as ADC/DAC modules for analog signal conversion, user LEDs offering visual indications, and user buttons for user input, enabling interactions and signal processing capabilities.

4.3.5.1 Analog Interface

The AXE5-Eagle board is equipped with Analog Devices' AD5592R multipurpose chip which is an 8-channel, 12-bit, configurable analog-to-digital, digital-to-analog converter with GPIO capabilities. It allows for handling both analog and digital data, supporting various configurations for sensing, measuring, and control functions.

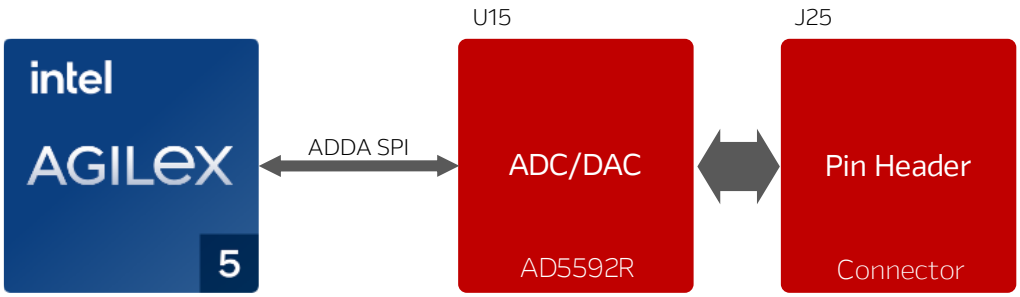

Figure 23 – ADC/DAC Connections

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
ADDA_RST	PIN_A17	-	Output	Reset	3.3-V LVCMOS
ADDA_SYNC	PIN_A14	-	Output	Synchronization	3.3-V LVCMOS
ADDA_CLK	PIN_B20	-	Output	Serial Clock	3.3-V LVCMOS
ADDA_DIN	PIN_A20	-	Output	Data Input	3.3-V LVCMOS
ADDA_DOUT	PIN_B14	-	Input	Data Output	3.3-V LVCMOS
ADDA_IO0	-	4	Analog	Analog I/O Channel [0]	-
ADDA_IO1	-	6	Analog	Analog I/O Channel [1]	-
ADDA_IO2	-	8	Analog	Analog I/O Channel [2]	-
ADDA_IO3	-	10	Analog	Analog I/O Channel [3]	-
ADDA_IO4	-	12	Analog	Analog I/O Channel [4]	-
ADDA_IO5	-	14	Analog	Analog I/O Channel [5]	-
ADDA_IO6	-	16	Analog	Analog I/O Channel [6]	-
ADDA_IO7	-	18	Analog	Analog I/O Channel [7]	-
3.3V	-	2	PWR	3.3V power to the connector	-
GND	-	1, 2, 3, 5, 7, 9, 11, 13, 15, 17, 19, 20	PWR	Ground to the connector	-

4.3.5.2 User-defined LEDs

The AXE5-Eagle board integrates four RGB LEDs directly connected to the FPGA, offering extensive user control over colours and illumination. Furthermore, there are two green user-controllable LEDs linked to the HPS, providing additional visual indicators. Each LED is individually addressable, offering precise control and illumination options, thereby enabling diverse applications and customizable visual feedback within the Agilex 5 SoC FPGA applications.

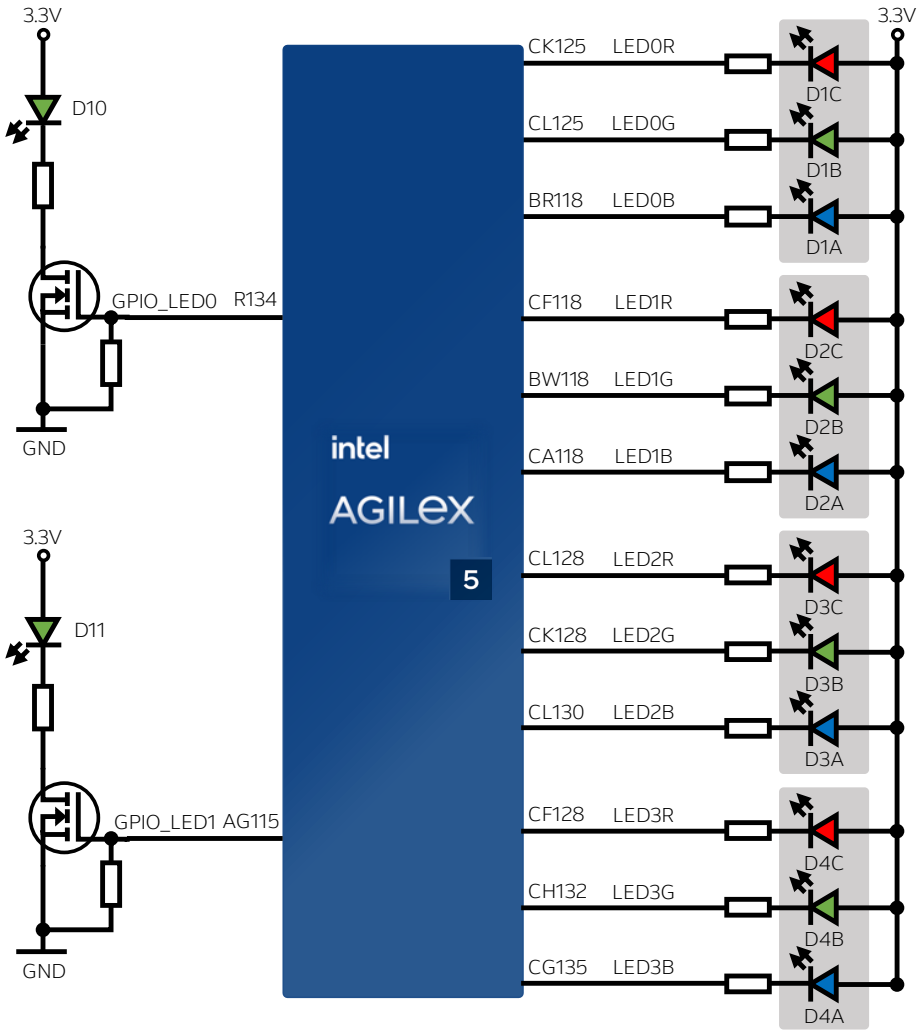

Figure 24 – LED Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
LED0R	PIN_CK125	Output	Red colour of D1 LED	3.3-V LVCMOS
LED0G	PIN_CL125	Output	Green colour of D1 LED	3.3-V LVCMOS
LED0B	PIN_BR118	Output	Blue colour of D1 LED	3.3-V LVCMOS
LED1R	PIN_CF118	Output	Red colour of D2 LED	3.3-V LVCMOS
LED1G	PIN_BW118	Output	Green colour of D2 LED	3.3-V LVCMOS
LED1B	PIN_CA118	Output	Blue colour of D2 LED	3.3-V LVCMOS
LED2R	PIN_CL128	Output	Red colour of D3 LED	3.3-V LVCMOS
LED2G	PIN_CK128	Output	Green colour of D3 LED	3.3-V LVCMOS
LED2B	PIN_CL130	Output	Blue colour of D3 LED	3.3-V LVCMOS
LED3R	PIN_CF128	Output	Red colour of D4 LED	3.3-V LVCMOS
LED3G	PIN_CH132	Output	Green colour of D4 LED	3.3-V LVCMOS
LED3B	PIN_CG135	Output	Blue colour of D4 LED	3.3-V LVCMOS
GPIO_LED0	PIN_R134	Output	HPS GPIO0_IO6 LED	1.8-V LVCMOS
GPIO_LED1	PIN_AG115	Output	HPS GPIO0_IO7 LED	1.8-V LVCMOS

4.3.5.3 User Buttons

The AXE5-Eagle board has seven push buttons connected to the SoC FPGA that allows user to interact with the Agilex 5 device. The buttons have different functions:

- 2 buttons connected to the HPS as user-defined push buttons
- 2 buttons connected to the FPGA as user-defined push buttons
- 1 button dedicated to HPS reset
- 1 button dedicated to FPGA reset
- 1 button for reconfiguration FPGA purpose

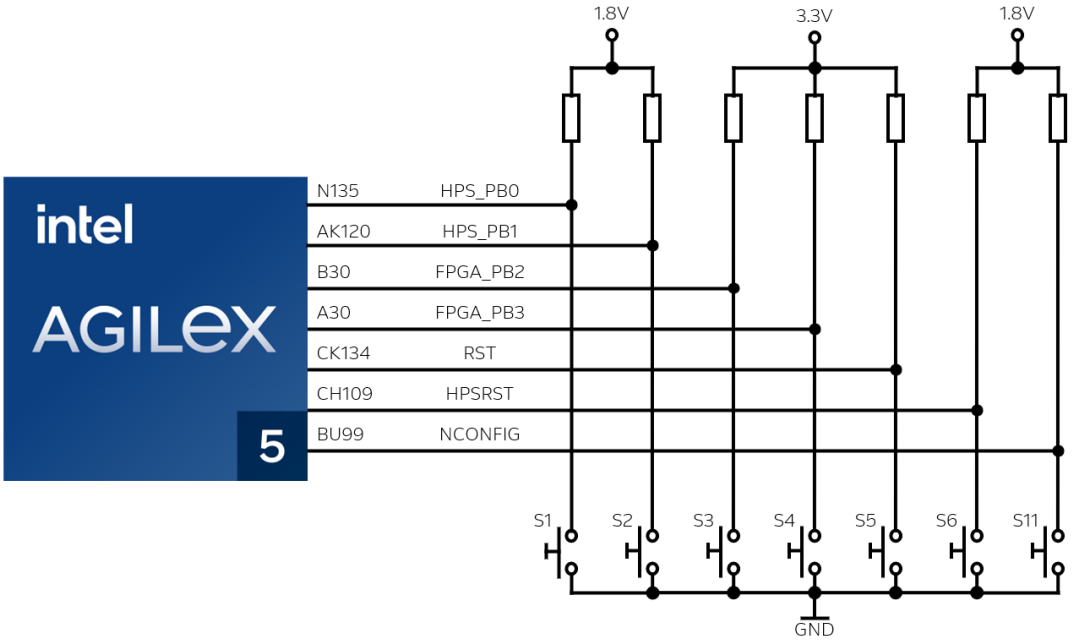

Figure 25 – Push Button Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
HPS_PB0	PIN_N135	Input	HPS user button (GPIO_IO8)	1.8-V LVCMOS
HPS_PB1	PIN_AK120	Input	HPS user button (GPIO_IO9)	1.8-V LVCMOS
FPGA_PB2	PIN_B30	Input	FPGA user button	3.3-V LVCMOS
FPGA_PB3	PIN_A30	Input	FPGA user button	3.3-V LVCMOS
RST	PIN_CK134	Input	FPGA reset	3.3-V LVCMOS
HPSRST	PIN_CH109	Input	HPS reset	1.8-V LVCMOS
NCONFIG	PIN_BU99	Input	nCONFIG trigger	1.8-V LVCMOS

4.4 Power Distribution System

The AXE5-Eagle development kit relies on a comprehensive power distribution system to efficiently manage power delivery to its components. This system ensures a coordinated flow of power, overseeing critical functions such as power sequencing, thermal protection, and the hierarchical power tree structure. These functionalities collectively ensure optimal performance and reliability across the AXE5-Eagle board operations.

4.4.1 Power Tree

The AXE5-Eagle is designed with a flexible power system that accommodates multiple power source options, including PCIe connectors and standalone power inputs. Employing diverse configurations with compact, small-footprinted power modules ensures reliable power delivery to the board and the connected mezzanine cards.

The following figure below shows the power tree structure on the AXE5-Eagle development board.

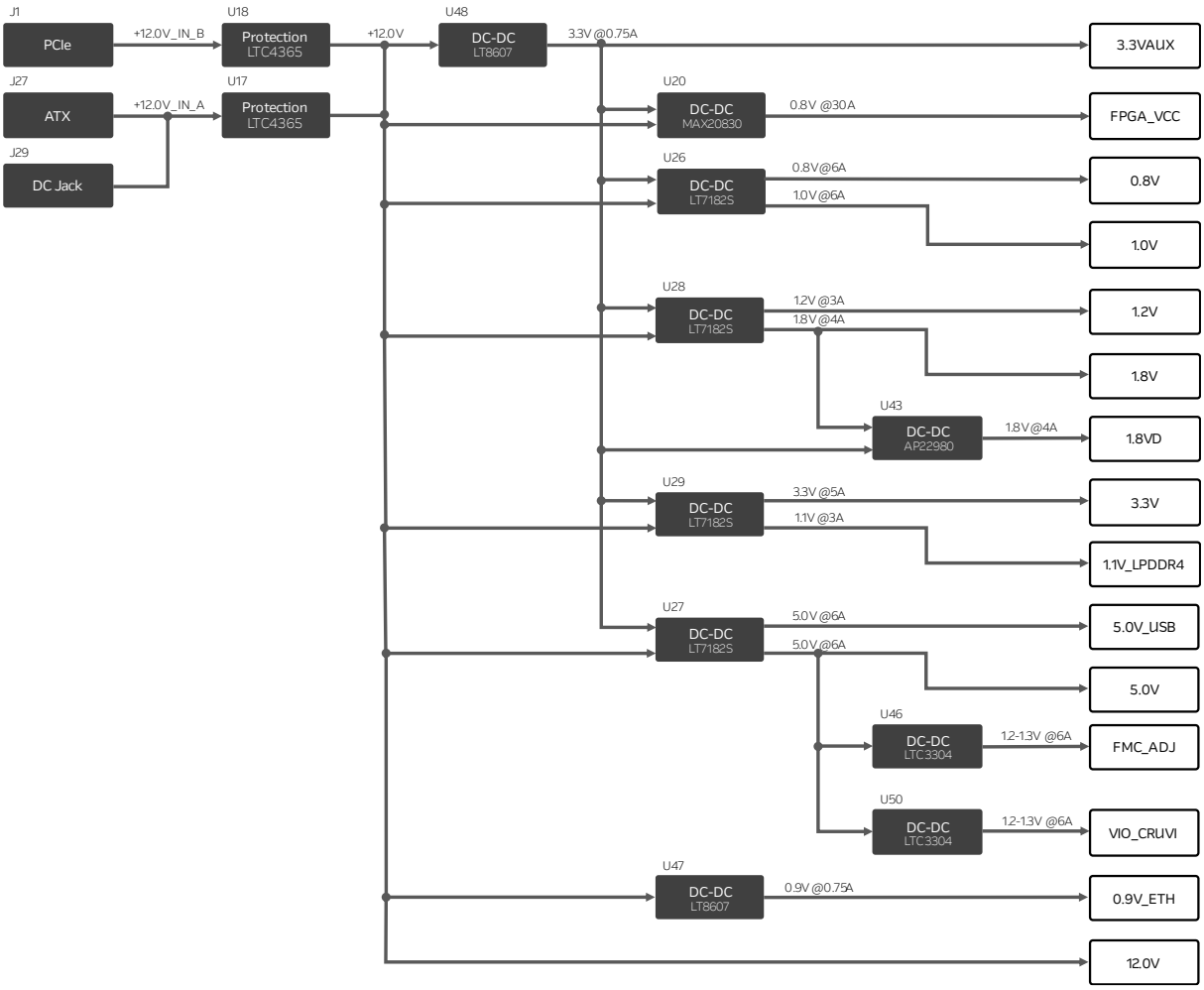

Figure 26 – Power Tree Structure

4.4.2 Power Sequence

Intel Agilex 5 SoC FPGA requires power-up sequencing. The AXE5-Eagle power system organizes power rails into power groups and enables them in the appropriate sequence for the Agilex 5 device.

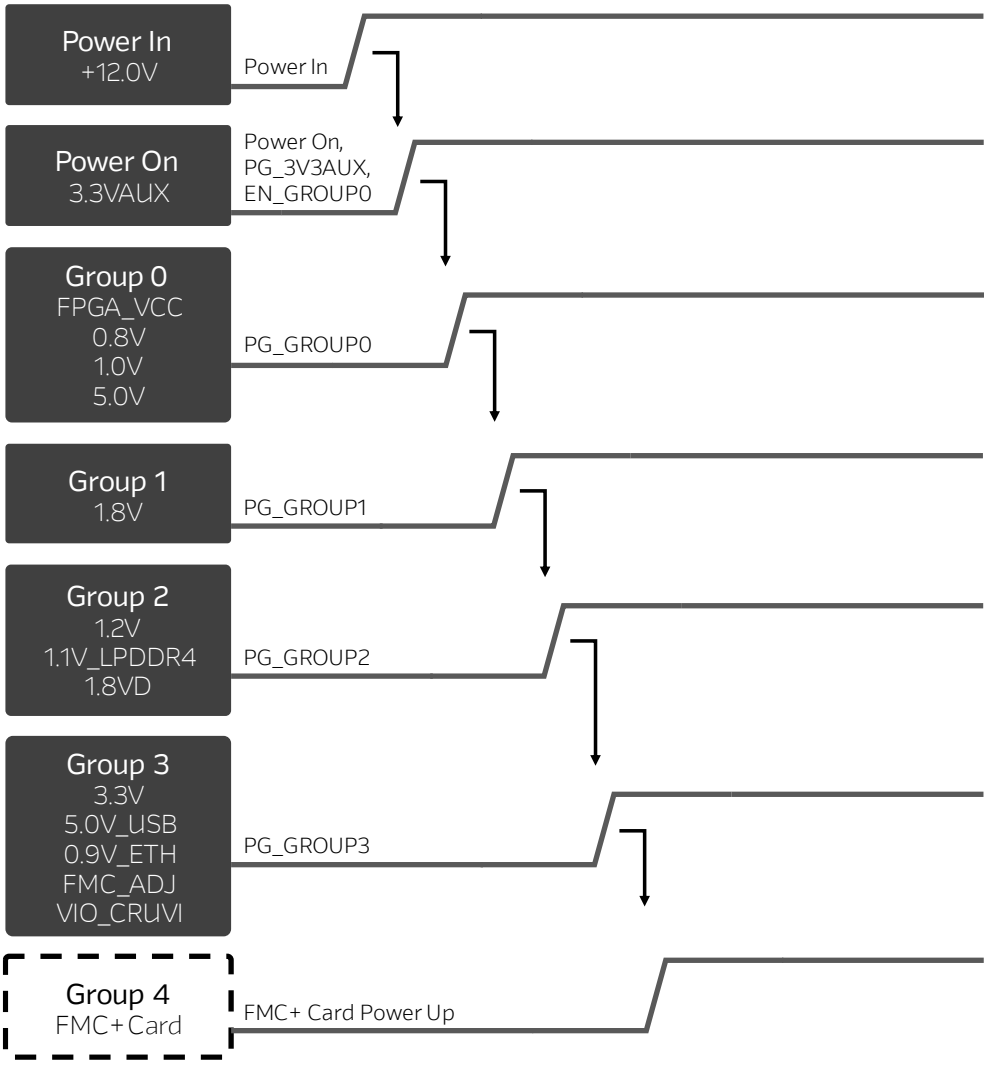

Figure 27 – Power Sequence

4.4.3 Thermal Protection

The AXE5-Eagle board is equipped with a heatsink and cooling fan to manage the Agilex 5 device power dissipation, and it is designed to operate in a typical laboratory environment with an ambient temperature of approximately 25 °C. However, the cooling system interfaces with the Agilex 5 device, allowing for parameterization based on application-specific needs and requirements.

The board is equipped not only with internal temperature diodes within various components, but also with separate, standalone temperature sensors. These sensors continuously monitor ambient temperatures and directly interface with the cooling system in addition to the FPGA.

U56 Temp Sensor is on the bottom layer of the board opposite the Power Supply Area.

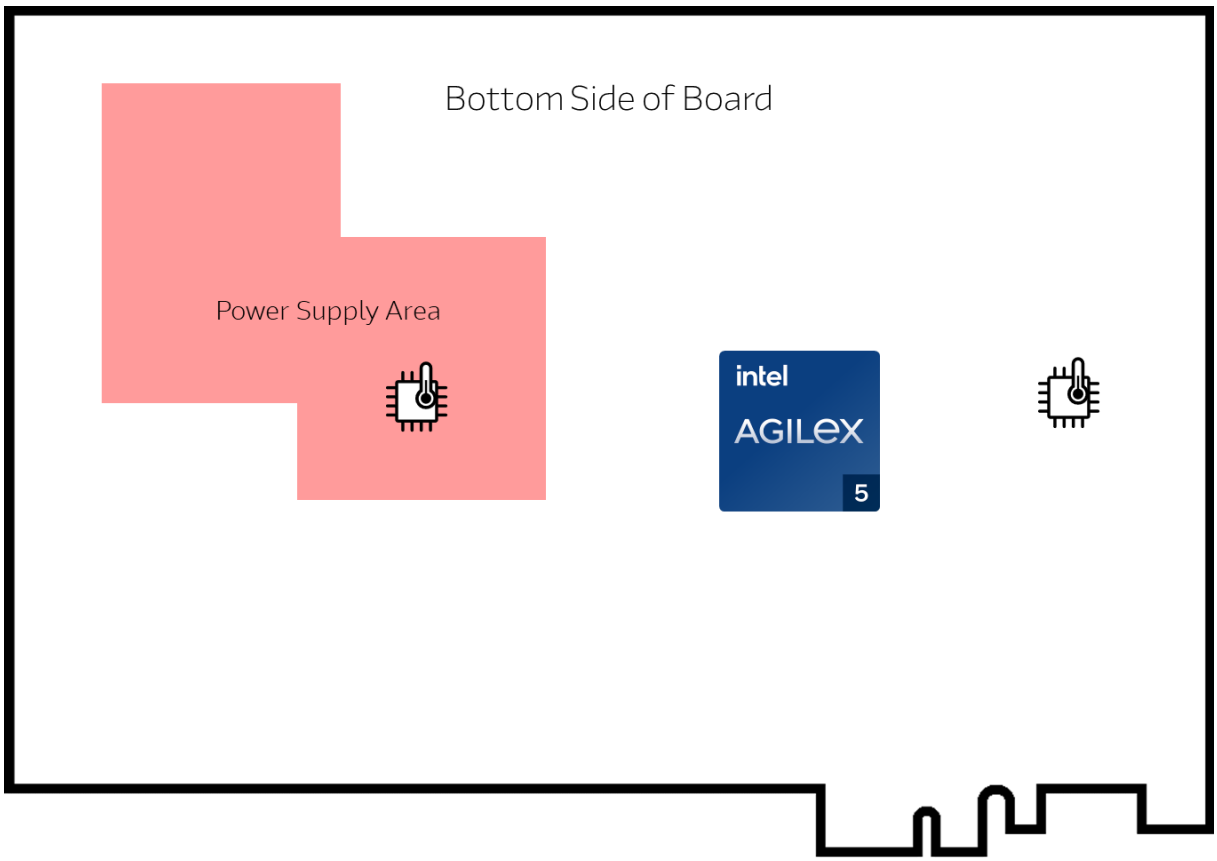

Figure 28 – Temperature Sensors locations

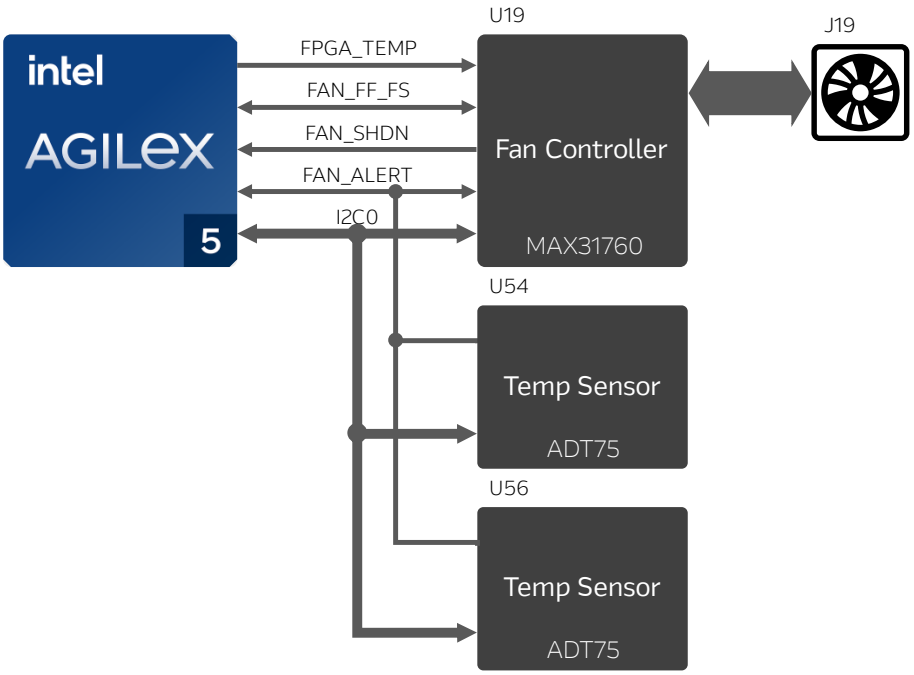

Figure 29 – Cooling solution

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
FAN_ALERT	PIN_A39	Bidir	ALERT input of fan controller	3.3-V LVCMOS
FAN_FF_FS	PIN_B35	Bidir	Fan-Failure Output and Full-Speed Input of fan controller	3.3-V LVCMOS
FAN_SHDN	PIN_CF121	Input	Shutdown output for over temperature	3.3-V LVCMOS
FPGA_TEMP_P	PIN_BE100	Input	Temperature Sensing Diode	1.8-V LVCMOS
FPGA_TEMP_N	PIN_BF100			
I2C0_SDA	PIN_U134	Bidir	Serial Data Line of I2C0	1.8-V LVCMOS
I2C0_SCL	PIN_AL120	Bidir	Serial Clock Line of I2C0	1.8-V LVCMOS

For detailed information about the I²C connection, please refer to the I²C Structure section.

Chapter 5 - Software and Driver Installation

The using and programming of the AXE5-Eagle development board require various program installation of which are detailed in this section.

First, it is necessary to create your Basic Intel Account if you do not already have one. This account is required for using the software, including licensing. Below, you will find step-by-step guides on installing the software and drivers for Windows operating systems.

5.1 Installing Quartus Prime Software

5.1.1 Go to the Intel Download Center: Link.

5.1.2 Make sure that **Quartus Prime Pro** and **24.1** are selected, or your preferred version[3] (highlighted in red).

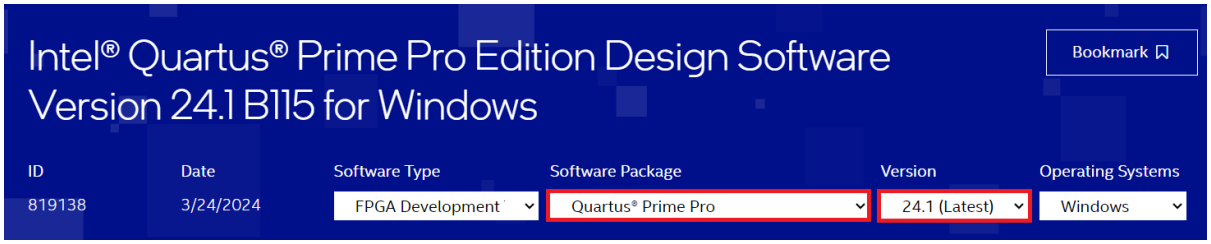

Figure 30 – Quartus Prime Pro Download

5.1.3 Download the following files from the "Individual Files" tab (highlighted in red) and save them in the same folder:

- **Intel Quartus Prime Pro Edition Part 1**
- **Intel Quartus Prime Pro Edition Part 2**
- **Questa – Intel FPGA and Starter Edition**
- **Intel Agilex 5 device support (Requires Intel Agilex common files)**
- **Intel Agilex common files**

If the download page redirects you to the Software License Agreement page, accept the Legal Disclaimer, and the downloading will start automatically.

[3] Please note, that Agilex 5 SoC FPGA is supported from version 24.1 in Quartus Prime Pro Edition.

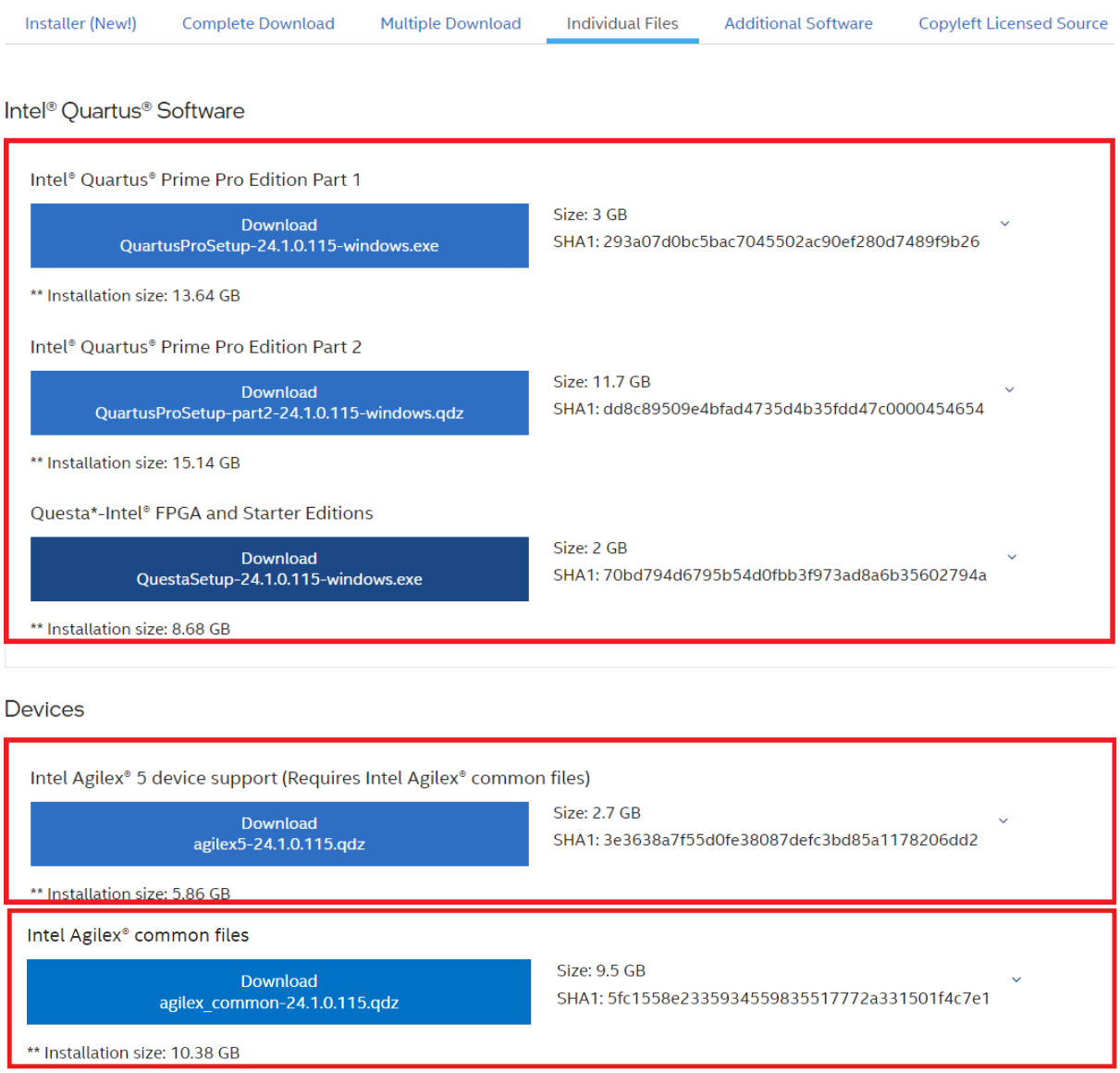

Figure 31 – Quartus Prime Pro Elements

5.1.4 After the download is finished, run the Quartus Prime installer.

5.1.5 When prompted to select the components, the installer will automatically detect the Agilex 5 device support and Questa packages when they are in the same folder. Make sure these components are selected:

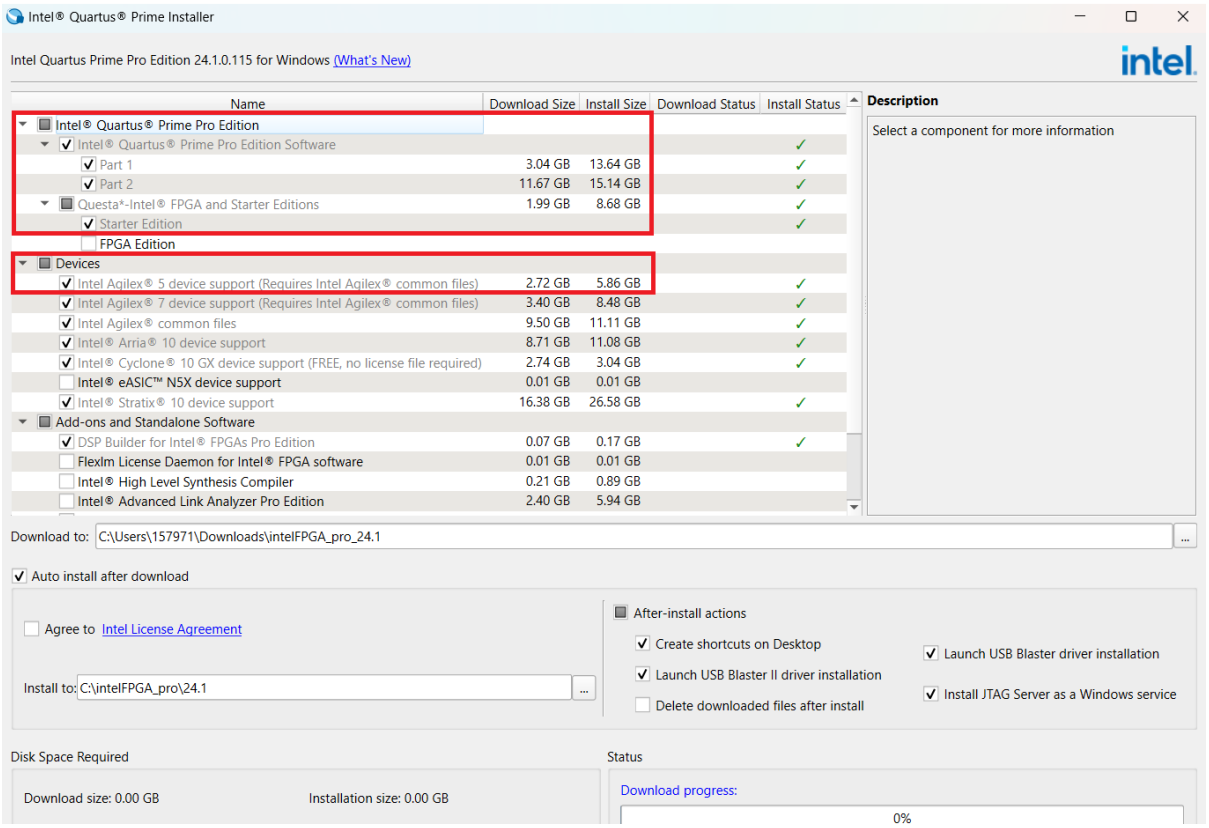

Figure 32 – Quartus Prime Pro Installation

5.1.6 Finish the installation of the Quartus Pro and proceeded to the next section to install Arrow USB Programmer2 to be able to connect to the AXE5-Eagle board.

5.2 Installing Arrow USB Programmer2

The AXE5-Eagle board uses version 2 of the Arrow USB Programmer2 programming solution, that is an FTDI FT2232H Hi-Speed USB controller plus a programmer DLL. Since this FTDI USB controller is a very common standard device, usually no specific drivers are needed to make the AXE5-Eagle work.

5.2.1 Download the appropriate version[4] of Arrow USB Programmer2 for AXE5-Eagle from Trenz Electronic Wiki page or alternatively this direct link.

[4] Modules produced after June 2020 are no longer compatible with older drivers. Please install driver version 2.4 or newer.

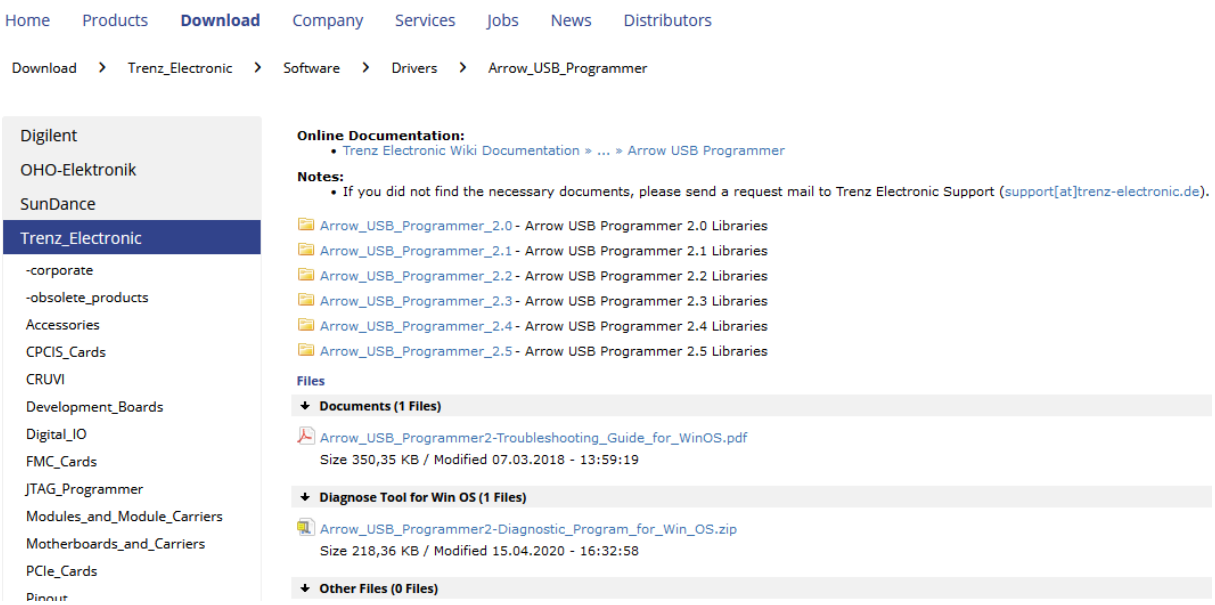

Figure 33 – Arrow USB Programmer Driver Installation

5.2.2 After downloading the file, run the installer to install the Arrow USB Programmer2. The setup executable installs the programmer DLL and adds some keys to the registry of the PC.

5.2.3 Make sure that the Arrow USB Programmer2 module is connected to the AXE5-Eagle board correctly.

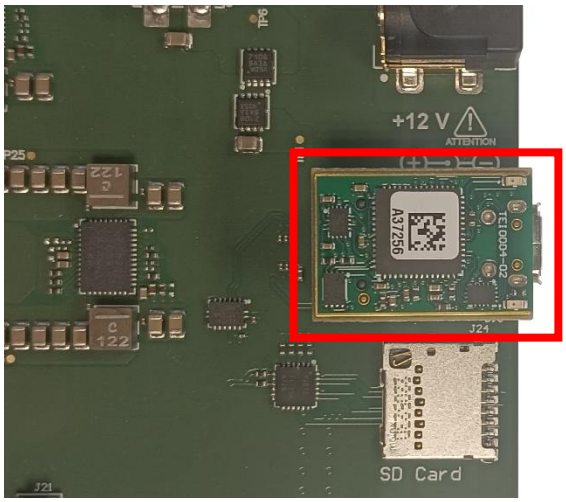

Figure 34 – TEI0004 Arrow USB Programmer

5.2.4 After connecting the AXE5-Eagle board to the PC, two unknown devices might appear in the “Other devices” section of device manager of the PC.

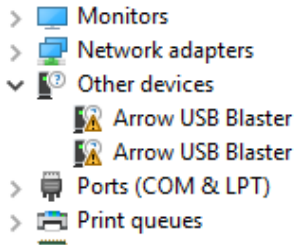

Figure 35 – Arrow USB Blaster in Device Manager

Windows usually automatically finds the appropriate drivers for these devices. After some time, the "Other devices" section should be empty. Instead, two USB Serial Converters should be listed in the section "USB Serial Bus controllers":

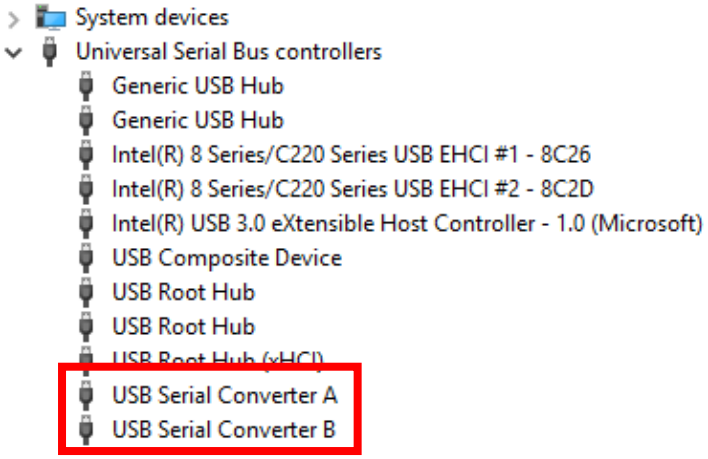

Figure 36 – Arrow USB Blaster listing

Furthermore, a USB Serial Port should be listed in the "Ports (COM & LPT)" section.

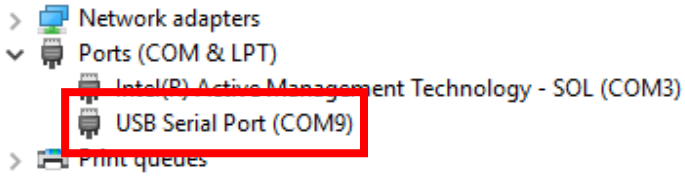

Figure 37 – Arrow USB Blaster as Serial COM port

Note that the number of the port will most probably be different from the one shown here.

In case Windows does not automatically find the appropriate drivers, go to http://www.ftdichip.com/Drivers/D2XX.htm to download the setup executable to install the required drivers.

5.3 License

Quartus Pro is free for Agilex 5, but needs a license. However, even though Questa Starter Edition can be used free of charge, you need to generate a free license for it.

5.3.1 Log in to Intel FPGA Self-Service Licensing Center

5.3.2 Go to **Sign up for Evaluation or Free Licenses** tab.

5.3.3 Select **Questa*-Intel® FPGA Starter Edition SW-QUESTA** option.

5.3.4 Set the seats and accept the terms of use this license.

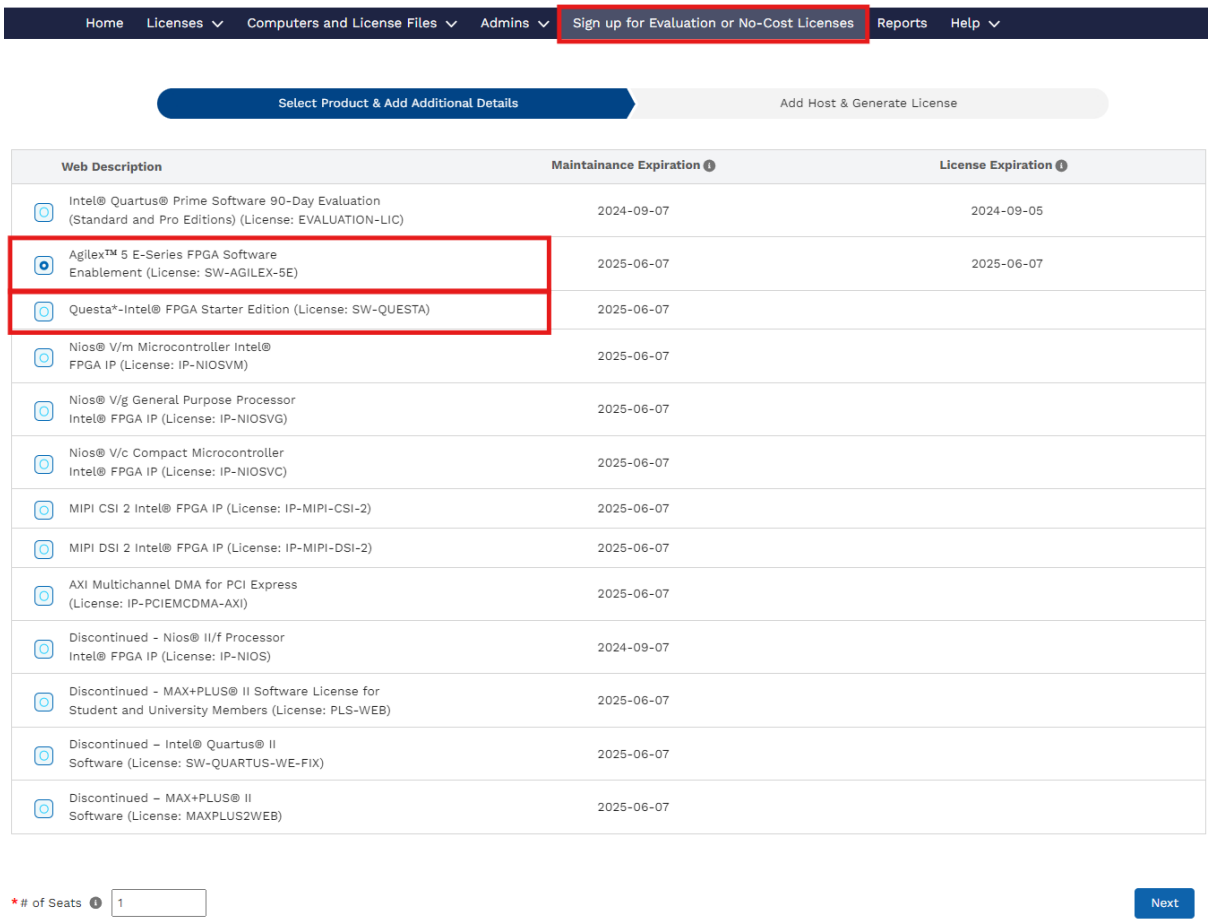

Figure 38 – Acquiring Agilex 5 Quartus License

5.3.5 Click on **Next** button.
5.3.6 In the next window select **+New computer**.
5.3.7 In the Create Computer window, fill in the fields with your computer details and click on **Save**.
5.3.8 Choose the computer you created and check the box agreeing to the license use terms.
5.3.9 Click the **Generate** button.
5.3.10 Repeat for **Questa*-Intel® FPGA Starter Edition SW-QUESTA** option.

The license file will be provided by email, or you can also download it under Intel® FPGA Self-Service Licensing Center.

Chapter 6 - Appendix

6.1 Revision History

Version	Change Log	Date of Change
V0.3	Preliminary Version release	02/09/2024
V0.4	Updated Version	02/29/2024
V0.5	Updated Version	03/22/2024
V0.6	Updated Version	04/26/2024
V1.0	Final Version (not published)	06/05/2024
V1.1	Updated rev3 PCB changes, removed Tutorials	06/07/2024

6.2 Legal Disclaimer

ARROW ELECTRONICS

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You shall not use the Evaluation Board in any safety critical or functional safety testing, including but not limited to testing of life supporting, military or nuclear applications. Arrow expressly disclaims any responsibility for such usage which shall be made at Your sole risk.

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You shall, at Your expense, defend Arrow and its Affiliates and Licensors against a claim or action brought by a third party for infringement or misappropriation of any patent, copyright, trade secret or other intellectual property right of a third party to the extent resulting from (1) Your combination of the Evaluation Board with any other component, system, software, or firmware, (2) Your modification of the Evaluation Board, or (3) Your use of the Evaluation Board in a manner not permitted under this Agreement. You shall indemnify Arrow and its Affiliates and Licensors against and pay any resulting costs and damages finally awarded against Arrow and its Affiliates and Licensors or agreed to in any settlement, provided that You have sole control of the defense and settlement of the claim or action, and Arrow cooperates in the defense and furnishes all related evidence under its control at Your expense. Arrow will be entitled to participate in the defense of such claim or action and to employ counsel at its own expense.

RECYCLING

The Evaluation Board is not to be disposed as an urban waste. At the end of its life cycle, differentiated waste collection must be followed, as stated in the directive 2002/96/EC. In all the countries belonging to the European Union (EU Dir. 2002/96/EC) and those following differentiated recycling, the Evaluation Board is subject to differentiated recycling at the end of its life cycle, therefore: It is forbidden to dispose the Evaluation Board as an undifferentiated waste or with other domestic wastes. Consult the local authorities for more information on the proper disposal channels. An incorrect Evaluation Board disposal may cause damage to the environment and is punishable by the law.