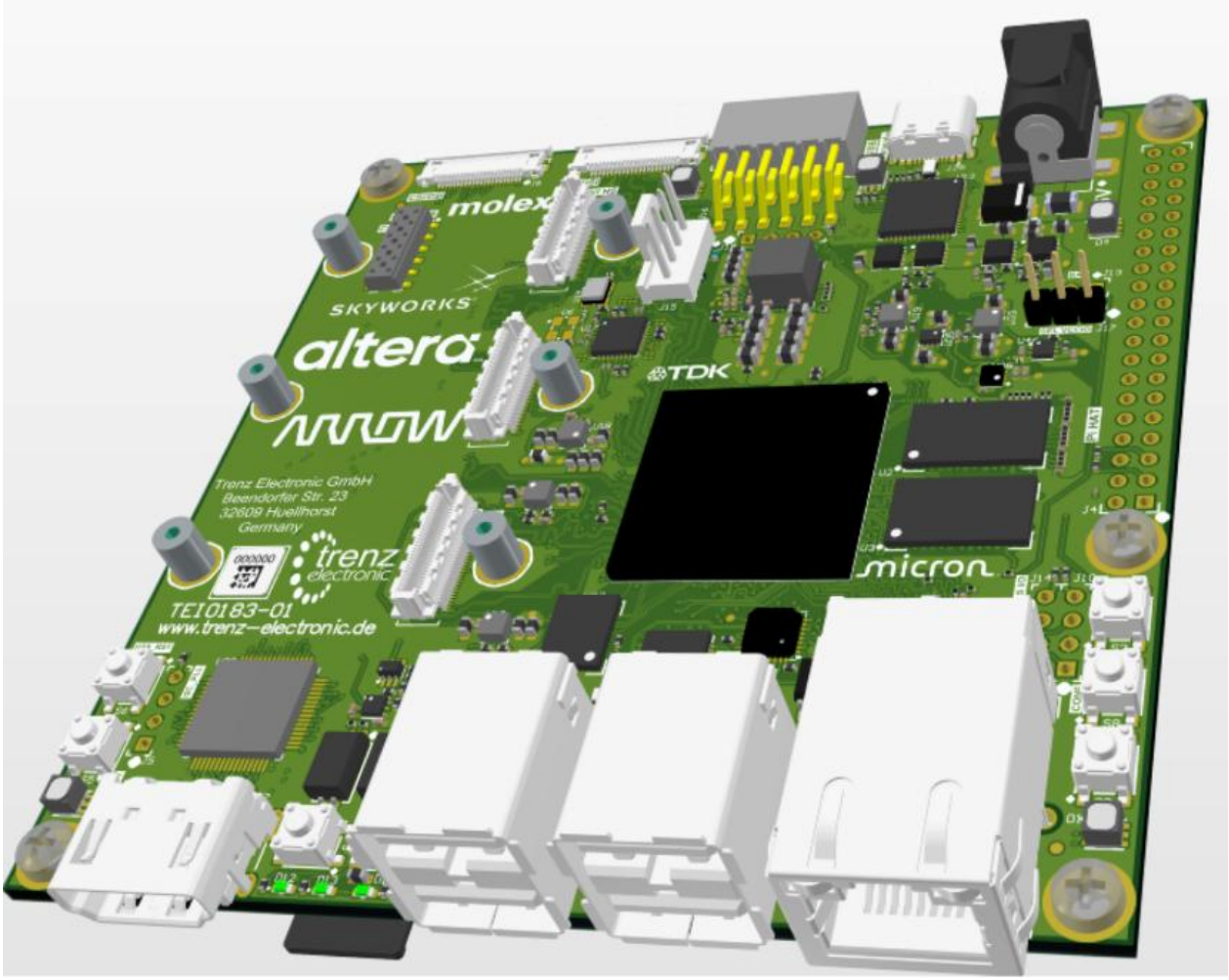
AXE5-Eagle User Guide



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Please read the legal disclaimer at the end of this document.

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1 AXE5-Falcon Development Kit

1.1 About the Arrow AXE5-Falcon Development Kit

The AXE5-Falcon Development Kit is a general-purpose, full-featured board, delivering a development platform for evaluating the features of the Altera™ Agilex™ 5 SoC FPGA. It supports various connector interfaces, FPGA, and Hard Processor System (HPS), providing a complete design environment to speed up development.

The evaluation board is based on the Altera™ Agilex™ 5 E-Series SoC FPGA which provides power-efficient performance and smaller form factors for midrange FPGA applications. This series is manufactured using Altera 7 technology and offers advanced features such as a second-generation Altera® Hyperflex™ FPGA architecture, and a processor system consisting of dual Arm Cortex-A55 cores. The capabilities and cutting-edge functionality of Altera™ Agilex™ 5 are suitable for a broad range of applications that require high performance, lower power consumption, smaller form factor, and lower logic densities.

The AXE5-Falcon board is equipped with HPS-enabled hardware features, DDR4 memory, 10/100/1000 Mbps Ethernet ports, 4 ports USB 2.0 Hi-Speed, HDMI 1.4, microSD card, flash memory, CRUVI HS and LS interfaces, PMOD, and Raspberry Pi Hat header.

The AXE5-Falcon Development Kit contains all the tools needed to use the board in conjunction with a computer that runs a 64-bit Linux or Microsoft Windows 10, Windows 11, or later operating system.

1.2 Useful Links

A set of useful links that can be used to get relevant information about the AXE5-Falcon development kit or the Agilex 5 FPGA and FPGA SoC.

- Altera Agilex 5 Webpage
- AXE5-Falcon Wiki Page

1.3 Getting Help

To get help for this development kit, contact us at fpga_support@arrow.com

1.4 Documentation Guidelines

The meaning of the icon in this User Guide as follow:

This icon signposts warnings and important items that must be taken care of and be aware of when operating the AXE5-Falcon Development Kit.

2 Introduction to the AXE-Eagle Board

1.1 Layout and Components

Figure 2-1 and Figure 2-2 show the top and the bottom view of the board. They depict the layout of the board and indicate the location of the various connectors and key components.

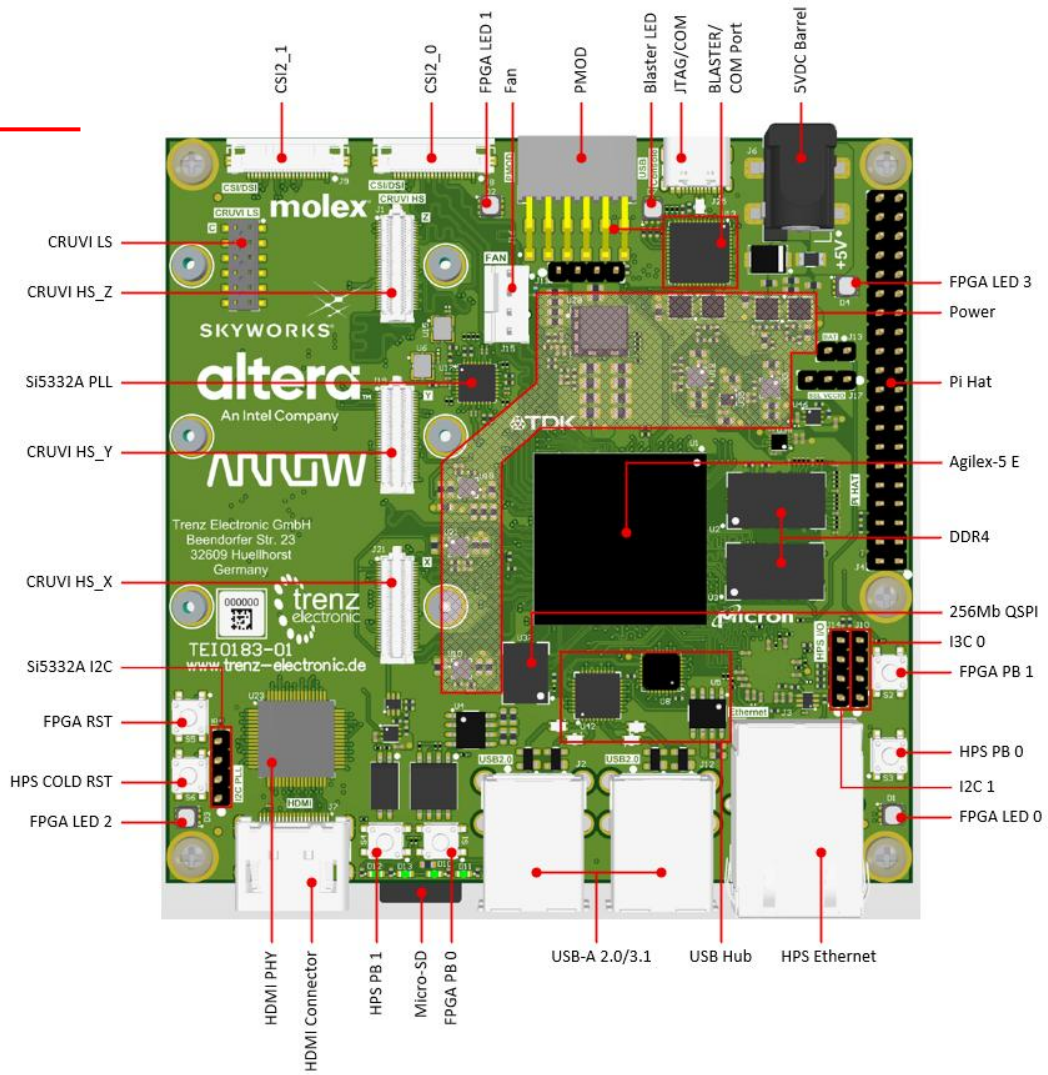

Figure 2-1 : AXE5-Falcon Board (top view)

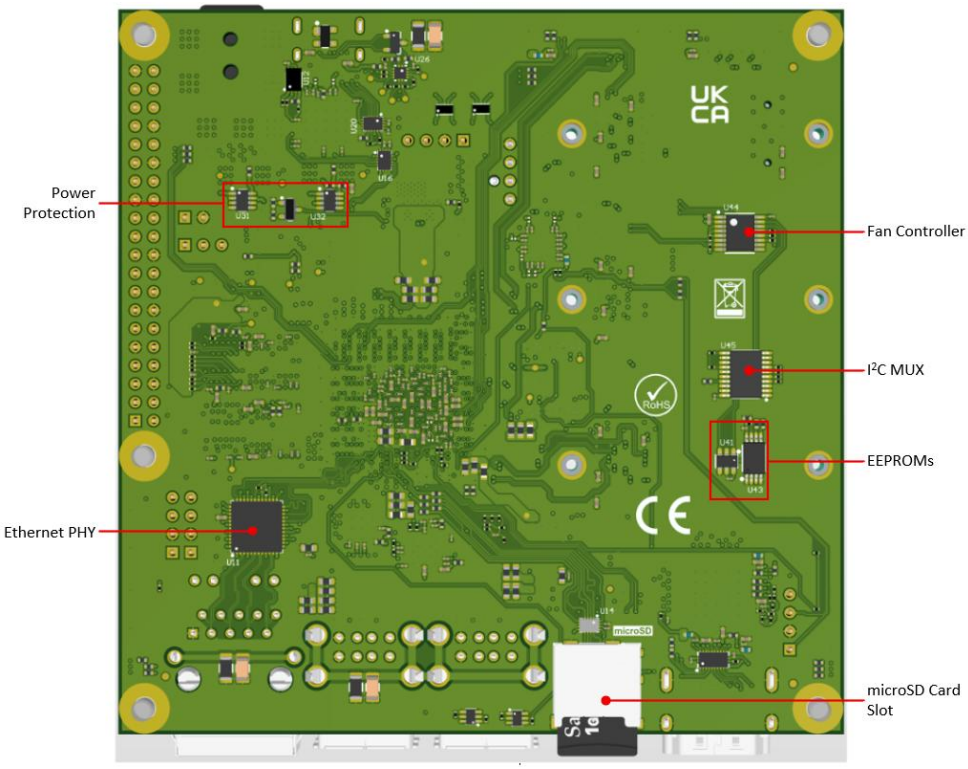

Figure 2-2 : AXE5-Falcon Board (bottom view)

2.1 Block Diagram

Figure 2-3 represents the block diagram of the board. All the connections are established through the Agilex SoC FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

A complete set of schematics and other board relevant files are available at Trenz Electronic.

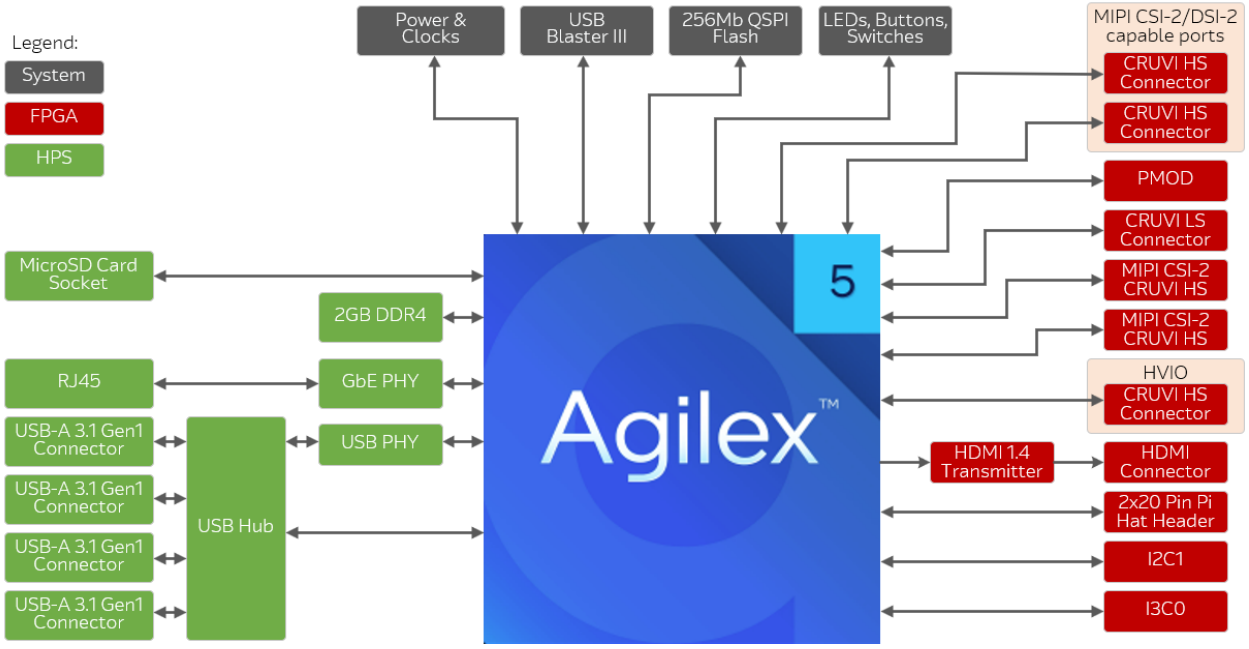

Figure 2-3 : AXE5-Falcon Block Diagram

2.2 Board Features

The following features are available on the AXE5-Falcon board:

System

FPGA Device:

- Altera Agilex® 5 E-Series SoC FPGA device:
  - A5EE013BB23BE6SCS (Production FPGA)

Features of the SoC FPGAs on the AXE5-Falcon Board:

Resources	Device
	A5EE013B ('B0' version)
Logic Elements (kLE)	656
Logic core architecture:	Second generation Altera Hyperflex™ FPGA architecture
M20K Memory (Mb)	358 (6.99Mb)
18x19 Multipliers	376
LVDS data rate	1.25 Gbps
MIPI D-PHY data rate	2.5 Gbps
Processor	Dual core Arm Cortex-A55 up to 1.25 GHz
Cache size	Shared: 1 MB L3 Cortex-A55: 32 KB L1, 128 KB L2
Process technology:	Altera 7
Package	795-pin VPBGA

Board Management System:

- Power Monitor
- Temperature Monitor
- Fan Control
- Configurable Clock Source

FPGA Configuration and Debug

- 10-pin header for USB Blaster Programmer – JTAG mode
- 256Mb QSPI Flash – AS x4 Configuration scheme
- Partial reconfiguration support

FPGA Fabric Side

Communication and Connectivity

- HDMI 1.4 Transmitter with HDMI connector
- 2x MIPI CSI-2 connectors (22-pin Pi)
- 2× CRUVI HS Connectors with MIPI D-PHY v2.5 interface
- 1× CRUVI LS Connectors
- Single or Dual Ethernet via CRUVI HS Connector on HVIO ports
- 40-pin Raspberry Pi Hat header
- 1x dual-row PMOC connector

HPS Side

Memory Devices

- 2 GByte 3200MT/s DDR4, 32 bits (operating at 1600MT/s)
- microSD Card socket

Communication and Connectivity

- 10/100/1000 Mbps Ethernet via RJ45 connector
- 4× USB-A 2.0 Connectors
- USB to UART Bridge via USB-C JTAG Connector

Others

Buttons and Indicators

- 4× user RGB LEDs
- 4× user push buttons
- 6× user DIP switches

Power

- DC Jack power input connector for standalone operation
- Recommended external supply voltage range: +5.0 V, 3.0 A (nominal)
- Recommended I/O signal voltage ranges[1]:
  - CRUVI HS (X and Z)interface: 0 to +1.3 V[1]
  - CRUVI HS (Y)interface: 0 to +1.8 V[1]
  - CRUVI LS interface: 0 to +3.3 V
  - PMOD interface: 0 to +3.3 V
  - Pi Hat interface: 0 to +3.3 V
  - MIPI CSI (0 and 1)interface: 0 to +1.3 V[1]

Mechanical

- 100 mm × 100 mm board size
- Optional heatsink fan

2.3 Ordering Information

Development Kit Version	Ordering Code	Core Device Part Number
Production (Q2/3 2026)	AXE5-Falcon	A5EE013BB23BE6SCS

2.4 Box Contents

The AXE5-Falcon Development Kit includes the following hardware:

- AXE5-Falcon development board
- 5VDC 15 W Power supply
- 1x USB-C cable

3 Development Board Setup

3.1 System Power

This development kit is designed to operate in standalone evaluation mode. The board must be powered by either the provided power supply connected to the power barrel connector J6, or the USB-C J25

The power source selection occurs automatically on the AXE5-Falcon board.

For detailed information about the AXE5-Falcon power system, see the Power Distribution System section.

3.2 Jumper Settings

There are jumpers on the AXE5-Falcon development kit that affect the basic functionality of the board.

3.2.1 J17

Jumper	position	Function	
J17	1 - 2	VCCIO of bank 2A_T = 1.2V for MIPI CSI-2 functions	
	2 - 3	SEL_1V3 I/O pin=0	VCCIO of bank 2A_T = VCCIO bank 2A_B = 1.2V
		SEL_1V3 I/O pin=1	VCCIO of bank 2A_T = VCCIO bank 2A_B = 1.3V

3.3 Board Status Elements

The Arrow AXE5-Falcon development kit has 3 board-specific status LEDs that indicate the status of the board. The following figure shows the status LED areas of the board.

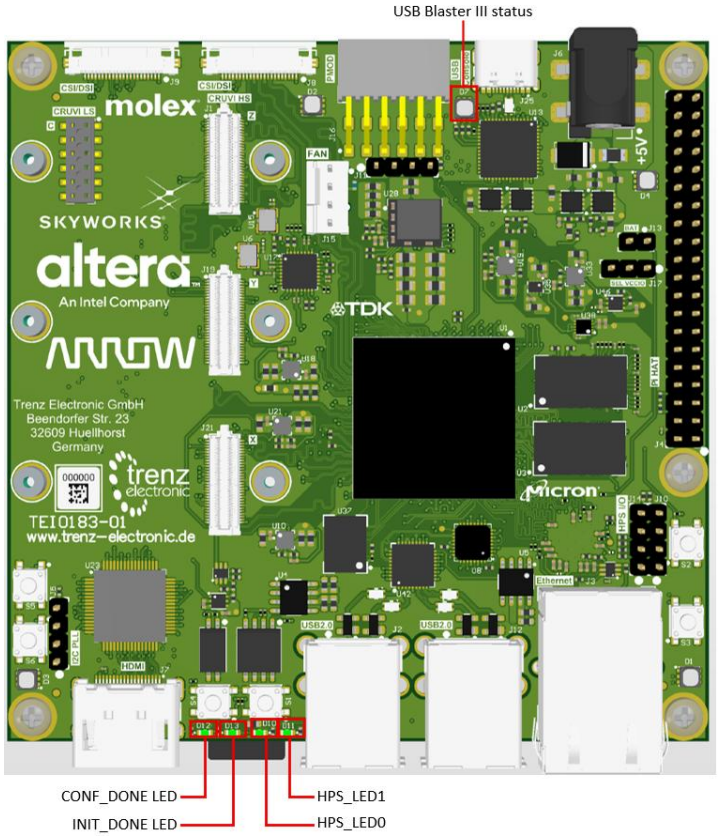

Figure 3-1 : Position of Indication LEDs

The following table defines the status LEDs. For user-controlled LED details, see User-defined LEDs section.

Board Reference	LED Name	Color	Description
D7	USB BLASTER	RGB	Status of USB Blaster III operation
D10	HPS_LED0	Green	Driven by HPS GPIO0_IO14
D11	HPS_LED1	Green	Driven by HPS GPIO0_IO15
D12	CONF_DONE	Green	ON when CONF_DONE pin is asserted
D13	INIT_DONE	Green	ON when INIT_DONE pin is asserted

4 Connections and Peripherals of the AXE5-Falcon Development Kit

4.1 Clock Circuitry

On the AXE5-Falcon board, the Altera Agilex 5 receives clock signals from multiple clock sources to ensure that the correct clock signal is directly available for different applications and interfaces.

The board contains two type of clock circuits:

- **On-Board Clock Circuits**

  This includes constant value oscillators and a preprogrammed, user-programmable PLL*, that are integrated into the board and provide all local clock signals for the operation of the AXE5-Falcon board including reference clocks for DDR4 memory interfaces, FPGA SDM, fabric, and the HPS core.
  **The programming of the PLL is not the focus of this document. For detailed information regarding Si5332A PLL programming, we recommend visiting the manufacturer's website, where datasheets and other related documents are available.*

- **Off-Board Clock I/Os**

  The development board has optional input clocks which can be driven onto the board. These clock I/Os are connected to the 3 CRUVI HS connevtors.

The clock system can be seen in Figure 4-1. For detailed clock connections, refer to the schematic.

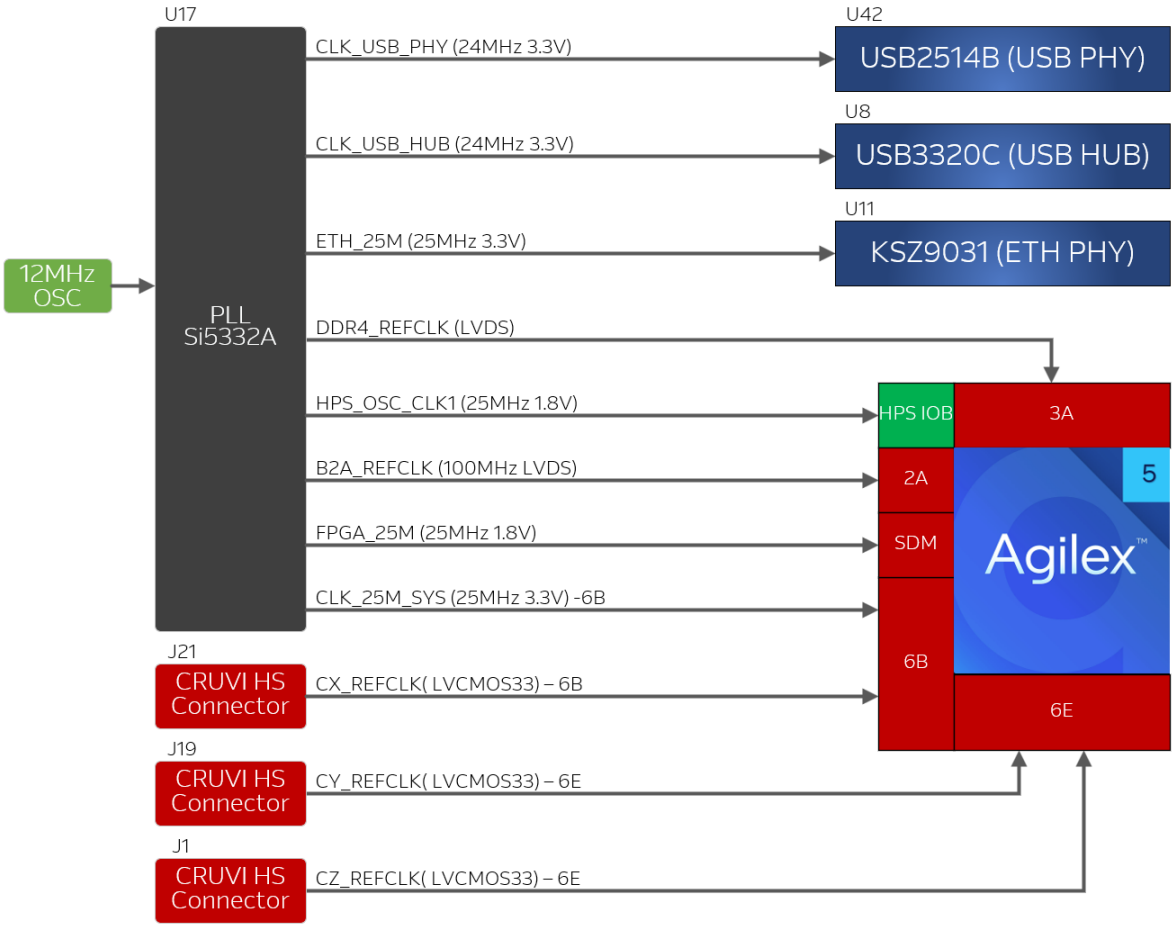

Figure 4-1 : Simplified Clock Connection Diagram

4.1.1 On-Board Clock Inputs

Board Reference	FPGA Pin No.	Clock Freq. (MHz)	Description	I/O Std
FPGA_25M	DB72	25	25 MHz clock for SDM	1.8-V
CLK_25M_SYS	CR6	25	25 MHz clock for FPGA Fabric	3.3-V LVCMOS
HPS_OSC_CLK1	AN67	25	25 MHz clock for HPS	1.8-V
DDR4_REFCK_P	J51	200	FPGA DDR4 reference clock	1.2V True Differential Signaling
DDR4_REFCK_N	G51			
B2A_REFCLK_P	DP55	25	FPGA fabric reference clock	Adjustable**
B2A_REFCLK_N	DN53			
CLK_USB_HUB	NA	24	USB HUB reference clock	1.8V
CLK_USB_PHY	NA	24	USB PHY reference clock	3.3V
ETH_CLK	NA	25		3.3V

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on SEL_1v3. Note: For True Differential Signaling, Input Termination must be set to "differential".*

4.1.2 Off-Board Clock I/Os

For detailed pinout information regarding off-board clock I/Os, please refer to the section associated with the CRUVI HS connectors.

4.2 I2C Structure

The I²C is a two-wire serial communication protocol that allows multiple devices to communicate with each other over a common bus.

The Altera Agilex 5 device use the I²C for reading and writing to the various components on the board and have option to utilize it as the I²C host for accessing the devices, adjusting clock frequencies, obtaining board status data or accessing EEPROM memory.

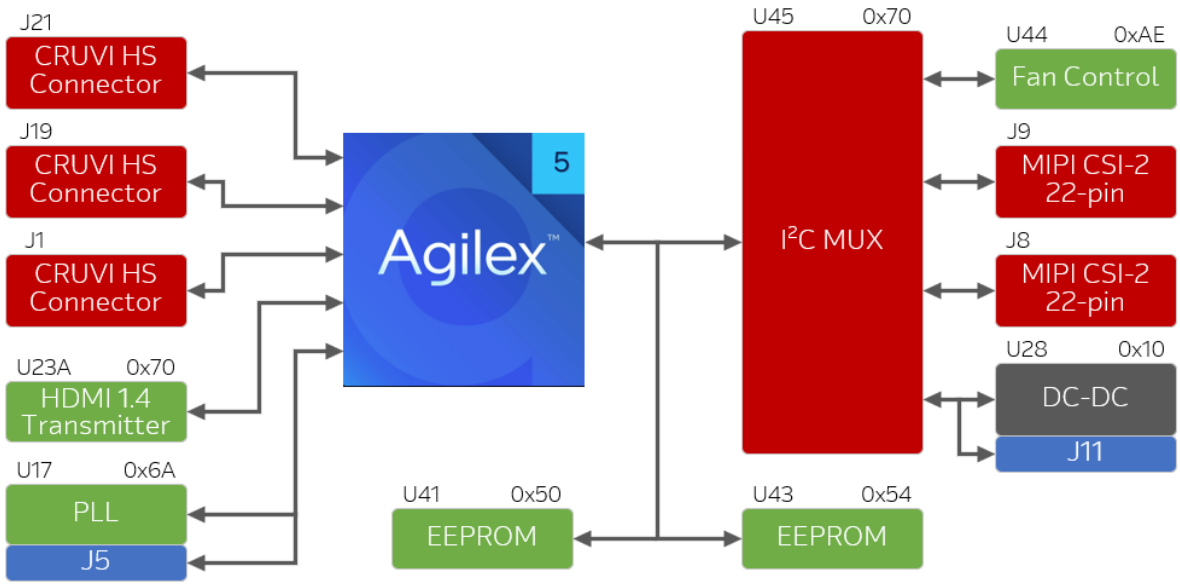

Figure 4-2 : I2C Structure Block Diagram

4.2.1 I²C Device Address Table

All I²C addresses are in 7-bit format.

Bus	Address	Device Part Number	Device Label	Device Name
I2C	0x50	24AA025E48T	U41	EEPROM
	0x54	24AA128T	U43	EEPROM
	0x70	TCA9544A	U45	I²C MUX
MUX_I2C	0xAE	MAX31760AEE+T	U44	Ch0: Fan Control
	-	22-pin Rpi CSI-2	J9	Ch1: MIPI CSI-2 ch 1 Camera
	-	22-pin Rpi CSI-2	J8	Ch2: MIPI CSI-2 ch 0 Camera
	0x10	FS1525	U28	Ch3: DC-DC converter
			J11	Pin Header
CZ_SMB			J1	CRUVI HS Connector
CY_SMB	-	-	J19	CRUVI HS Connector
CX_SMB	-	-	J21	CRUVI HS Connector
PLL	0x6A	Si5332A	U17	PLL
			J5	Pin Header

4.3 System Control

The I²C bus forms the essential interface for board management.

- **MAC Address EEPROMs:** 24AA025E48T from Microchip, which is a serial pre-programmed EEPROM memory. It only contains its own unique number to give individual identification and Internet addressing;
- **User EEPROM:** 24AA128T from Microchip, which is a serial EEPROM for custom application-related configuration data;
- **Fan Controller:** in accordance with data measured by various temperature sensors, supervising and regulating the fan speed to prevent the FPGA device and the board from overheating;
- **PLL:** provides clock to the FPGA.
- CRUVI HS connectors
- MIPI SCI-2 connectors

4.3.1 I²C MUX and FPGA Peripherals

Since there are devices with conflicting I2C addresses, an I2C MUX is used to help resolve them.

To select a channel, do an I2C write with the value in the channel select column to the MUX TCA9544 (U45) at I2C address 0x70.

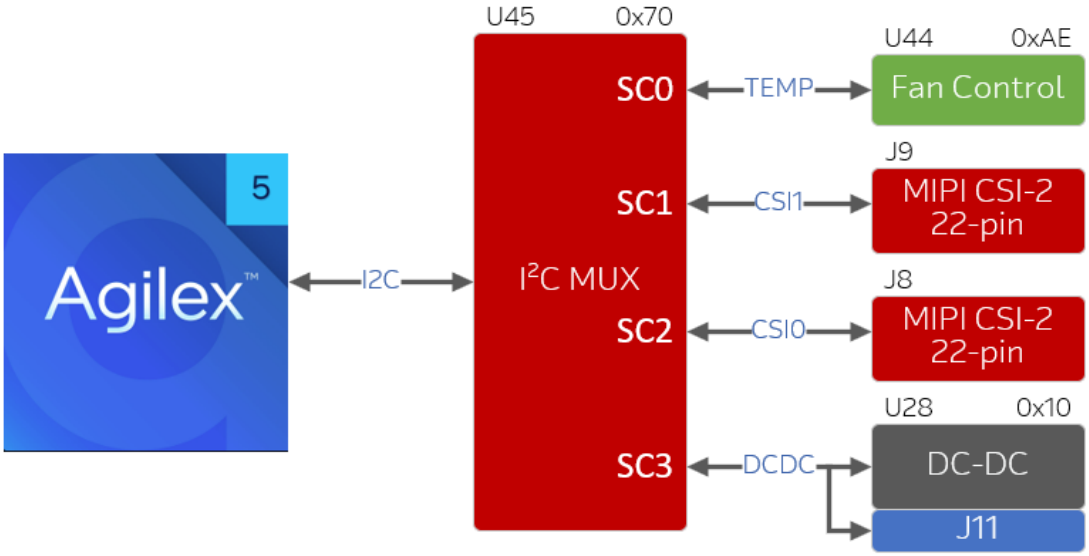

Figure 4-3 : I2C MUX Connections

4.3.1.1 I2C MUX Channel Assignment

Channel	Channel Select	Device Label	I2C Address	Device Name
0	0x04	U44	0xAE	Fan Control
1	0x05	J9	-	MIPI CSI-2 Ch 1
2	0x06	J8	-	MIPI CSI-2 Ch 0
3	0x07	U28	0x10	FS1525 DC-DC

4.3.1.2 FPGA Pin Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
I2C_SDA	PIN_AC1	Bidir	Serial Data Line	1.8-V LVCMOS
I2C_SCL	PIN_AC2	Bidir	Serial Clock Line	1.8-V LVCMOS
MUX_I2C_INT	PIN_AF1	Input	Peripheral Interrupts	1.8-V LVCMOS

For further connections of the interfaces, please refer to the section about the specific interface.

4.4 Peripherals Connected to the Agilex 5 SoC FPGA

The Agilex 5 SoC FPGA connects to various peripherals for both the FPGA and HPS parts. The versatile peripheral integration offers a flexible platform and ensures efficient and seamless system operation with the SoC FPGA, resulting in faster and smoother development cycles.

4.4.1 Configuration

There are 2 types of configuration methods supported by AXE5-Falcon:

- **JTAG Configuration**: Configuration using JTAG ports. JTAG configuration scheme allows you to directly configure the device core. The Quartus Prime software automatically generates a .sof that can be downloaded to the Agilex through the Quartus Prime Programmer. The AXE5-Falcon board uses an on-board USB Blaster III to perform FPGA configuration via the USB-C connector (J25).
- **Active Serial Configuration from QSPI flash**: Configuration using external QSPI flash. Before configuration, you need to program the configuration data .jic into the configuration flash memory which provides non-volatile storage for the bit stream. The information is retained within flash memory even if the AXE5-Falcon is turned off. When the board is powered on, the configuration data in the flash memory is automatically loaded into the Agilex 5 FPGA.

For detailed information about how to configure the Agilex 5, please refer to Chapter 7.

4.4.2 Memory Interfaces

The AXE5-Falcon development board supports an array of volatile and non-volatile interface options. From high-speed DDR4 memory to large-capacity flash memory, it provides adaptable solutions in various applications by addressing a broad spectrum of memory integration.

4.4.2.1 DDR4 memory

The AXE5-Falcon board uses DDR4 memory devices giving the user a 16 Gbit density, operating at a speed of 1600 MT/s. The memory block is comprised of 2 16-bit devices. Below are the connections and pinning of the DDR4 used in the AXE5-Falcon.

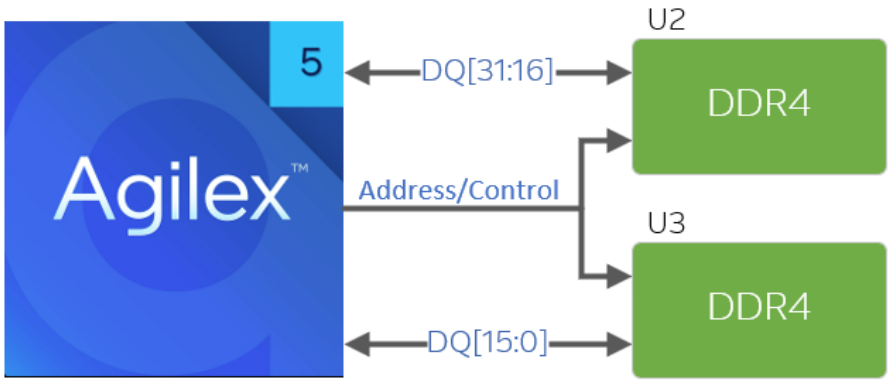

Figure 4-4 : DDR4 Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
DDR4_CLK0_P	PIN_AB48	Input	Differential clock	1.2-V True Differential Signaling
DDR4_CLK0_N	PIN_W48			
DDR4_CKE0	PIN_T59	Output	Clock enable	
DDR4_CS	PIN_T65	Output	Chip select	
DDR4_PAR	PIN_M51	Output	Parity for command/address	
DDR4_ODT0	PIN_AB56	Output	On-die Termination	
DDR4_ACT	PIN_M65	Output	Command Input	
DDR4_RESET	PIN_W62	Output	Reset_n	
DDR4_ALERT	PIN_T39	Input	Alert_n	
DDR4_BG0	PIN_E39	Output	Bank Group Address	
DDR4_BA1	PIN_G39	Output	Bank Address	
DDR4_BA0	PIN_M39	Output	Bank Address	
DDR4_A0	PIN_B66	Output	Address	
DDR4_A1	PIN_A68	Output	Address	
DDR4_A2	PIN_B68	Output	Address	
DDR4_A3	PIN_A70	Output	Address	

DDR4_A4	PIN_B63	Output	Address	
DDR4_A5	PIN_A66	Output	Address	
DDR4_A6	PIN_A61	Output	Address	
DDR4_A7	PIN_B61	Output	Address	
DDR4_A8	PIN_B58	Output	Address	
DDR4_A9	PIN_A60	Output	Address	
DDR4_A10	PIN_B55	Output	Address	
DDR4_A11	PIN_A58	Output	Address	
DDR4_A12	PIN_M48	Output	Address	
DDR4_A13	PIN_G48	Output	Address	
DDR4_A14	PIN_E48	Output	WE_n/A14	
DDR4_A15	PIN_J42	Output	CAS_n/A15	
DDR4_A16	PIN_G42	Output	RAS_n/A16	
DQ0	PIN_J65	Bidir	Data [0]	
DQ1	PIN_G65	Bidir	Data [1]	
DQ2	PIN_T62	Bidir	Data [2]	
DQ3	PIN_M62	Bidir	Data [3]	
DQ4	PIN_T56	Bidir	Data [4]	
DQ5	PIN_M56	Bidir	Data [5]	
DQ6	PIN_G56	Bidir	Data [6]	
DQ7	PIN_E56	Bidir	Data [7]	
DQ8	PIN_A50	Bidir	Data [8]	
DQ9	PIN_B50	Bidir	Data [9]	
DQ10	PIN_B53	Bidir	Data [10]	
DQ11	PIN_A55	Bidir	Data [11]	
DQ12	PIN_B41	Bidir	Data [12]	
DQ13	PIN_A43	Bidir	Data [13]	
DQ14	PIN_A38	Bidir	Data [14]	
DQ15	PIN_B38	Bidir	Data [15]	
DQ16	PIN_AB39	Bidir	Data [16]	
DQ17	PIN_W39	Bidir	Data [17]	
DQ18	PIN_M42	Bidir	Data [18]	
DQ19	PIN_T42	Bidir	Data [19]	
DQ20	PIN_AB24	Bidir	Data [20]	
DQ21	PIN_W24	Bidir	Data [21]	
DQ22	PIN_T27	Bidir	Data [22]	
DQ23	PIN_M27	Bidir	Data [23]	
DQ24	PIN_J35	Bidir	Data [24]	
DQ25	PIN_G35	Bidir	Data [25]	
DQ26	PIN_T32	Bidir	Data [26]	
DQ27	PIN_M32	Bidir	Data [27]	
DQ28	PIN_T24	Bidir	Data [28]	
DQ29	PIN_M24	Bidir	Data [29]	

DQ30	PIN_G24	Bidir	Data [30]	
DQ31	PIN_E24	Bidir	Data [31]	
DDR4_DQS0_P	PIN_G62	Bidir	Data strobe	
DDR4_DQS0_N	PIN_E62			
DDR4_DQS1_P	PIN_B45	Bidir	Data strobe	
DDR4_DQS1_N	PIN_A47			
DDR4_DQS2_P	PIN_AB32	Bidir	Data strobe	
DDR4_DQS2_N	PIN_W32			
DDR4_DQS3_P	PIN_G32	Bidir	Data strobe	
DDR4_DQS3_N	PIN_E32			
DDR4_DM0	PIN_J59	Bidir	Data mask	
DDR4_DM1	PIN_B43	Bidir	Data mask	
DDR4_DM2	PIN_T35	Bidir	Data mask	
DDR4_DM3	PIN_J27	Bidir	Data mask	

4.4.2.2 MicroSD Card

The AXE5-Falcon board features a microSD card interface with x4 data lanes, primarily designed to function as an external storage solution for the HPS. The SD card can also be utilized for booting purposes, allowing for firmware execution directly from the card. Additionally, the SD card socket is equipped with a Card Detect pin, facilitating automatic detection of card insertion or removal, enhancing system responsiveness and user convenience.

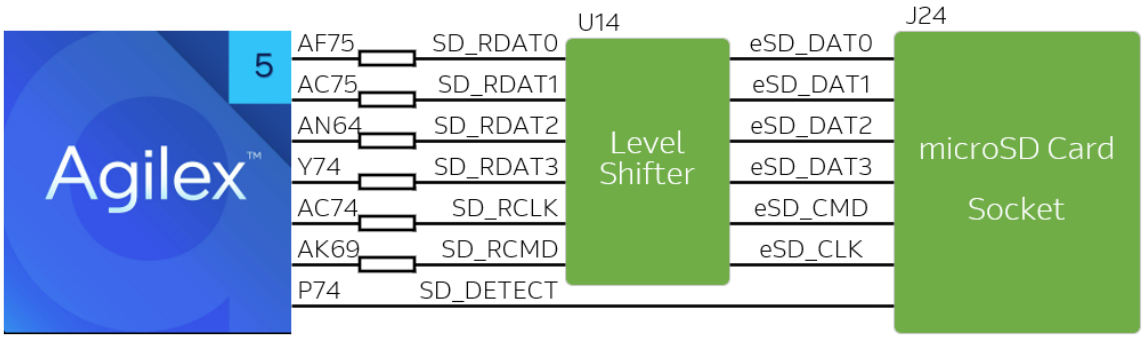

Figure 4-5 : MicroSD Card Socket Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
HPS_IOB1/SD_RDAT0	PIN_AF75	Bidir	Data line [0]	1.8-V
HPS_IOB2/SD_RDAT1	PIN_AC75	Bidir	Data line [1]	1.8-V
HPS_IOB6/SD_RDAT2	PIN_AN64	Bidir	Data line [2]	1.8-V
HPS_IOB7/SD_RDAT3	PIN_Y74	Bidir	Data line [3]	1.8-V
HPS_IOB8/SD_RCMD	PIN_AK69	Bidir	Command line	1.8-V
HPS_IOB3/SD_RCLK	PIN_AC74	Output	SD Clock	1.8-V
HPS_GPIO1_IO11/SD_DETECT	PIN_P74	Input	HPS GPIO for Card detect pin	1.8-V

4.4.3 Data Communication Interfaces

The AXE5-Falcon development board offers various data communication interfaces, including Ethernet, USB 3.1, and HDMI, ensuring high-level integration in an extensive range of applications.

4.4.3.1 10/100/1000 Ethernet PHY

The development kit is equipped with one standard RJ45-connected Gigabit Ethernet port using an external Microchip KSZ9301 PHY chip.

The MAC-to-PHY interface is configured to an RGMII interface connections with MDIO interface for management.

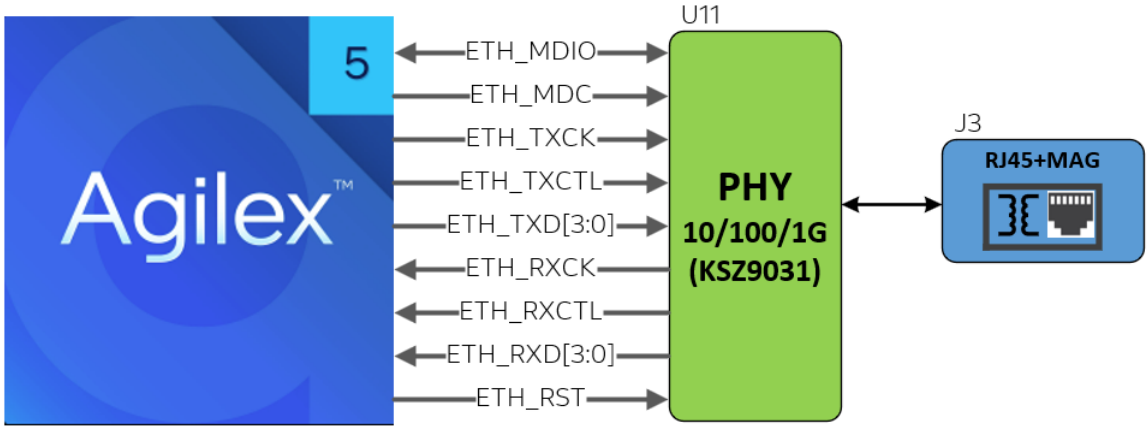

Figure 4-6 : Connections between the Agilex-5 and Ethernet PHY

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
ETH_MDIO	PIN_U74	Bidir	Management Data	1.8-V LVCMOS
ETH_MDC	PIN_AK67	Output	Management Clock	1.8-V LVCMOS
ETH_TXCK	PIN_L75	Output	Transmit Clock	1.8-V LVCMOS

ETH_TXCTL	PIN_N72	Output	Transmit Control Signal	1.8-V LVCMOS
ETH_TXD0	PIN_F75	Output	Transmit data [0]	1.8-V LVCMOS
ETH_TXD1	PIN_AD71	Output	Transmit data [1]	1.8-V LVCMOS
ETH_TXD2	PIN_F74	Output	Transmit data [2]	1.8-V LVCMOS
ETH_TXD3	PIN_AA71	Output	Transmit data [3]	1.8-V LVCMOS
ETH_RXCK	PIN_N71	Input	Receive Clock	1.8-V LVCMOS
ETH_RXCTL	PIN_AD72	Input	Receive Control Signal	1.8-V LVCMOS
ETH_RXD0	PIN_K71	Input	Receive data [0]	1.8-V LVCMOS
ETH_RXD1	PIN_AK71	Input	Receive data [1]	1.8-V LVCMOS
ETH_RXD2	PIN_C74	Input	Receive data [2]	1.8-V LVCMOS
ETH_RXD3	PIN_D71	Input	Receive data [3]	1.8-V LVCMOS
ETH_RST	PIN_P75	Output	PHY Reset	1.8-V LVCMOS

4.4.3.2 HDMI Transmitter

The development board provides a High Performance HDMI Transmitter via the Texas Instruments TFP410PAP, which supports pixel rates up to 165MHz including 1080p and WUXGA at 60Hz. The TFP410PAP is controlled via a serial I²C bus interface (See Section 4.2), which is connected to the Agilex 5 SoC FPGA.

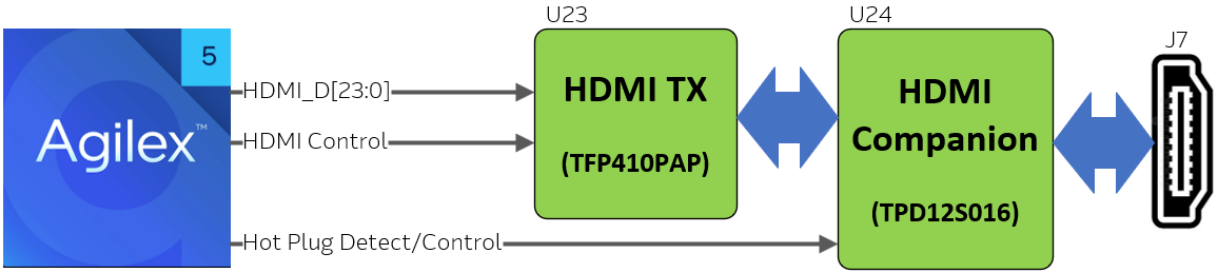

Figure 4-7 : HDMI Transmitter Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
HDMI_VS	PIN_DC1	Output	Vertical Synchronization	3.3-V LVCMOS
HDMI_HS	PIN_DH1	Output	Horizontal Synchronization	3.3-V LVCMOS
HDMI_CLK	PIN_CE19	Output	Video Pixel Clock	3.3-V LVCMOS
HDMI_DE	PIN_DE1	Output	Data Enable Signal for Digital Video	3.3-V LVCMOS
HDMI_D0	PIN_DH2	Output	Video Data bus [0]	3.3-V LVCMOS
HDMI_D1	PIN_DC2	Output	Video Data bus [1]	3.3-V LVCMOS
HDMI_D2	PIN_CV4	Output	Video Data bus [2]	3.3-V LVCMOS
HDMI_D3	PIN_CV6	Output	Video Data bus [3]	3.3-V LVCMOS
HDMI_D4	PIN_CV11	Output	Video Data bus [4]	3.3-V LVCMOS
HDMI_D5	PIN_CV14	Output	Video Data bus [5]	3.3-V LVCMOS
HDMI_D6	PIN_CV16	Output	Video Data bus [6]	3.3-V LVCMOS
HDMI_D7	PIN_CV19	Output	Video Data bus [7]	3.3-V LVCMOS
HDMI_D8	PIN_CR11	Output	Video Data bus [8]	3.3-V LVCMOS
HDMI_D9	PIN_CR14	Output	Video Data bus [9]	3.3-V LVCMOS
HDMI_D10	PIN_CR19	Output	Video Data bus [10]	3.3-V LVCMOS
HDMI_D11	PIN_CH16	Output	Video Data bus [11]	3.3-V LVCMOS
HDMI_D12	PIN_CH19	Output	Video Data bus [12]	3.3-V LVCMOS
HDMI_D13	PIN_CH14	Output	Video Data bus [13]	3.3-V LVCMOS
HDMI_D14	PIN_CG23	Output	Video Data bus [14]	3.3-V LVCMOS
HDMI_D15	PIN_CE14	Output	Video Data bus [15]	3.3-V LVCMOS
HDMI_D16	PIN_CG26	Output	Video Data bus [16]	3.3-V LVCMOS
HDMI_D17	PIN_CD23	Output	Video Data bus [17]	3.3-V LVCMOS
HDMI_D18	PIN_CH4	Output	Video Data bus [18]	3.3-V LVCMOS
HDMI_D19	PIN_CA23	Output	Video Data bus [19]	3.3-V LVCMOS

HDMI_D20	PIN_BV11	Output	Video Data bus [20]	3.3-V LVCMOS
HDMI_D21	PIN_BV19	Output	Video Data bus [21]	3.3-V LVCMOS
HDMI_D22	PIN_BV16	Output	Video Data bus [22]	3.3-V LVCMOS
HDMI_D23	PIN_BV14	Output	Video Data bus [23]	3.3-V LVCMOS
HDMI_PD	PIN_DM2	Output	Power Down – active-low	3.3-V LVCMOS
HDMI_SDA	PIN_DD3	Bidir	Serial Data Line	3.3-V LVCMOS
HDMI_SCL	PIN_CR8	Bidir	Serial Clock Line	3.3-V LVCMOS
CT_HPD	PIN_DN2	Output	Hot Plug Detect Control	3.3-V LVCMOS

4.4.3.3 USB 2.0

The AXE5-Falcon board features a Microchip's USB2514B USB Hub that offers a total of four

USB-A connectivity options. This USB Hub is fully compliant with the USB 2.0 specification and supports High Speed, Full Speed and Low-Speed USB signalling.

The USB 2.0 controller within the HPS is interfaced with a USB PHY via ULPI, establishing a connection to the upstream port of the USB Hub.

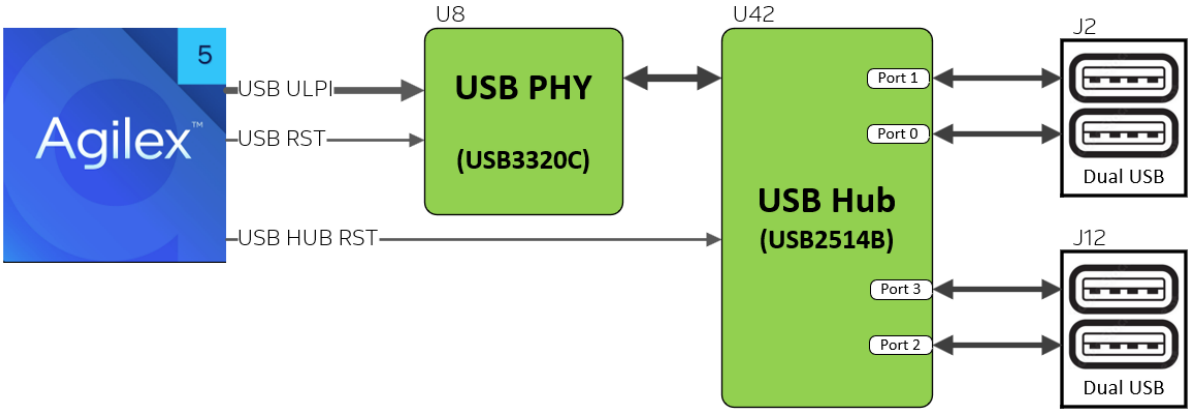

Figure 4-8 : USB Connection for Agilex-5 SoC FPGA

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
USB_CLK	PIN_BC64	Bidir	ULPI Clock	1.8-V
USB_STP	PIN_BC67	Output	ULPI STP signal	1.8-V
USB_DIR	PIN_AY67	Input	Direction of ULPI	1.8-V
USB_NXT	PIN_BA75	Input	ULPI NXT signal	1.8-V
USB_DATA0	PIN_AN72	Bidir	ULPI data bus [0]	1.8-V
USB_DATA1	PIN_AY69	Bidir	ULPI data bus [1]	1.8-V
USB_DATA2	PIN_BC71	Bidir	ULPI data bus [2]	1.8-V
USB_DATA3	PIN_AU74	Bidir	ULPI data bus [3]	1.8-V
USB_DATA4	PIN_AY71	Bidir	ULPI data bus [4]	1.8-V
USB_DATA5	PIN_AU75	Bidir	ULPI data bus [5]	1.8-V
USB_DATA6	PIN_BC72	Bidir	ULPI data bus [6]	1.8-V
USB_DATA7	PIN_BP74	Bidir	ULPI data bus [7]	1.8-V
USB_RST	PIN_AY75	Output	USB PHY Reset (HPS_GPIO1_IO4)	1.8-V
USB_HUB_RST	PIN_BJ23	Output	USB Hub reset (FPGA pin)	3.3-V LVCMOS

4.4.3.4 USB to UART Bridge

Besides the USB 2.0 interfaces from the HPS, the AXE5-Falcon board uses an additional FT4232H chip to perform UART communication over USB. The FTDI chip converts signals from dual USB 2.0 to standard UART interfaces, which is routed to the HPS UART0 and DBG_UART (FPGA Fabric) modules.

The USB to UART Bridge communicates over the USB-C connector labelled as J25.

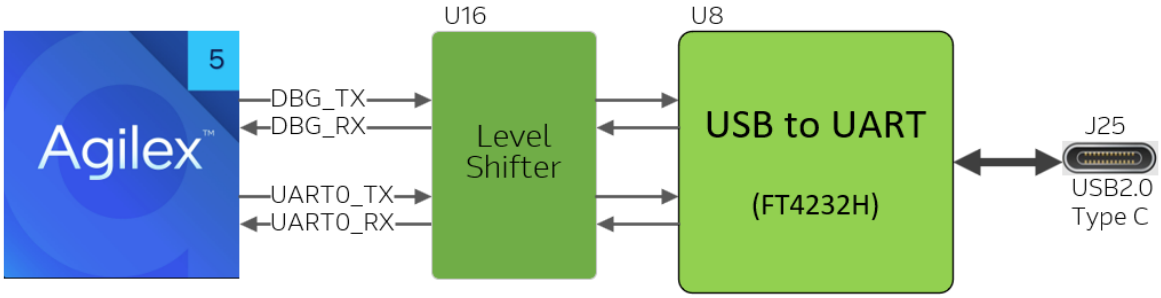

Figure 4-9 : FTDI Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
UART0_RX	PIN_AJ75	Input	HPS UART0 Rx pin	1.8-V
UART0_TX	PIN_AJ74	Output	HPS UART0 Tx pin	1.8-V
DBG_RX	PIN_AJ1	Input	FPGA UART Rx pin	1.8-V LVCMOS
DBG_TX	PIN_AJ2	Output	FPGA UART Tx pin	1.8-V LVCMOS

4.4.4 Expansion Connectors

The AXE5-Falcon development kit features expansion options with support for PMOD, Pi Hat, MIPI CSI-2, CRUVI HS, and CRUVI LS connectors. This flexibility allows users to easily integrate additional peripherals, functionalities, and customize the development environment to their specific needs.

4.4.4.1 PMOD

The AXE5-Falcon development board supports a dual row PMOD connection.

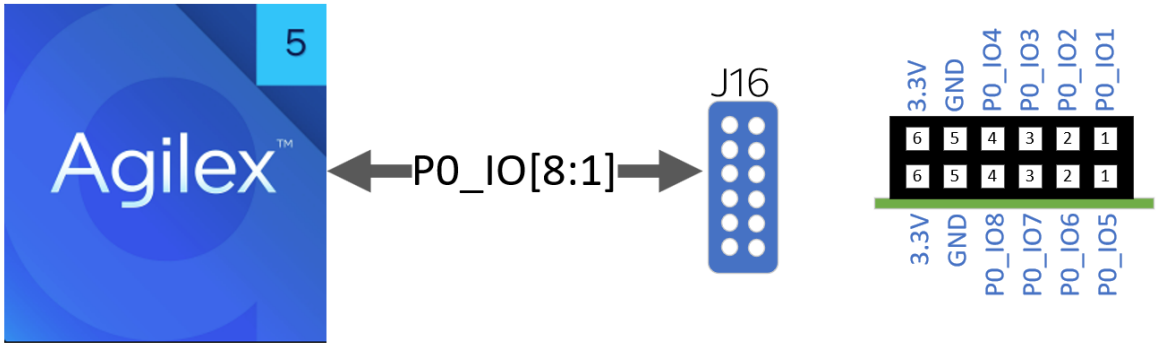

Figure 4-10 : PMOD Connection

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
P0_IO1	PIN_AH11	Bidir	Upper Row pin 1	3.3-V LVCMOS
P0_IO2	PIN_AE8	Bidir	Upper Row pin 2	3.3-V LVCMOS
P0_IO3	PIN_AE6	Bidir	Upper Row pin 3	3.3-V LVCMOS
P0_IO4	PIN_V4	Bidir	Upper Row pin 4	3.3-V LVCMOS
P0_IO5	PIN_AH14	Bidir	Lower Row pin 1	3.3-V LVCMOS
P0_IO6	PIN_V6	Bidir	Lower Row pin 2	3.3-V LVCMOS
P0_IO7	PIN_V11	Bidir	Lower Row pin 3	3.3-V LVCMOS
P0_IO8	PIN_AG23	Bidir	Lower Row pin 4	3.3-V LVCMOS

4.4.4.2 CRUVI High Speed Connectors

The AXE5-Falcon board features three CRUVI HS connectors. CRUVI is an open ecosystem, low-pin-count interface solution that enables the integration of a wide range of peripherals into the system, accommodating both high-speed signalling and support for low-speed device interfaces at the same time. CRUVI HS allows the connection of high-speed interfaces such as Gigabit Ethernet, camera, and other types of multimedia peripherals.

The AXE5-Falcon board provides 5.0 V, 3.3 V, 1.8V on one of them, an VCCIO_2A_B on the other two, through CRUVI HS connectors. The power control of the VCCIO_2A_B power rail is managed by the U21 DCDC regulator. This rail powers the VADJ pin 36 of J1 and J21 connectors, as well as the 2A_B I/O half bank of Agilex 5 SoC FPGA. The FPGA I/O standards of the CRUVI HS ports can be adjusted by configuring n FPGA pin (SEL_1V3).

For custom add-on cards with CRUVI HS interface, the recommended counterpart for the connector is ST4-30-1.50-L-D-P from Samtec.

For hardware module mounting, use M2x6mm pan head Philips drive screw.

Below is the connection diagram and pinning information.

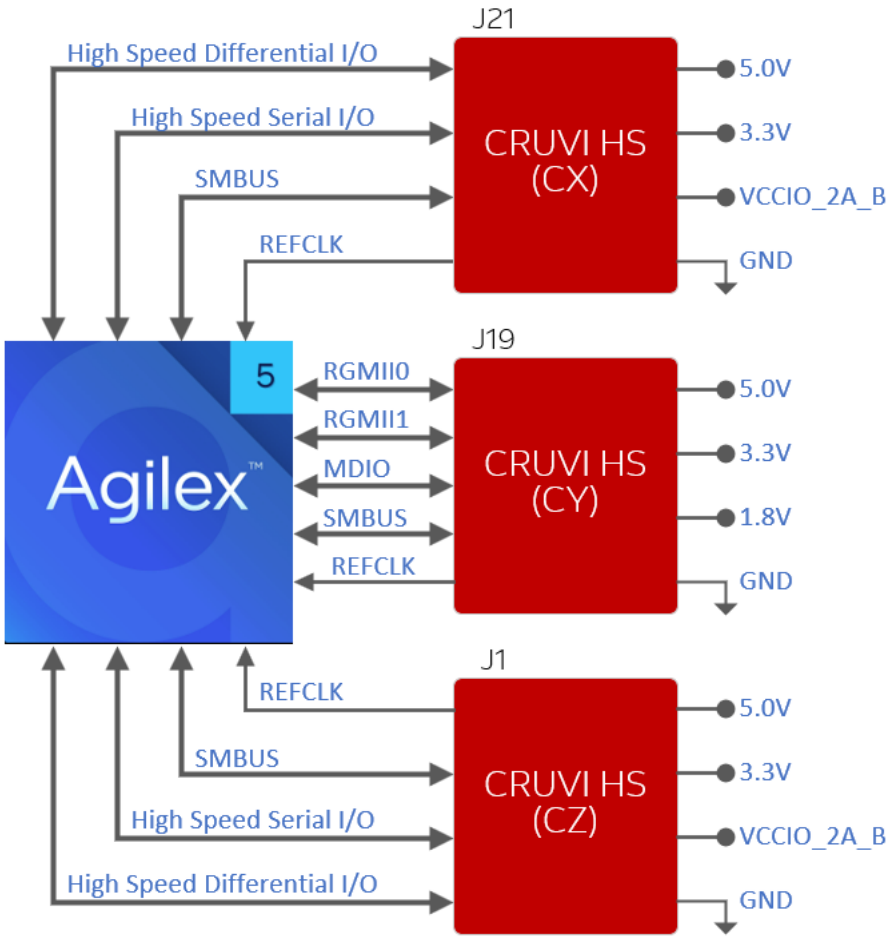

Figure 4-11 : CRUVI-HS Connections

CRUVI HS CX Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CX_A0_P	PIN_DP60	14	Bidir	HS Differential Data A[0]_p	Adjustable[1]
CX_A0_N	PIN_DN58	16	Bidir	HS Differential Data A[0]_n	Adjustable[1]
CX_A1_P	PIN_DP70	20	Bidir	HS Differential Data A[1]_p	Adjustable[1]
CX_A1_N	PIN_DN68	22	Bidir	HS Differential Data A[1]_n	Adjustable[1]
CX_A2_P	PIN_DN73	26	Bidir	HS Differential Data A[2]_p	Adjustable[1]
CX_A2_N	PIN_DN74	28	Bidir	HS Differential Data A[2]_n	Adjustable[1]
CX_A3_P	PIN_DP66	32	Bidir	HS Differential Data A[3]_p	Adjustable[1]
CX_A3_N	PIN_DN63	34	Bidir	HS Differential Data A[3]_n	Adjustable[1]
CX_A4_P	PIN_DJ27	38	Bidir	HS Differential Data A[4]_p	Adjustable[2]
CX_A4_N	PIN_DF27	40	Bidir	HS Differential Data A[4]_n	Adjustable[2]
CX_A5_P	PIN_DP68	44	Bidir	HS Differential Data A[5]_p	Adjustable[1]
CX_A5_N	PIN_DN66	46	Bidir	HS Differential Data A[5]_n	Adjustable[1]

CX_B0_P	PIN_DK39	15	Bidir	HS Differential Data B[0]_p	Adjustable[1]
CX_B0_N	PIN_DJ39	17	Bidir	HS Differential Data B[0]_n	Adjustable[1]
CX_B1_P	PIN_DP61	21	Bidir	HS Differential Data B[1]_p	Adjustable[1]
CX_B1_N	PIN_DN61	23	Bidir	HS Differential Data B[1]_n	Adjustable[1]
CX_B2_P	PIN_DK32	27	Bidir	HS Differential Data B[2]_p	Adjustable[2]
CX_B2_N	PIN_DJ32	29	Bidir	HS Differential Data B[2]_n	Adjustable[2]
CX_B3_P	PIN_DJ35	33	Bidir	HS Differential Data B[3]_p	Adjustable[2]
CX_B3_N	PIN_DF35	35	Bidir	HS Differential Data B[3]_n	Adjustable[2]
CX_B4_P	PIN_DD35	39	Bidir	HS Differential Data B[4]_p	Adjustable[2]
CX_B4_N	PIN_DD32	41	Bidir	HS Differential Data B[4]_n	Adjustable[2]
CX_B5_P	PIN_DD27	45	Bidir	HS Differential Data B[5]_p	Adjustable[2]
CX_B5_N	PIN_DD24	47	Bidir	HS Differential Data B[5]_n	Adjustable[2]
CX_HSI	PIN_DP47	10	Input	HS Serial In	Adjustable[1]
CX_HSIO	PIN_DJ42	2	Bidir	HS Serial Data I/O	Adjustable[1]
CX_HSO	PIN_DF42	6	Output	HS Serial Out	Adjustable[1]
CX_RESET	PIN_DN43	8	Output	Serial Reset	Adjustable[1]
CX_SMB_ALERT	PIN_CE8	3	Input	SMBus interrupt signal	3.3-V LVCMOS
CX_SMB_SDA	PIN_DJ3	5	Bidir	SMBus Data Line	3.3-V LVCMOS
CX_SMB_SCL	PIN_CE6	7	Bidir	SMBus Data Clock Line	3.3-V LVCMOS
CX_REFCLK	PIN_CH6	11	Input	Clock Input	3.3-V LVCMOS
5V	-	60	PWR	5V power to the connector	-
3.3V	-	4, 9	PWR	3.3V power to the connector	-
VCCIO_2A_B	-	36	PWR	HS IO Bank voltage	[1]
GND	-	12, 13, 18, 19, 24, 25, 30, 31, 37, 42, 43, 48, 49, 54	PWR	Ground to the connector	-
n.c.	-	1, 50, 51, 52, 53, 55, 56, 57, 58, 59	-	Not connected	-

[1] *"1.2V True Differential Signalling" or "1.3V True Differential Signalling". Depending on CRUVI_ADJ*

[2] J17*selects "1.2V True Differential Signalling" or "1.2V/1.3V True Differential Signalling", depending on SEL_1V3*

CRUVI HS CY Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
RGMII1_RXD0	PIN_BD2	14	Bidir	HS Differential Data A[0]_p	1.8-V LVCMOS
RGMII1_RXD1	PIN_BD1	16	Bidir	HS Differential Data A[0]_n	1.8-V LVCMOS
RGMII1_TXD0	PIN_BL2	20	Bidir	HS Differential Data A[1]_p	1.8-V LVCMOS
RGMII1_TXD1	PIN_BL1	22	Bidir	HS Differential Data A[1]_n	1.8-V LVCMOS

RGMII1_TXD2	PIN_BH4	26	Bidir	HS Differential Data A[2]_p	1.8-V LVCMOS
RGMII1_TXD3	PIN_BG2	28	Bidir	HS Differential Data A[2]_n	1.8-V LVCMOS
RGMII0_TXD2	PIN_CU2	32	Bidir	HS Differential Data A[3]_p	1.8-V LVCMOS
RGMII0_TXD3	PIN_BV6	34	Bidir	HS Differential Data A[3]_n	1.8-V LVCMOS
RGMII0_RXD0	PIN_CP1	38	Bidir	HS Differential Data A[4]_p	1.8-V LVCMOS
RGMII0_RXD1	PIN_CP2	40	Bidir	HS Differential Data A[4]_n	1.8-V LVCMOS
RGMII1_RX_CK	PIN_AP1	44	Bidir	HS Differential Data A[5]_p	1.8-V LVCMOS
RGMII1_RX_CTL	PIN_AP2	46	Bidir	HS Differential Data A[5]_n	1.8-V LVCMOS
RGMII1_RDX2	PIN_BH6	15	Bidir	HS Differential Data B[0]_p	1.8-V LVCMOS
RGMII1_RXD3	PIN_BA1	17	Bidir	HS Differential Data B[0]_n	1.8-V LVCMOS
RGMII0_TX_CK	PIN_CJ1	21	Bidir	HS Differential Data B[1]_p	1.8-V LVCMOS
RGMII0_TX_CTL	PIN_CJ2	23	Bidir	HS Differential Data B[1]_n	1.8-V LVCMOS
RGMII0_RX_CK	PIN_CF2	27	Bidir	HS Differential Data B[2]_p	1.8-V LVCMOS
RGMII0_RX_CTL	PIN_CF1	29	Bidir	HS Differential Data B[2]_n	1.8-V LVCMOS
RGMII0_RXD2	PIN_CM1	33	Bidir	HS Differential Data B[3]_p	1.8-V LVCMOS
RGMII0_RXD3	PIN_BV4	35	Bidir	HS Differential Data B[3]_n	1.8-V LVCMOS
RGMII0_TXD0	PIN_DA1	39	Bidir	HS Differential Data B[4]_p	1.8-V LVCMOS
RGMII0_TXD1	PIN_DA2	41	Bidir	HS Differential Data B[4]_n	1.8-V LVCMOS
RGMII1_TX_CK	PIN_AP1	45	Bidir	HS Differential Data B[5]_p	1.8-V LVCMOS
RGMII1_TX_CTL	PIN_AU1	47	Bidir	HS Differential Data B[5]_n	1.8-V LVCMOS
RGMII_IRQ	PIN_BW2	10	Input	HS Serial In	3.3-V LVCMOS
RGMII_MDIO	PIN_CB2	2	Bidir	HS Serial Data I/O	3.3-V LVCMOS
RGMII_MDC	PIN_BW1	6	Output	HS Serial Out	3.3-V LVCMOS
RGMII_RESET	PIN_BR6	8	Output	Serial Reset	3.3-V LVCMOS
CY_SMB_ALERT	PIN_BU23	3	Input	SMBus interrupt signal	3.3-V LVCMOS
CY_SMB_SDA	PIN_BE19	5	Bidir	SMBus Data Line	3.3-V LVCMOS
CY_SMB_SCL	PIN_AV19	7	Bidir	SMBus Data Clock Line	3.3-V LVCMOS
CY_REFCLK	PIN_BH14	11	Input	Clock Input	3.3-V LVCMOS
5V	-	60	PWR	5V power to the connector	-
3.3V	-	4, 9	PWR	3.3V power to the connector	-
1V8	-	36	PWR	HS IO Bank voltage (1.8V)	-
GND	-	12, 13, 18, 19, 24, 25, 30, 31, 37, 42, 43, 48, 49, 54	PWR	Ground to the connector	-
n.c.	-	1, 50, 51, 52, 53, 55, 56, 57, 58, 59	-	Not connected	-

CRUVI HS CZ Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CZ_A0_P	PIN_DK56	14	Bidir	HS Differential Data A[0]_p	Adjustable[1]
CZ_A0_N	PIN_DJ56	16	Bidir	HS Differential Data A[0]_n	Adjustable[1]
CZ_A1_P	PIN_DJ65	20	Bidir	HS Differential Data A[1]_p	Adjustable[1]
CZ_A1_N	PIN_DF65	22	Bidir	HS Differential Data A[1]_n	Adjustable[1]
CZ_A2_P	PIN_DD65	26	Bidir	HS Differential Data A[2]_p	Adjustable[1]
CZ_A2_N	PIN_DD62	28	Bidir	HS Differential Data A[2]_n	Adjustable[1]
CZ_A3_P	PIN_DJ59	32	Bidir	HS Differential Data A[3]_p	Adjustable[1]
CZ_A3_N	PIN_DF59	34	Bidir	HS Differential Data A[3]_n	Adjustable[1]
CZ_A4_P	PIN_DP30	38	Bidir	HS Differential Data A[4]_p	Adjustable[2]
CZ_A4_N	PIN_DN28	40	Bidir	HS Differential Data A[4]_n	Adjustable[2]
CZ_A5_P	PIN_DK62	44	Bidir	HS Differential Data A[5]_p	Adjustable[1]
CZ_A5_N	PIN_DJ62	46	Bidir	HS Differential Data A[5]_n	Adjustable[1]
CZ_B0_P	PIN_DP23	15	Bidir	HS Differential Data B[0]_p	Adjustable[2]
CZ_B0_N	PIN_DN22	17	Bidir	HS Differential Data B[0]_n	Adjustable[2]
CZ_B1_P	PIN_DD59	21	Bidir	HS Differential Data B[1]_p	Adjustable[1]
CZ_B1_N	PIN_DD56	23	Bidir	HS Differential Data B[1]_n	Adjustable[1]
CZ_B2_P	PIN_DP33	27	Bidir	HS Differential Data B[2]_p	Adjustable[2]
CZ_B2_N	PIN_DN30	29	Bidir	HS Differential Data B[2]_n	Adjustable[2]
CZ_B3_P	PIN_DP36	33	Bidir	HS Differential Data B[3]_p	Adjustable[2]
CZ_B3_N	PIN_DN33	35	Bidir	HS Differential Data B[3]_n	Adjustable[2]
CZ_B4_P	PIN_DP38	39	Bidir	HS Differential Data B[4]_p	Adjustable[2]
CZ_B4_N	PIN_DN38	41	Bidir	HS Differential Data B[4]_n	Adjustable[2]
CZ_B5_P	PIN_DP25	45	Bidir	HS Differential Data B[5]_p	Adjustable[2]
CZ_B5_N	PIN_DN25	47	Bidir	HS Differential Data B[5]_n	Adjustable[2]
CZ_HSI	PIN_DJ51	10	Input	HS Serial In	Adjustable[1]
CZ_HSIO	PIN_DJ48	2	Bidir	HS Serial Data I/O	Adjustable[1]
CZ_HSO	PIN_DK48	6	Output	HS Serial Out	Adjustable[1]
CZ_RESET	PIN_DD48	8	Output	Serial Reset	Adjustable[1]
CZ_SMB_ALERT	PIN_AV14	3	Input	SMBus interrupt signal	3.3-V LVCMOS
CZ_SMB_SDA	PIN_AV16	5	Bidir	SMBus Data Line	3.3-V LVCMOS
CZ_SMB_SCL	PIN_AV11	7	Bidir	SMBus Data Clock Line	3.3-V LVCMOS
CZ_REFCLK	PIN_BF23	11	Input	Clock Input	3.3-V LVCMOS
5V	-	60	PWR	5V power to the connector	-
3.3V	-	4, 9	PWR	3.3V power to the connector	-
VCCIO_2A_B	-	36	PWR	HS IO Bank voltage	[1]

GND	-	12, 13, 18, 19, 24, 25, 30, 31, 37, 42, 43, 48, 49, 54	PWR	Ground to the connector	-
n.c.	-	1, 50, 51, 52, 53, 55, 56, 57, 58, 59	-	Not connected	-

[1] *"1.2V True Differential Signalling" or "1.3V True Differential Signalling". Depending on CRUVI_ADJ*

[2] J17 *selects "1.2V True Differential Signalling" or "1.2V/1.3V True Differential Signalling", depending on SEL_1V3*

4.4.4.3 CRUVI Low-Speed Connectors

CRUVI LS is the low-speed version of the CRUVI ecosystem that provides a connection for the simple peripheral modules. It features a simple 2mm-pitch layout with standard pins for power, ground, and several digital I/O signals. It offers an array of ready-to-use modules for easy prototyping and extends functional capabilities. This compact interface simplifies the connection of sensors, communication devices, and other components.

Delivering power to the mezzanine board, the AXE5-Falcon board offers both 5.0 V and 3.3 V via the CRUVI LS port.

The AXE5-Falcon development board provides one CRUVI LS interface.

For custom add-on cards with CRUVI LS interface, the recommended counterpart for the connector is TMMH-106-04-F-DV-A-M from Samtec.

For hardware module mounting, use M2x6mm pan head Philips drive screw.

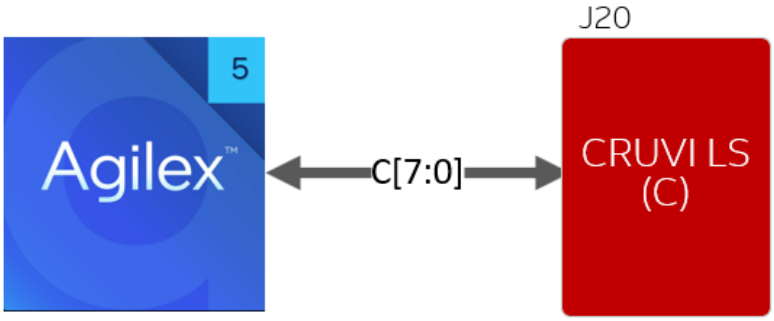

Figure 4-12 : CRUVI-LS Connections

CRUVI LS C Connections

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
C0	PIN_BE11	3	Bidir	CRUVI LS Data [0]	3.3-V LVCMOS
C1	PIN_BR11	5	Bidir	CRUVI LS Data [1]	3.3-V LVCMOS
C2	PIN_BH16	7	Bidir	CRUVI LS Data [2]	3.3-V LVCMOS
C3	PIN_BH19	9	Bidir	CRUVI LS Data [3]	3.3-V LVCMOS
C4	PIN_BR19	4	Bidir	CRUVI LS Data [4]	3.3-V LVCMOS
C5	PIN_BH11	8	Bidir	CRUVI LS Data [5]	3.3-V LVCMOS
C6	PIN_BE14	1	Bidir	CRUVI LS Data [6]	3.3-V LVCMOS
C7	PIN_BR14	2	Bidir	CRUVI LS Data [7]	3.3-V LVCMOS
5.0V	-	12	PWR	5V power to the connector	-
3.3V	-	10	PWR	3.3V power to the connector	-
GND	-	8	PWR	Ground to the connector	-
n.c.	-	11	-	Not connected	-

4.4.4.4 MIPI CSI-2

MIPI interface is a high-speed serial interface standard designed for efficient data transfer between components like cameras, displays, and sensors. The Altera Agilex 5 FPGA and SoCs support native MIPI IP D-PHY. The MIPI D-PHY implements MIPI transmit and receive interfaces, enabling the Camera Serial Interface (CSI-2) and the Display Serial Interface (DSI-2) at a data rate of 2.5 Gbps per lane.

The AXE5-Falcon board has two standalone connections for MIPI CSI-2 interface, which are accessible through 22-pin ZIF FPC connectors. They support an interface with 1-Clock and up to 4-Data lanes.

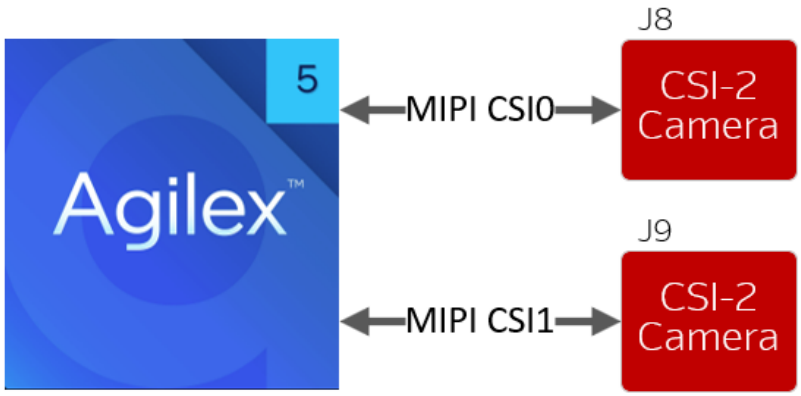

Figure 4-13 : MIPI D-PHY Connections

MIPI CSI0 (J8) Connections

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CSI0_D0_N	PIN_DN17	21	Input	Camera Data Lane 0	Adjustable[2]
CSI0_D0_P	PIN_DP20	20	Input	Camera Data Lane 0	Adjustable[2]
CSI0_D1_N	PIN_DN20	18	Input	Camera Data Lane 1	Adjustable[2]
CSI0_D1_P	PIN_DP22	17	Input	Camera Data Lane 1	Adjustable[2]
CSI0_C_N	PIN_DN15	15	Input	Camera Clock Lane	Adjustable[2]
CSI0_C_P	PIN_DP15	14	Input	Camera Clock Lane	Adjustable[2]
CSI0_D2_N	PIN_DP13	12	Input	Camera Data Lane 2	Adjustable[2]
CSI0_D2_P	PIN_DP10	11	Input	Camera Data Lane 2	Adjustable[2]
CSI0_D3_N	PIN_DN10	9	Input	Camera Data Lane 3	Adjustable[2]
CSI0_D3_P	PIN_DP7	8	Input	Camera Data Lane 3	Adjustable[2]
CSI0_GPIO0	PIN_AE11	6	Bidir	Camera GPIO0	3.3-V LVCMOS
CSI0_GPIO1	PIN_R6	5	Bidir	Camera GPIO1	3.3-V LVCMOS
CSI0_SCL	[3]	3	Bidir	Camera SMBUS	3.3-V LVCMOS
CS0_SDA	[3]	2	Bidir	Camera SMBUS	3.3-V LVCMOS
3.3V	-	1	PWR	3.3V power to the connector	-
GND	-	F1, F2, 4, 7, 10,	PWR	Ground to the connector	-

		13,16, 19, 22			

[2] *J17 selects "1.2V True Differential Signalling" or "1.2V/1.3V True Differential Signalling". Depending on SEL_1V3*
[3] *See* I²C MUX and FPGA Peripherals *Channel 2*

MIPI CSI1 (J9) Connections

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
CSI1_D0_N	PIN_DF21	21	Input	Camera Data Lane 0	Adjustable[2]
CSI1_D0_P	PIN_DJ21	20	Input	Camera Data Lane 0	Adjustable[2]
CSI1_D1_N	PIN_DD18	18	Input	Camera Data Lane 1	Adjustable[2]
CSI1_D1_P	PIN_DD21	17	Input	Camera Data Lane 1	Adjustable[2]
CSI1_C_N	PIN_DJ18	15	Input	Camera Clock Lane	Adjustable[2]
CSI1_C_P	PIN_DK18	14	Input	Camera Clock Lane	Adjustable[2]
CSI1_D2_N	PIN_DF12	12	Input	Camera Data Lane 2	Adjustable[2]
CSI1_D2_P	PIN_DJ12	11	Input	Camera Data Lane 2	Adjustable[2]
CSI1_D3_N	PIN_DD9	9	Input	Camera Data Lane 3	Adjustable[2]
CSI1_D3_P	PIN_DD12	8	Input	Camera Data Lane 3	Adjustable[2]
CSI1_GPIO0	PIN_AV6	6	Bidir	Camera GPIO0	3.3-V LVCMOS
CSI1_GPIO1	PIN_AV4	5	Bidir	Camera GPIO1	3.3-V LVCMOS
CSI1_SCL	[3]	3	Bidir	Camera SMBUS	3.3-V LVCMOS
CS1_SDA	[3]	2	Bidir	Camera SMBUS	3.3-V LVCMOS
3.3V	-	1	PWR	3.3V power to the connector	-
GND	-	F1, F2, 4, 7, 10, 13,16, 19, 22	PWR	Ground to the connector	-

[2] *J17 selects "1.2V True Differential Signalling" or "1.2V/1.3V True Differential Signalling" depending on SEL_1V3*
[3] *See* I²C MUX and FPGA Peripherals *Channel 1*

4.4.5 Pi Hat

The AXE5-Falcon development kit provides a 40-pin Pi Hat header for additional I/O expansion.

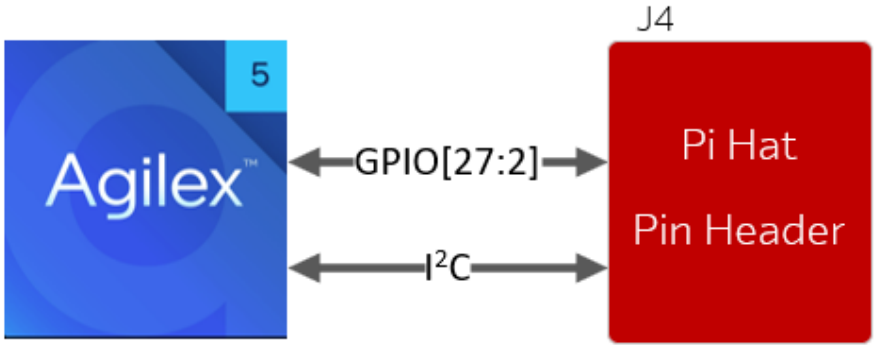

Figure 4-14 : Pi Hat Connections

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
GPIO2	PIN_C14	3	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO3	PIN_A13	5	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO4	PIN_C11	7	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO5	PIN_P2	29	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO6	PIN_P1	31	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO7	PIN_B5	26	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO8	PIN_A10	24	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO9	PIN_B15	21	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO10	PIN_B2	19	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO11	PIN_C8	23	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO12	PIN_F2	32	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO13	PIN_U2	33	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO14	PIN_A15	8	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO15	PIN_B10	10	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO16	PIN_V16	36	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO17	PIN_H16	11	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO18	PIN_B3	12	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO19	PIN_Y1	35	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO20	PIN_Y2	38	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO21	PIN_C2	40	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO22	PIN_H14	15	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO23	PIN_H6	16	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO24	PIN_H4	18	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO25	PIN_R14	22	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO26	PIN_AH16	37	Bidir	General Purpose I/O	3.3-V LVCMOS
GPIO27	PIN_H11	13	Bidir	General Purpose I/O	3.3-V LVCMOS
ID_SCL	PIN_L1	28	Bidir	I^2C Clock	3.3-V LVCMOS
ID_SDA	PIN_C6	27	Bidir	I^2C Data	3.3-V LVCMOS
3V3	-	1, 17		3.3V power to the connector	
5V	-	2,4	PWR	5.0V power to the connector	-
GND	-	6, 9, 14, 20, 25, 30, 34, 39	PWR	Ground to the connector	-

4.4.5.1 User-Defined LEDs

The AXE5-Falcon board integrates four RGB LEDs directly connected to the FPGA, offering extensive user control over colors and illumination. Furthermore, there are two green user-controllable LEDs linked to the HPS, providing additional visual indicators. Each LED is individually addressable, offering precise control and illumination options, thereby enabling diverse applications and customizable visual feedback within the Agilex 5 SoC FPGA applications.

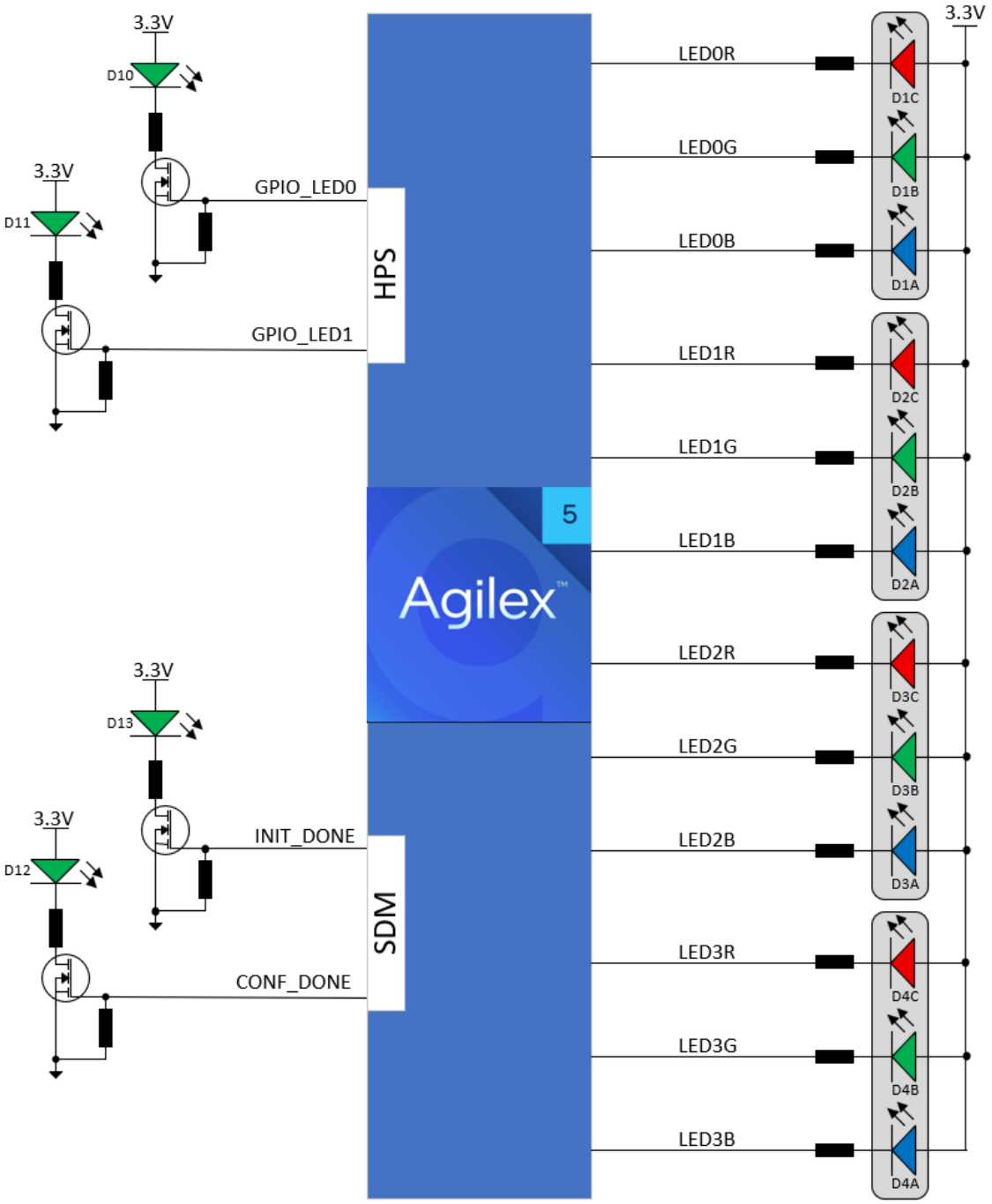

Figure 4-15 : LED Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
LED0R	PIN_AE14	Output	Red color of D1 LED	3.3-V LVCMOS
LED0G	PIN_R11	Output	Green color of D1 LED	3.3-V LVCMOS
LED0B	PIN_R8	Output	Blue color of D1 LED	3.3-V LVCMOS
LED1R	PIN_AT8	Output	Red color of D2 LED	3.3-V LVCMOS
LED1G	PIN_AH4	Output	Green color of D2 LED	3.3-V LVCMOS
LED1B	PIN_AH6	Output	Blue color of D2 LED	3.3-V LVCMOS
LED2R	PIN_AE19	Output	Red color of D3 LED	3.3-V LVCMOS
LED2G	PIN_V19	Output	Green color of D3 LED	3.3-V LVCMOS
LED2B	PIN_V14	Output	Blue color of D3 LED	3.3-V LVCMOS
LED3R	PIN_C19	Output	Red color of D4 LED	3.3-V LVCMOS
LED3G	PIN_B17	Output	Green color of D4 LED	3.3-V LVCMOS
LED3B	PIN_R19	Output	Blue color of D4 LED	3.3-V LVCMOS
GPIO_LED0	PIN_BL75	Output	HPS GPIO0_IO14 LED	1.8-V
GPIO_LED1	PIN_AP74	Output	HPS GPIO0_IO15 LED	1.8-V

4.4.5.2 User Buttons

The AXE5-Falcon board has six push buttons connected to the SoC FPGA that allows user to interact with the Agilex 5 device. The buttons have different functions:

- 2 buttons connected to the HPS as user-defined push buttons
- 2 buttons connected to the FPGA as user-defined push buttons
- 1 button dedicated to HPS Cold reset
- 1 button dedicated to FPGA reset
- 1 button for NCONFIG to initiate FPGA/SoC configuration

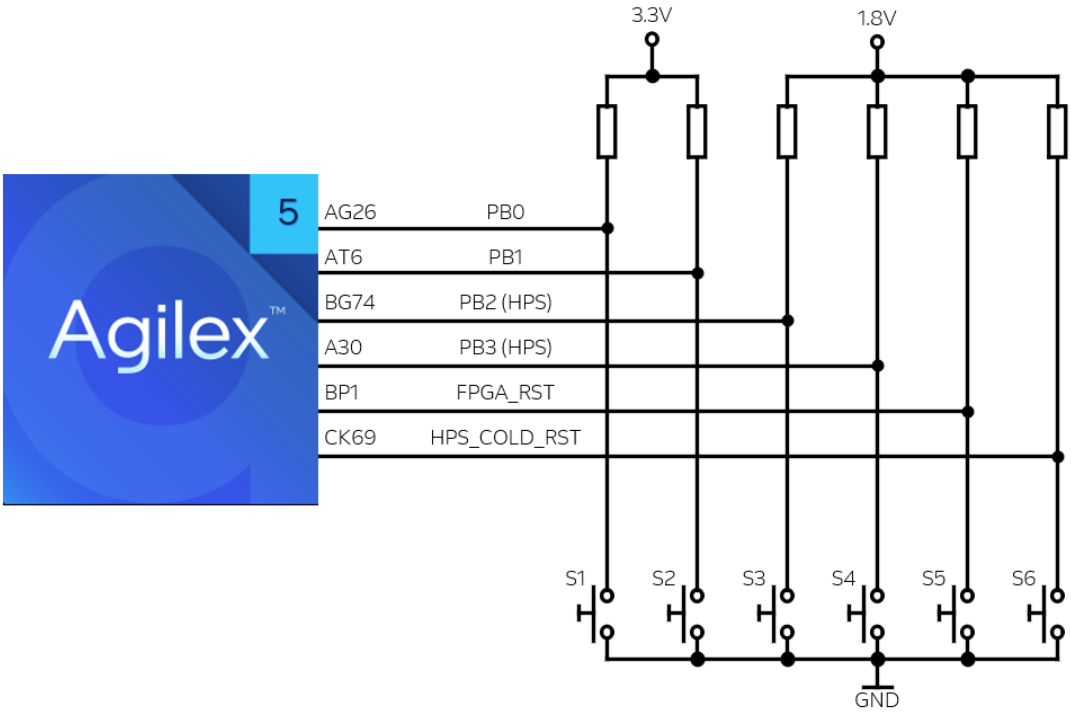

Figure 4-16 : Push-Button Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
PB0	PIN_AG26	Input	FPGA user button	3.3-V LVCMOS
PB1	PIN_AT6	Input	FPGA user button	3.3-V LVCMOS
PB2	PIN_BG74	Input	HPS user button (GPIO_IO8)	1.8-V
PB3	PIN_A30	Input	HPS user button (GPIO_IO9)	1.8-V
HPS_COLD_RST	PIN_CK69	Input	HPS reset	1.8-V
FPGA_RST	PIN_CK69	Input	FPGA reset	1.8-V LVCMOS

4.4.5.3 User DIP Switches

The AXE5-Falcon board has six DIP switches connected to the SoC FPGA that allows user to interact with the Agilex 5 device. The switches have different functions:

- 2 switches connected to the HPS as user defined
- 4 switches connected to the FPGA as user-defined

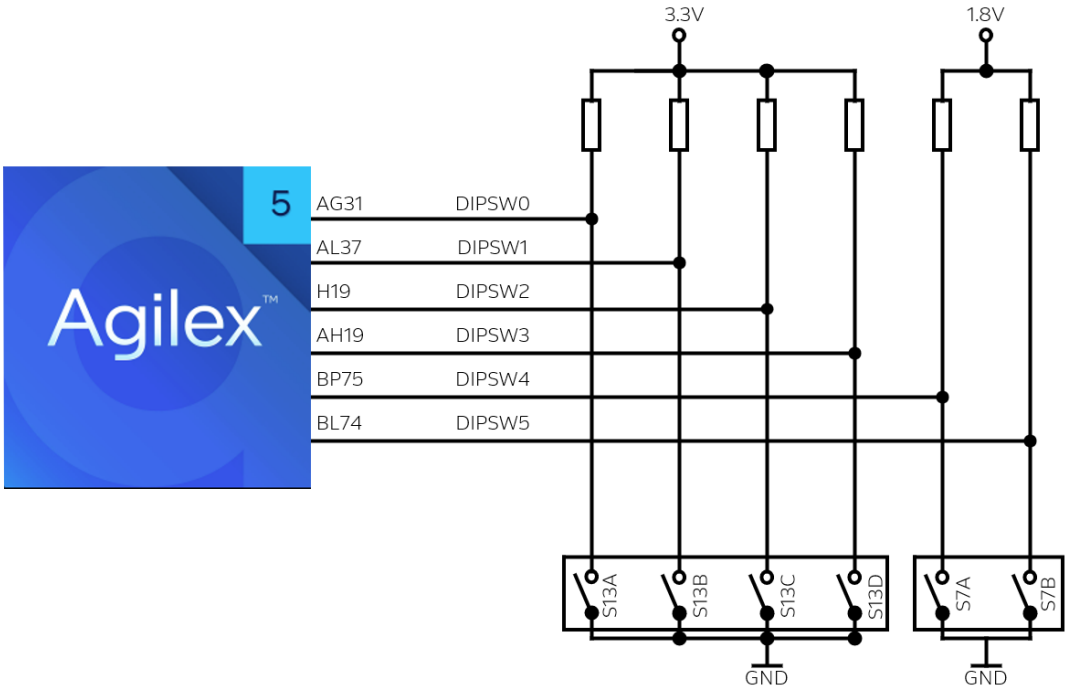

Figure 4-17 : DIP Switch Connections

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
DIPSW0	PIN_AG31	Input	FPGA user switch	3.3-V LVCMOS
DIPSW1	PIN_AL37	Input	FPGA user switch	3.3-V LVCMOS
DIPSW2	PIN_H19	Input	FPGA user switch	3.3-V LVCMOS
DIPSW3	PIN_AH19	Input	FPGA user switch	3.3-V LVCMOS
DIPSW4	PIN_BP75	Input	HPS user switch (GPIO_IO12)	1.8-V
DIPSW5	PIN_BL74	Input	HPS user switch (GPIO_IO13)	1.8-V

4.5 Power Distribution System

The AXE5-Falcon development kit relies on a comprehensive power distribution system to efficiently manage power delivery to its components. This system ensures a coordinated flow of power, overseeing critical functions such as power sequencing, thermal protection, and the hierarchical power tree structure. These functionalities collectively ensure optimal performance and reliability across the AXE5-Falcon board operations.

4.5.1 Power Tree and Sequencing

The AXE5-Falcon is designed with a flexible power system that accommodates multiple power source options, including USB-C and standalone power inputs. Employing diverse

configurations with compact, small-footprinted power modules, ensures reliable power delivery to the board and the connected mezzanine cards.

The figure below shows the power tree structure on the AXE5-Falcon development board. The color coding shows the sequencing order that these rail follow.

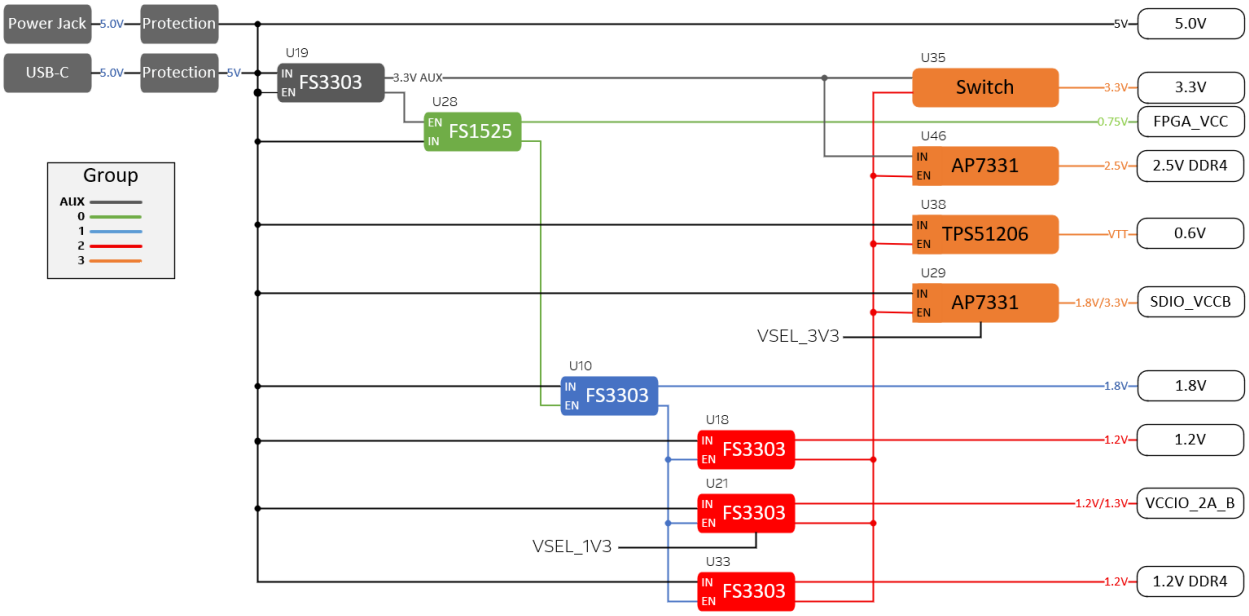

Figure 4-18 : Power Tree Structure and Sequencing

4.5.2 Thermal Protection

The AXE5-Falcon board is equipped with a fan manager, in case the Agilex 5 device power dissipation gets high and a heatsink/fan are required. The board is designed to operate in a typical laboratory environment with an ambient temperature of approximately 25 °C. However, the cooling system interfaces with the Agilex 5 device, allowing for parameterization based on application-specific needs and requirements.

The fan controller sensor continuously monitors the FPGA temperature diode in order to control the fan efficiently. The fan controller is programmable via an I2C interface, and comes blank from the factory, which tells fan to run at full speed. The user can change the controller programming to suit their needs.

The fan runs on 5V power and is PWM controller.

Communicating with the controller is done via an I2C interface which passes through an I2C MUX. The controller is connected to channel 0 of the MUX. The MUX needs to be initialized to select channel 0 prior to communicating with the controller.

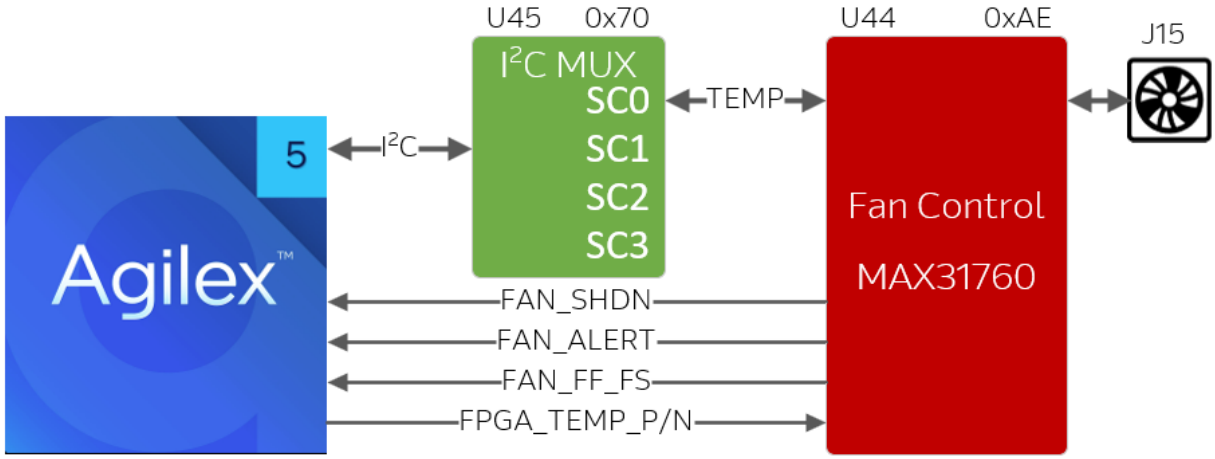

Figure 4-19 : Cooling Solution

Board Reference	FPGA Pin No.	Pin Func.	Description	I/O Std
FAN_ALERT	PIN_AT19	Input	ALERT input of fan controller	3.3-V LVCMOS
FAN_FF_FS	PIN_AT14	Input	Fan-Failure Output and Full-Speed Input of fan controller	3.3-V LVCMOS
FAN_SHDN	PIN_AT11	Input	Shutdown output for over temperature	3.3-V LVCMOS
FPGA_TEMP_P	PIN_CK71	Output	Temperature Sensing Diode	1.8-V LVCMOS
FPGA_TEMP_N	PIN_CN72			
I2C_SDA	PIN_AC1	Bidir	Serial Data Line of I2C	1.8-V LVCMOS
I2C_SCL	PIN_AC2	Bidir	Serial Clock Line of I2C	1.8-V LVCMOS

5 Software and Driver Installation

The using and programming of the AXE5-Falcon development board require various program installation of which are detailed in this section.

First, it is necessary to create your Basic Altera Account if you do not already have one. This account is required for using the software, including licensing. Below, you will find step-by-step guides on installing the software and drivers for Windows operating systems.

5.1 Installing Quartus Prime Software

- Go to the Altera Download Center: Link.
- Make sure that Quartus Prime Pro and your desired version (25.3 or later) are selected (highlighted in red).

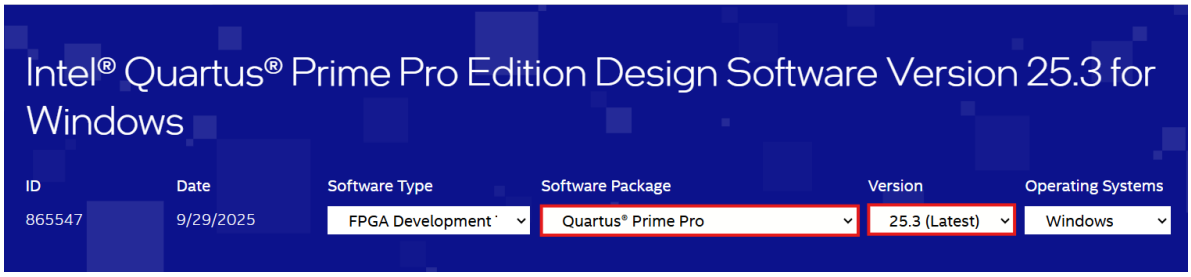

Figure 5-1 : Quartus Prime Pro Download

- It is recommended to download the Installer and run it:
    - It asks the user to select the components they wish to install. At a minimum, you need the Agilex common files and Agilex 5 device support files.
    - It downloads them and installs them.

If you don't ***check*** the box to agree to the license, the download page redirects you to the Software License Agreement page, accept the Legal Disclaimer, and the downloading will start automatically.

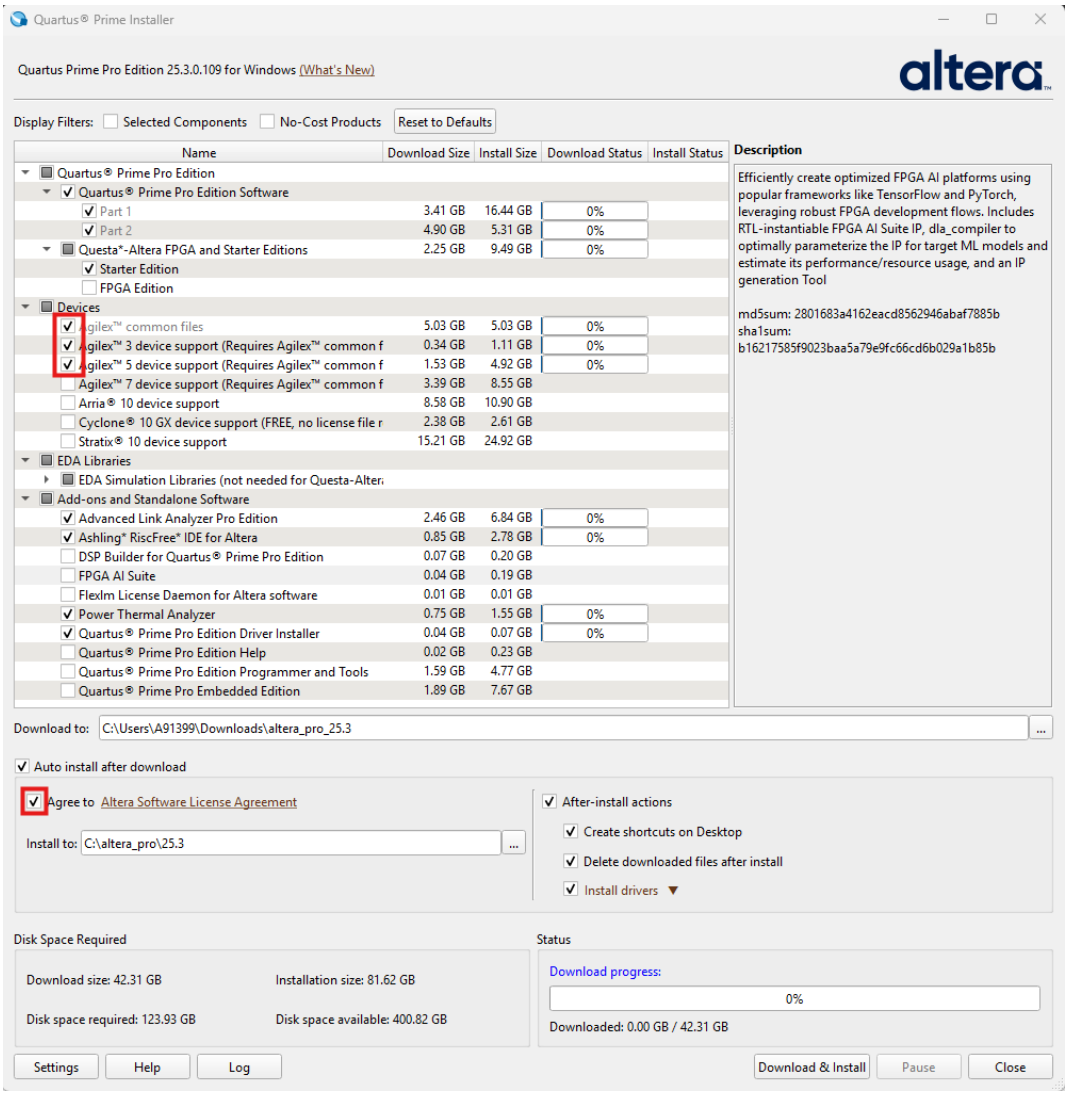

Figure 5-2 : Quartus Prime Pro Elements

5.2 License

Quartus Pro is free for Agilex 5, but needs a license. However, even though Questa Starter Edition can be used free of charge, you need to generate a free license for it.

- Log in to [Altera FPGA Self-Service Licensing Center]
- Go to **Sign up for Evaluation or Free Licenses** tab.
- Select **Questa*-Altera® FPGA Starter Edition SW-QUESTA** option.
- Set the seats and accept the terms of use this license.

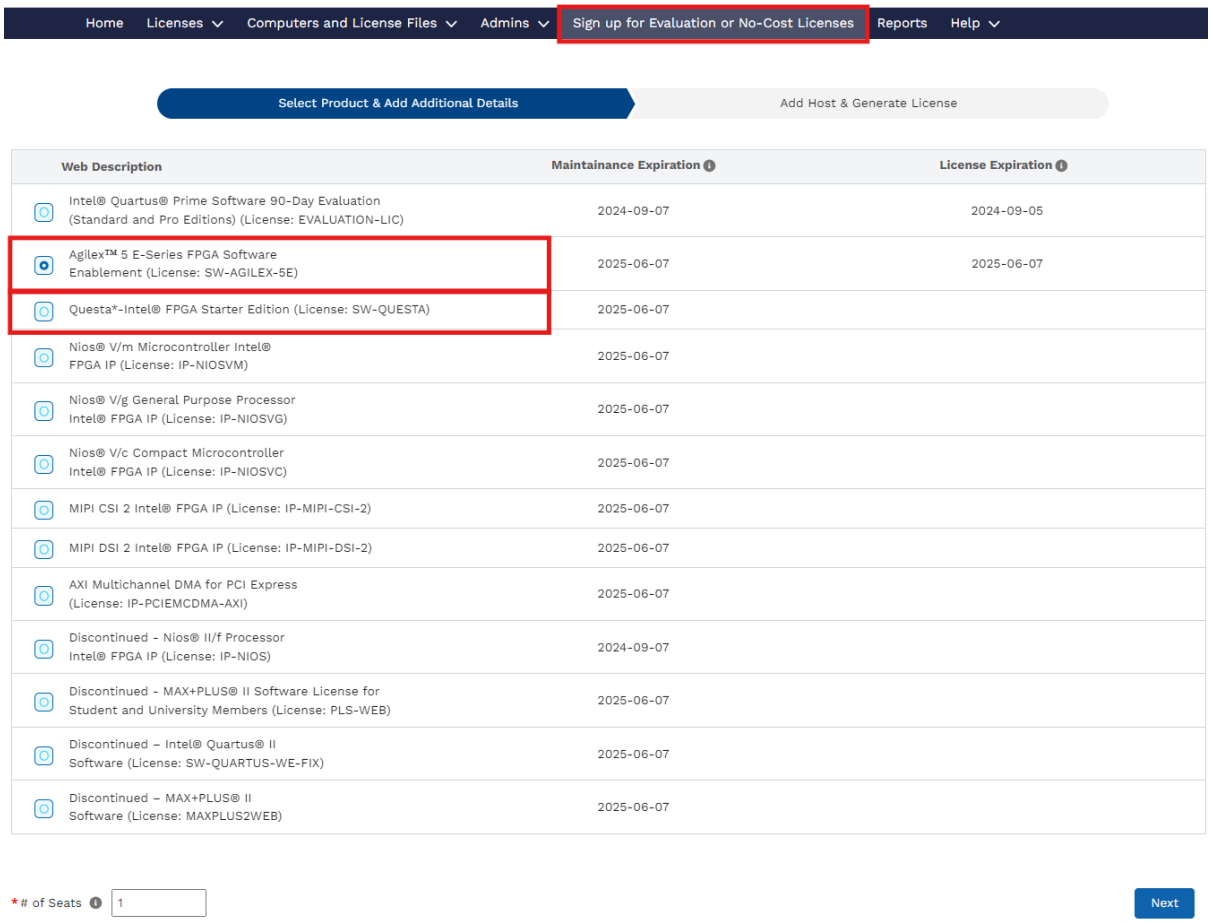

Figure 5-3 : Acquire Agilex 5 Quartus License

- Click on **Next** button.
- In the next window select **+New computer**.
- In the Create Computer window, fill in the fields with your computer details and click on **Save**.
- Choose the computer you created and check the box agreeing to the license use terms.
- Click the **Generate** button.
- Repeat for **Questa*-Altera® FPGA Starter Edition SW-QUESTA** option.

The license file will be provided by email, or you can also download it under Altera FPGA Self-Service Licensing Center.

6 Appendix

6.1 Revision History

Version	Change Log	Date of Change
V01.0	Initial Version release	10/16/2025

6.2 Legal Disclaimer

ARROW ELECTRONICS

EVALUATION BOARD LICENSE AGREEMENT

By using this evaluation board or kit (together with all related software, firmware, components, and documentation provided by Arrow, “Evaluation Board”), You (“You”) are agreeing to be bound by the terms and conditions of this Evaluation Board License Agreement (“Agreement”). Do not use the Evaluation Board until You have read and agreed to this Agreement. Your use of the Evaluation Board constitutes Your acceptance of this Agreement.

PURPOSE

The purpose of this evaluation board is solely intended for evaluation purposes. Any use of the Board beyond these purposes is on your own risk. Furthermore, according the applicable law, the offering Arrow entity explicitly does not warrant, guarantee or provide any remedies to you with regard to the board.

LICENSE

Arrow grants You a non-exclusive, limited right to use the enclosed Evaluation Board offering limited features only for Your evaluation and testing purposes in a research and development setting. Usage in a live environment is prohibited. The Evaluation Board shall not be, in any case, directly or indirectly assembled as a part in any production of Yours as it is solely developed to serve evaluation purposes and has no direct function and is not a finished product.

EVALUATION BOARD STATUS

The Evaluation Board offers limited features allowing You only to evaluate and test purposes. The Evaluation Board is not intended for consumer or household use. You are not authorized to use the Evaluation Board in any production system, and it may not be offered for sale or lease, or sold, leased or otherwise distributed for commercial purposes.

OWNERSHIP AND COPYRIGHT

Title to the Evaluation Board remains with Arrow and/or its licensors. This Agreement does not involve any transfer of Alteralectual property rights (“IPR) for evaluation board. You may not remove any copyright or other proprietary rights notices without prior written authorization from Arrow or it licensors.

RESTRICTIONS AND WARNINGS

Before You handle or use the Evaluation Board, You shall comply with all such warnings and other instructions and employ reasonable safety precautions in using the Evaluation Board. Failure to do so may result in death, personal injury, or property damage.

You shall not use the Evaluation Board in any safety critical or functional safety testing, including but not limited to testing of life supporting, military or nuclear applications. Arrow expressly disclaims any responsibility for such usage which shall be made at Your sole risk.

WARRANTY

Arrow warrants that it has the right to provide the evaluation board to you. This warranty is provided by Arrow in lieu of all other warranties, written or oral, statutory, express or implied, including any warranty as to merchantability, non-infringement, fitness for any particular purpose, or uninterrupted or error-free operation, all of which are expressly disclaimed. The evaluation board is provided “as is” without any other rights or warranties, directly or indirectly.

You warrant to Arrow that the evaluation board is used only by electronics experts who understand the dangers of handling and using such items, you assume all responsibility and liability for any improper or unsafe handling or use of the evaluation board by you, your employees, affiliates, contractors, and designees.

LIMITATION OF LIABILITIES

In no event shall Arrow be liable to you, whether in contract, tort (including negligence), strict liability, or any other legal theory, for any direct, indirect, special, consequential, incidental, punitive, or exemplary damages with respect to any matters relating to this agreement. In no event shall arrow’s liability arising out of this agreement in the aggregate exceed the amount paid by you under this agreement for the purchase of the evaluation board.

IDENTIFICATION

You shall, at Your expense, defend Arrow and its Affiliates and Licensors against a claim or action brought by a third party for infringement or misappropriation of any patent, copyright, trade secret or other Alteralectual property right of a third party to the extent resulting from (1) Your combination of the Evaluation Board with any other component, system, software, or firmware, (2) Your modification of the Evaluation Board, or (3) Your use of the Evaluation Board in a manner not permitted under this Agreement. You shall indemnify Arrow and its Affiliates and Licensors against and pay any resulting costs and damages finally awarded against Arrow and its Affiliates and Licensors or agreed to in any settlement, provided that You have sole control of the defense and settlement of the

claim or action, and Arrow cooperates in the defense and furnishes all related evidence under its control at Your expense. Arrow will be entitled to participate in the defense of such claim or action and to employ counsel at its own expense.

RECYCLING

The Evaluation Board is not to be disposed as an urban waste. At the end of its life cycle, differentiated waste collection must be followed, as stated in the directive 2002/96/EC. In all the countries belonging to the European Union (EU Dir. 2002/96/EC) and those following differentiated recycling, the Evaluation Board is subject to differentiated recycling at the end of its life cycle, therefore: It is forbidden to dispose the Evaluation Board as an undifferentiated waste or with other domestic wastes. Consult the local authorities for more information on the proper disposal channels. An incorrect Evaluation Board disposal may cause damage to the environment and is punishable by the law.