AXE5000 Evaluation Board
User Guide

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Table of Contents

1 AXE5000 Evaluation Board

1.1 About Arrow AXE5000 Evaluation Board

The AXE5000 Development Kit is a general-purpose board for evaluating the features of the Altera™ Agilex™ 5 FPGA.

The AXE5000 board includes a HyperRAM for user data storage, and connectivity options such as CRUVI HS, RGB LED, 3-axis accelerometer, and Arduino MKR standard pads for adapter boards. The board's low power consumption allows it to be powered via USB or a 5V supply.

Configuration is managed through a 256 Mbit QSPI flash with space for additional data storage. The kit supports applications including vision and camera systems, and includes starter labs, design examples, and a full programmer/debugger for the FPGA. Arrow provides a starter guide, demo designs on GitHub, and options for customized modifications. Compatible with 64-bit Linux, Windows 10, and Windows 11 systems, the AXE5000 accelerates development for a wide range of innovative applications.

1.2 Useful Links

A set of useful links that can be used to get relevant information about the AXE5000 development kit or the Agilex 5 FPGA and FPGA SoC.

- AXE5000 at Arrow Shop
- Altera Agilex 5 Webpage
- AXE5000 Wiki Page

1.3 Getting Help

To get help for this development kit, contact us at fpga_support@arrow.com

2 Introduction to the AXE5000 Board

2.1 Layout and Components

Figure 2-1 and Figure 2-2 show the top and bottom views of the board. It depicts the layout of the board and indicates the location of the various connectors and key components.

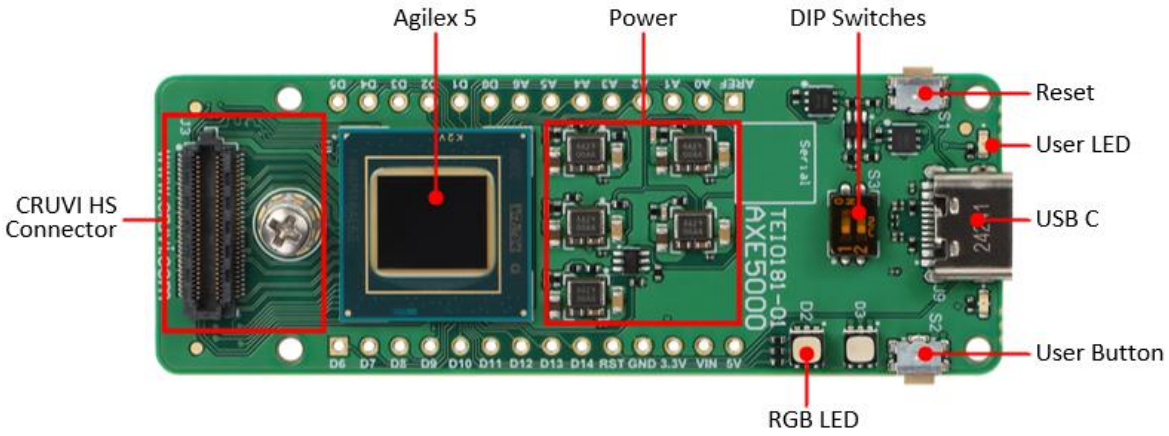

Figure 2-1 : AXE5000 Board (top view)

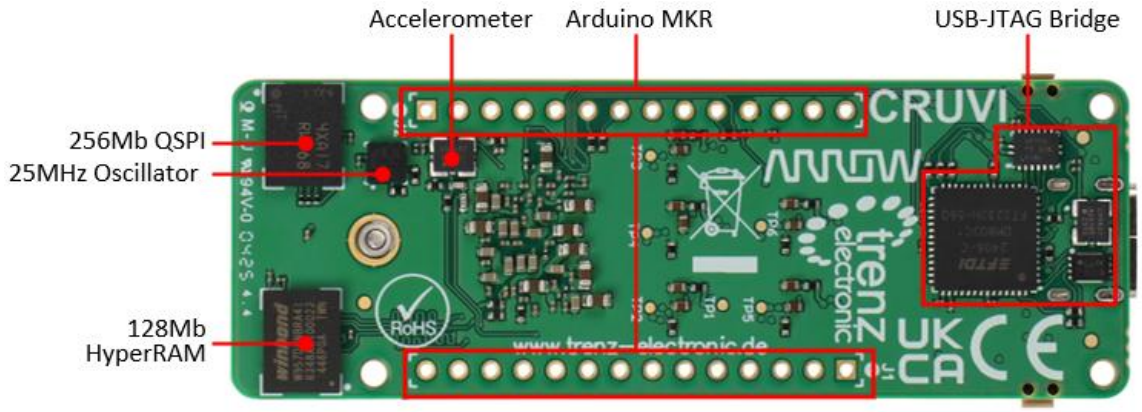

Figure 2-2 : AXE5000 Board (bottom view)

- Agilex™ 5 - A5EC008BM16AE6S (M16A)
  * 85 kLE
  * 116 DSP blocks
  * 232 multipliers 18x19
  * 3.05 Peak INT8 (TOPS)
  * 4.47 Mb internal memory
  * MIPI D-PHY interface

  * LVDS pairs at 1.250 Mbps
  * Secure Device Manager
- HyperRAM: 128 Mbit
- QSPI Config Flash: 256 Mbit
- 3-axis accelerometer
- RGB LED
- Push button and 2x DIP switches
- CRUVI HS connector
- Arduino MKR standard pads (user IOs)
- On-board Programmer/Debugger
- 5V Power via USB (or VIN of MKR header)
- Size: 25x71 mm²

2.2 Block Diagram

Figure 2-3 represents the block diagram of the board. All the connections are established through the Agilex 5 FPGA device to provide maximum flexibility for users. Users can configure the FPGA to implement any system design.

A complete set of schematics and other board relevant files are available on the GitHub Wiki.

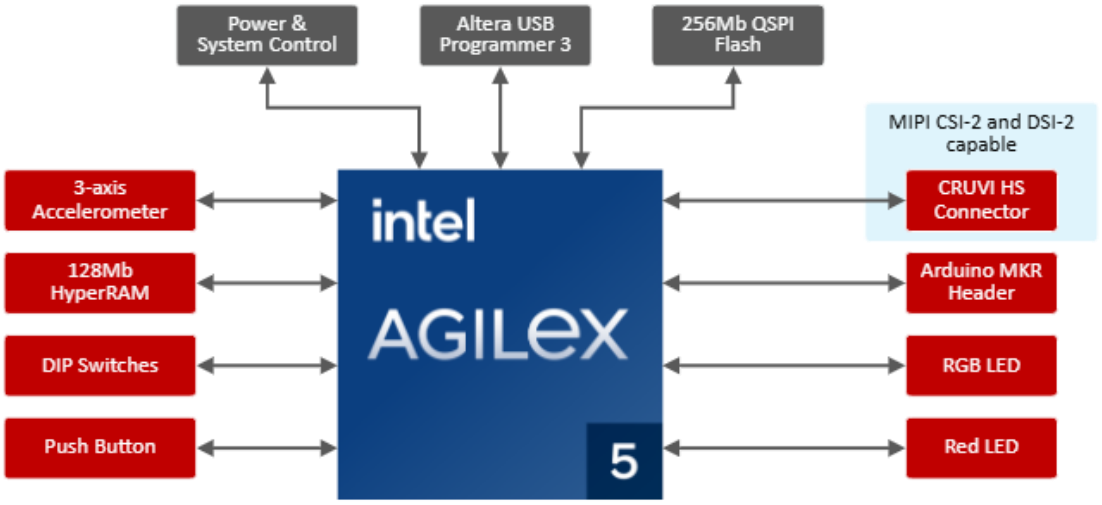

Figure 2-3 : AXE5000 Block Diagram

2.3 Board Features

FPGA Device:

- Altera™ Agilex™ 5 E-Series FPGA (non-HPS) device:
- A5EC008BM16AE6S

Features of the FPGA on the AXE5000 Board:

Resources	Device
	A5EC008BM16AE6S
Logic Elements (LE)	85,196
Logic core architecture	Second generation Intel Hyperflex™ FPGA architecture
Maximum Embedded Memory	5.56 Mb
M20K Memory (Mb)	229 (4.47Mb)
18x19 Multipliers	232
Digital Signal Processing (DSP) Blocks	116
LVDS pairs at 1,250 Mbps	96
MIPI D-PHY data rate	2.5 Gbps
Adaptive Logic Module (ALM) Registers	28,800
I/O	200 HVIO (1.8V – 3.3V) 192 HSIO (1.05V – 1.3V)
Additional Memory (RAM)	128 Mb Winbond HyperRAM (1.2 V, 250 MHz)

System

AXE5000 Configuration and Debug

- On-board USB-C port for power and communication (5 V @ 1.5 A)
- USB-JTAG/UART Bridge (UB3 FTDI) providing:
    - x5 JTAG lines
    - x2 UART interface signals

Memory Devices

- 256 Mb QSPI external flash memory for FPGA configuration

- 128 Mb Winbond HyperRAM (1.2 V, 250 MHz)

Headers and Interfaces

- CRUVI HS interface with:
    - x25 HSIO (High-Speed IO)
    - x7 HVIO (High-Voltage IO)
- Arduino MKR Pads:
    - x10 GPIO
    - x12 signals (additional connectivity)

Buttons and Indicators

- 1x user RGB LEDs
- 1x user red LEDs
- 1x user push buttons
- 1x user 2-POS DIP switches

Sensors

- 3-axis accelerometer connected via I2C:
    - x2 I2C lines

Power

- 5.0V over USB type-C (or VIN of MKR header)
- FPGA I/O Voltage Levels:
    - Bank 5A/5B: 3.3 V
    - Bank 2A: 1.2/1.3 V
    - Bank 3A: 1.2 V

Oscillators

- 12 MHz (for USB-JTAG/UART Bridge)
- 25 MHz (for FPGA clocking)

Mechanical

- 25mm x 71 mm board size

2.4 Ordering Information

Development Kit Version	Ordering Code	Core Device Part Number
Production (Q2 2025)	AXE5000	A5EC008BM16AE6S

2.5 Box Contents

The AXE5000 Development Kit includes the following hardware:

- AXE5000 evaluation board

3 Connections and Peripherals of the AXE5000 Evaluation Board

3.1 Clock Circuitry

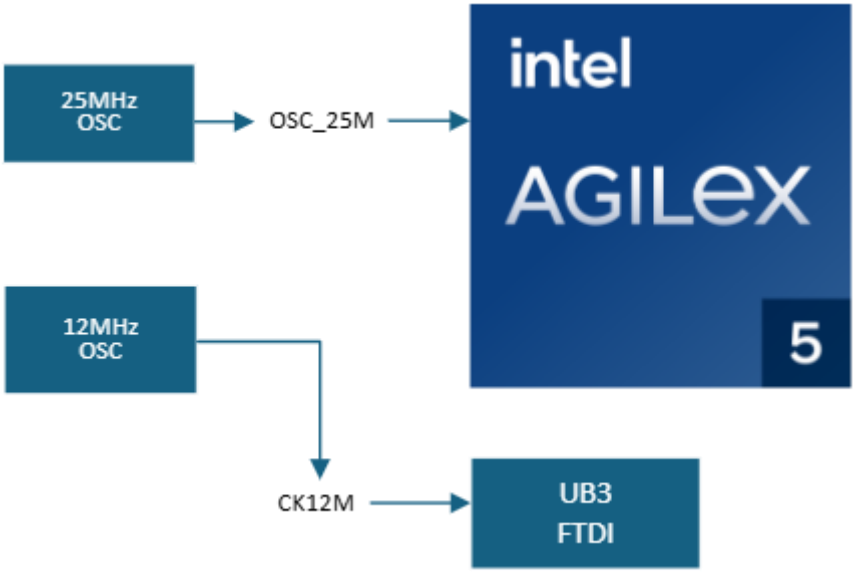

Figure 3-1 : Simplified Clock Connection Diagram

On-Board Clock Inputs

Board Reference	FPGA Pin No.	Clock Freq. (MHz)	Description	I/O Std
OSC_CLK_1	AG11	25	For Configuration	1.8V
CLK_25M_C	AD5	25	User Clock	VADJ(1.2V/1.3V)
CLK_25M_C	A7	25	User Clock	1.2V

Off-Board Clock I/O

The FPGA can accept clocks via the Arduino MKR and CRUVI-HS connectors.

Board Reference	FPGA Pin No.	I/O Std
CRUVI-HS (B2_P/B2_N)	AC6/AC5	VADJ
CRUVI-HS (A0_P/A0_N)	N2/N1	VADJ
CRUVI-HS REFCLK	AJ28	3.3V
Arduino MKR (All)		3.3V

3.2 DIP Switches

The development board features a DIP switch (S3) to be used by the user. S3 has 2 switches which require the user to enable the internal weak pullup resistor when being used. The switch has a plastic protective screen which needs to be removed prior to use.

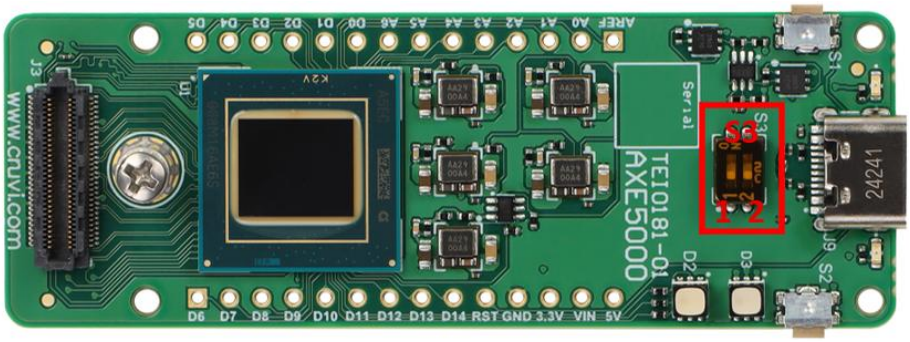

Figure 3-2 : DIP Switch location

S3 DIP Switch Settings

Board Label	FPGA Pin No	Description	I/O Std
S3-1	A14	DIP Switch (SW0)	1.2V
S3-2	A13	DIP Switch (SW1)	1.2V

3.3 Push Buttons

The board features two push buttons for interacting with the FPGA.

The RESET (CONFIG) button is designed to initiate the FPGA's reset process (configuration) when pressed, driving the associated line to a low logic level.

The USER button provides a general-purpose input for user interaction. When pressed, it drives the associated signal line to a low logic level. When released, the signal line is open. The user is responsible for adding an internal weak pullup resistor.

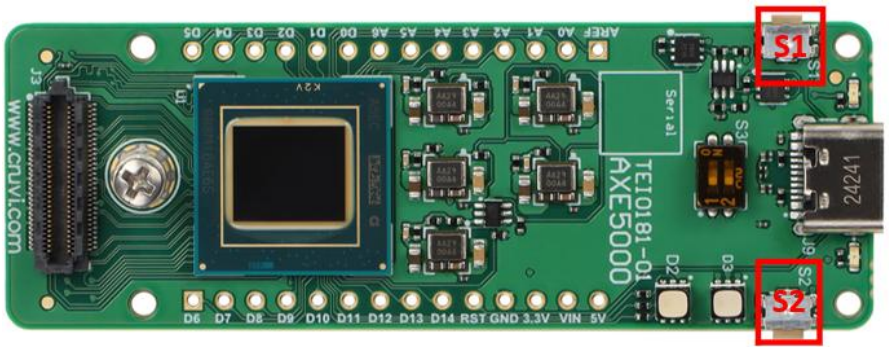

Figure 3-3 : Push Button locations

Board Label	FPGA Pin No	Description	I/O Std
S1	AG15	nCONFIG/RSTn	1.8V
S2	A12	User button	1.2V

3.4 Accelerometer

The board includes a digital accelerometer (LIS3DH), commonly known as the G-Sensor. This G-Sensor is a compact, thin, ultra-low-power 3-axis accelerometer with a standard digital I2C/SPI serial interface. The LIS3DH offers user-selectable full-scale ranges of ±2g, ±4g, ±8g, and ±16g and is capable of measuring accelerations with output data ranging from 1 Hz to 5 kHz.

When using the I2C protocol, the connection to the accelerometer is made through the FPGA's SDA (Serial Data Line) and SCL (Serial Clock Line) pins.

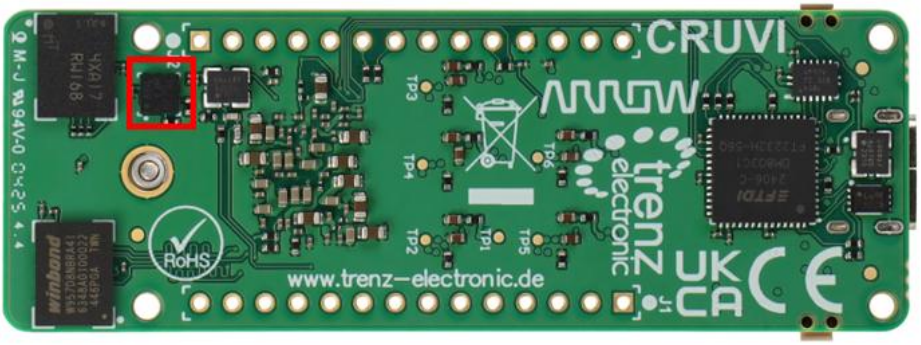

Figure 3-4 : Accelerometer location

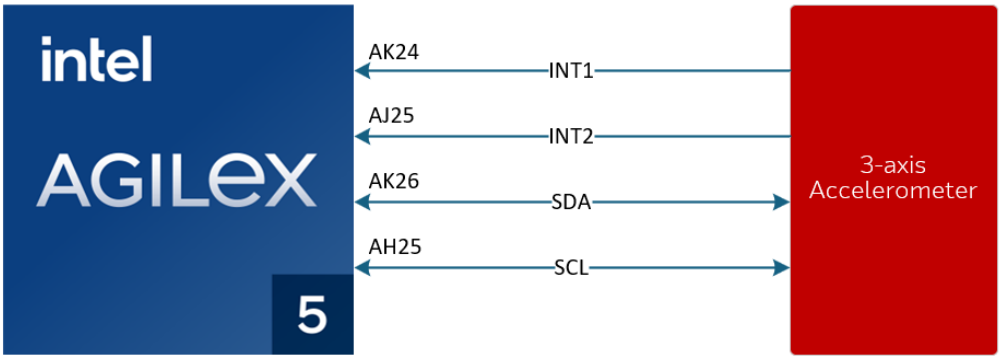

Figure 3-5 : Accelerometer wiring

Board Label	FPGA Pin No	Description	I/O Standard
INT1	AK24	Interrupt 1	3.3V
INT2	AJ25	Interrupt 2	3.3V
SDA	AK26	I 2C serial data (SDA)	3.3V
SCL	AH25	I 2C serial clock (SCL)	3.3V

3.5 User LEDs

The are 2 user LEDs on the AXE5000 board. One is RGB (D2) and one is Red (D10).

All LEDs are illuminated using an active-low signal.

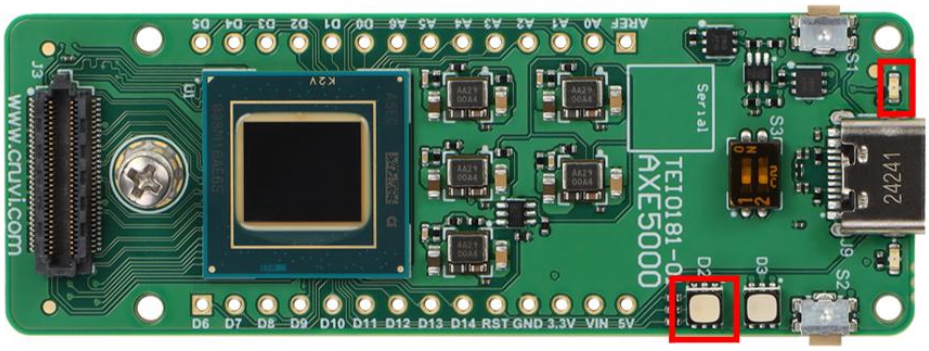

Figure 3-6 : User LEDs

Board Reference	FPGA Pin No.	I/O Std
RLED	AH22	3.3V
GLED	AK21	3.3V
BLED	AK20	3.3V
LED1	AG21	3.3V

3.6 HyperRAM memory

The AXE5000 has a 128Mb HyperRAM memory component.

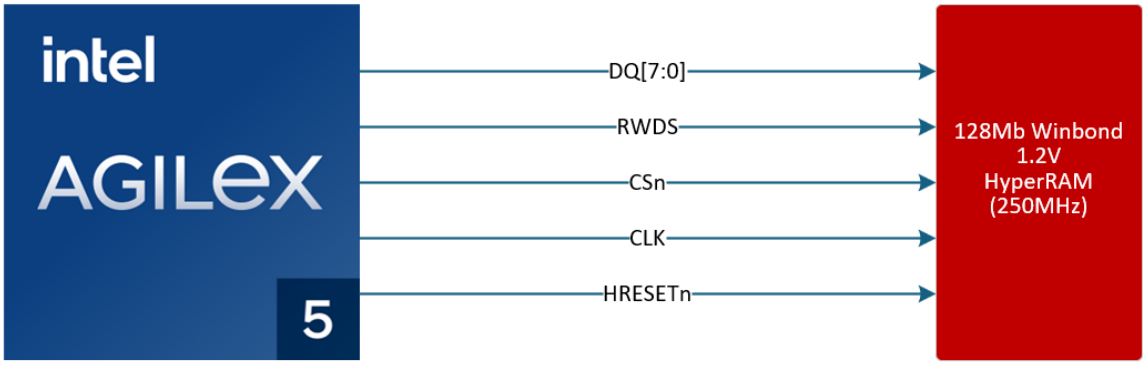

Figure 3-7 : HyperRAM wiring

Signal Name	FPGA Pin No.	Description	I/O Standard
DQ0	C3	Address/Command/DDR data bit 0	1.2V
DQ1	C2	Address/Command/DDR data bit 1	1.2V
DQ2	B4	Address/Command/DDR data bit 2	1.2V
DQ3	B6	Address/Command/DDR data bit 3	1.2V
DQ4	D3	Address/Command/DDR data bit 4	1.2V
DQ5	A4	Address/Command/DDR data bit 5	1.2V
DQ6	B3	Address/Command/DDR data bit 6	1.2V
DQ7	C6	Address/Command/DDR data bit 7	1.2V
HRESETn	F7	Active-Low Reset output	1.2V
CSn	D8	Active-Low Chip Select output	1.2V
RWDS	A6	Read/Write Data Strobe output	1.2V
CLK	D7	Transaction Clock output	1.2V

3.7 Board Status Elements

The board has a few status indicators (LEDs).

D1 (Green LED), when lit, indicated that the board is receiving power.

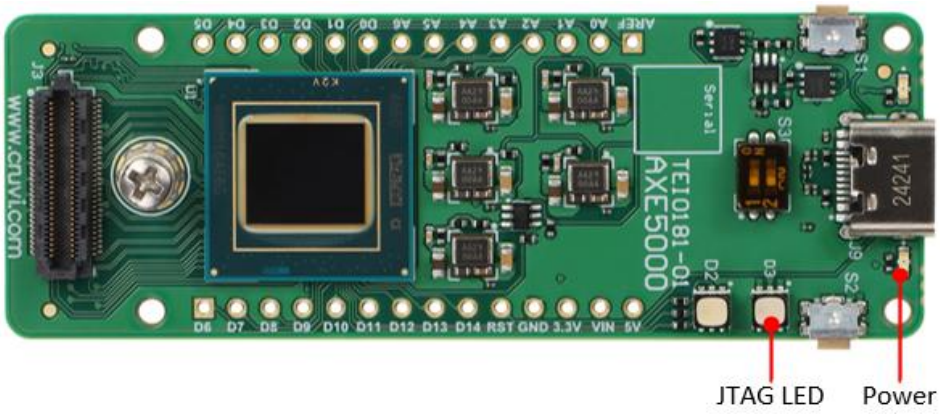

Figure 3-8 : LED status indicators

D3 (RGB LED) indicates the status of activity happening on the JTAG USB Blaster.

- **Off**: No power / not connected / suspend mode
- **Blue**: Connected, not in use
- **Green**: Connected, an application is using JTAG, no traffic
- **Green flickering**: Connected, data is moving through the JTAG interface
- **Purple flashing**: Identify function has been triggered on this cable

3.8 I2C Structure

The TDK uPOL power modules used on the board have a PMBUS interface available to the user to query some telemetric data from the module. All 5 power module PMBUS pins are connected to the same I2C pins on the FPGA.

Board Label	FPGA Pin No	Description	I/O Std
SCL	AH25	I2C Clock	3.3V
SDA	AK26	I2C Data	3.3V

uPOL	I2C Address	Voltage Rail
U6	0x10	FPGA_VCC (0.75V)
U8	0x11	VADJ (1.2V/1.3V)
U10	0x14	1.8V
U11	0x13	1.2V
U14	0x15	3.3V

3.9 I/O expansion

The AXE5000 has 2 I/O expansion interfaces, the Arduino MKR header and the CRUVI-HS.

3.9.1 CRUVI High-Speed Connector

The AXE5000 board features one CRUVI HS connector. CRUVI is an open ecosystem, low-pin-count interface solution that enables the integration of a wide range of peripherals into the system while accommodating both high-speed signaling and support for low-speed device interfaces at the same time. The board provides 5.0 V, 3.3 V and VADJ power through CRUVI HS connector. The power control of the VADJ power rail is managed by the U8 power module. The VADJ defaults to 1.2V but the user can set it to 1.3V by driving the VSEL_1V3 pin from the FPGA to a logic high level. The FPGA pins connected to the CRUVI HS can be set to either 1.2V or 1.3V I/O standard.

For custom add-on cards with CRUVI HS interface, the recommended mating connector is ST4-30-1.50-L-D-P from Samtec.

For hardware module mounting, use a M2x6mm pan head Philips drive screw.

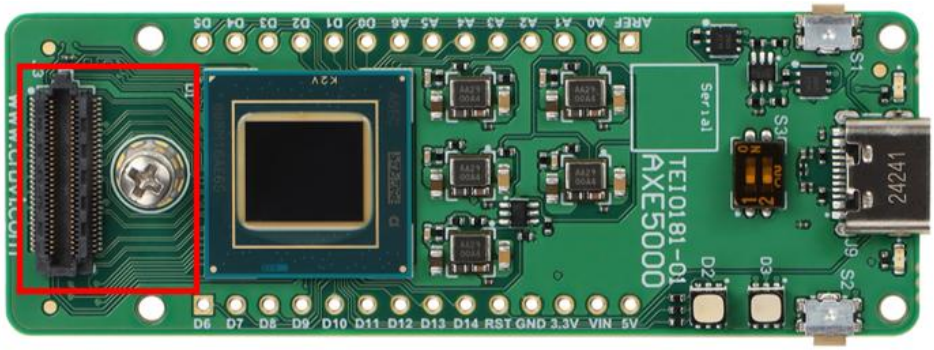

Figure 3-9 : CRUVI HS Connector and Mounting post

CRUVI HS Connection

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	Description	I/O Std
A0_P/A0_N	N2/N1	14/16	Bidir	HS Differential Data A[0]	Adjustable**
A1_P/A1_N	R2/T1	20/22	Bidir	HS Differential Data A[1]	Adjustable**
A2_P/A2_N	T2/U1	26/28	Bidir	HS Differential Data A[2]	Adjustable**
A3_P/A3_N	V1/V2	32/34	Bidir	HS Differential Data A[3]	Adjustable**
A4_P/A4_N	T3/R4	38/40	Bidir	HS Differential Data A[4]	Adjustable**
A5_P/A5_N	Y1/W2	44/46	Bidir	HS Differential Data A[5]	Adjustable**
B0_P/B0_N	V6/W5	15/17	Bidir	HS Differential Data B[0]	Adjustable**
B1_P/B1_N	AC7/AD7	21/23	Bidir	HS Differential Data B[1]	Adjustable**
B2_P/B2_N***	U5/T4, AC6/AC5	27/29	Bidir	HS Differential Data B[2]	Adjustable**
B3_P/B3_N	V3/W3	33/35	Bidir	HS Differential Data B[3]	Adjustable**
B4_P/B4_N	U4/U3	39/41	Bidir	HS Differential Data B[4]	Adjustable**
B5_P/B5_N	P5/P4	45/47	Bidir	HS Differential Data B[5]	Adjustable**
HSI	AE1	10	Input	HS Serial In	Adjustable**
HSMIO	N7	2	Bidir	HS Serial Data I/O	Adjustable**
HSO	N6	6	Output	HS Serial Out	Adjustable**
HSRST	AF1	8	Output	Serial Reset	Adjustable**
SMB_ALERT	AH26	3	Input	SMBus interrupt signal	3.3-V LVCMOS
SMB_SDA	AJ29	5	Bidir	SMBus Data Line	3.3-V LVCMOS
SMB_SCL	AJ27	7	Bidir	SMBus Data Clock Line	3.3-V LVCMOS
REFCLK	AJ28	11	Input	Clock Input	3.3-V LVCMOS
5V	-	60	PWR	5V power to the connector	-
3.3V	-	4, 9	PWR	3.3V power to the connector	-
VADJ	-	36	PWR	HS IO Bank voltage	-
VSEL_1V3	AJ24			Selecy VADJ to 1.2V or 1.3V	
GND	-	12, 13, 18, 19, 24, 25, 30, 31, 37, 42, 43, 48, 49, 54	PWR	Ground to the connector	-
n.c.	-	1, 50, 51, 52, 53, 55, 56, 57, 58, 59	-	Not connected	-

*** "1.2V True Differential Signaling" or "1.3V True Differential Signaling". Depending on VADJ set by VSEL_1V3 pin*

**** B2_P/B2_N are assigned to 2 sets of pins on the FPGA due to MIPI Hard IP pin placement*

3.9.2 Arduino MKR Header

The AXE5000 board offers connectivity to Arduino MKR compatible shields that could also alternatively be used as GPIOs. The MKR connectors offer up to 7 analogue inputs and 15 digital I/Os. There is also an option to use or not use the 4.7k Ohm pull-up resistor lines for communication interfaces.

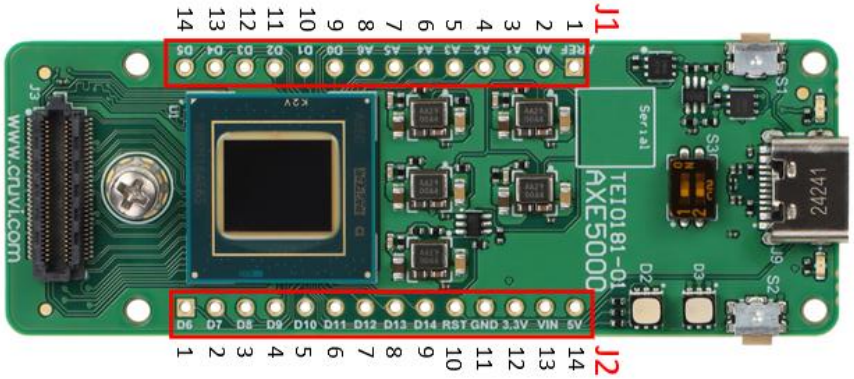

Figure 3-10 : Arduino MKR Header

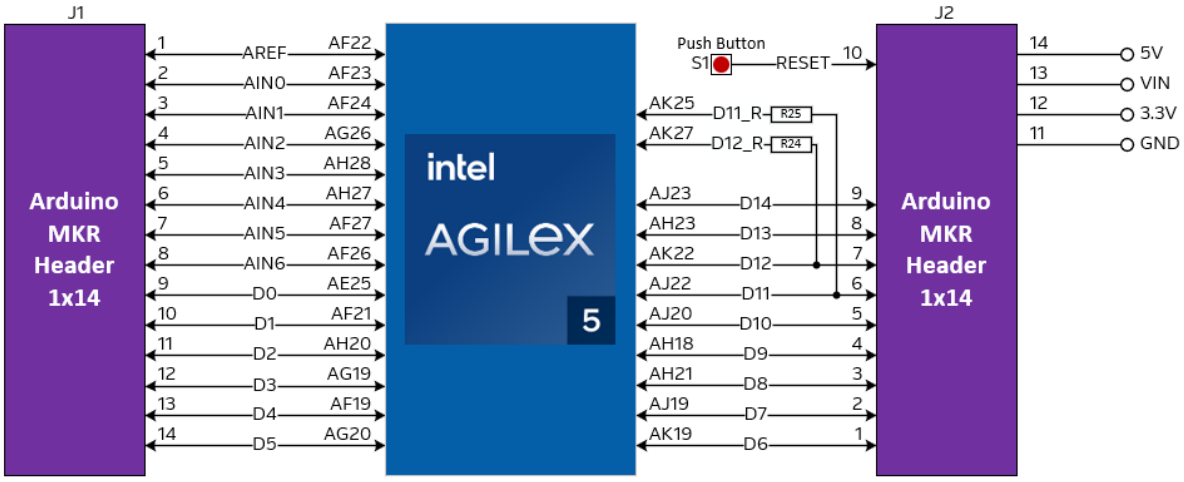

Figure 3-11 : Arduino MKR Header Connections

Board Reference	FPGA Pin No.	Conn. Pin No.	Pin Func.	I/O Std
AREF		J1-1	Bidir	Adjustable**
AIN0		J1-2	Bidir	Adjustable**
AIN1		J1-3	Bidir	Adjustable**
AIN2		J1-4	Bidir	Adjustable**
AIN3		J1-5	Bidir	Adjustable**

AIN4		J1-6	Bidir	Adjustable**
AIN5		J1-7	Bidir	Adjustable**
AIN6		J1-8	Bidir	Adjustable**
D0		J1-9	Bidir	Adjustable**
D1		J1-10	Bidir	Adjustable**
D2		J1-11	Bidir	Adjustable**
D3		J1-12	Bidir	Adjustable**
D4		J1-13	Bidir	Adjustable**
D5		J1-14	Bidir	Adjustable**
D6		J2-1	Bidir	Adjustable**
D7		J2-2	Bidir	Adjustable**
D8		J2-3	Bidir	Adjustable**
D9		J2-4	Bidir	Adjustable**
D10		J2-5	Bidir	Adjustable**
D11		J2-6	Bidir	Adjustable**
D12		J2-7	Bidir	Adjustable**
D13		J2-8	Bidir	Adjustable**
D14		J2-9	Bidir	Adjustable**
D11_R		-	Bidir	Adjustable**
D12_R		-	Input	Adjustable**
RESET		J2-10	Output	Adjustable**
5V	-	J2-14	Output	-
3.3V	-	J2-12	Output	-
VIN	-	J2-13	Input	-
GND	-	J2-11	Ground	-

3.10 Communication and Configuration

The AXE5000 uses a single chip to perform configuration of the FPGA and provide a USB to UART communication link.

3.10.1 UART Communication

The UART to USB communication is supported over a USB 2.0 High Speed (up to 480 Mbps) link via a USB-C connector.

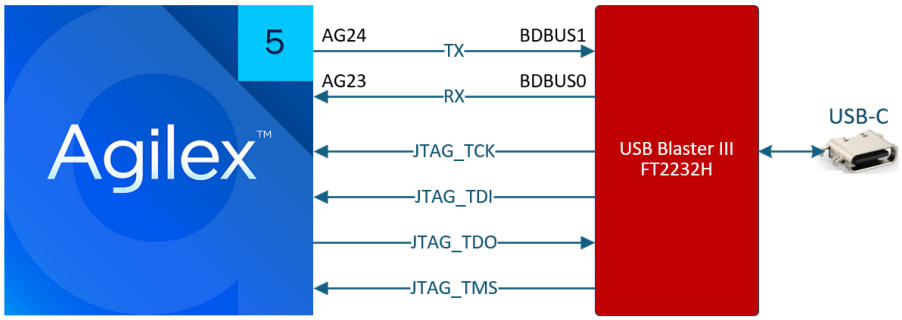

Figure 3-12 : UART to USB communication

Board Label	FPGA Pin No	Description	I/O Std
TX	AG24	UART TxD	3.3V
RX	AG23	UART RxD	3.3V

3.10.2 JTAG Configuration

JTAG configuration allows the user to configure the FPGA, or program the QSPI configuration Flash through the JTAG pins (TDI, TDO, TMS and TCK pins). The Quartus Prime Programmer is used to transfer configuration data over a USB cable to the AXE5000, through the FTDI devices and into the Agilex-5 FPGA.

4 Power Distribution

The AXE5000 relies on a comprehensive power distribution system to efficiently manage power delivery to its components.

4.1 Power Tree and Sequencing

The AXE5000 is designed with a flexible power system that accommodates multiple power source options. 5V power entry can be via either the USB-C connector or the Arduino MKR VIN pin.

The Altera Agilex 5 FPGA requires power-up sequencing. The AXE5000 power system organizes power rails into power groups and enables them in the appropriate sequence to satisfy the Agilex 5 device.

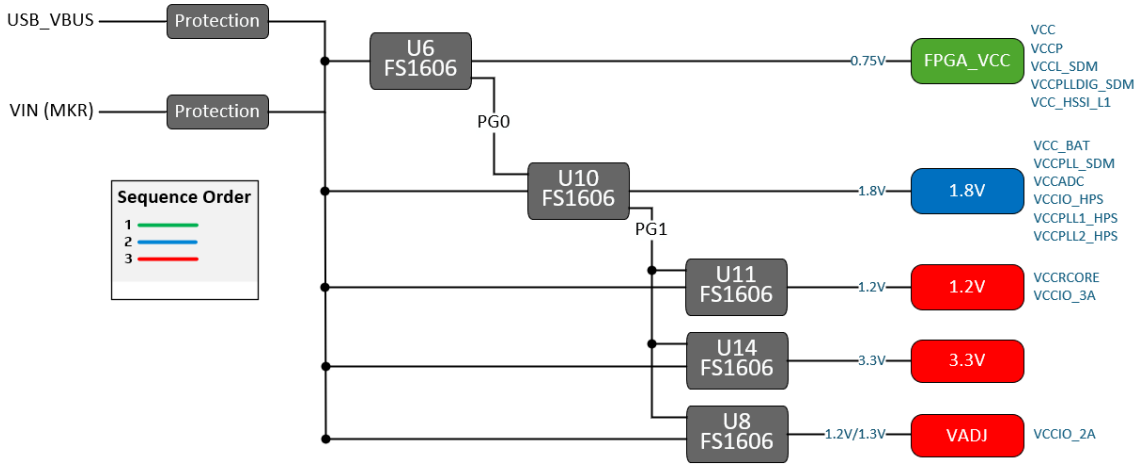

Figure 4-1 : Power Tree and Sequencing

5 Legal Disclaimer

ARROW ELECTRONICS

EVALUATION BOARD LICENSE AGREEMENT

By using this evaluation board or kit (together with all related software, firmware, components, and documentation provided by Arrow, “Evaluation Board”), You (“You”) are agreeing to be bound by the terms and conditions of this Evaluation Board License Agreement (“Agreement”). Do not use the Evaluation Board until You have read and agreed to this Agreement. Your use of the Evaluation Board constitutes Your acceptance of this Agreement.

PURPOSE

The purpose of this evaluation board is solely intended for evaluation purposes. Any use of the Board beyond these purposes is on your own risk. Furthermore, according the applicable law, the offering Arrow entity explicitly does not warrant, guarantee or provide any remedies to you with regard to the board.

LICENSE

Arrow grants You a non-exclusive, limited right to use the enclosed Evaluation Board offering limited features only for Your evaluation and testing purposes in a research and development setting. Usage in a live environment is prohibited. The Evaluation Board shall not be, in any case, directly or indirectly assembled as a part in any production of Yours as it is solely developed to serve evaluation purposes and has no direct function and is not a finished product.

EVALUATION BOARD STATUS

The Evaluation Board offers limited features allowing You only to evaluate and test purposes. The Evaluation Board is not intended for consumer or household use. You are not authorized to use the Evaluation Board in any production system, and it may not be offered for sale or lease, or sold, leased or otherwise distributed for commercial purposes.

OWNERSHIP AND COPYRIGHT

Title to the Evaluation Board remains with Arrow and/or its licensors. This Agreement does not involve any transfer of intellectual property rights (“IPR) for evaluation board. You may not remove any copyright or other proprietary rights notices without prior written authorization from Arrow or it licensors.

RESTRICTIONS AND WARNINGS

Before You handle or use the Evaluation Board, You shall comply with all such warnings and other instructions and employ reasonable safety precautions in using the Evaluation Board. Failure to do so may result in death, personal injury, or property damage.

You shall not use the Evaluation Board in any safety critical or functional safety testing, including but not limited to testing of life supporting, military or nuclear applications.

Arrow expressly disclaims any responsibility for such usage which shall be made at Your sole risk.

WARRANTY

Arrow warrants that it has the right to provide the evaluation board to you. This warranty is provided by Arrow in lieu of all other warranties, written or oral, statutory, express or implied, including any warranty as to merchantability, non-infringement, fitness for any particular purpose, or uninterrupted or error-free operation, all of which are expressly disclaimed. The evaluation board is provided “as is” without any other rights or warranties, directly or indirectly.

You warrant to Arrow that the evaluation board is used only by electronics experts who understand the dangers of handling and using such items, you assume all responsibility and liability for any improper or unsafe handling or use of the evaluation board by you, your employees, affiliates, contractors, and designees.

LIMITATION OF LIABILITIES

In no event shall Arrow be liable to you, whether in contract, tort (including negligence), strict liability, or any other legal theory, for any direct, indirect, special, consequential, incidental, punitive, or exemplary damages with respect to any matters relating to this agreement. In no event shall arrow’s liability arising out of this agreement in the aggregate exceed the amount paid by you under this agreement for the purchase of the evaluation board.

IDENTIFICATION

You shall, at Your expense, defend Arrow and its Affiliates and Licensors against a claim or action brought by a third party for infringement or misappropriation of any patent, copyright, trade secret or other intellectual property right of a third party to the extent resulting from (1) Your combination of the Evaluation Board with any other component, system, software, or firmware, (2) Your modification of the Evaluation Board, or (3) Your use of the Evaluation Board in a manner not permitted under this Agreement. You shall indemnify Arrow and its Affiliates and Licensors against and pay any resulting costs and damages finally awarded against Arrow and its Affiliates and Licensors or agreed to in any settlement, provided that You have sole control of the defense and settlement of the claim or action, and Arrow cooperates in the defense and furnishes all related evidence under its control at Your expense. Arrow will be entitled to participate in the defense of such claim or action and to employ counsel at its own expense.

RECYCLING

The Evaluation Board is not to be disposed as an urban waste. At the end of its life cycle, differentiated waste collection must be followed, as stated in the directive 2002/96/EC. In all the countries belonging to the European Union (EU Dir. 2002/96/EC) and those following differentiated recycling, the Evaluation Board is subject to differentiated recycling at the end of its life cycle, therefore: It is forbidden to dispose the Evaluation Board as an undifferentiated waste or with other domestic wastes. Consult the local

authorities for more information on the proper disposal channels. An incorrect Evaluation Board disposal may cause damage to the environment and is punishable by the law.