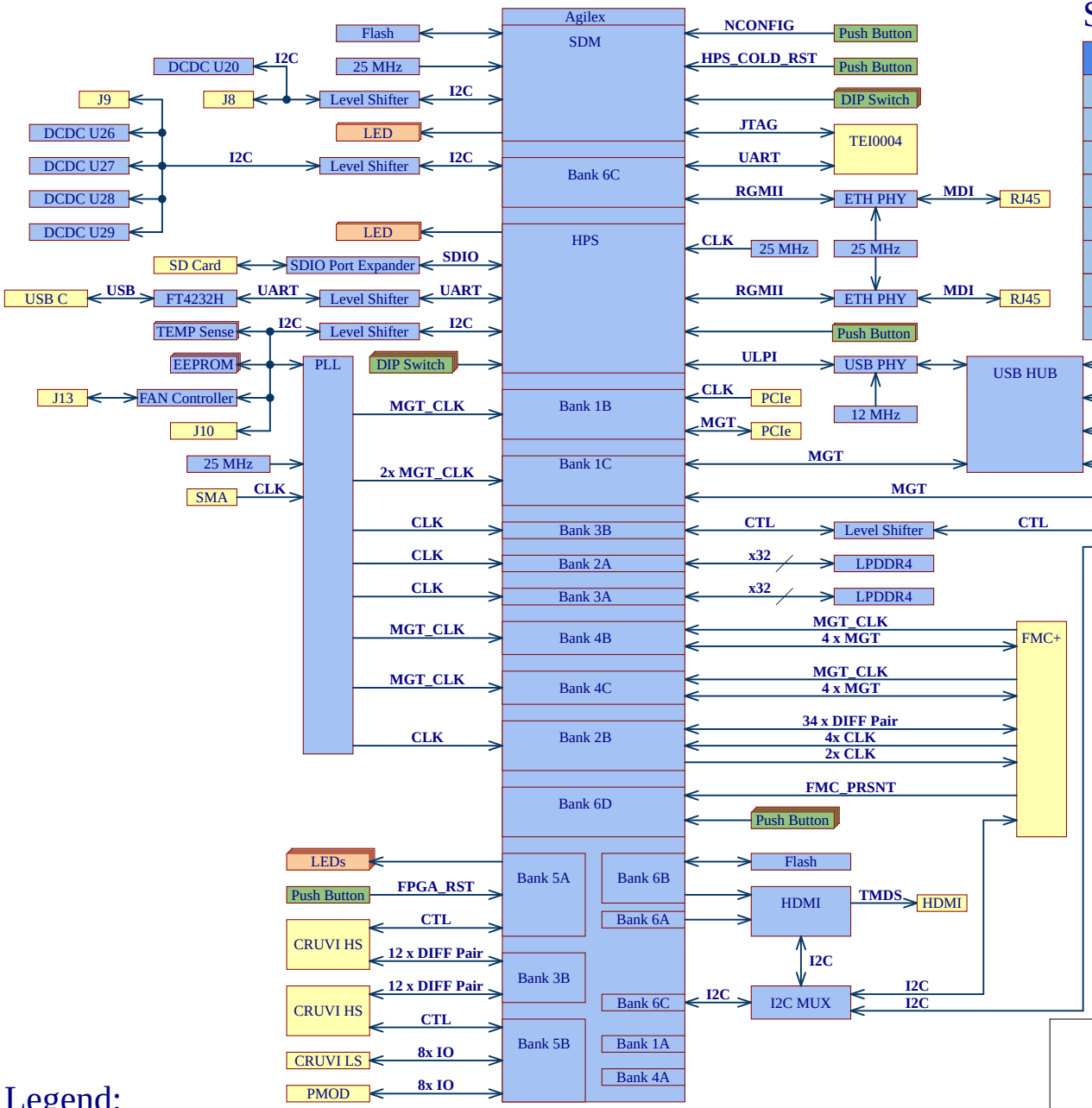


Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
+12.0V_IN_A	IN	+12.0 V	+/- 5 %	Board Power	Primary Main Power
+12.0V_IN_B	IN	+12.0 V	+/- 5 %	Board Power	Secondary Main Power
3.3VAUX	OUT	+3.3 V	+/- 3 %	Board Power	Management Power
12.0V	OUT	+12.0 V	+/- 5 %	Board Power	Main Power Supply
5.0V	OUT	+5.0 V	+/- 5 %	Board Power	Interface Power Supply
3.3V	OUT	+3.3 V	+/- 3 %	Board Power	Interface and Bank Power Supply
1.8V	OUT	+1.8 V	+/- 3 %	Board Power	SoC Power Supply
FMC_ADJ	OUT	+1.0 V - +1.3 V	+/- 3 %	FMC+ Power	FMC+ and Bank Power Supply

SSD NVME x1

MIPI D-PHY

TEI0185 TEI0185.SchDoc	FPGA_NC FPGA_NC.SchDoc	PWR_3 PWR_3.SchDoc
FMC+_2 FMC+_2.SchDoc	FPGA_GND FPGA_GND.SchDoc	PWR_4 PWR_4.SchDoc
FMC+_PWR FMC+_PWR.SchDoc	PWR_IN PWR_IN.SchDoc	PWR_5 PWR_5.SchDoc
FPGA_PWR FPGA_PWR.SchDoc	PWR_1 PWR_1.SchDoc	PWR_6 PWR_6.SchDoc
FPGA_PWR2 FPGA_PWR2.SchDoc	PWR_2 PWR_2.SchDoc	

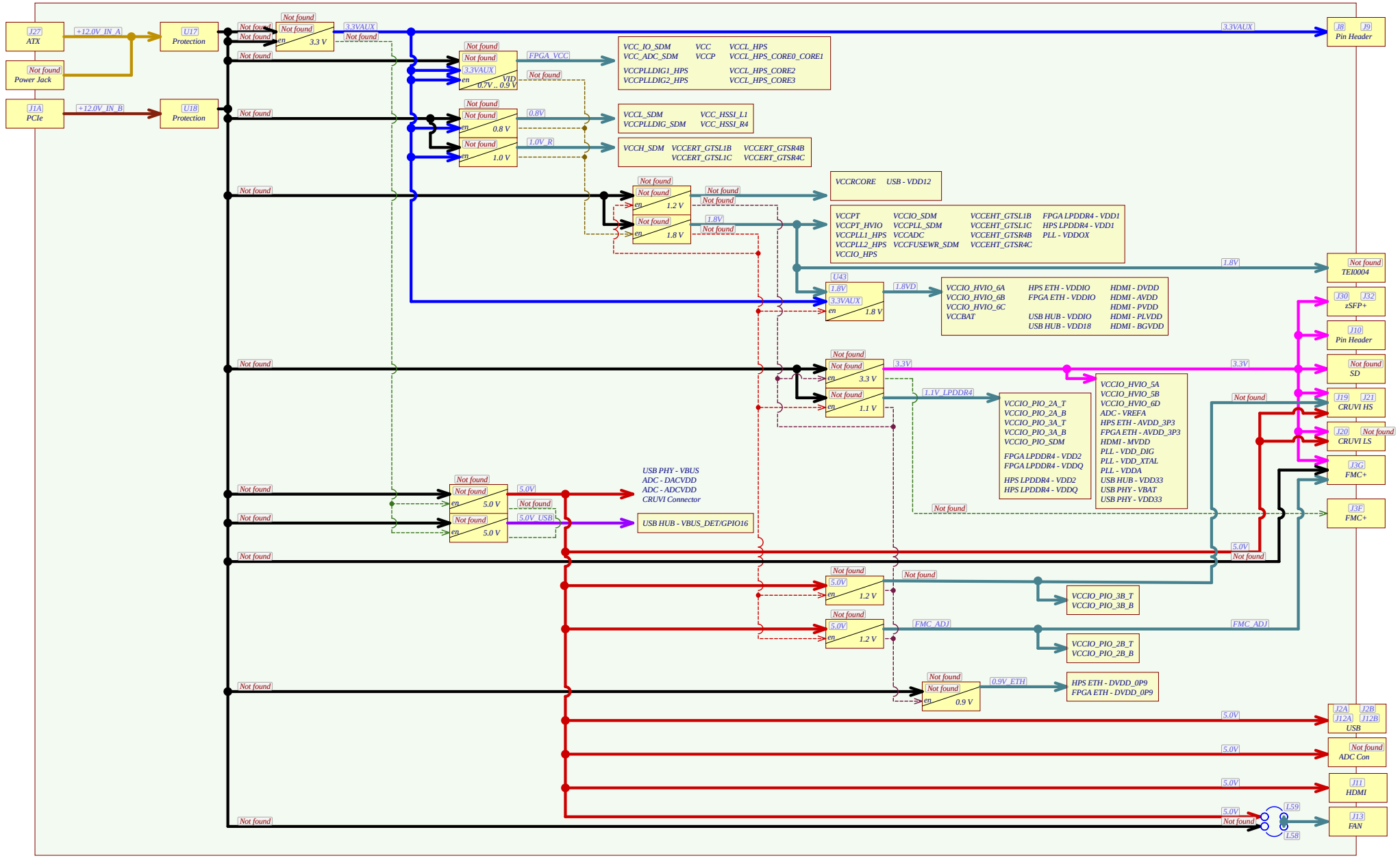
Legend:

Connector | LED Interface | Switchable Interface | On-board Components

Title: TEI0185 - System Overview		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 31.03.2026	Copyright: Trenz Electronic GmbH	Page 1 of 50
Filename: System Overview.SchDoc		

REV	Description	
-01	Initial revision	VT
-02	1. Change J29 power connector 2. Added clock signal 25MHz HPS_OSC_CLK1 to HPS_IOA_12 3. Added series resistor R394 to HPS_OSC_CLK1 4. Changed resistors value R169, R172, R179, R190 33R to 100R 5. DIPSW1 connected from HPS_IO12 to HPS_IO2 6. Added additional clock signal FPGA_25M_CLK to FPGA (pin U1.A23). Net Not found (pin U1.A23) connect to pin U1.B14 7. Added series resistor R396 to FPGA_25M_CLK 8. Added resistor Not found (set as DNP) 9. Added ability to recognise PCB version (pin U1.A8 is connected to GND)	VT
-03	1. Swapped nets ETH1_RXCK and ETH1_RXD1 2. Changed voltage 1.2V to VIO_CRUVI on the pull-up R371, R374 3. Fixed I2C connection on the I2C Mux (U57): SFPA_SDA<>SFPA_SCL, SFPB_SDA<>SFPB_SCL 4.Added additional resistors R397, R398 (assembly option) for select voltage VCCIO_PIO_SDM 5.Added additional resistors R399,R400,R401 to unsued JTAG FMC+ 6. Changed capacitor size 0201 to 0603 for C159 7. Changed PCB revision recognition (pin U1.A8 is set as NC, pin U1.B4 is connected to GND)	VT
-04	1. Swapped RGMII nets in bank 6C as recommended Altera specification (ug-813266, p17)	VT

Title: TE0185 - Revision Changes		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 2 of 50
Filename: Revision Changes.SchDoc		



Series	Device Group	Speed-grade	Power Option	FPGA_VCC
E	A (VID support)	1	V	0.70 V - 0.90 V *
		2	E	
		2	V	
		3	V	
	B	4	S	0.8 V
		5	S	0.78 V
		6	S	0.75 V
		6	X	0.75 V

*: The typical value is based on SmartVID programmed value.

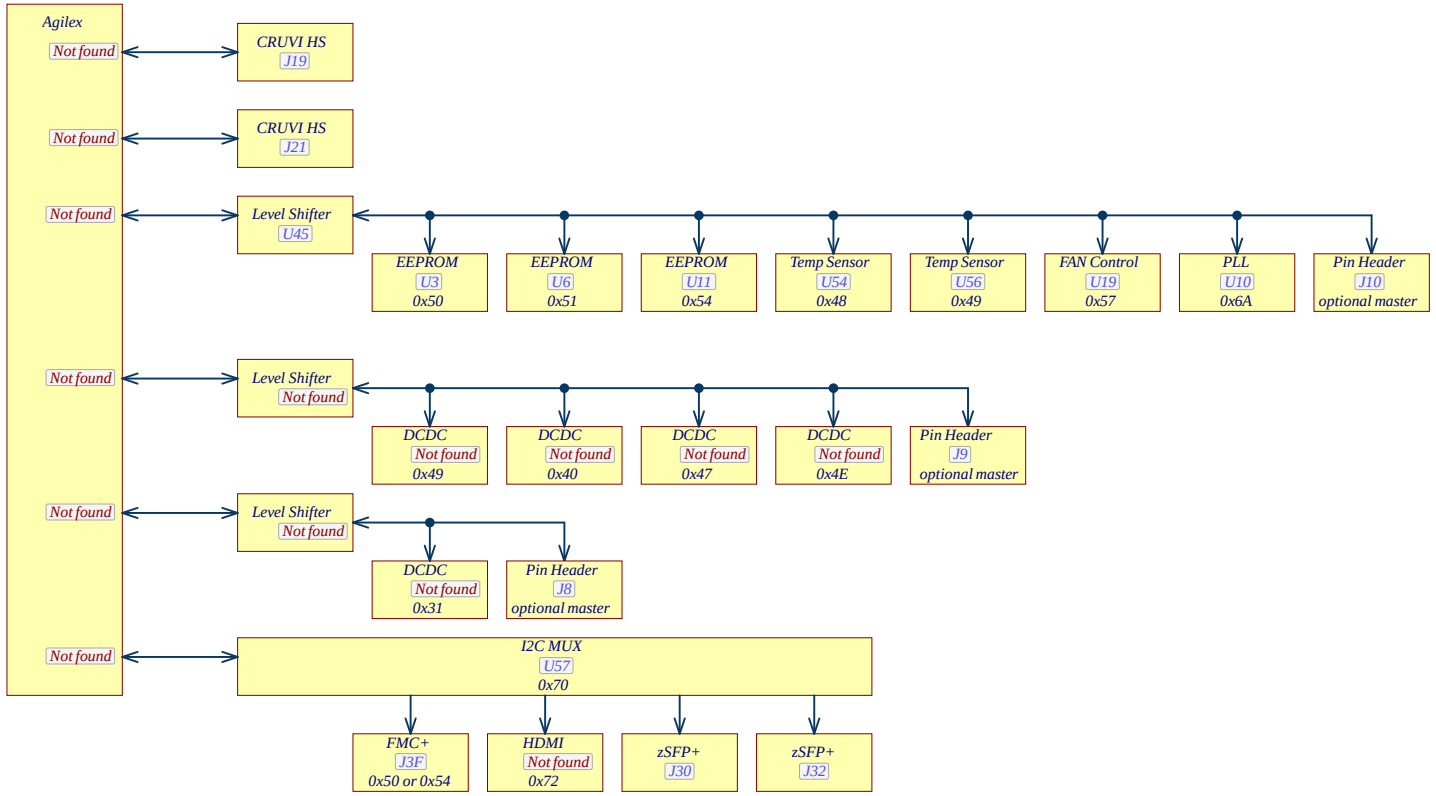
Power Option Index:

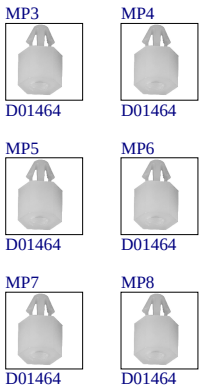
V - standard power (VID)
E - low power (VID)
S - standard power (fixed voltage)
X - low power (fixed voltage)

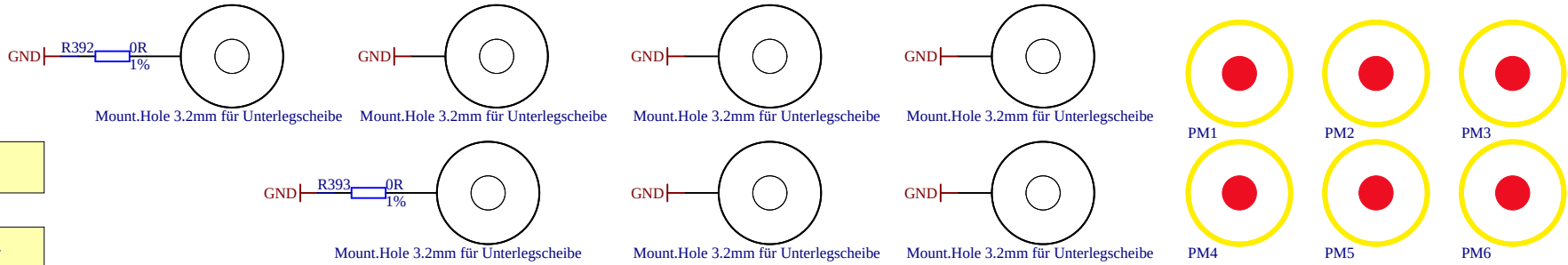
Not found — Net name
Power bus
Control signal
PI_DCIN 0.9V — Power converter

Title: TEI0185 - Power Diagram			
A3	Nummer: TEI0185 G1E13-A		Rev. 04
Datum: 24.03.2026	Copyright: Trenz Electronic GmbH		Page 3 of 50
Filename: Power_Diagram.SchDoc			

I2C Structure:







CE

CE Logo on Top Overlay

CE-TOPOVERLAY

RoHS

RoHS Logo on Top Overlay

RoHS-TOPOVERLAY

WEEE

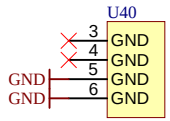
WEEE Logo on Top Overlay

WEEE-TOPOVERLAY

Serial1

Serial

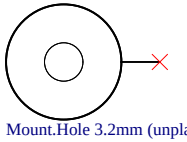
Serialnumber 6,3 x 6.3mm



Single FMC Commercial Baseboard Snap

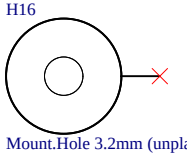
Design drawn by: VT		Title: TEI0185	
Checked by:			
Assembly variant: G1E13-A		A4	Number: TEI0185 G1E13-A	Rev. 04
Created by:			
Modified by:		Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 4 of 50
Modified at:		Filename: TEI0185.SchDoc	

H14



Mount.Hole 3.2mm (unplated)

H16

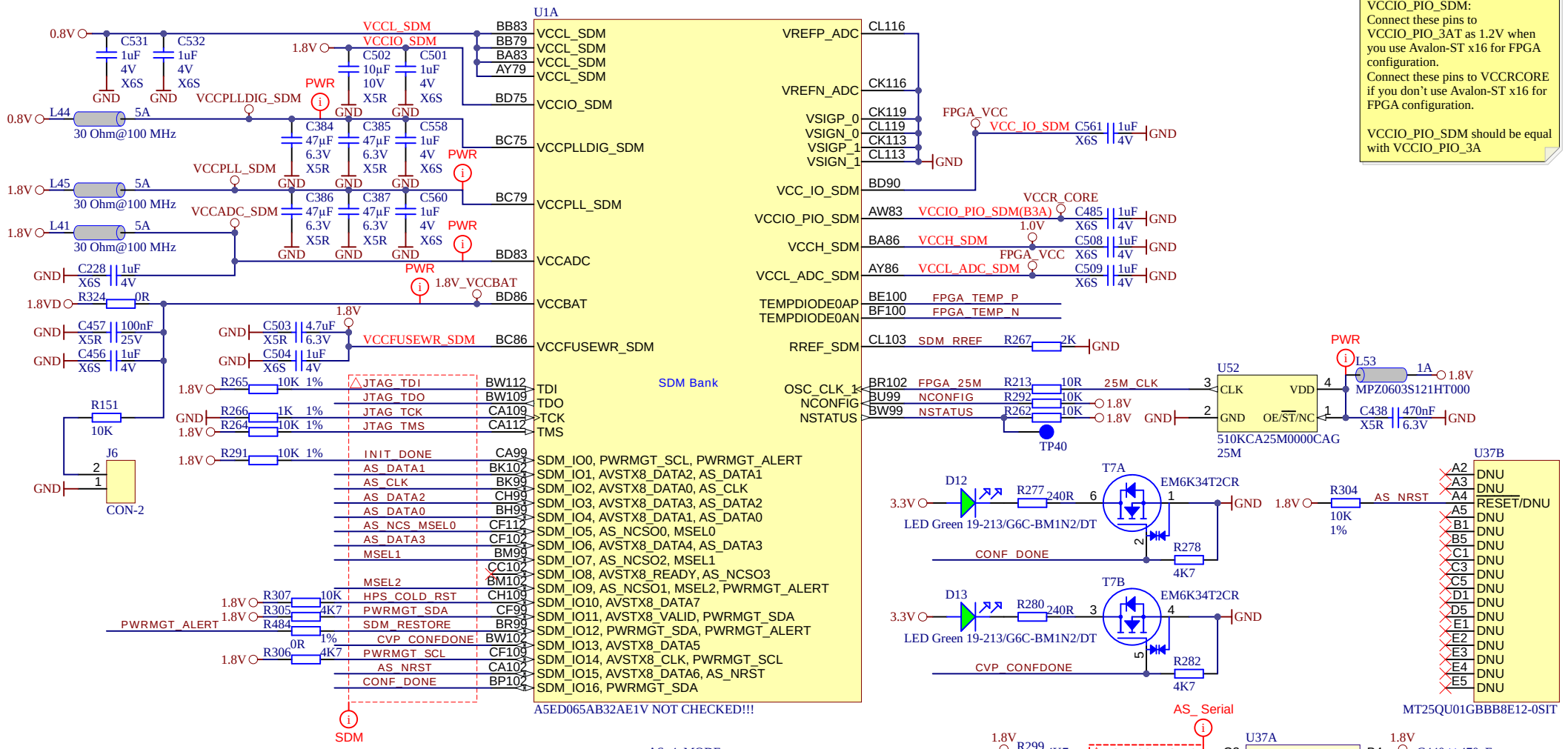


Mount.Hole 3.2mm (unplated)

KK1

Heatsink HSB43-454515P

Title: FPGA		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.04.2026	Copyright: Trenz Electronic GmbH	Page 5 of 50
Filename: FPGA.SchDoc		

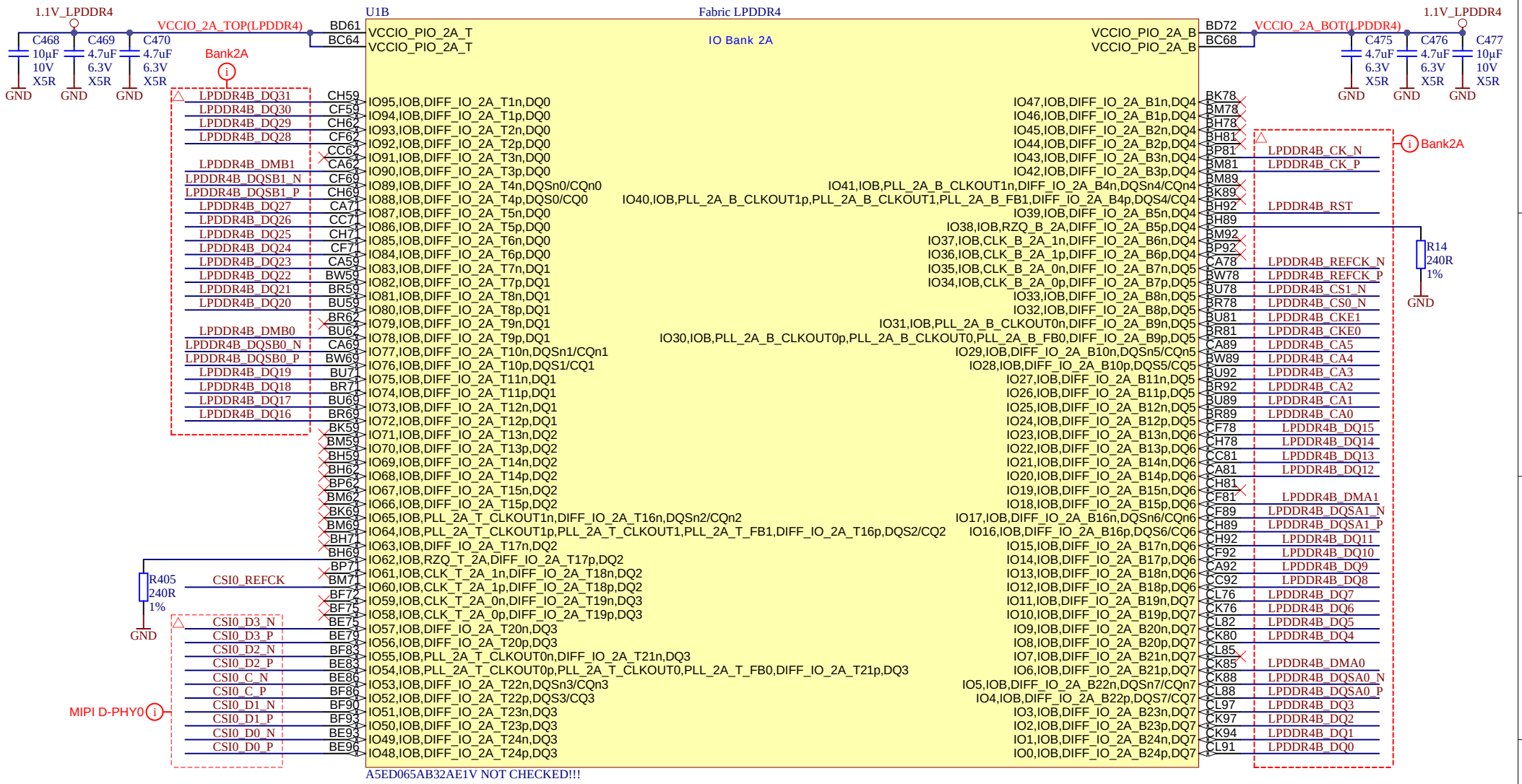


VCCIO_PIO_SDM:
Connect these pins to VCCIO_PIO_3AT as 1.2V when you use Avalon-ST x16 for FPGA configuration.
Connect these pins to VCCRCORE if you don't use Avalon-ST x16 for FPGA configuration.

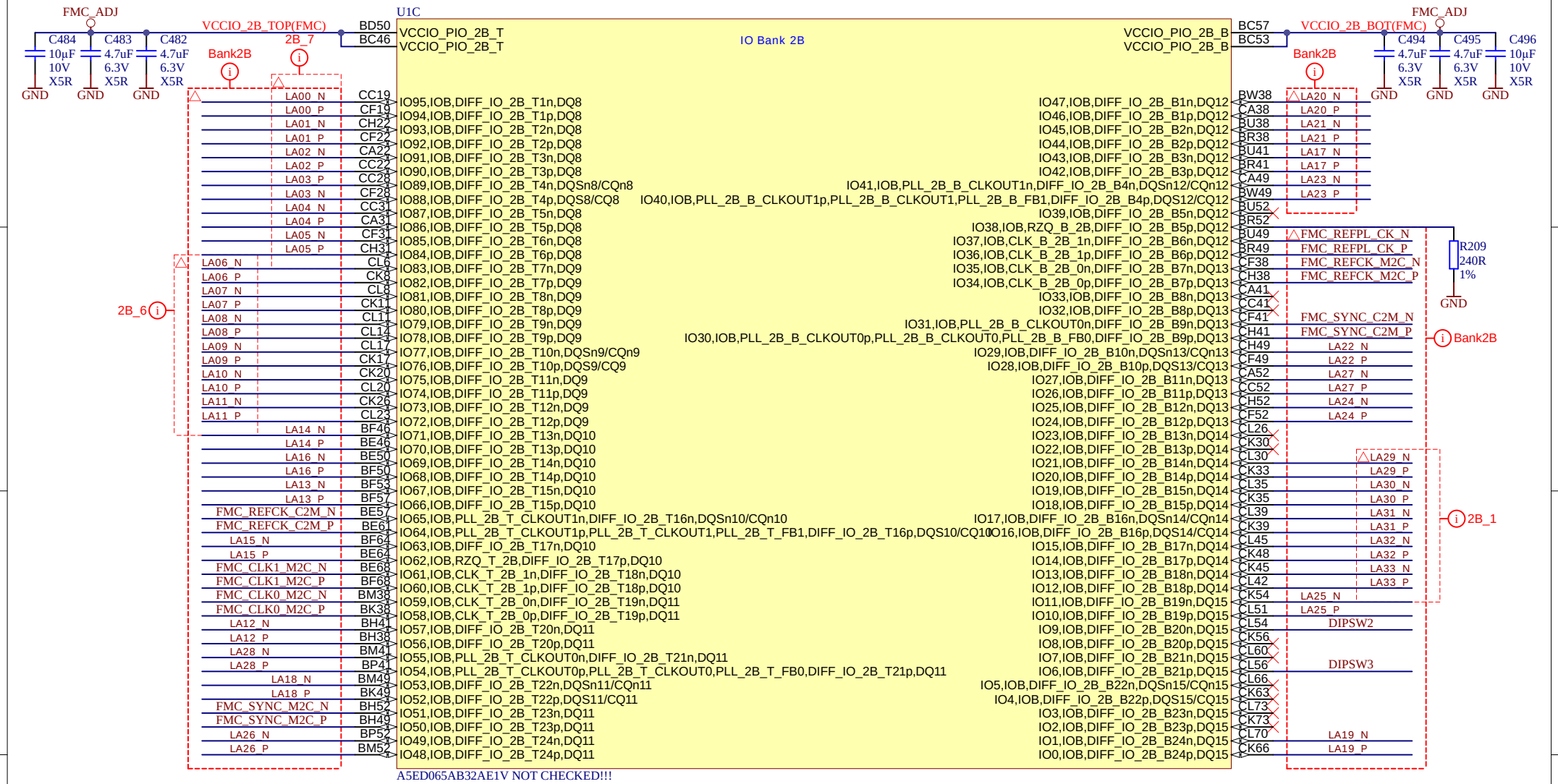
VCCIO_PIO_SDM should be equal with VCCIO_PIO_3A

BOOT MODE	MSEL2	MSEL1	MSEL0
JTAG only	1	1	1
AS (Normal mode)	0	1	1
AS (Fast mode - for CvP)	0	0	1

Title: FPGA_SDM			
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 04.05.2026	Copyright: Trenz Electronic GmbH		Page 6 of 50
Filename: FPGA_SDM.SchDoc			



Title: FPGA_2A		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 7 of 50
Filename: FPGA_Bank_2A.SchDoc		



Title: FPGA_2B		
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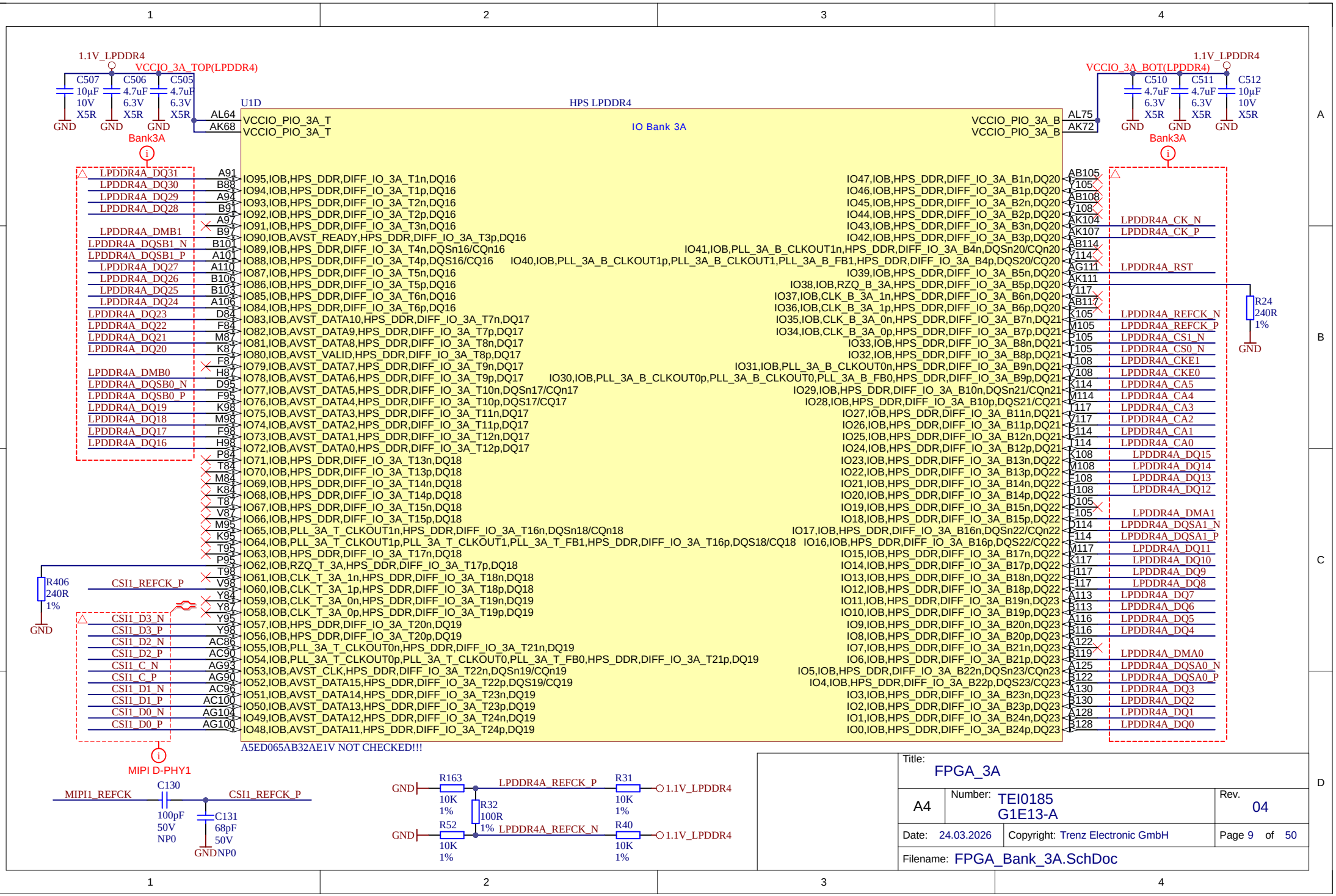
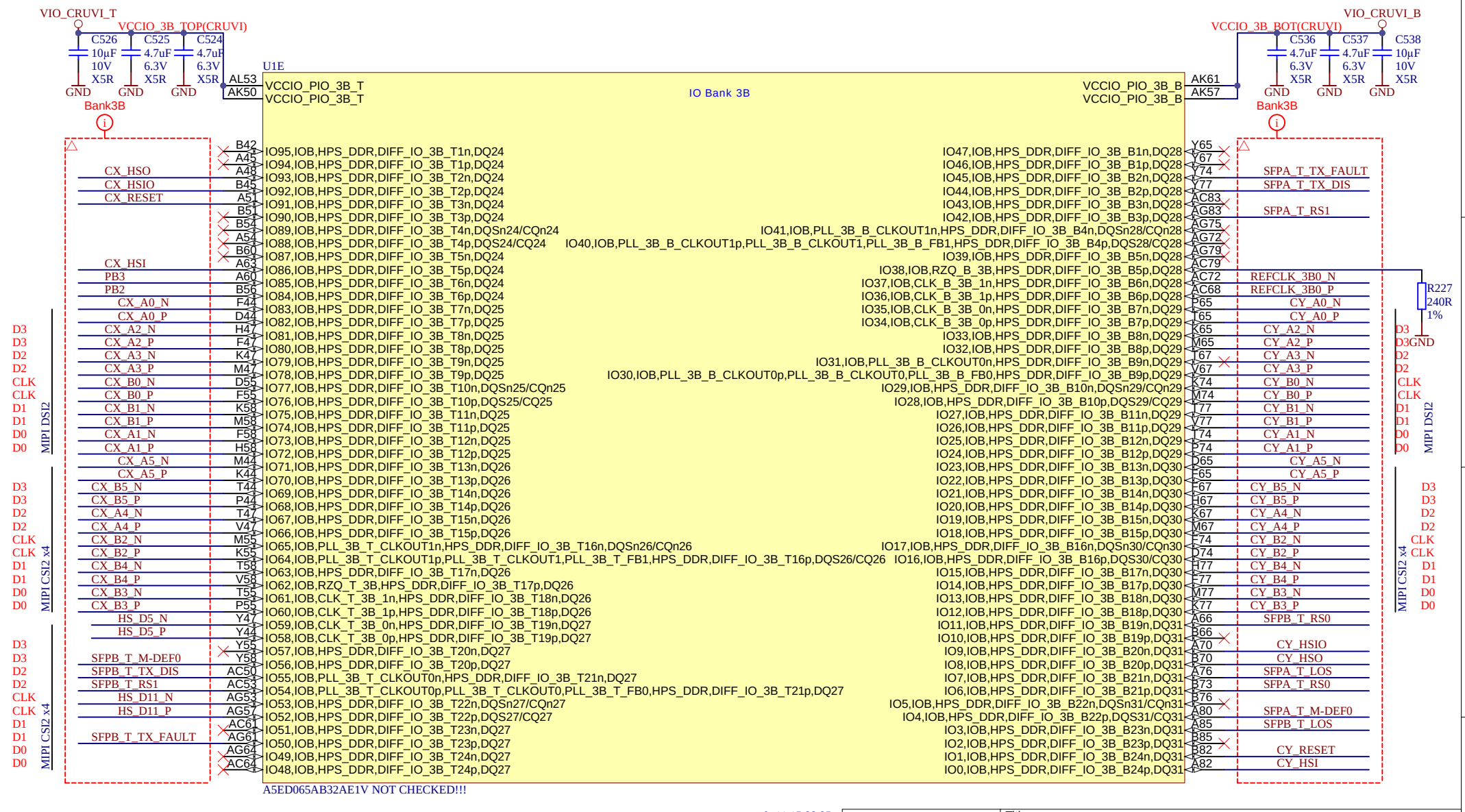
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 8 of 50
Filename: FPGA_Bank_2B.SchDoc		



Title: FPGA_3A			
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH		Page 9 of 50
Filename: FPGA_Bank_3A.SchDoc			



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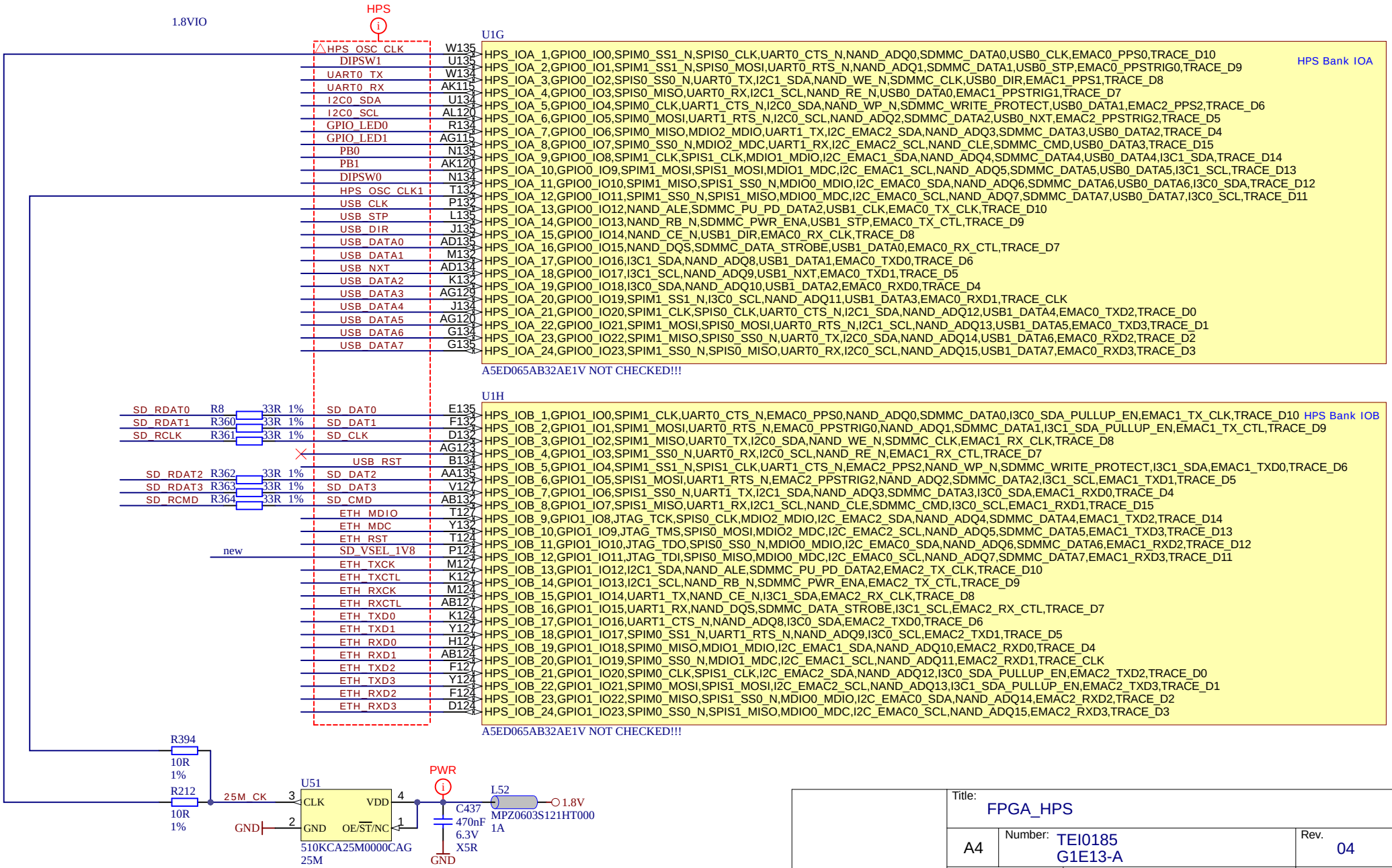
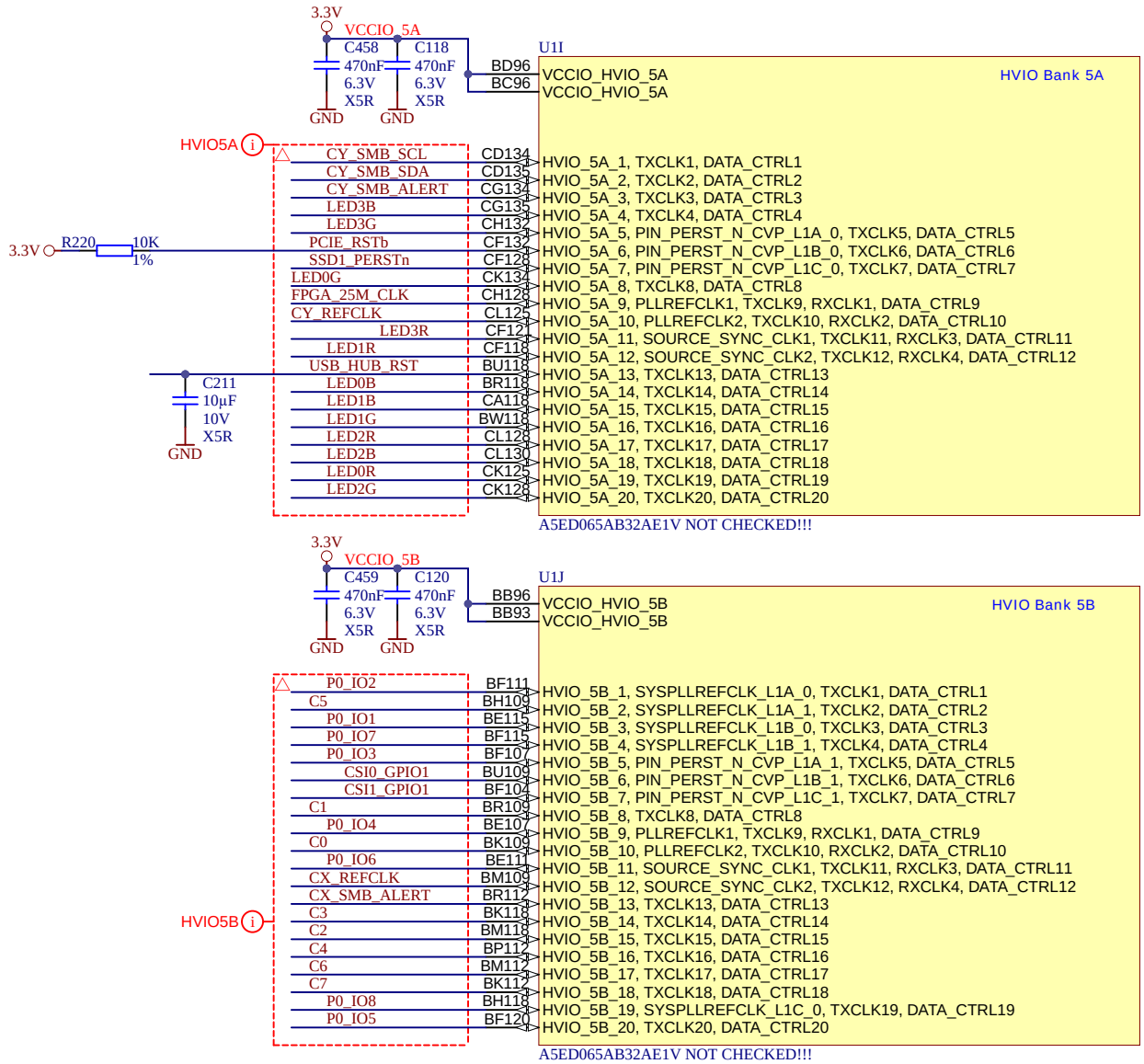
Date: 15.05.2026	Copyright: Trenz Electronic GmbH		Page 10 of 50
Filename: FPGA_Bank_3B.SchDoc			



Title: FPGA_HPS		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 11 of 50
Filename: FPGA_Bank_HPS.SchDoc		



Title: FPGA_5A_5B			
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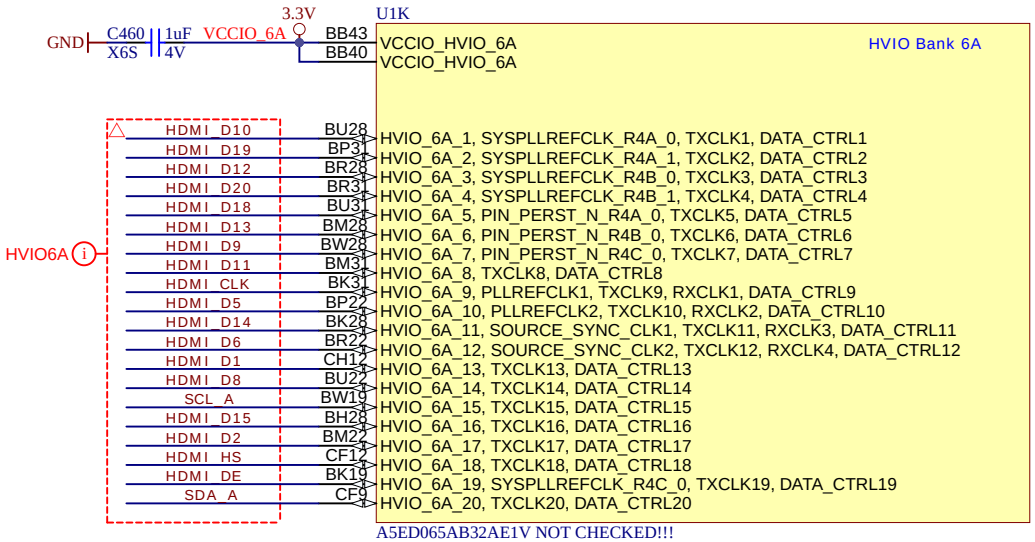
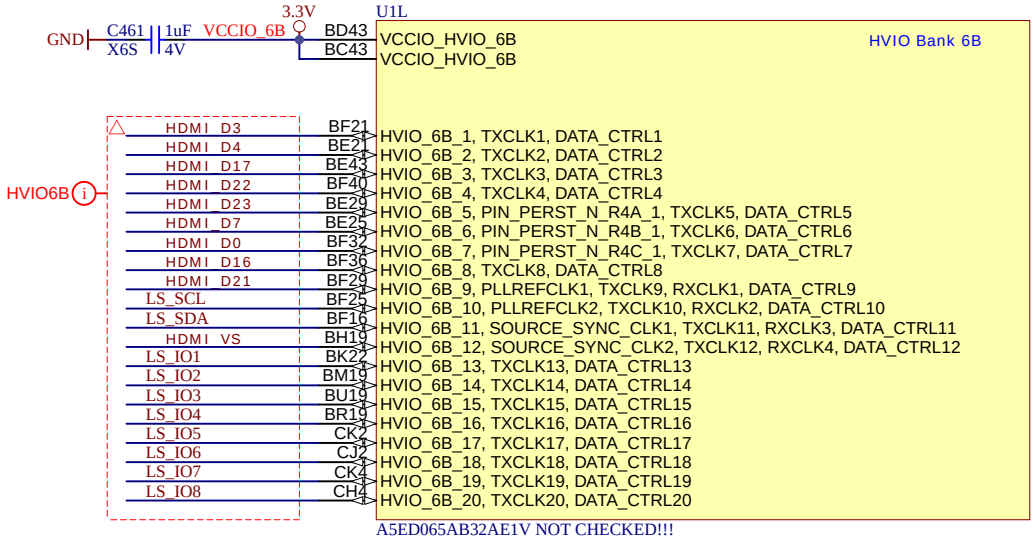
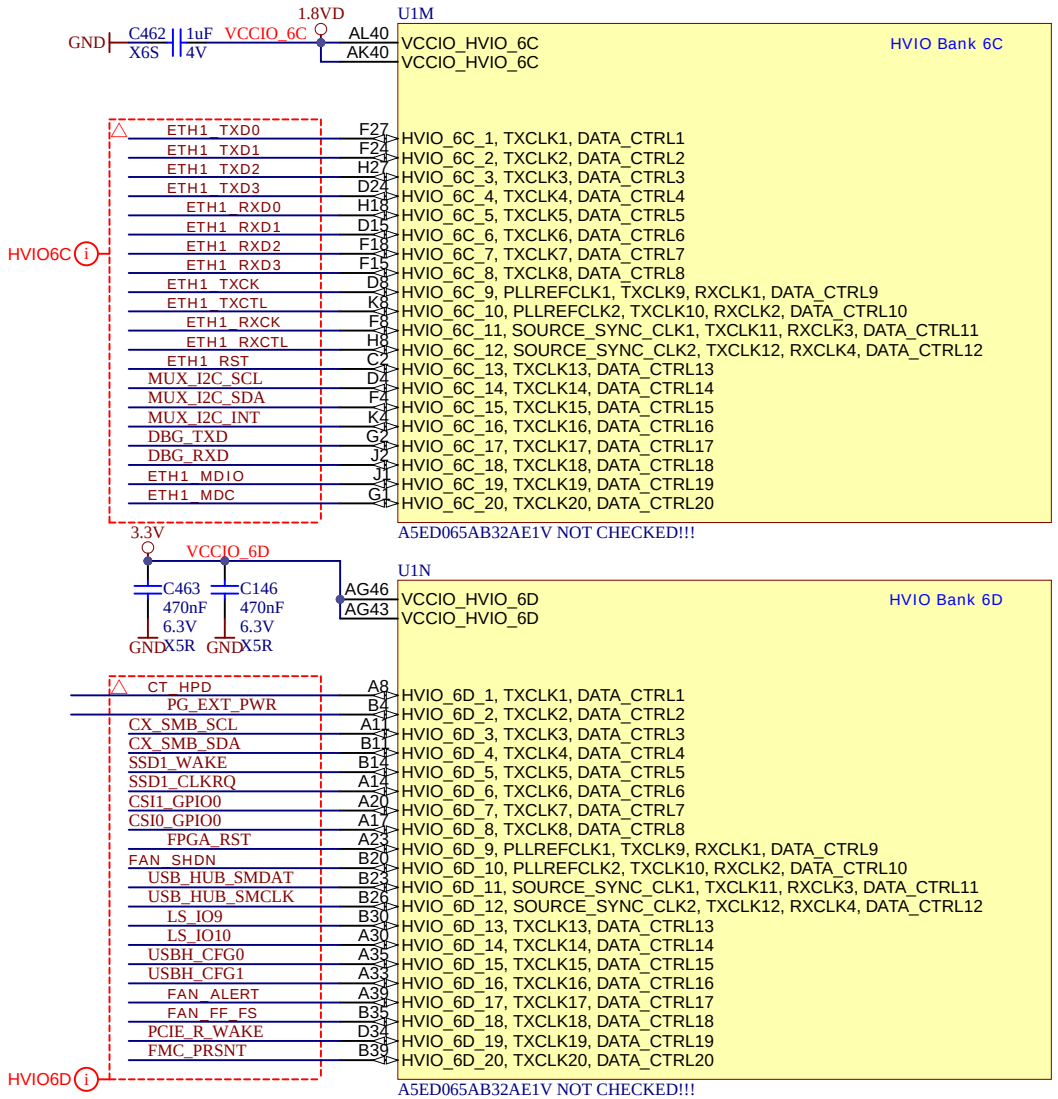
Date: 20.05.2026	Copyright: Trenz Electronic GmbH		Page 12 of 50
Filename: FPGA_Bank_HVIO_5A_5B.SchDoc			

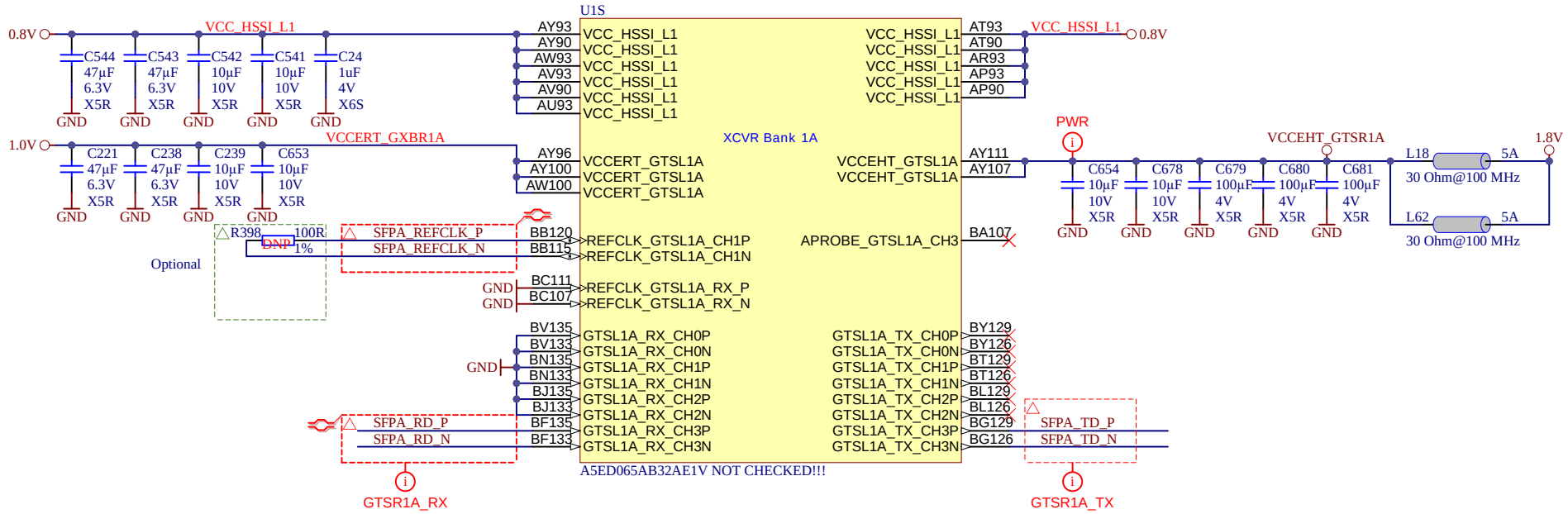




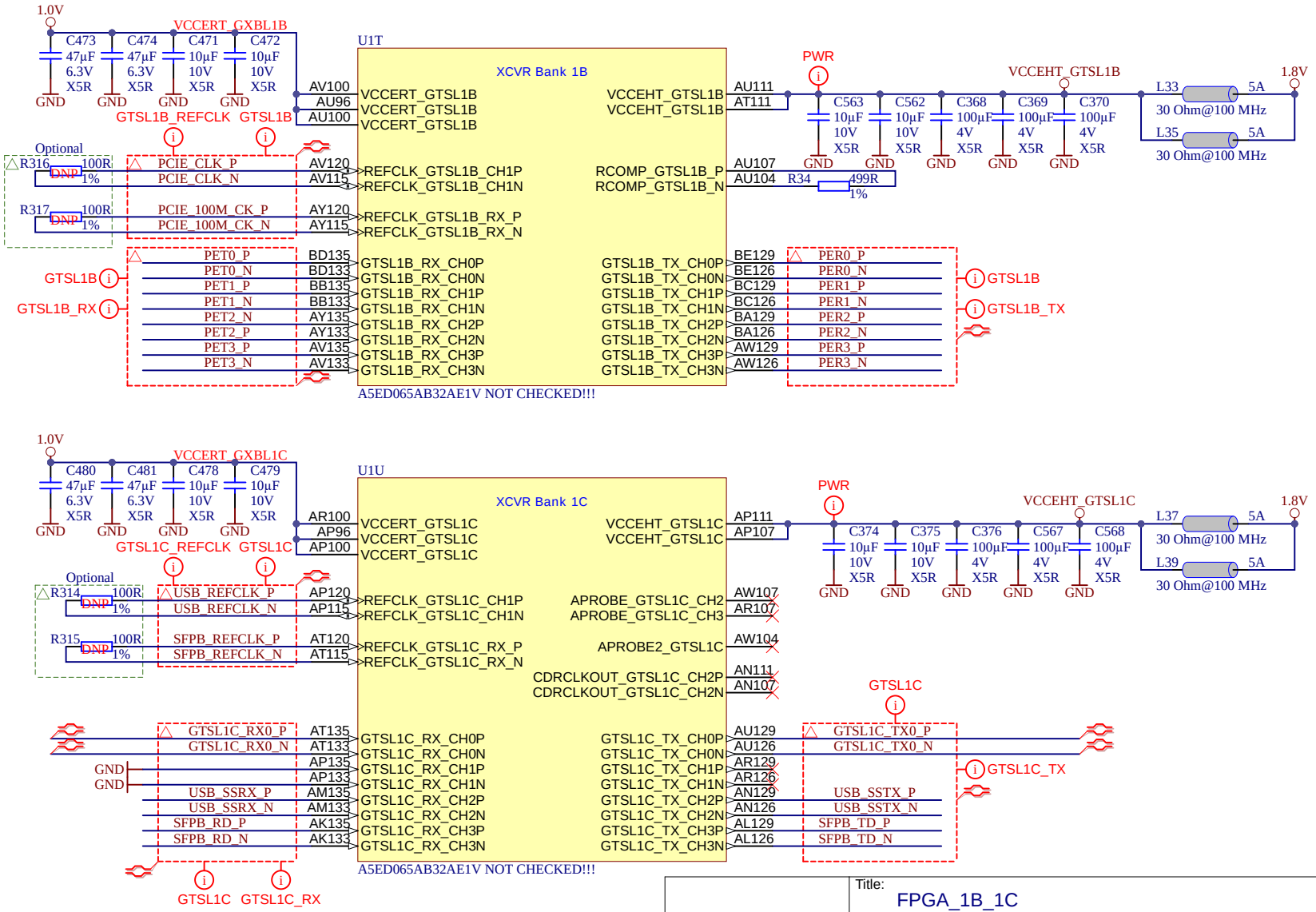
Title: FPGA_6A_6B		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 15.05.2026	Copyright: Trenz Electronic GmbH	Page 13 of 50
Filename: FPGA_Bank_HVIO_6A_6B.SchDoc		



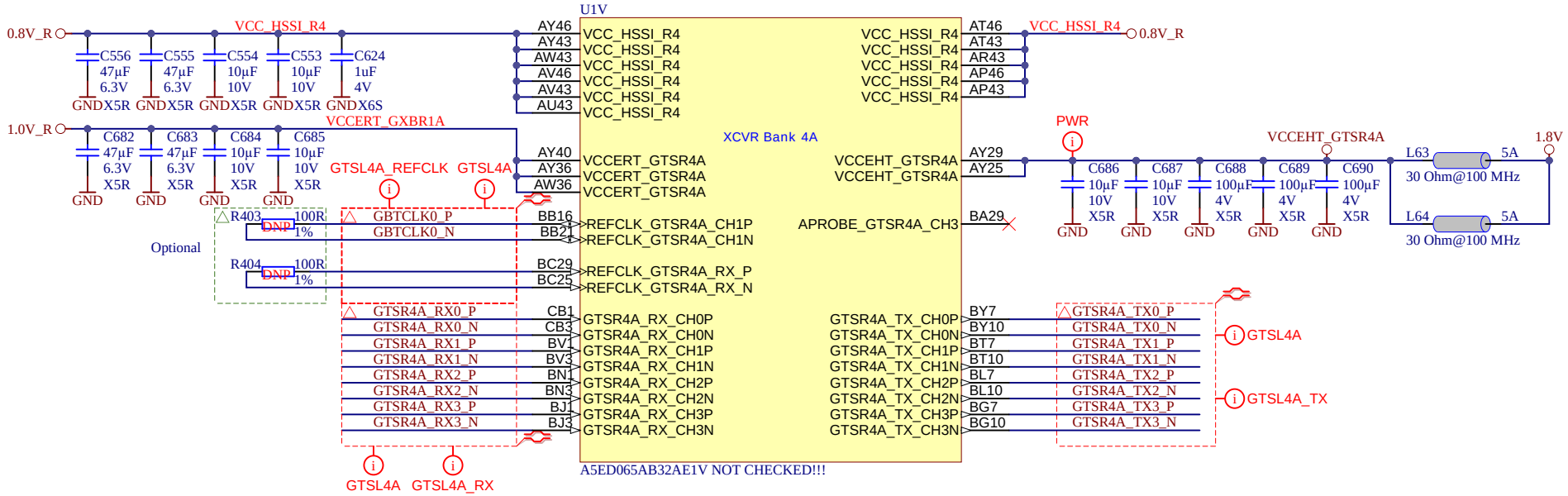
Title: FPGA_6C_6D		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 15.05.2026	Copyright: Trenz Electronic GmbH	Page 14 of 50
Filename: FPGA_Bank_HVIO_6C_6D.SchDoc		



Title: FPGA_1A		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 15 of 50
Filename: FPGA_XCVR_1A.SchDoc		



Title: FPGA_1B_1C			
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 08.05.2026	Copyright: Trenz Electronic GmbH		Page 16 of 50
Filename: FPGA_XCVR_1B_1C.SchDoc			



Title: FPGA_4A		
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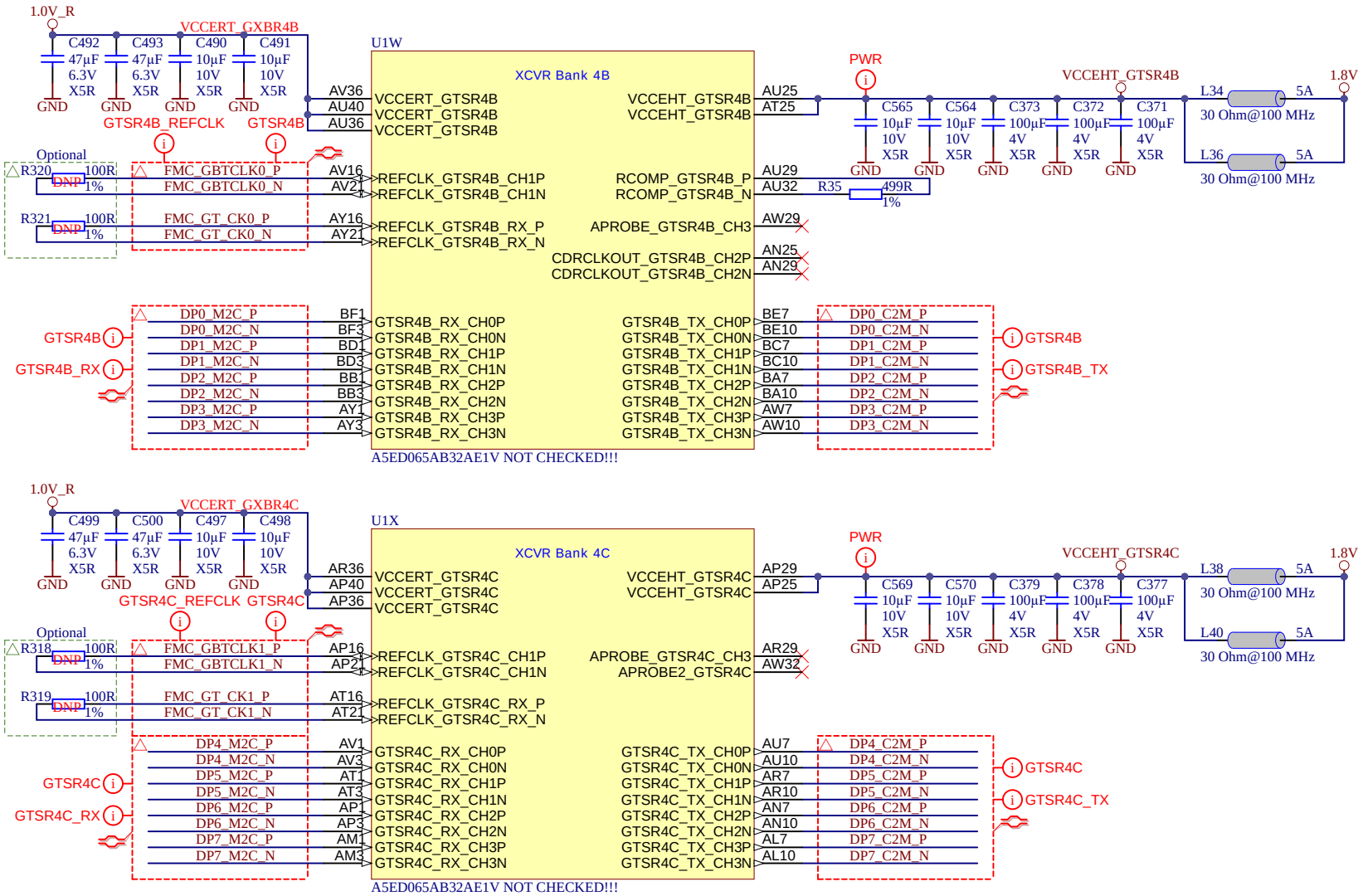
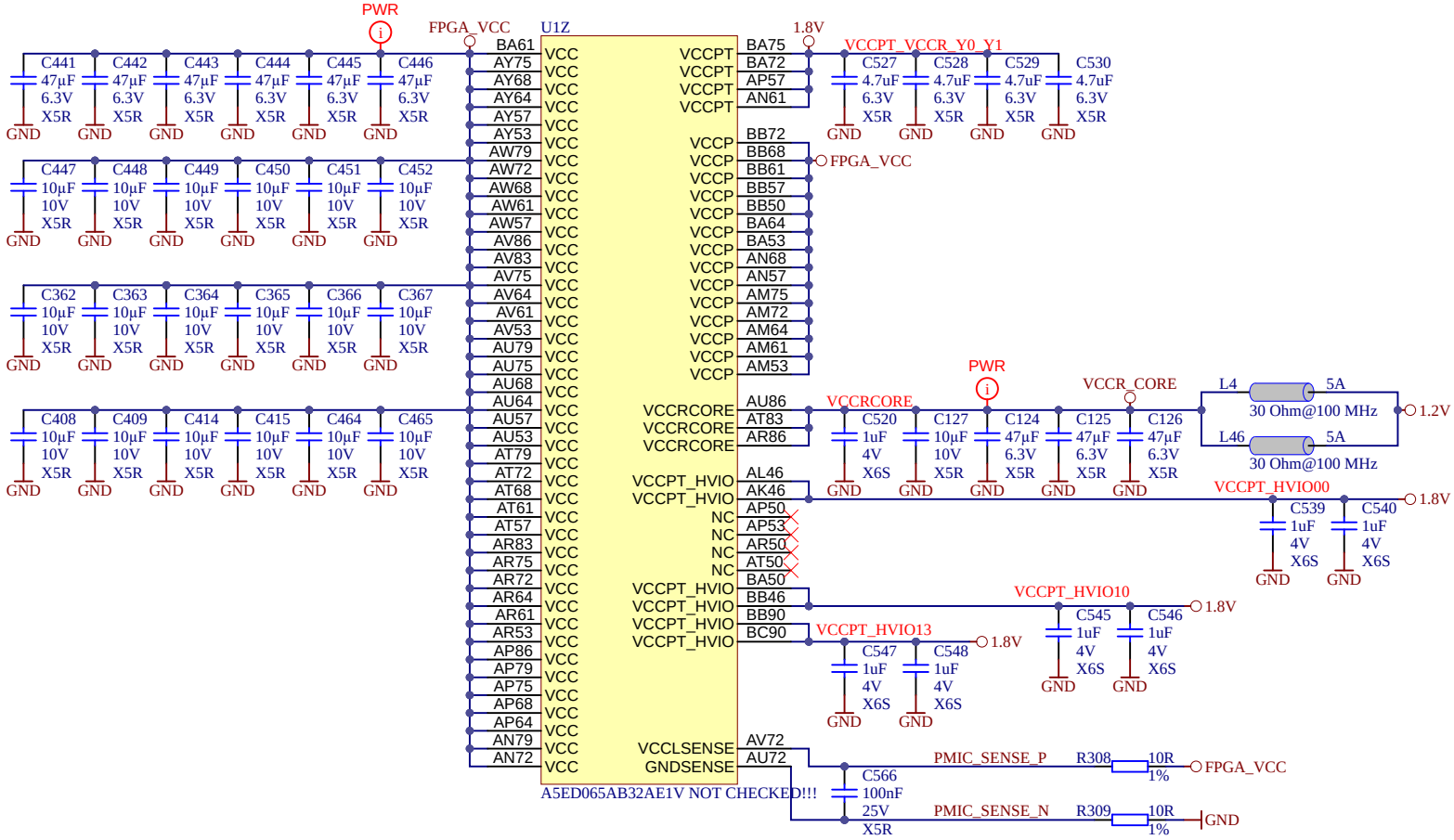
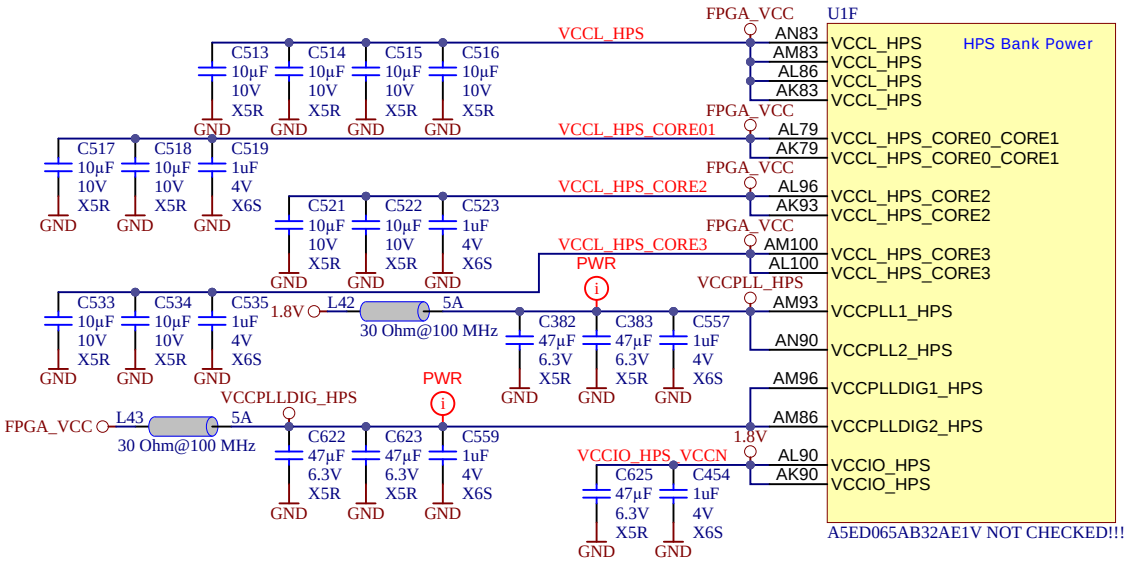
Date: 24.04.2026	Copyright: Trenz Electronic GmbH	Page 17 of 50
Filename: FPGA_XCVR_4A.SchDoc		



Title: FPGA_4B_4C		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 25.03.2026	Copyright: Trenz Electronic GmbH	Page 18 of 50
Filename: FPGA_XCVR_4B_4C.SchDoc		



Title: FPGA_Power		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 19 of 50
Filename: FPGA_PWR.SchDoc		



Title: FPGA_Power		
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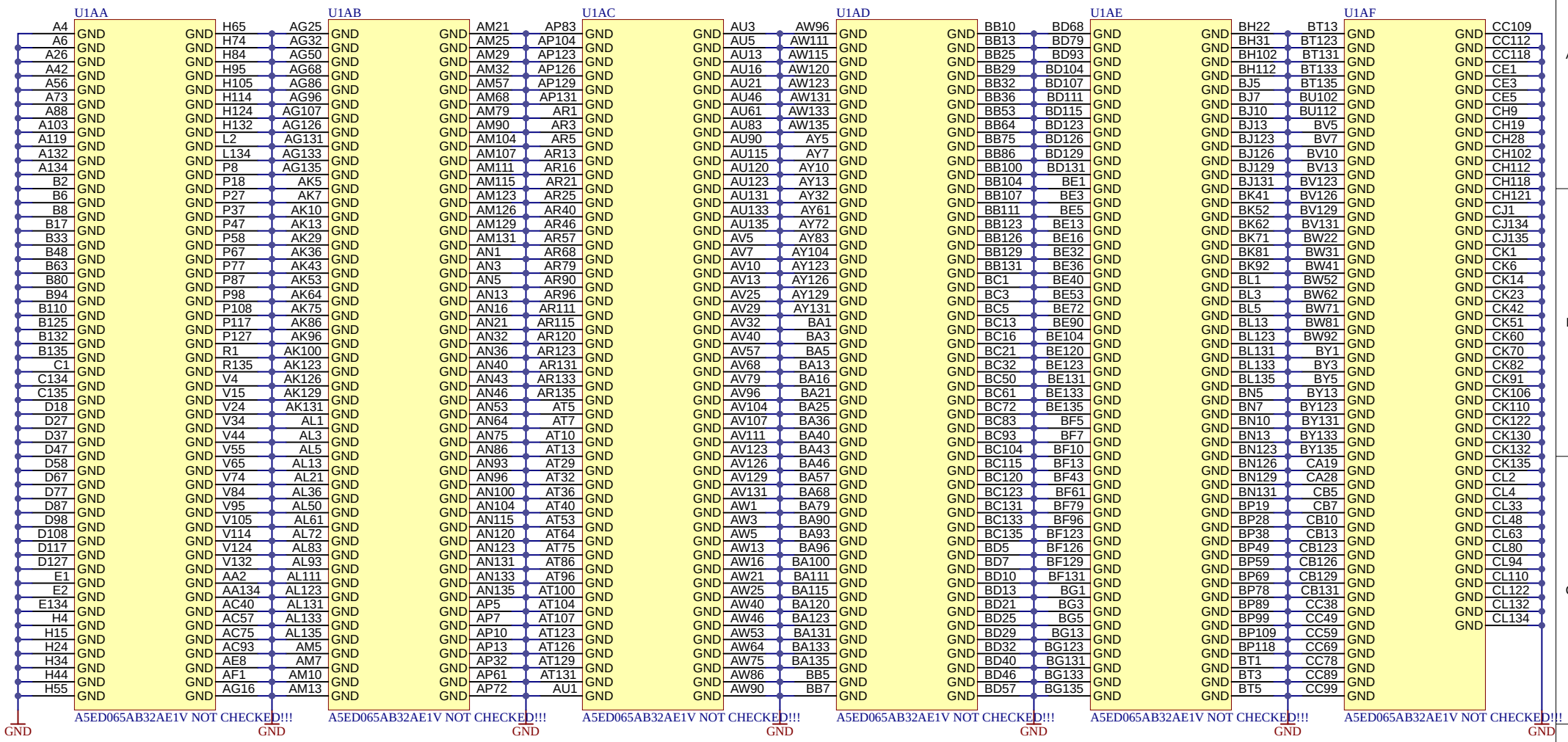
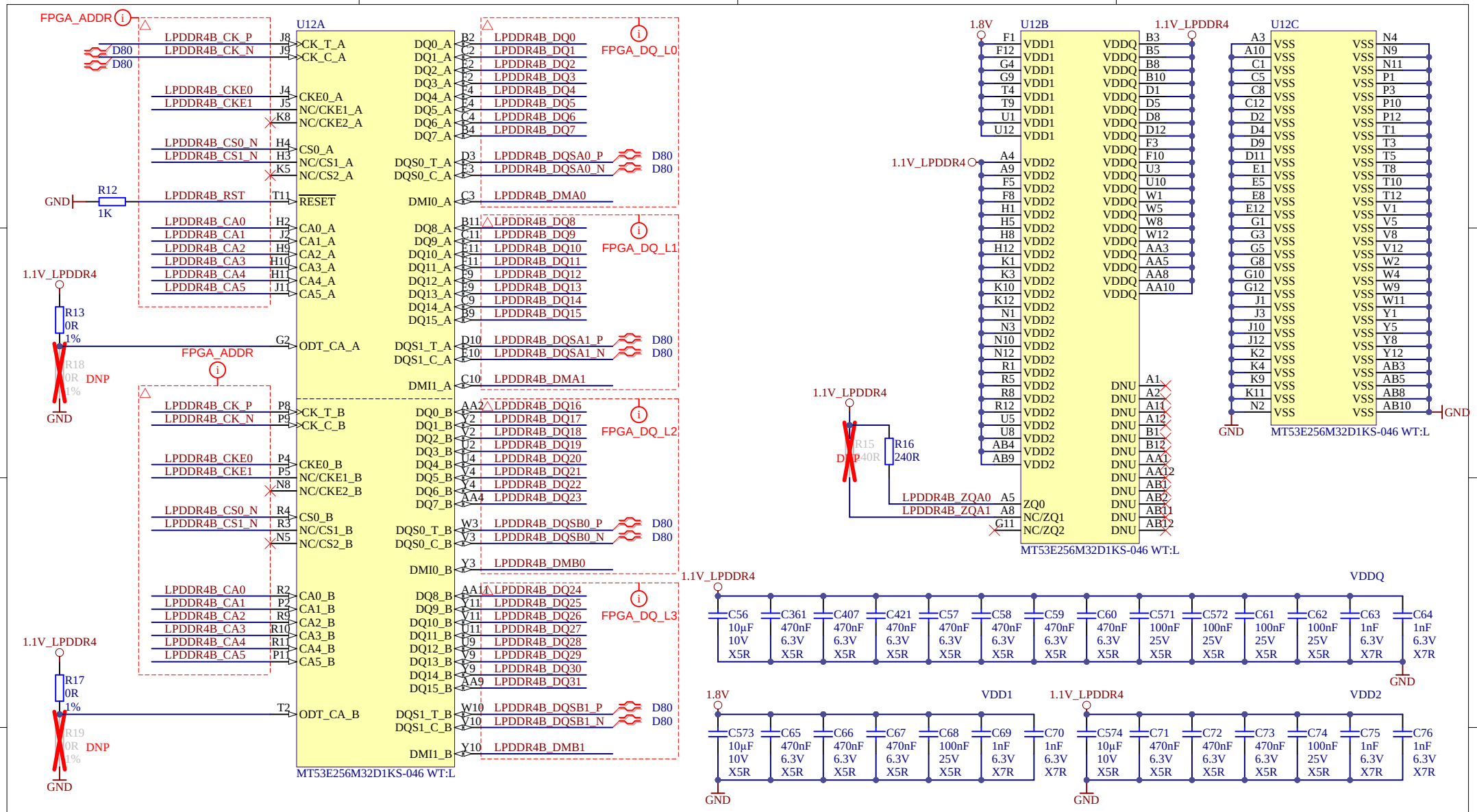
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 20 of 50
Filename: FPGA_PWR2.SchDoc		



Title: FPGA_GND		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 21 of 50
Filename: FPGA_GND.SchDoc		

Title: FPGA_GND		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 22 of 50
Filename: FPGA_NC.SchDoc		



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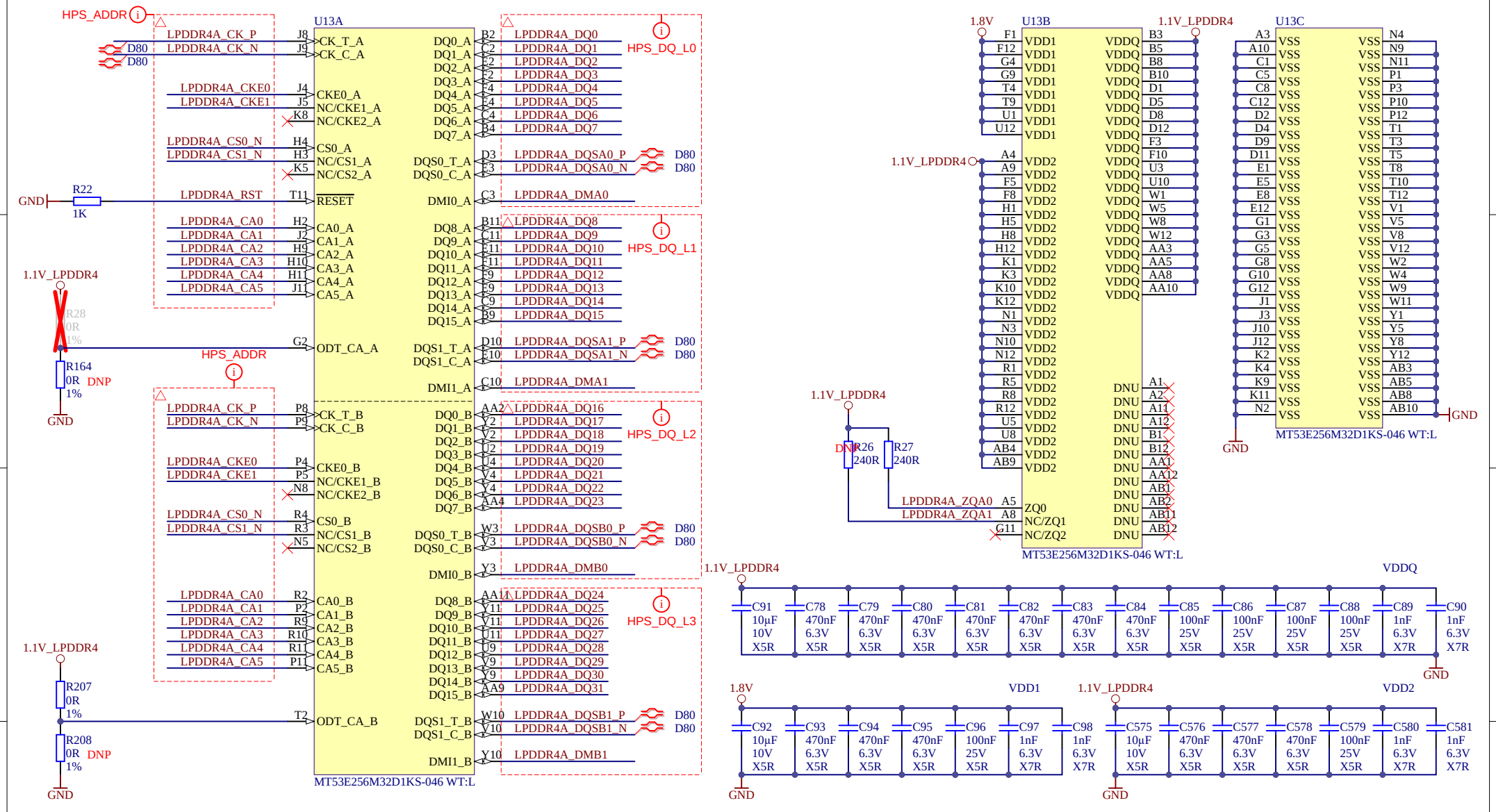
Date: 24.03.2026	Copyright: Trenz Electronic GmbH		Page 23 of 50
Filename: LPDDR4_FPGA.SchDoc			



Title: LPDDR4			
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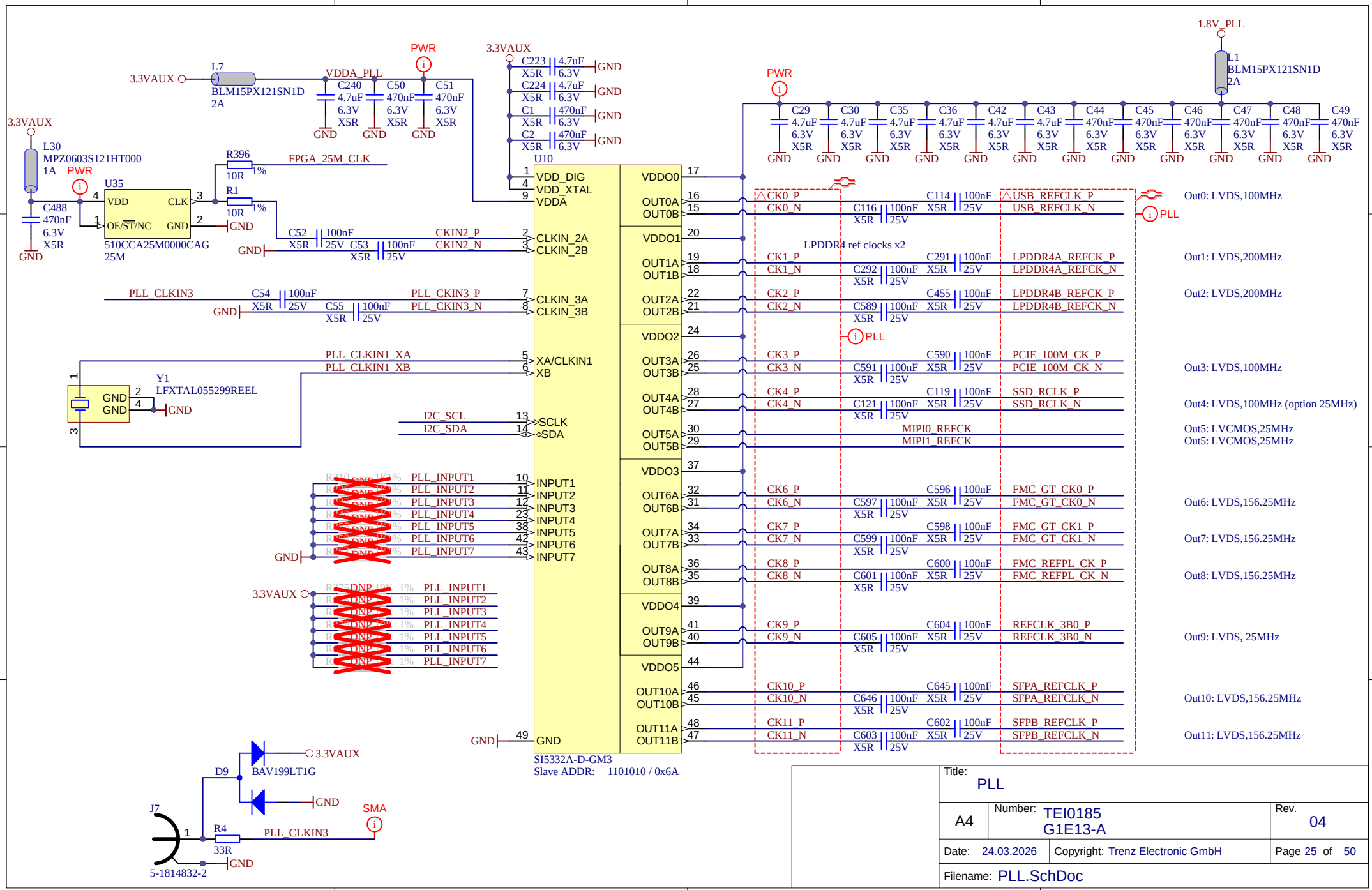
Date: 24.03.2026	Copyright: Trenz Electronic GmbH		Page 24 of 50
Filename: LPDDR4_HPS.SchDoc			



Title: PLL		
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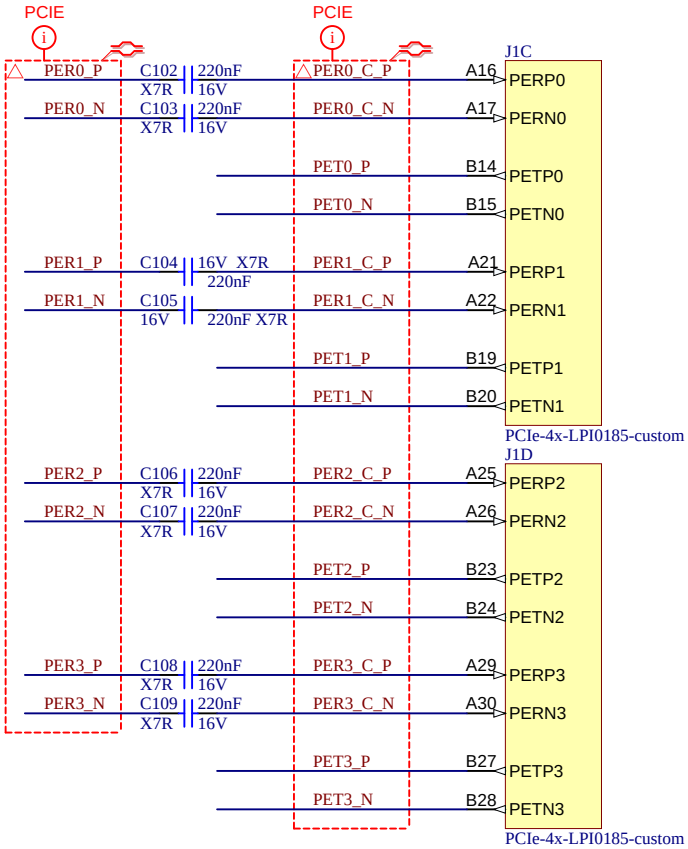
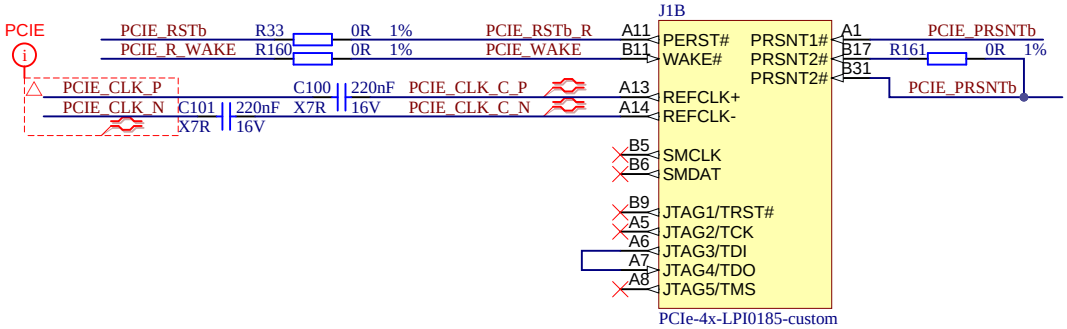
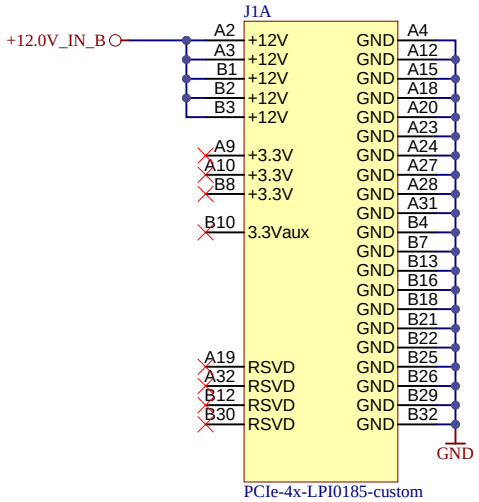
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 25 of 50
Filename: PLL.SchDoc		







Title: PCIE x4		
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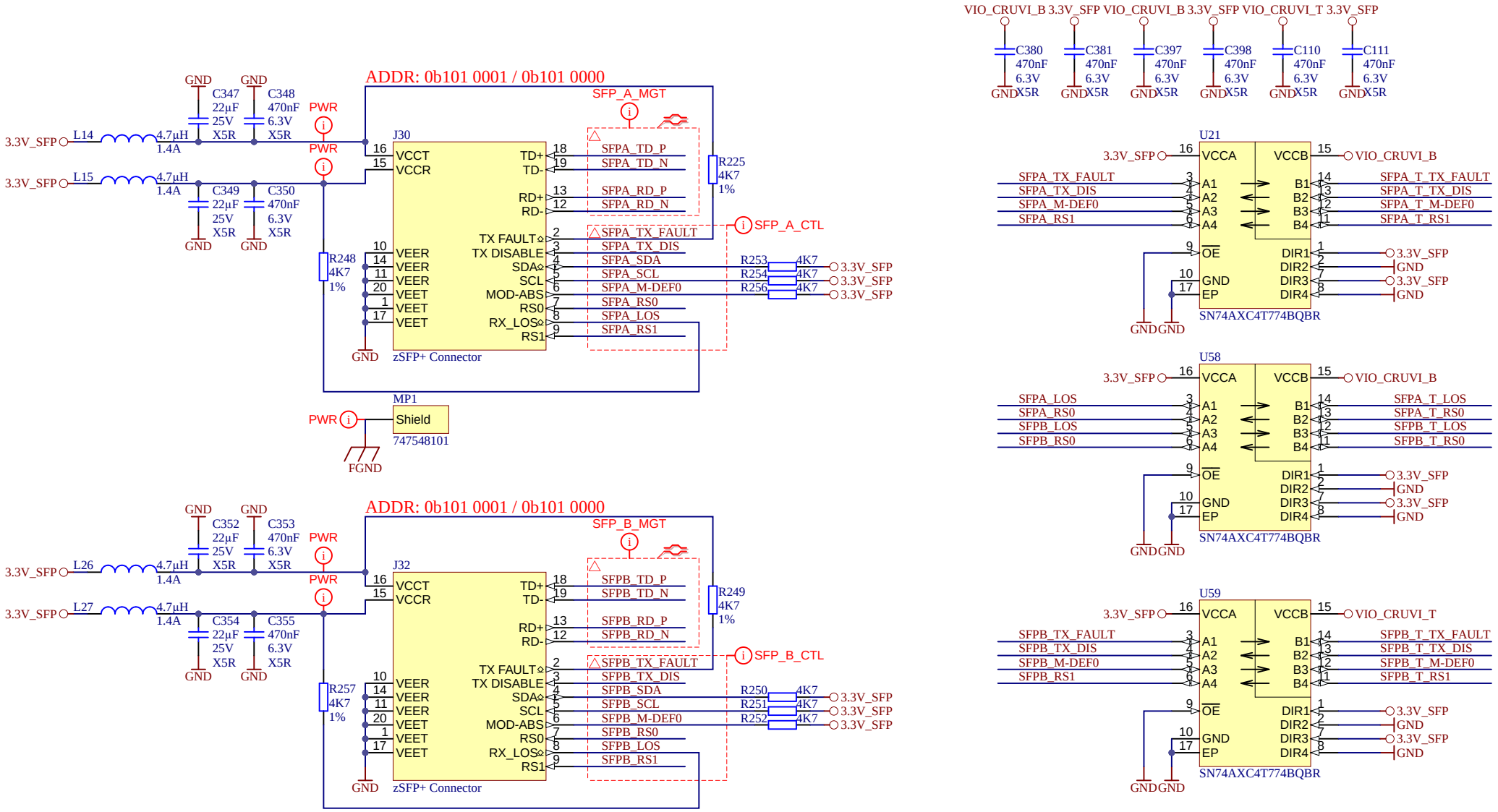
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 26 of 50
Filename: PCIE_CONN.SchDoc		



Title: zSFP+		
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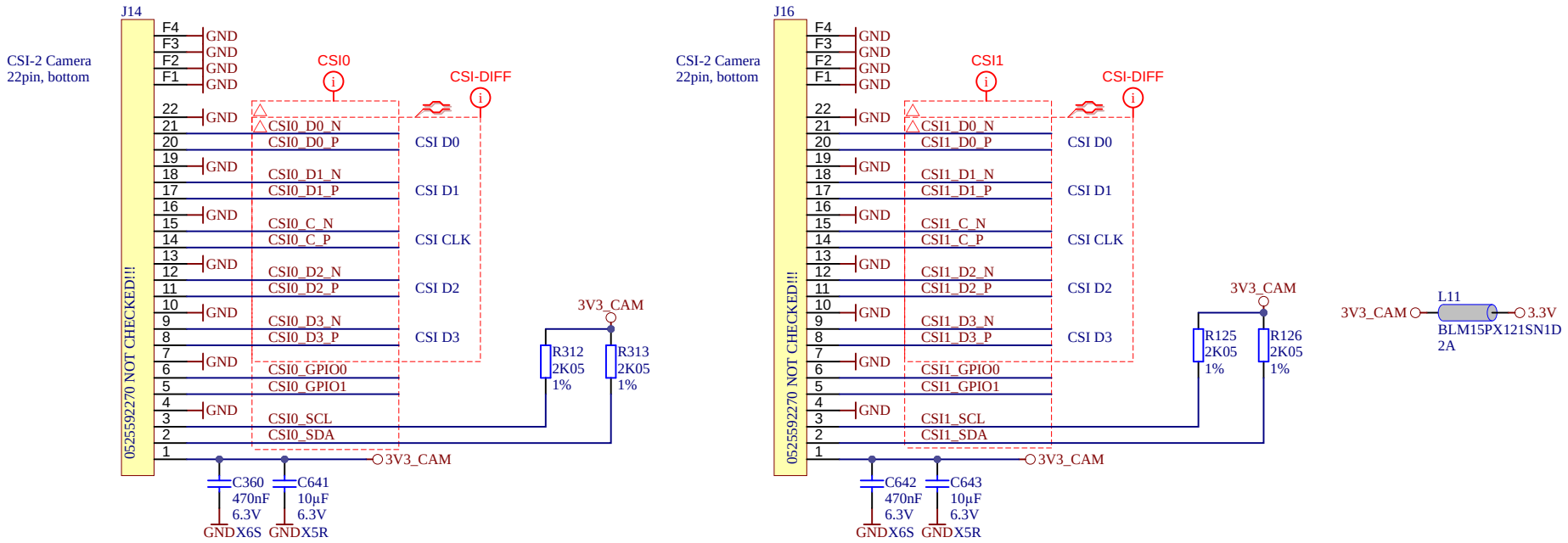
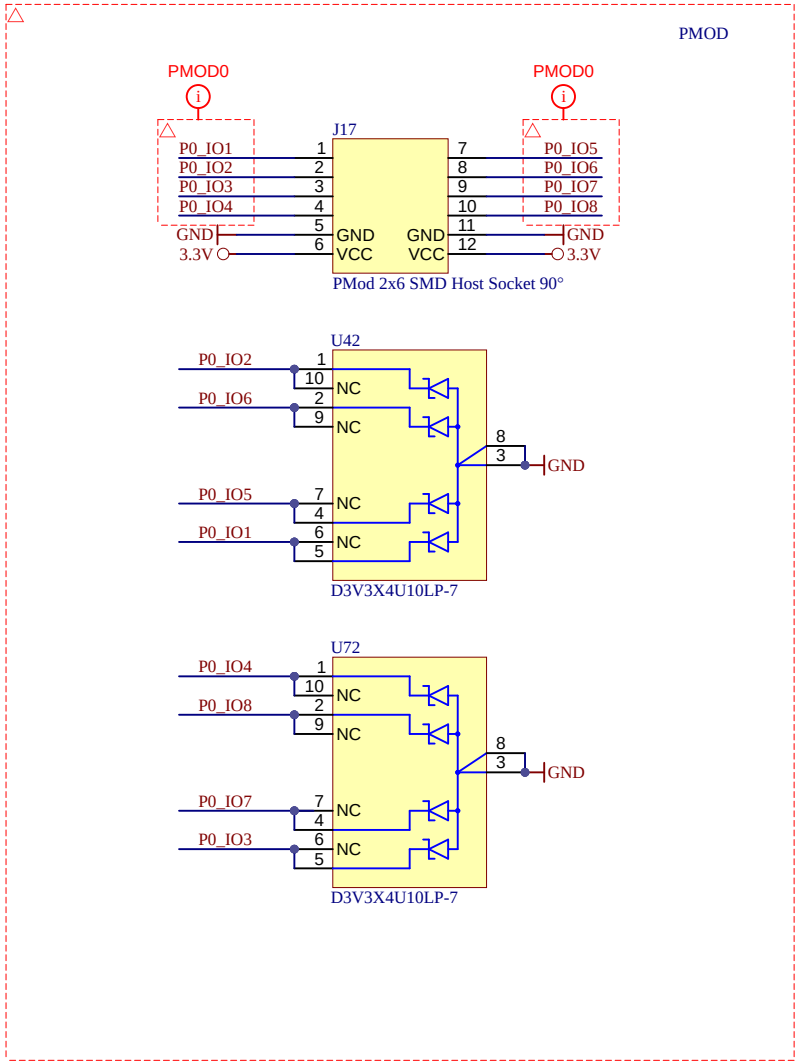
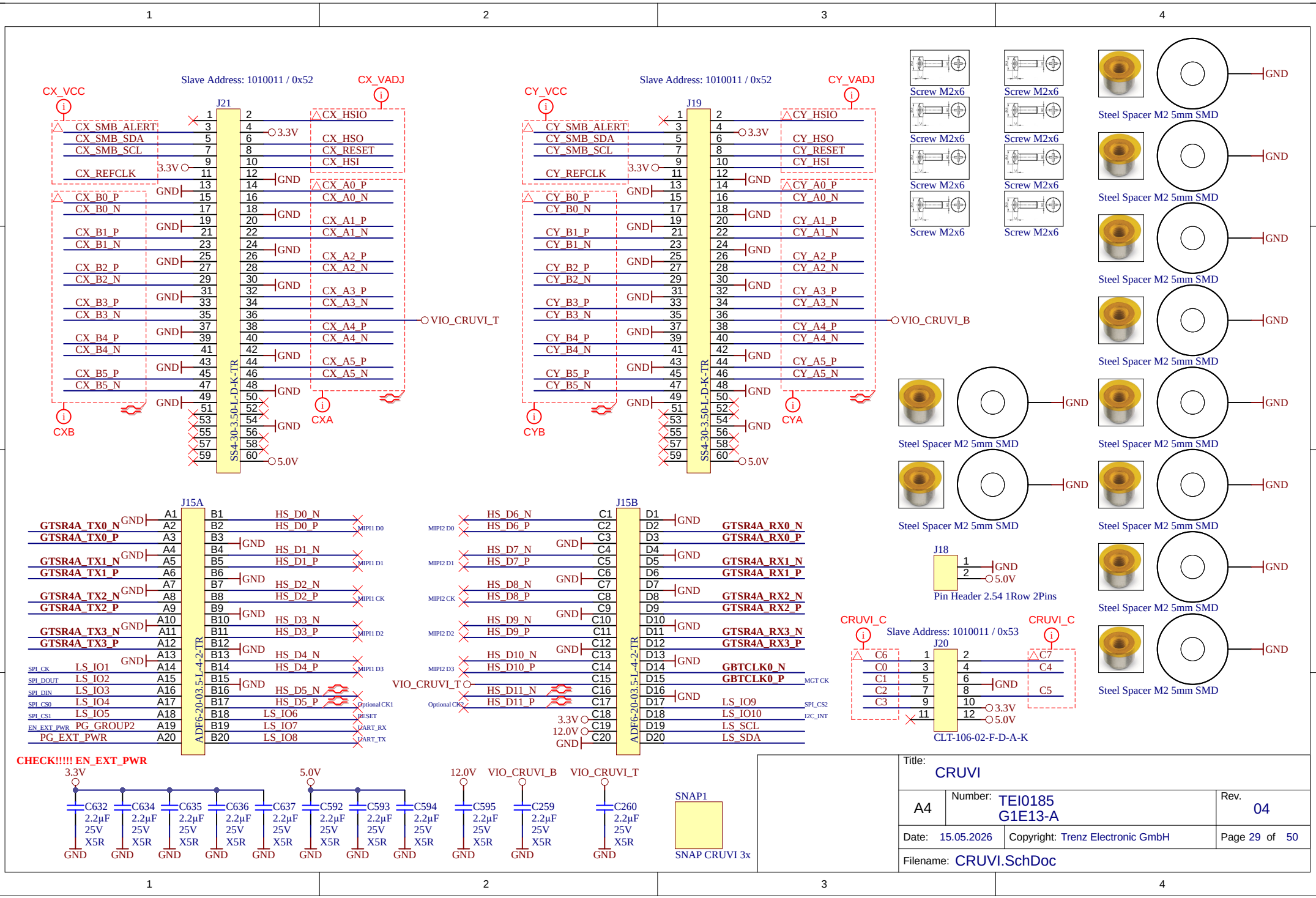
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 27 of 50
Filename: zSFP+.SchDoc		



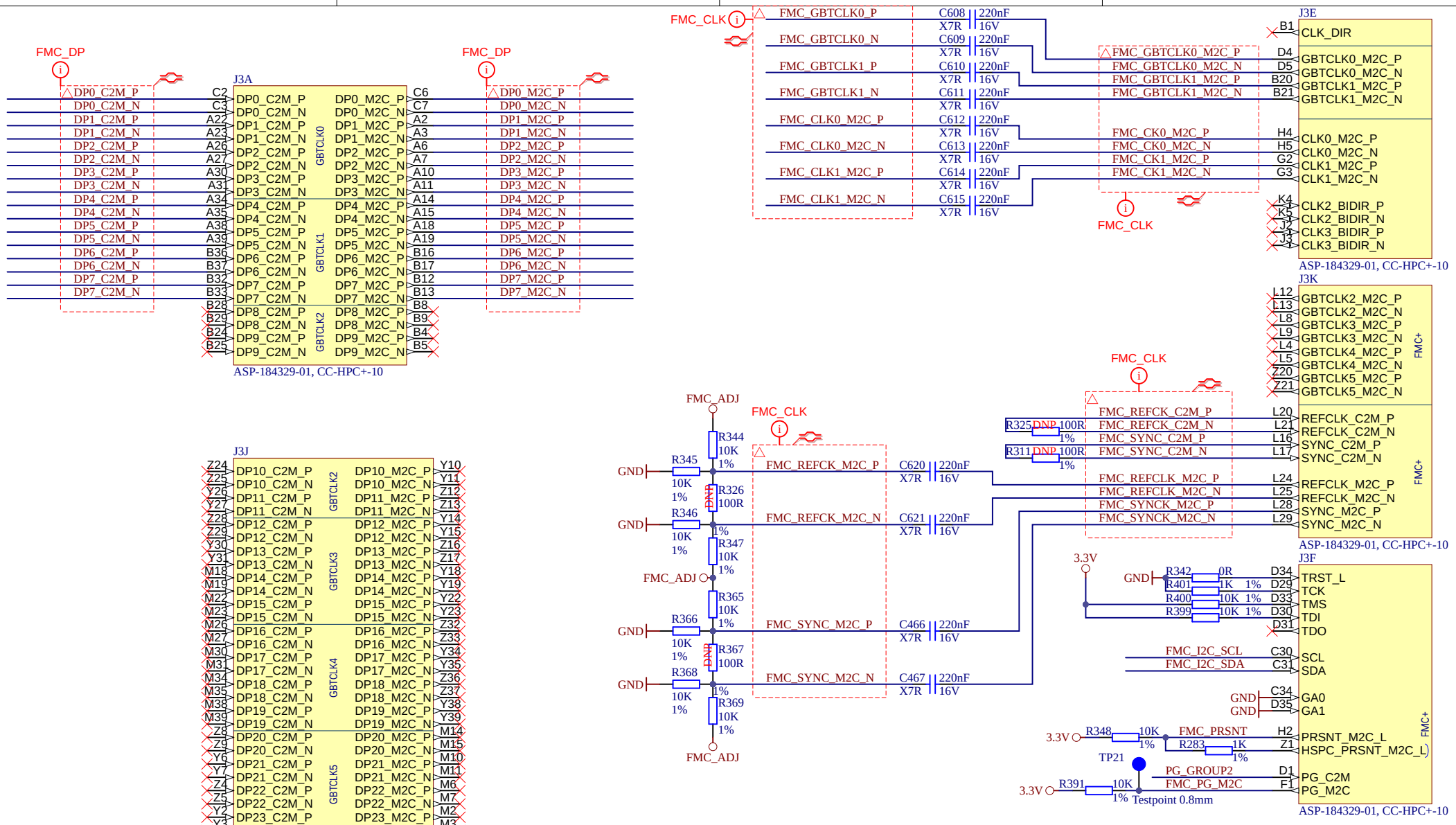
trenz electronic	Title: MIPI CSI/DSI		
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH		Page 28 of 50
Filename: CAM_0_1.SchDoc			



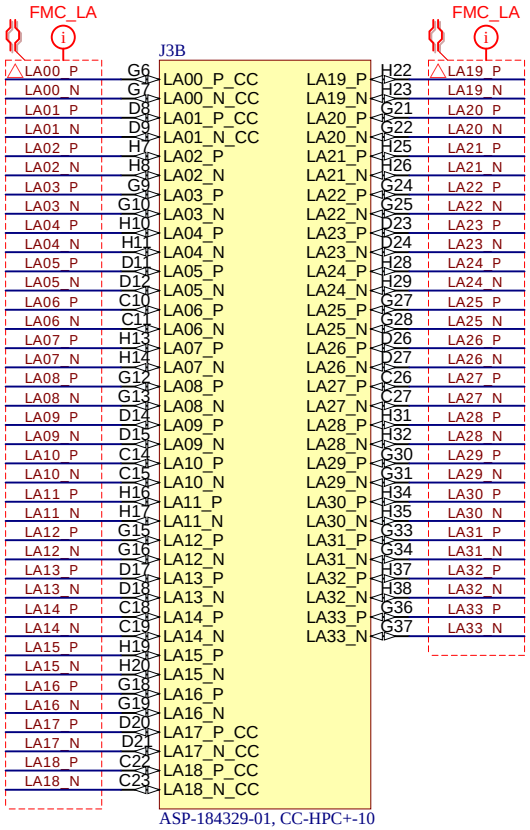
trenz electronic	Title: Falcon - Pi HAT		
A4	Number: TEI0183 G1E13-A		Rev. 01
Date: 2025-09-30	Copyright: Trenz Electronic GmbH		Page29 of 34
Filename: PMOD.SchDoc			

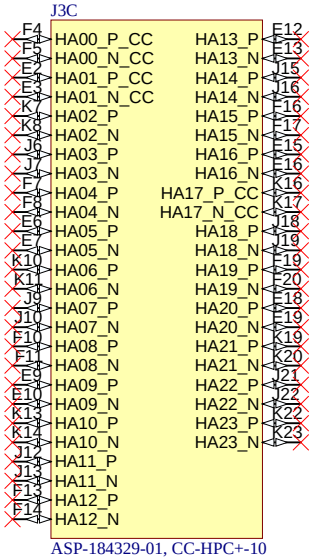


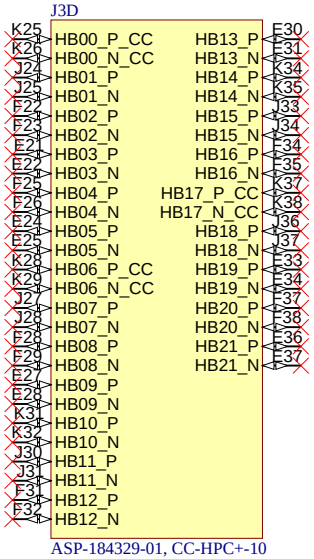
Title: CRUVI			
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 15.05.2026	Copyright: Trenz Electronic GmbH		Page 29 of 50
Filename: CRUVI.SchDoc			



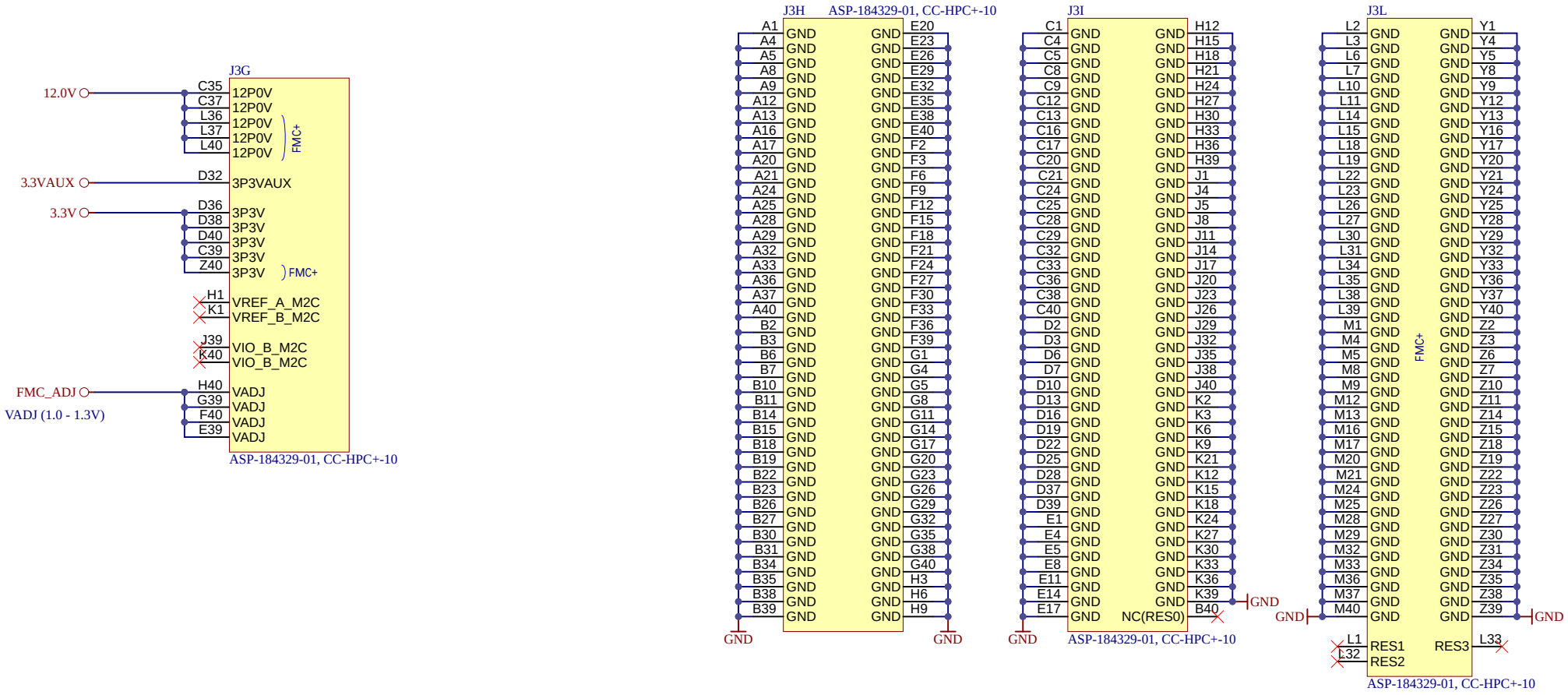
Title: FMC+			
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 15.05.2026	Copyright: Trenz Electronic GmbH		Page 30 of 50
Filename: FMC+_1.SchDoc			



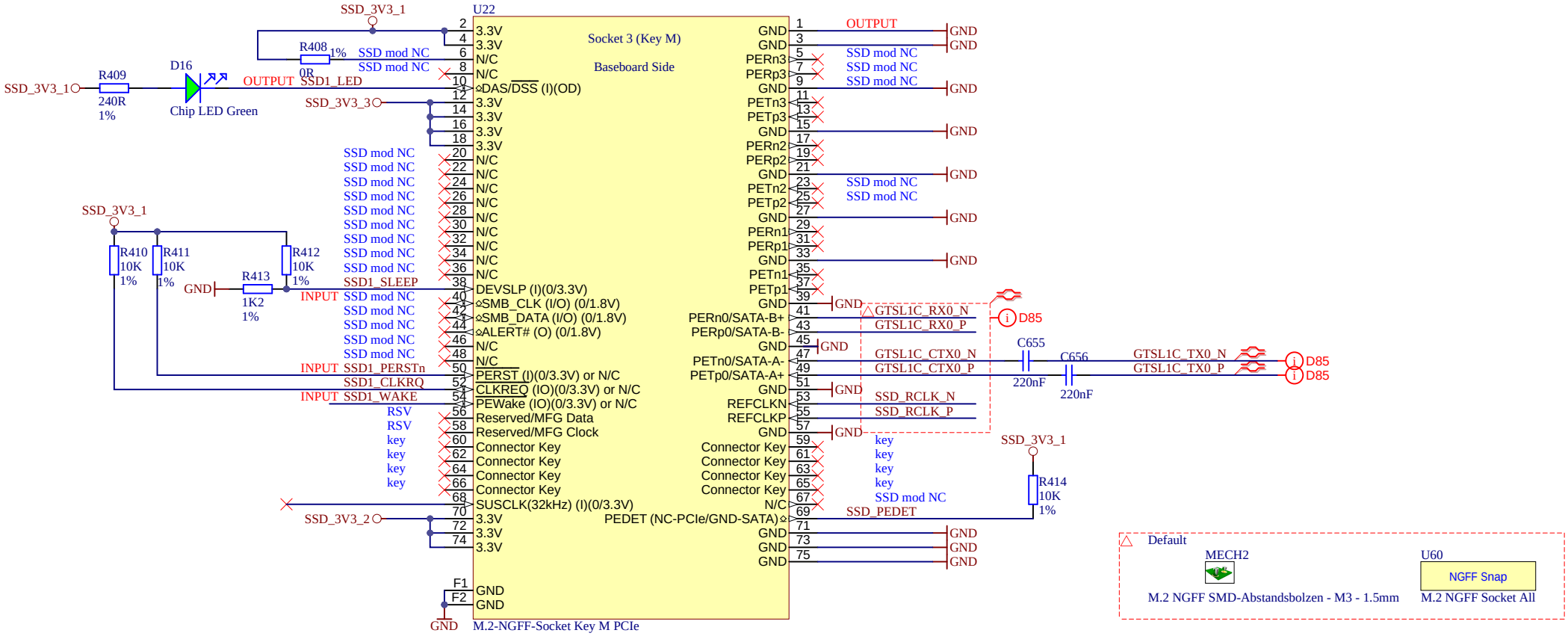




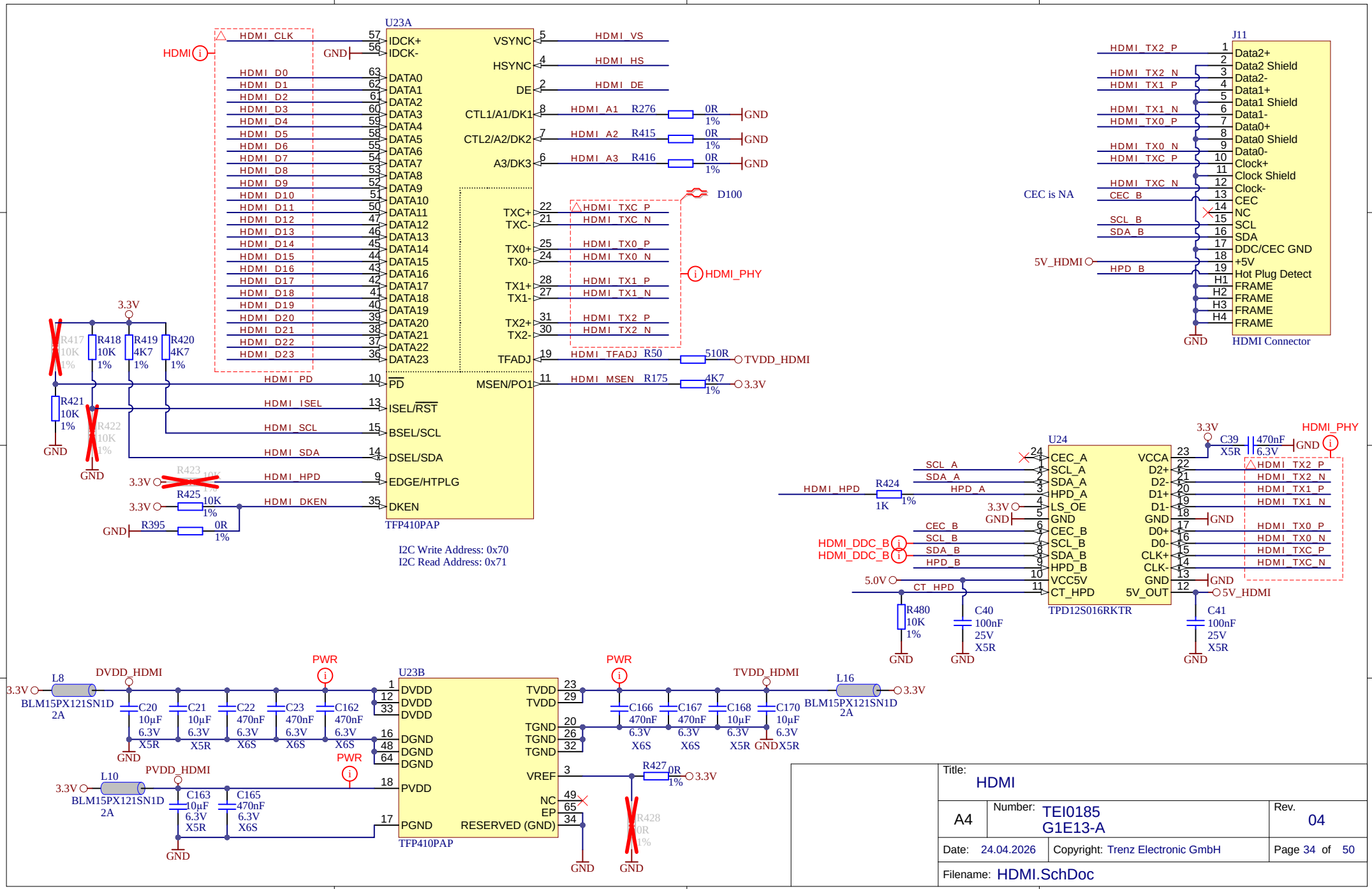
Title: FMC+			
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH		Page 31 of 50
Filename: FMC+_2.SchDoc			



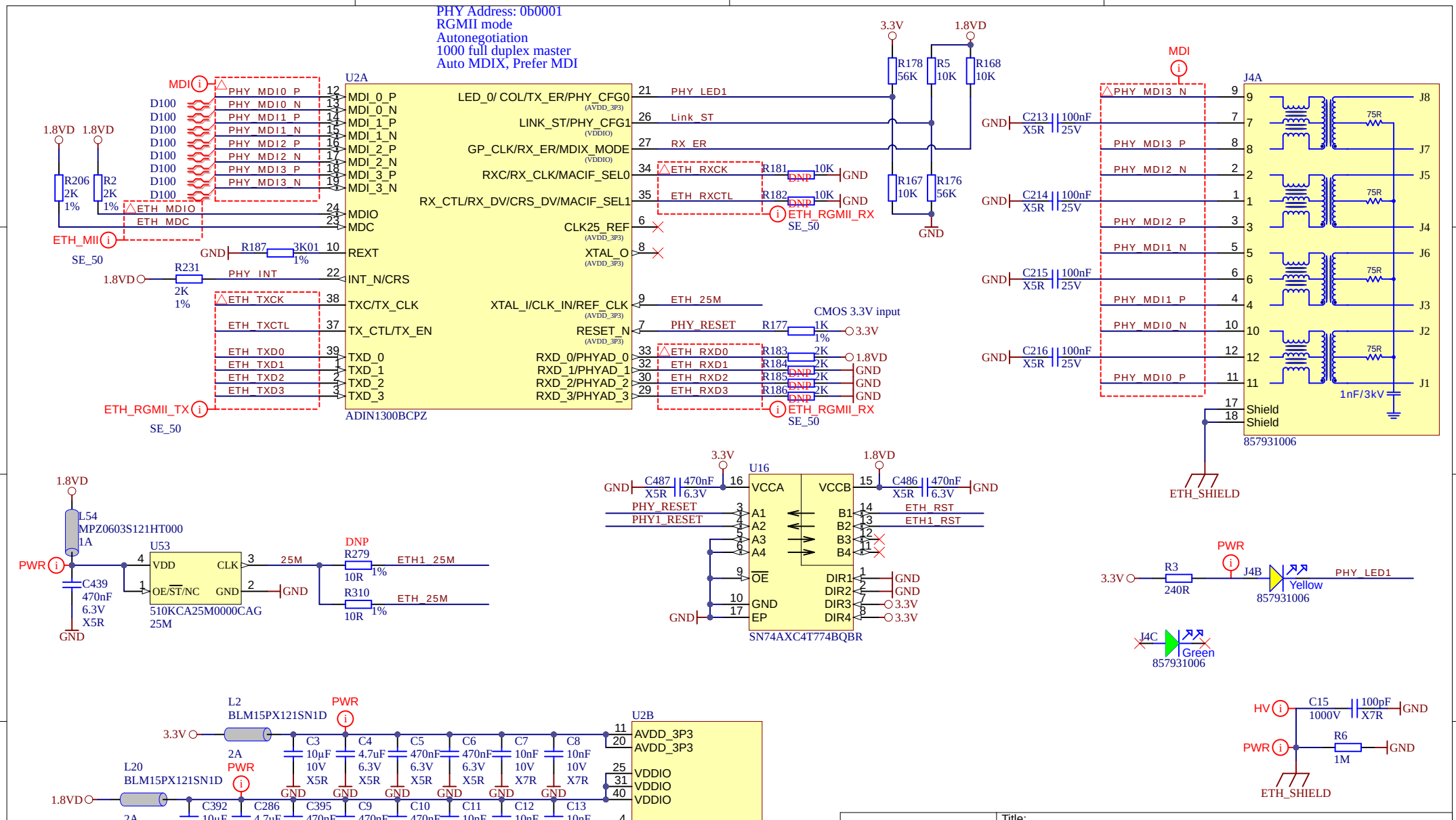
Title: FMC+		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 32 of 50
Filename: FMC+_PWR.SchDoc		



trenz electronic	Title: SSD		
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 02.04.2026	Copyright: Trenz Electronic GmbH		Page 33 of 50
	Filename: SSD.SchDoc		

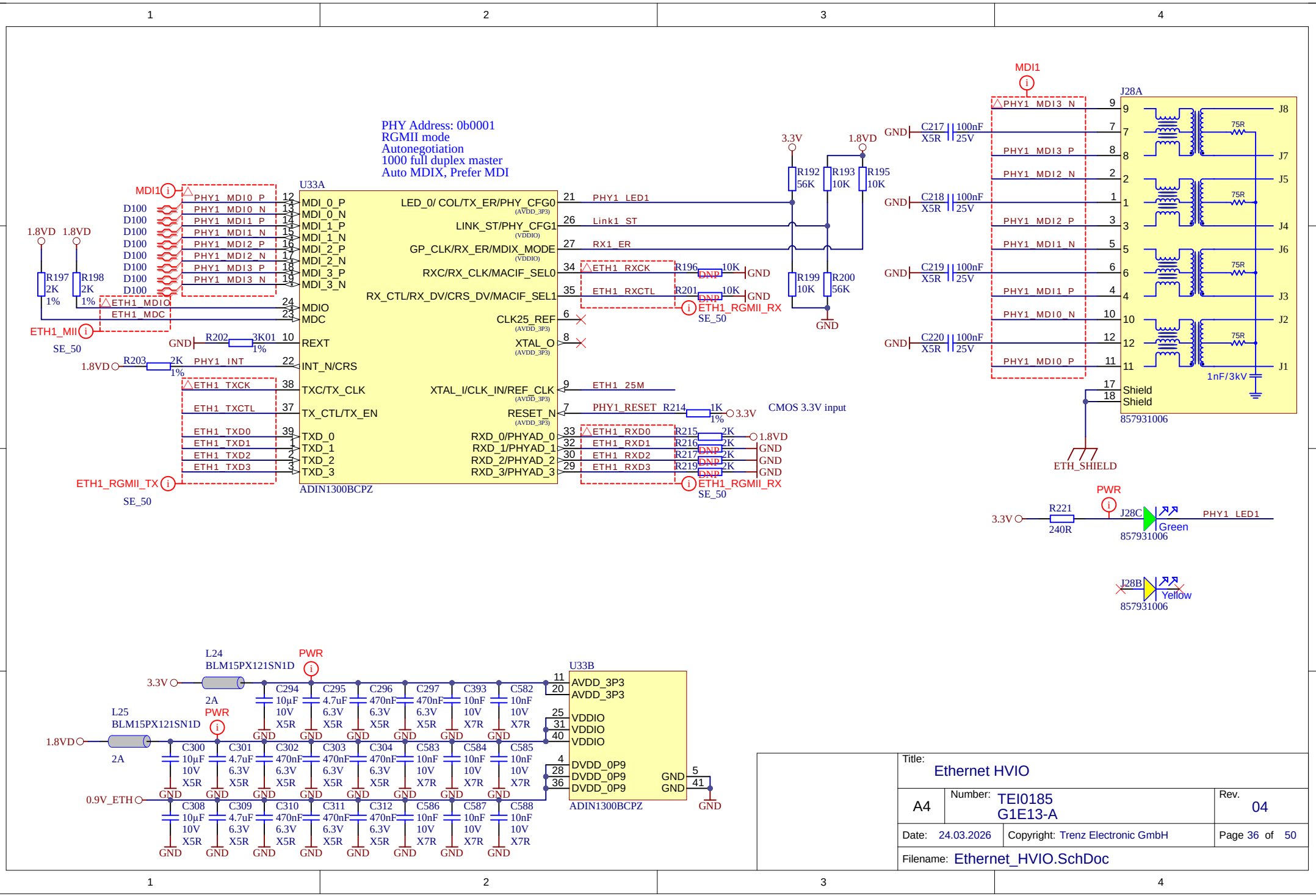


Title: HDMI		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.04.2026	Copyright: Trenz Electronic GmbH	Page 34 of 50
Filename: HDMI.SchDoc		

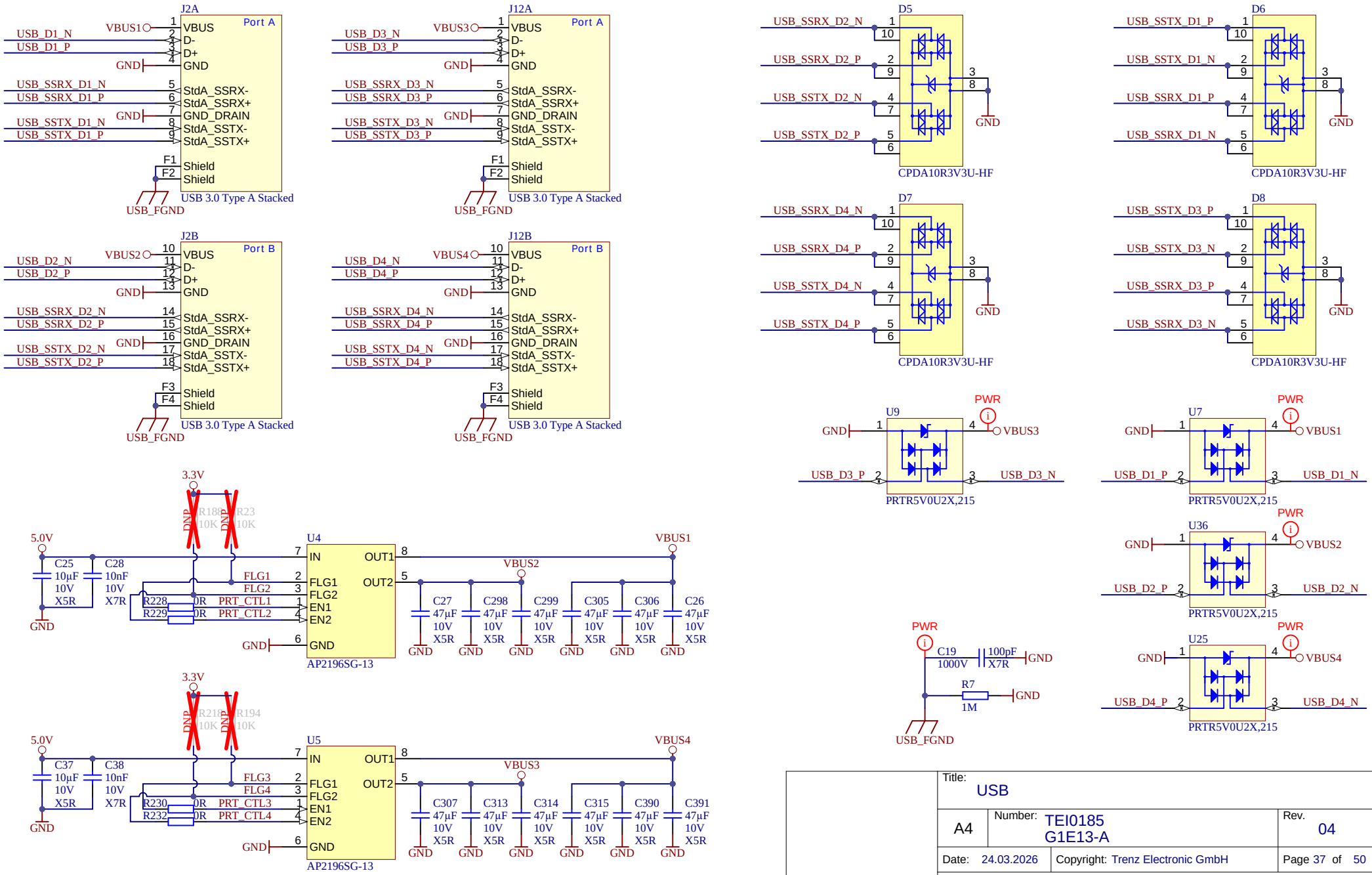


Title: Ethernet

A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 35 of 50
Filename: Ethernet.SchDoc		

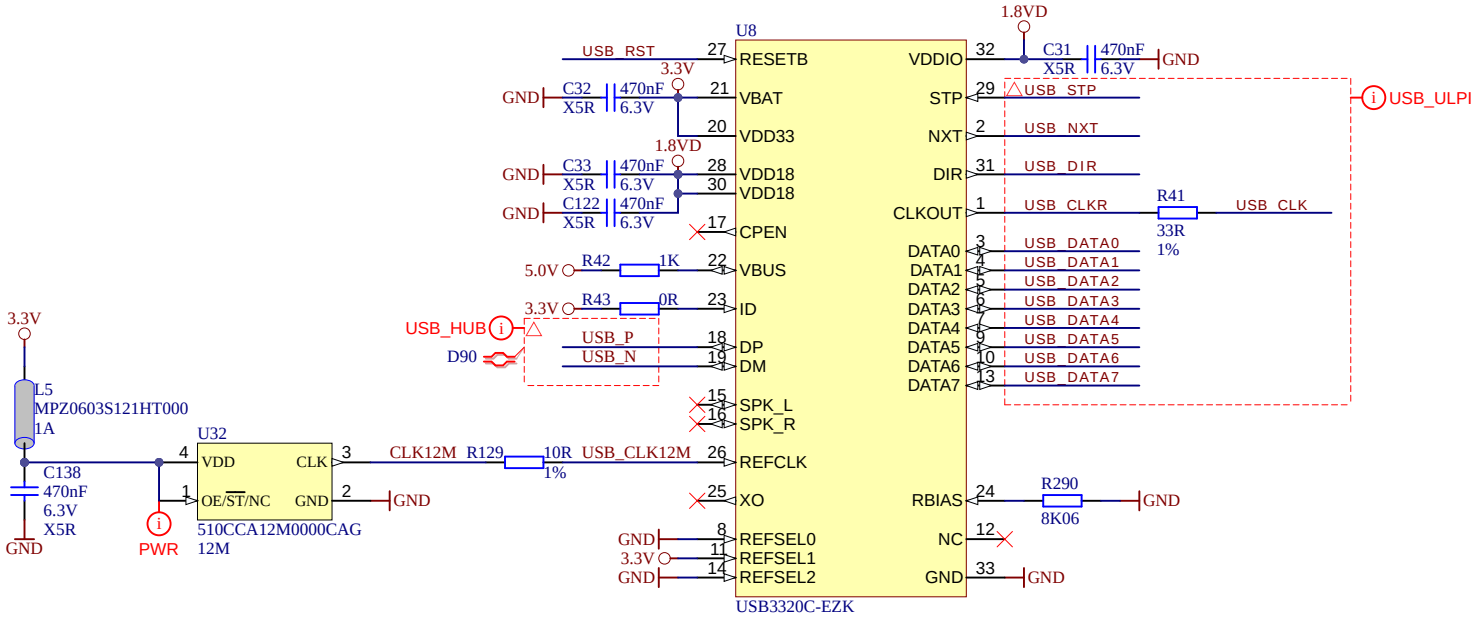


Title: Ethernet HVIO		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 36 of 50
Filename: Ethernet_HVIO.SchDoc		

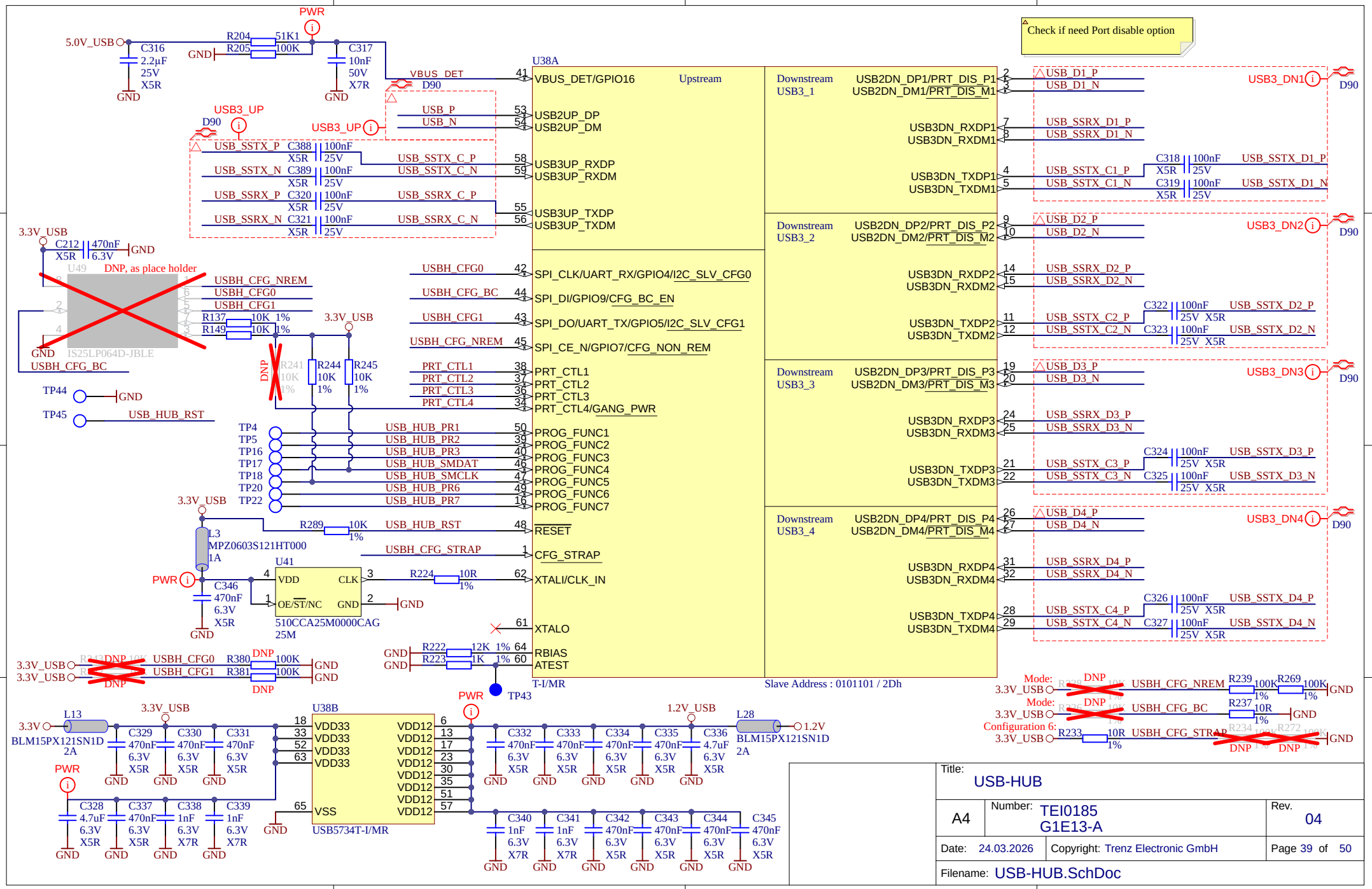


Title: USB		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 37 of 50
Filename: USB.SchDoc		

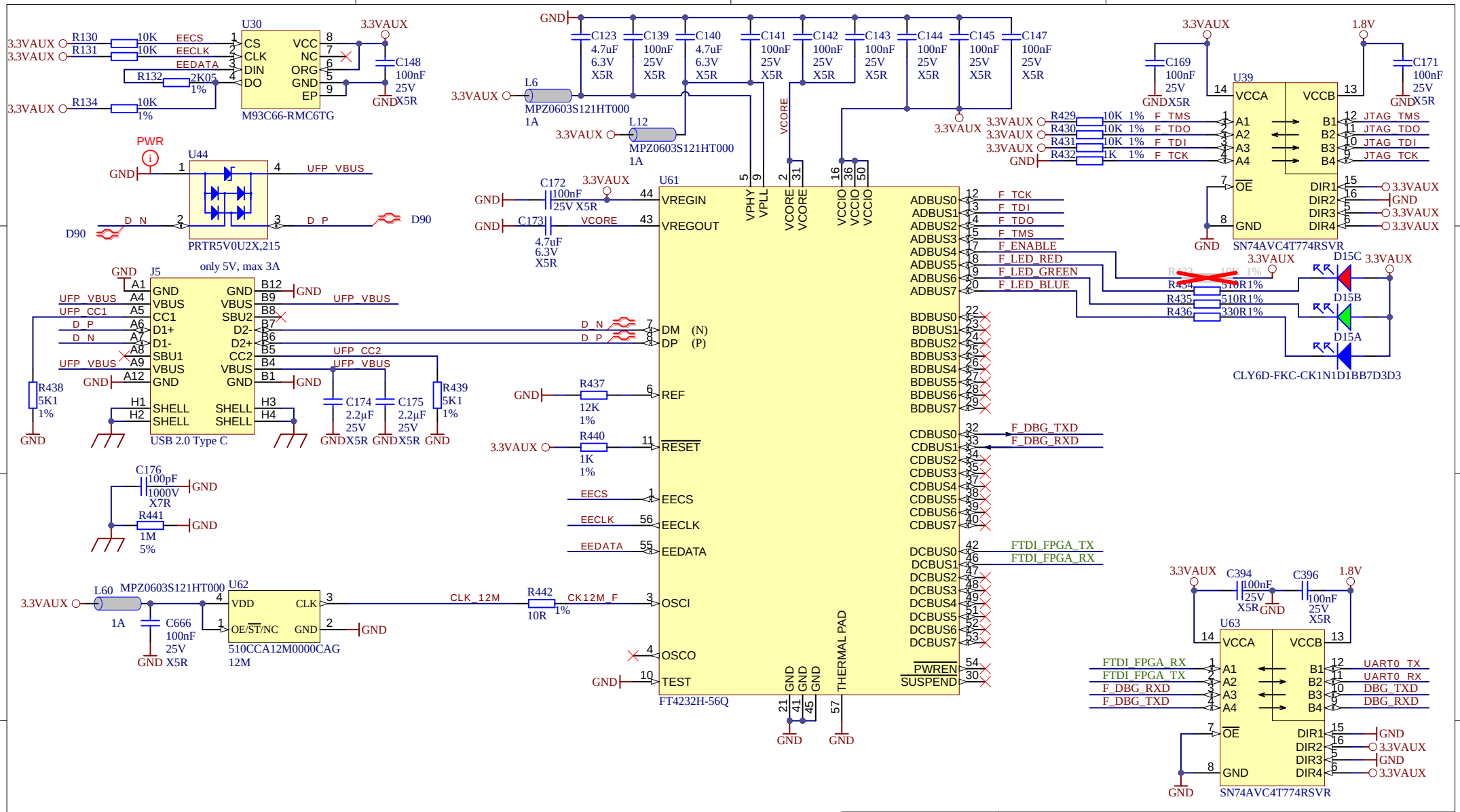
VBAT, VDD33, and VDD18 can be applied in any order.
The VDD18 supply must be turned on and stable before
the VDDIO supply is applied. This does not apply in
cases where the VDD18 and VDDIO are tied together.



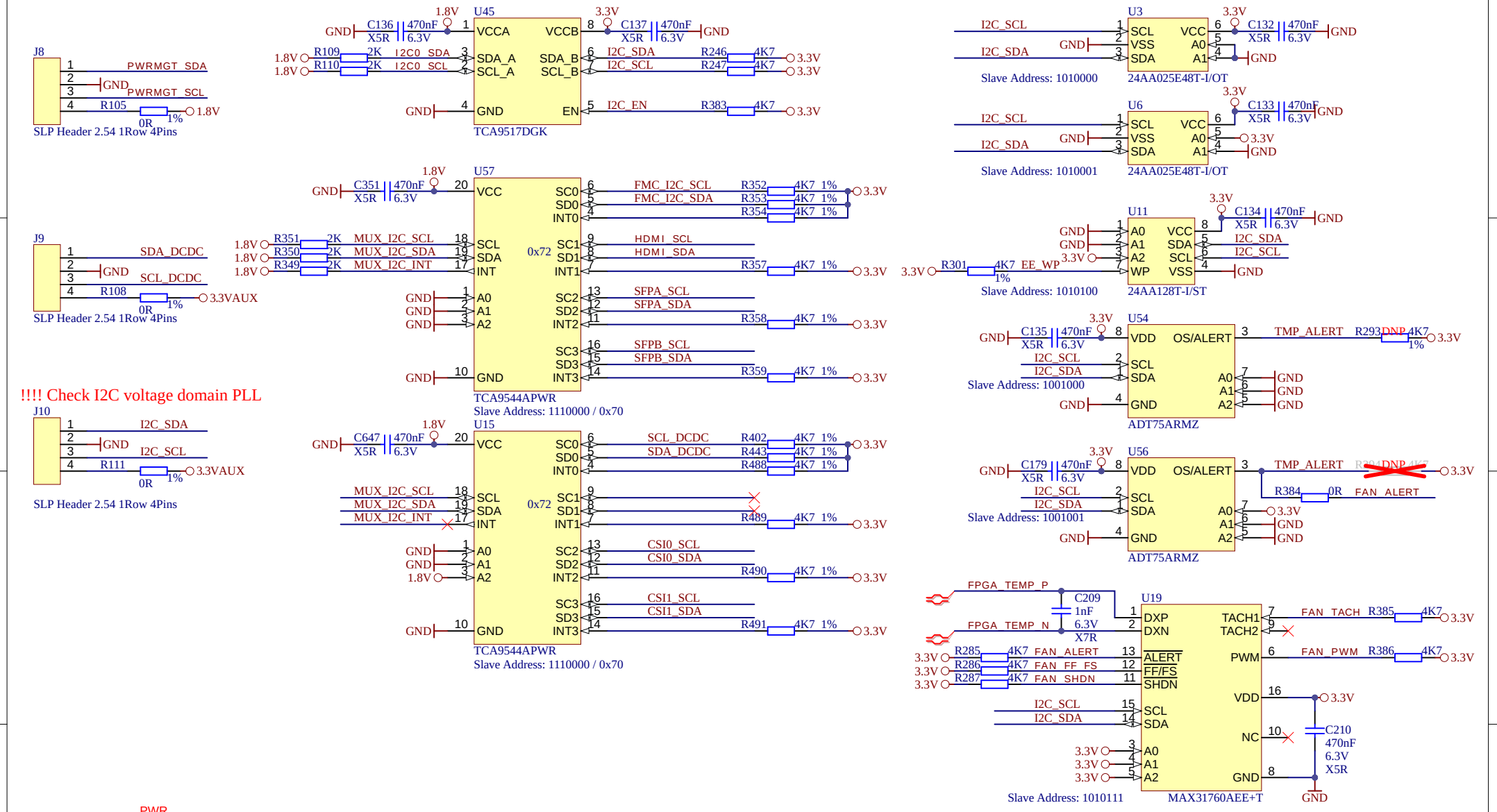
Title: USB-PHY		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 27.04.2026	Copyright: Trenz Electronic GmbH	Page 38 of 50
Filename: USB-PHY.SchDoc		



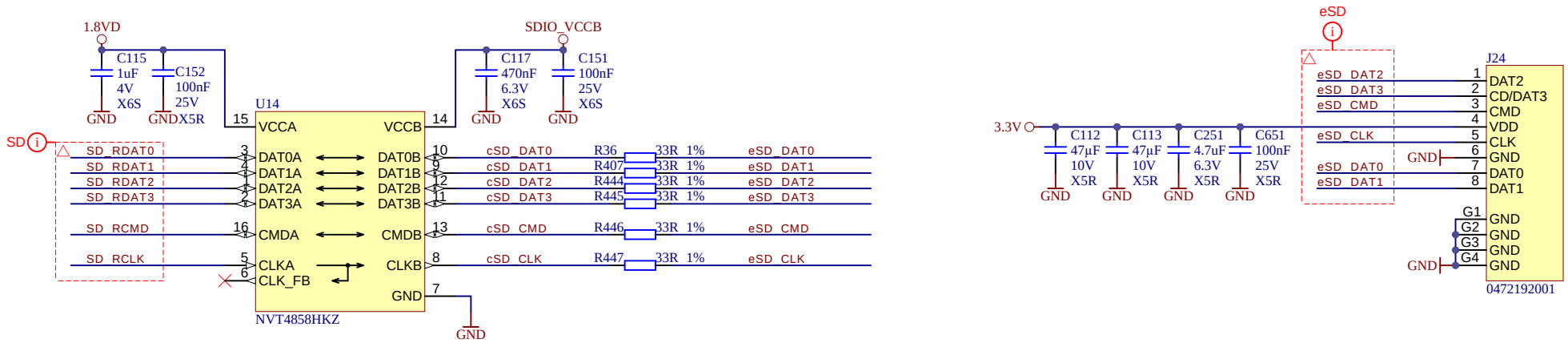
Title: USB-HUB		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 39 of 50
Filename: USB-HUB.SchDoc		



Title: FTDI_JTAG		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 19.05.2026	Copyright: Trenz Electronic GmbH	Page 40 of 50
Filename: FTDI_JTAG.SchDoc		

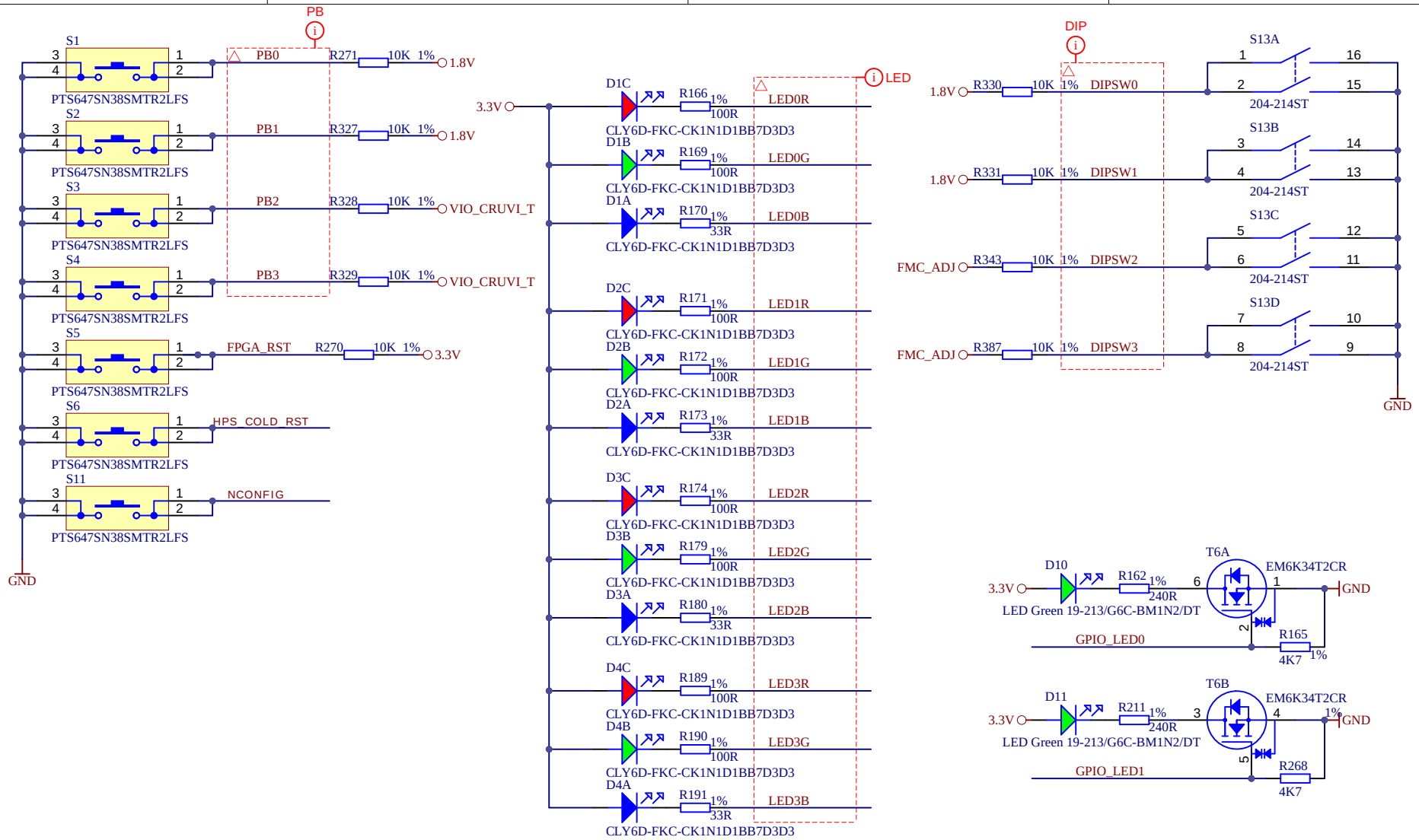


Title: Sensor_EEPROM		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 41 of 50
Filename: I2C_SENSOR_EEPROM.SchDoc		

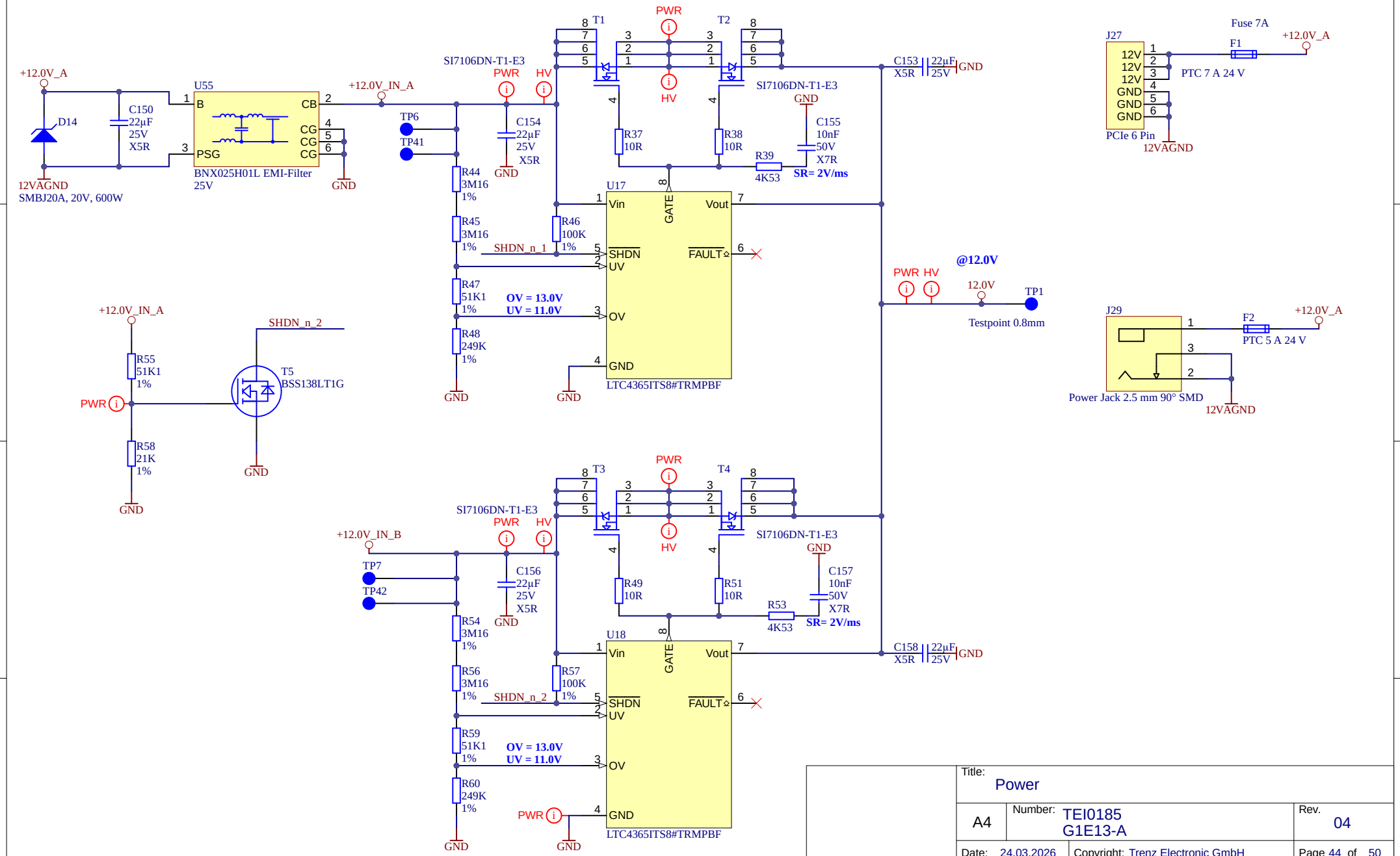


Support SD3.0

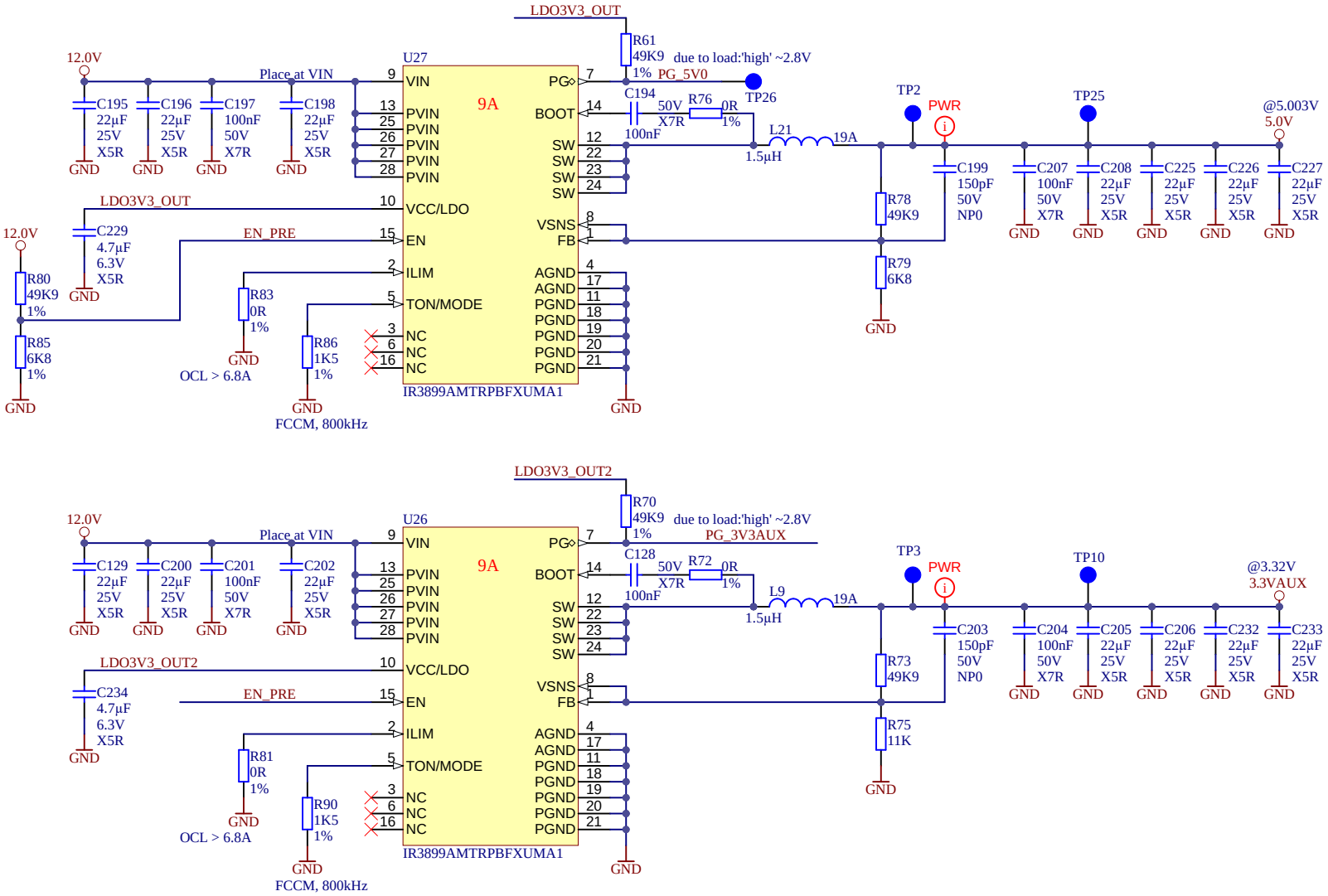
Title: SD		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 42 of 50
Filename: SD.schdoc		



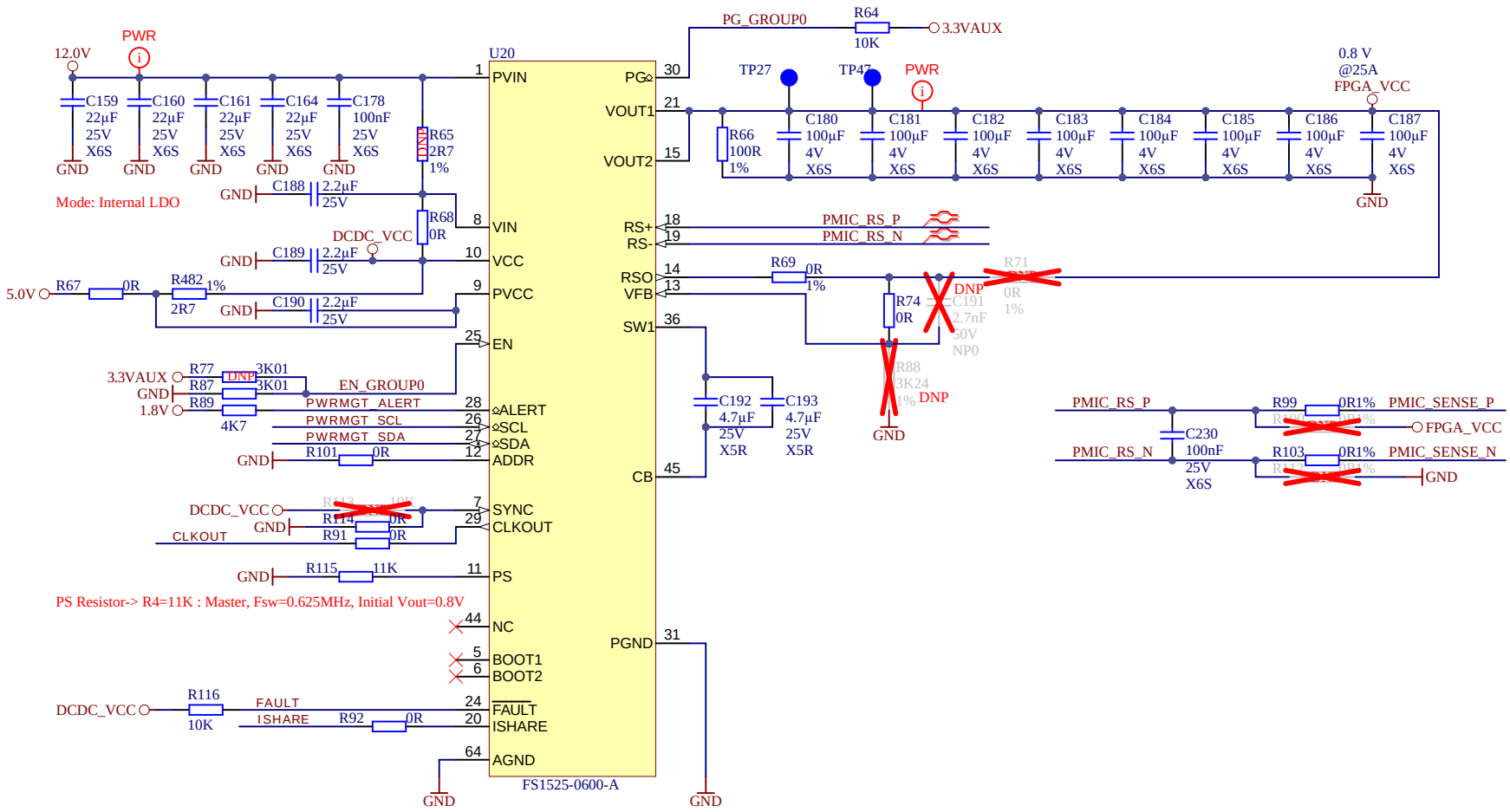
Title: Misc		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 15.05.2026	Copyright: Trenz Electronic GmbH	Page 43 of 50
Filename: MISC.SchDoc		



Title: Power		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 44 of 50
Filename: PWR_IN.SchDoc		

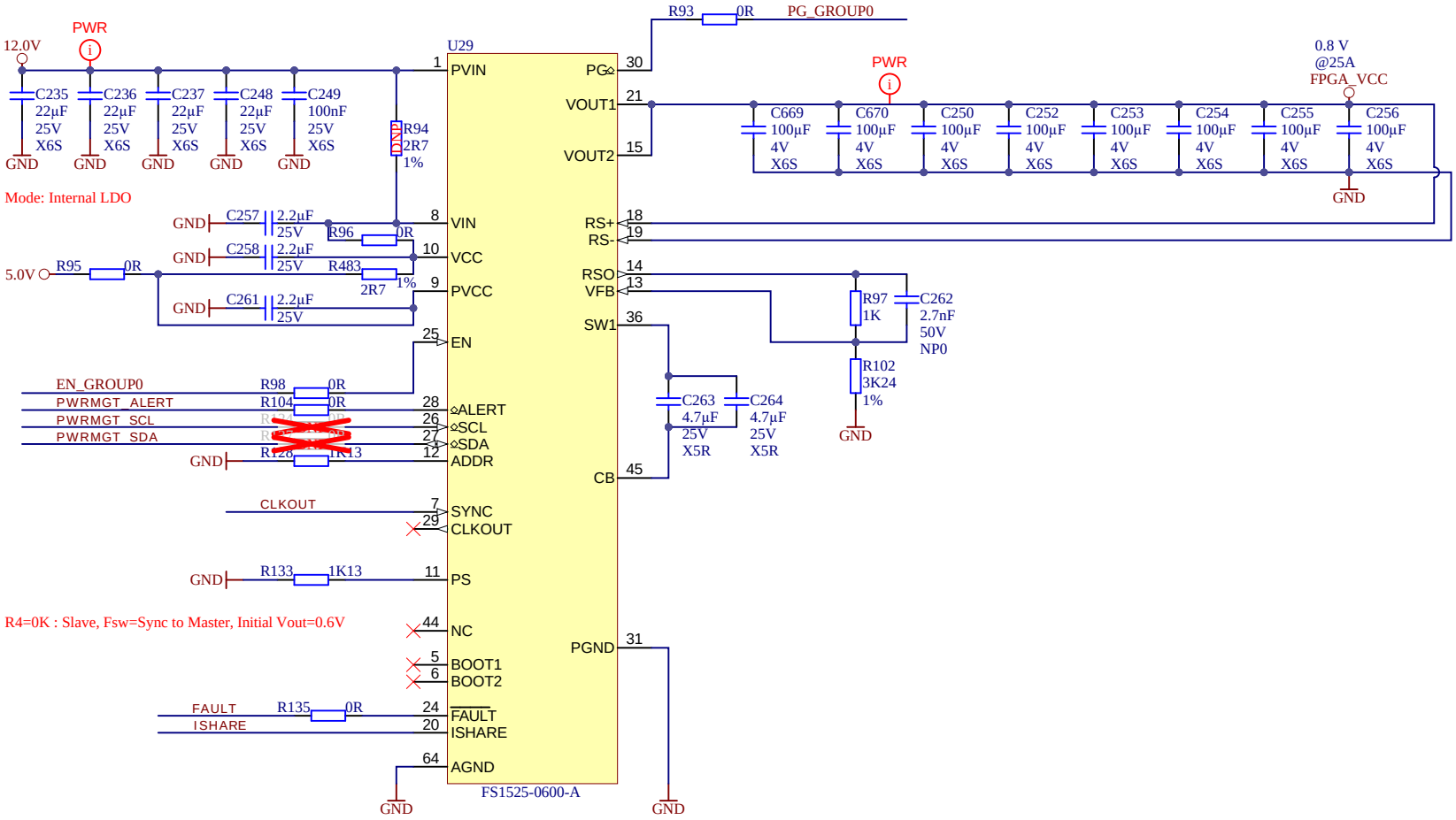


Title: Power		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 45 of 50
Filename: PWR_1.SchDoc		



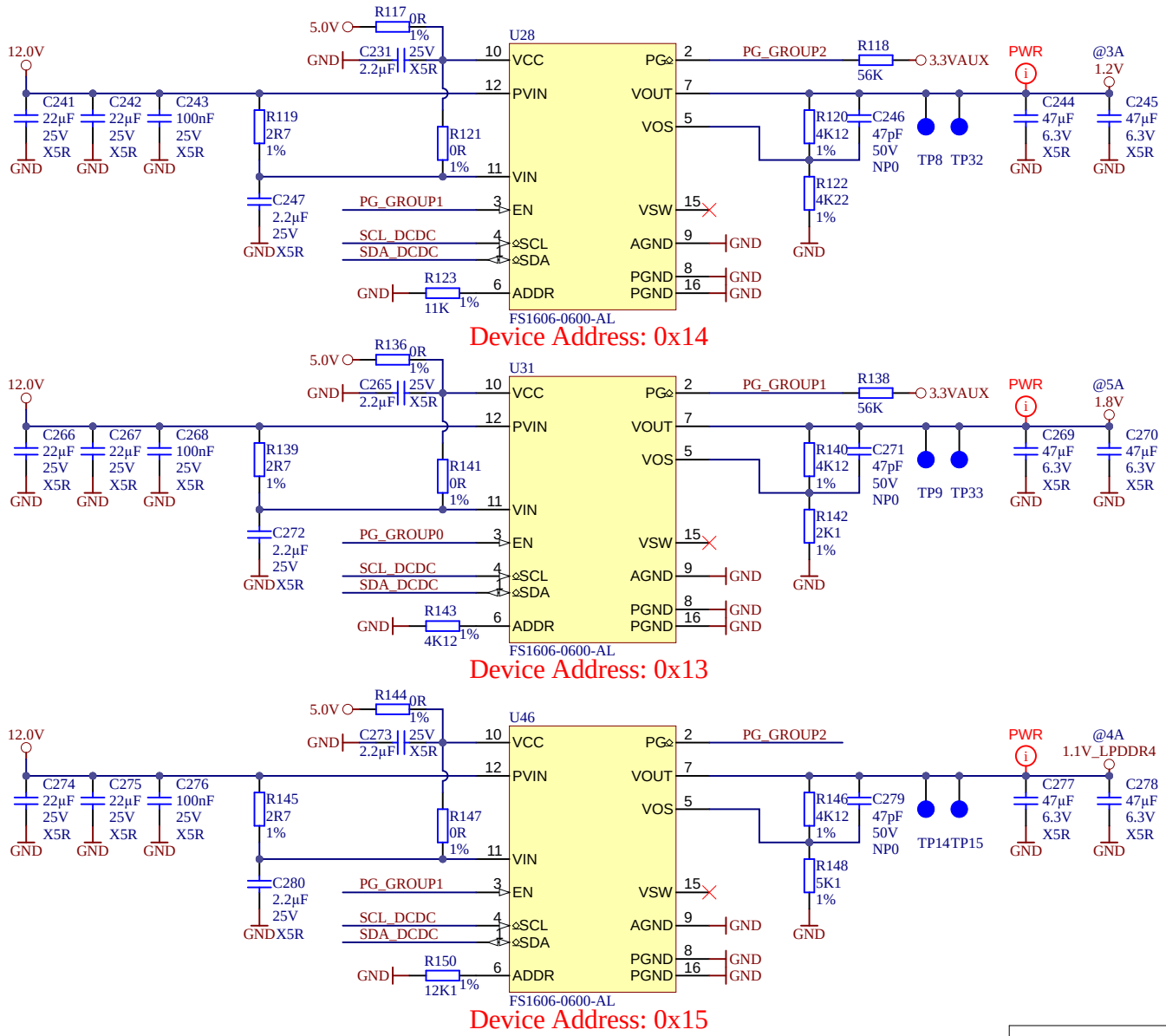
Device Address I2C: 0x10
Device Address PMBus: 0x70

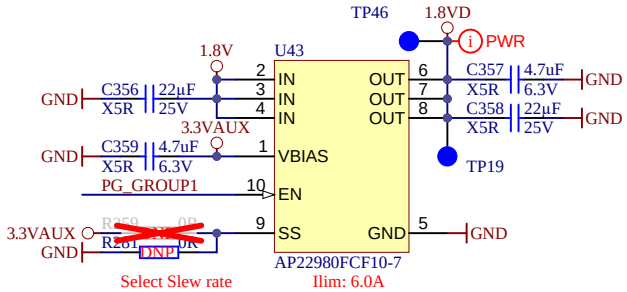
Title: Power		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 46 of 50
Filename: PWR_2.SchDoc		



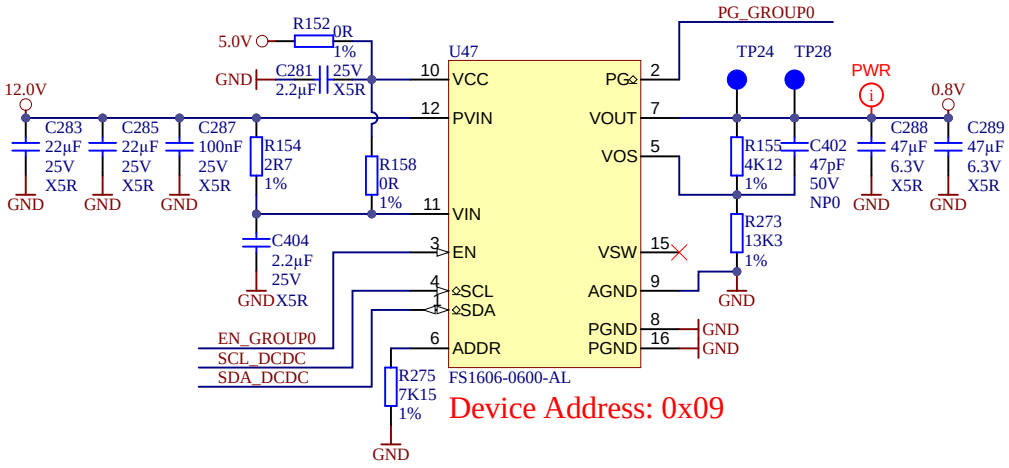
Device Address I2C: 0x11
Device Address PMBus: 0x71

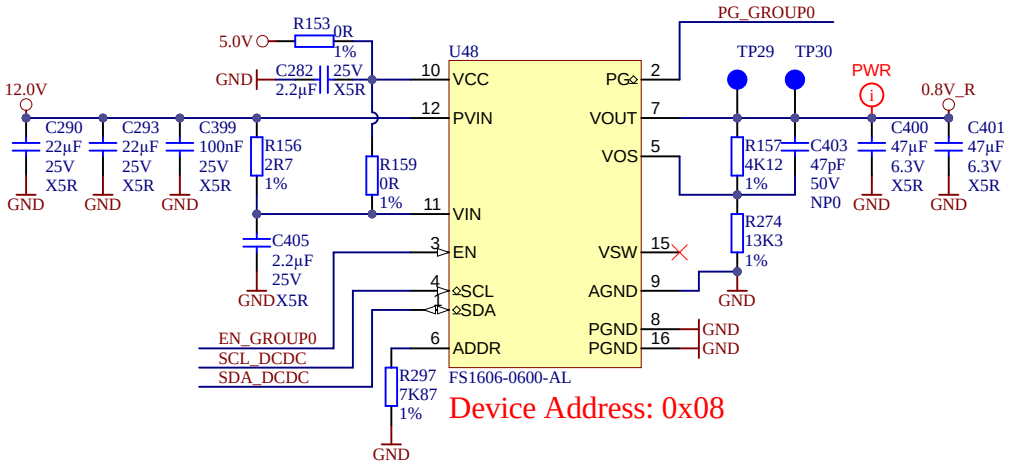
Title: Power			
A4	Number: TEI0185 G1E13-A		Rev. 04
Date: 08.04.2026	Copyright: Trenz Electronic GmbH		Page 47 of 50
Filename: PWR_3.SchDoc			

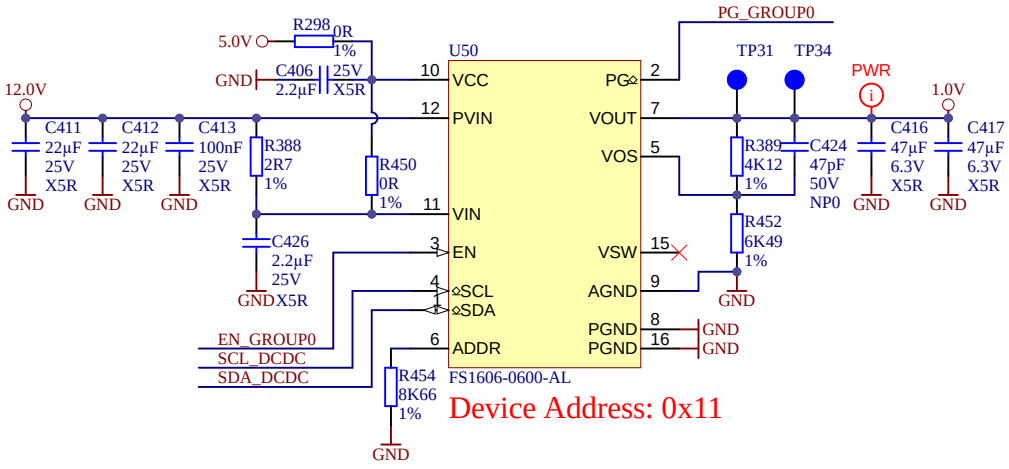


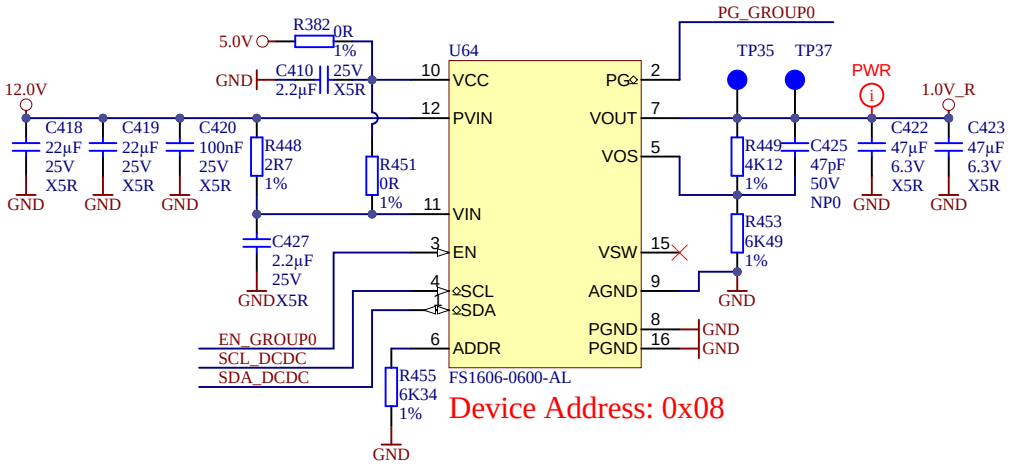


Title: Power		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 48 of 50
Filename: PWR_4.SchDoc		

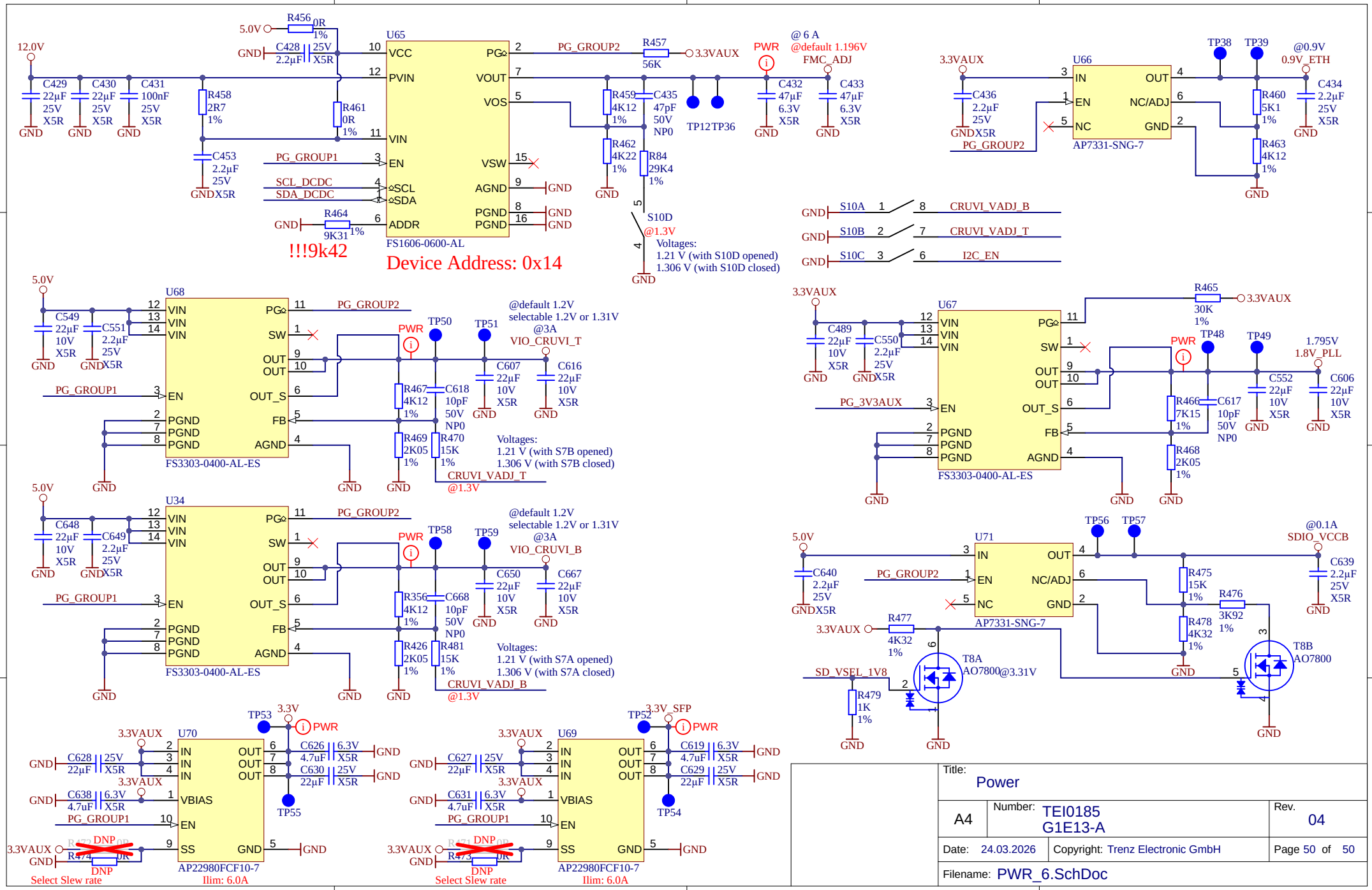








Title: Power		
A4	Number: TEI0185 G1E13-A	Rev. 04
Date: 24.03.2026	Copyright: Trenz Electronic GmbH	Page 49 of 50
Filename: PWR_5.SchDoc		


U65
FS1606-0600-AL
Device Address: 0x14
!!!9k42
U66
AP7331-SNG-7
U68
FS3303-0400-AL-ES
U67
FS3303-0400-AL-ES
U34
FS3303-0400-AL-ES
U71
AP7331-SNG-7
U70
AP22980FCF10-7
Ilim: 6.0A
U69
AP22980FCF10-7
Ilim: 6.0A
Voltages:
1.21 V (with S10D opened)
1.306 V (with S10D closed)
Voltages:
1.21 V (with S7B opened)
1.306 V (with S7B closed)
Voltages:
1.21 V (with S7A opened)
1.306 V (with S7A closed)
Select Slew rate
Title:
Power
A4
Number:
TEI0185
G1E13-A
Rev.
04
Date:
24.03.2026
Copyright:
Trenz Electronic GmbH
Page 50 of 50
Filename:
PWR_6.SchDoc