Hardware Design Document
Arrow iMX8XML Reference Design

Version	1.0
Status	Baselined
Date	21th December 2018

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1 DOCUMENT DETAILS

1.1 Document History

Version	Author		Reviewer		Approver	
	Name	**Date (DD-MM-YYYY)**	**Name**	**Date (DD-MMM-YYYY)**	**Name**	**Date (DD-MM-YYYY)**
Draft 0.1	Divyesh Patel	10-October-2018	Preeti Viramgami	15-October-2018		
Draft 0.2	Divyesh Patel	15-October-2018	Kinjan Patel	6-November-2018		
Draft 0.3	Divyesh Patel	6-November-2018	Kinjan Patel	6-November-2018	Kinjan Patel	6-November-2018
1.0	Nimesh Kotak	21-December-2018	Prajose John	21-December-2018	Prajose John	21-December-2018

Table 1: Document History

Version	Description of Change
Draft 0.1	Initial draft version created
Draft 0.2	Initial Section 5 added, header name changed as per template
Draft 0.3	Review comment 441 to 463 from review tracker implemented
1.0	Baselined

Table 2: Description of Change

1.2 Definition, Acronyms and Abbreviations

Definition/ Acronym/ Abbreviation	Description
HRS	Hardware Requirement Specification
USB	Universal Serial Bus
BT	Bluetooth
DSI	Display Serial Interface
LPDDR	Low Power Double Data Rate
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
QA	Quality Assurance
RAM	Random Access Memory
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
SOW	Scope of Work
TBD	To Be Decided

Definition/ Acronym/ Abbreviation	Description
SPI	Serial Peripheral Interface
I2C	Inter-Integrated Circuit
WLAN	Wide Local Area Network
HDMI	High-Definition Multimedia Interface
RTC	Real Time Clock
PMIC	Power Management IC
CRN	Change Request Note
GPU	Graphics Processing Unit
QTS	Query Tracking Sheet
Reference Design	Single Board Computer
RTM	Requirement Traceability Matrix
CE	Consumer Edition
ML	Machine Learning
RD	Reference Design
iMX8X ML RD	i.MX 8X Machine Learning Reference Design
MEK	Multisensory Enablement Kit
LVDS	Low Voltage Differential Signal

Table 3: Definition, Acronyms and Abbreviation

1.3 References

#	Document	Version	Remarks
1	96BoardsCESpecificationv1.0-EA1	1.0 (January 2015)	96Boards Consumer Edition
2	eI_Arrow_iMX8XML_RD_BlockDiagram	1.2	Block Diagram
3	Proposal-Draft	Draft version	Initial Proposal to Customer
4	eInfochips SOW#1_iMX8X_MLPlatfrom-Rev1-NC (1)	1.0	SOW
5	eI_Arrow_iMX8XML_RD_QueryTrackingSheet	Draft	QTS updated as per Discussion with Customer
6	eI_Arrow_iMX8XML_RD_CriticalPartsSelection	0.11	Component selection ***shall*** be as per Arrow preferred vendor list
7	eI_Arrow_iMX8XML_RD_Schematic.dsn	1.0	Schematic version 1.0
8	eI_Arrow_iMX8XML_RD_BOM.xls	1.0	BOM version 0.5
9	eI_Arrow_iMX8XML_RD_Layout.brd	1.0	Layout file of Board
11	eI_Arrow_iMX8XML_RD_HRS.pdf	1.1	HRS file
12	eI_Arrow_iMX8XML_RD_PowerBudgetAnalysis.xls	1.0	Power Budget

Table 4: References

2 INTRODUCTION

This document enlists the design details for the Arrow iMX8XML Reference Design which includes:

a) **Design requirements**: These are mentioned more elaborately in Hardware requirement specifications.

b) **High level design**: The system design and hardware block diagrams based on the requirements.

c) **Design Considerations**: This includes various measures that were taken to meet the design specifications

d) **Design Decisions**: Decisions taken during the design: This includes the various design decisions that were taken during the design execution

2.1 Specifications

2.1.1 Electrical Specifications:

These are the electrical specifications of the design. This may vary from the design requirements as they may include optional interfaces or design changes

Device	Specification	
Microprocessor	Processor name (Package) : iMX8 QUADX (21x21 mm, 609 pins) Part Number: PIMX8QX6AVLFZAA Manufacturer : NXP	
	Internal core operation	Four ARM Cortex®-A35 One Cortex-M4F
	Bus Frequency	LPDDR4 Clock Speed: 1.2GHz (Maximum)
	External Oscillator (for processor)	Part Number: ABM3-24.000MHZ-D2Y-T Frequency : 24MHz
	Core Power Supply	Core power supplies shall be generated by two LTM4643 as per power sequence provided by ADM1266
	Peripheral Power supply	Peripheral power supplies shall be generated by two LTM4643 as per power sequence provided by ADM1266
Memory Peripherals	2GB LPDDR4 SDRAM	Model Name : MT53B512M32D2NP-062 WT Manufacturer : Micron Size : 2GB Number of devices:1 Total Size: 10x14.5 mm
	NOR FLASH	Model Name : MT25QL512ABB1EW9-0SIT TR Manufacturer : Micron Alternate Part Model Name: IS25LP512M-JLLE-TR Manufacturer : ISSI Size : 8 x 6 mm
	EEPROM	Model Name : M24128-DRMF3TG/K Manufacturer : ST Microelectronics Size : 2 x 3 mm
	SD Card	Micro SD card Connector : 2201778-1 (TE) Maximum memory support : 64GB
	Camera (MIPI CSI0)	Lane: 4 Lane interface At High speed expansion connector: 5177983-2 (TE) Camera : At Mezzanine Card
	Display (MIPI DSI0)	Lane: 4 Lane interface At High speed expansion connector: 5177983-2 (TE) Display : At Mezzanine Card
	Display (DSI1)	Lane: 4 Lane interface DSI to HDMI Transmitter : ADV7535 (ADI) HDMI Connector: 5-1903015-1 (TE)
	USB	1. 2 x USB 3.0 Type A slave ports 1932258-1 (TE) 2. 1 x USB 2.0 Type Micro AB OTG port 0475890001 (TE) 3. 1 x USDB 2.0 to Quectel Module PCIe M2 connector 1775838-2 (TE)

	Debug UART	1. FTDI_UART0 2. FTDI_M40_UART0 Both UART are converted into USB through FTDI Chip FT2232D-REEL and provided to USB 2.0 Micro AB Connector 0475890001 (TE)
	Wi-Fi + BT	Module Part Number : 450-0169C (based on Silicon LAB chip) Manufacturer : LSR Wi-Fi IEEE 802.11 a/b/g/n/ac (single stream n) Bluetooth 4.2 (Bluetooth Low Energy)
	JTAG	JTAG Connector name : 20021111-00010T4LF (FCI) No of pins : 10
	IOT Security	Model Name : A71CH Manufacturer : NXP Interface : I2C
	Audio	X4 On board MIC Part Number : SPH0645LM4H-B Manufacturer : Knowles
	Sensor	Part Number : LSM6DS33TR Type : Accelerometer and Gyroscope Manufacturer : STMicroelectronics
	Ethernet RGMII	Trans receiver Part Number : KSZ9031RNXCA Manufacturer : Microchip Technology Ethernet Connector : 1-2301994-2 (TE)
User Control	Switches/Buttons	1. Power ON/OFF Button 2. Processor RESET Button 3. Boot Mode(x4) selection Switch
Clock	Crystal	External Crystal: ABM3-24.000MHZ-D2Y-T → 24 MHz TSX-3225 25.0000MF20P-C0 → 25 MHz FC7BQCCMM6.0-T1 → 6 MHz FA-118T 26.0000MF12Z-AC3 → 26 MHz ABS07-32.768KHZ-TT3 → 32.768 KHz FC-135 32.7680KA-AC0 → 32.768 KHz ASDK-32.768KHZ-LRT → 32.768 KHz
Power Supply	Input	+12V DC typical(8V-18V DC@60W) from adapter to DC jack connector PJ-041H (CUI)
	Power Regulators	Regulator1 : ADP2386ACPZN-R7 Regulator2 : ADP5023ACPZ-R7 Regulator3 : LTM4643 (x2) Sequencer : ADM1266 Manufacturer : Analog Devices Inc.
Board Specifications	Board Size	85 x 100 mm (96boards Extended-B form factor)
	Number of Layers	12 Layers

Table 5: Outline Specification

2.1.2 Mechanical

2.1.2.1 Specifications

Mechanical outline shall be as per page number 26 of 96boards standard.
https://www.96boards.org/documentation/Specifications/96Boards-CE-Specification.pdf

TOP **SIDE**
PLACEMENT

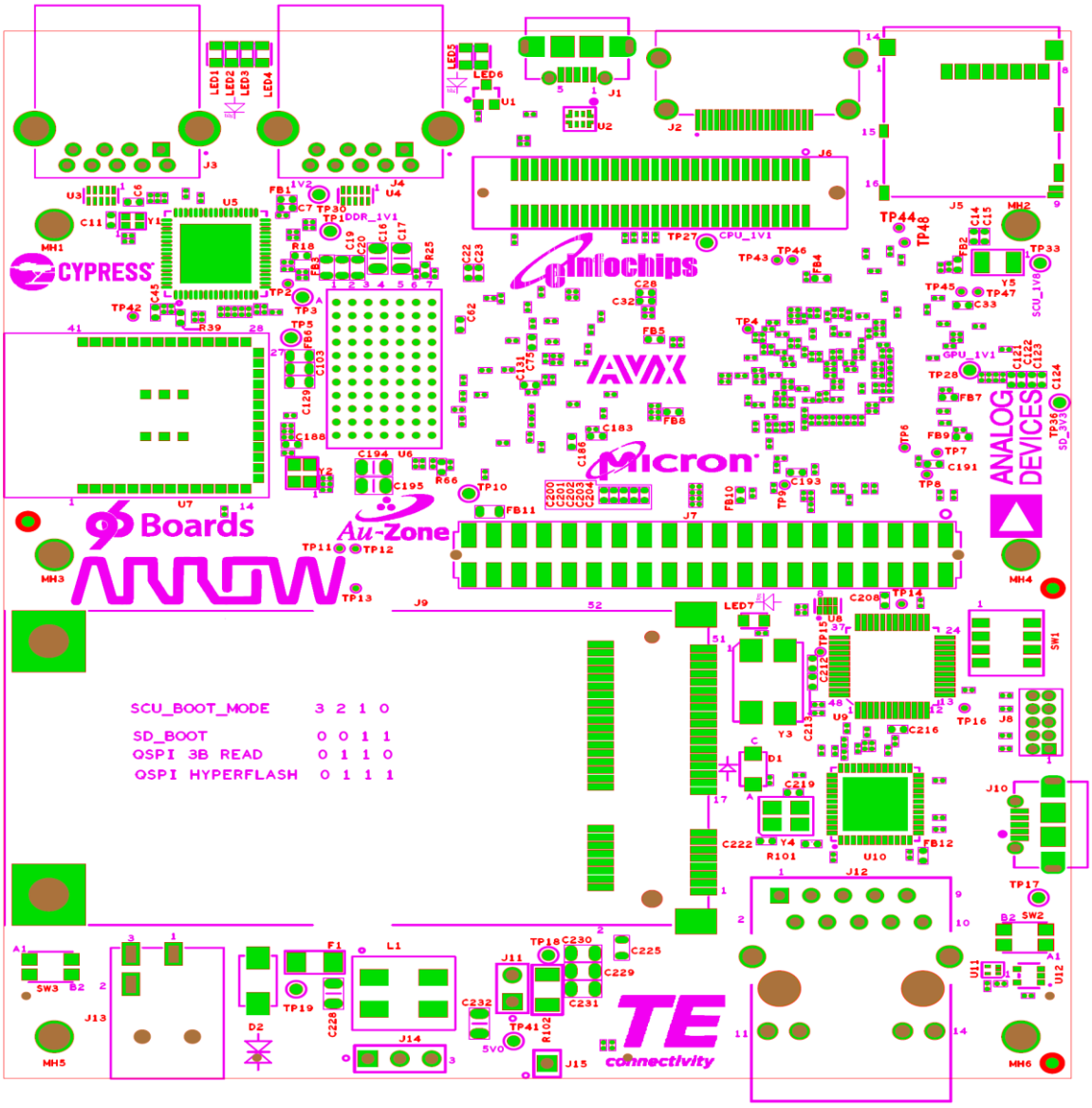


Figure 1 : iMX8XML Reference Design top side placement

BOTTOM SIDE PLACEMENT

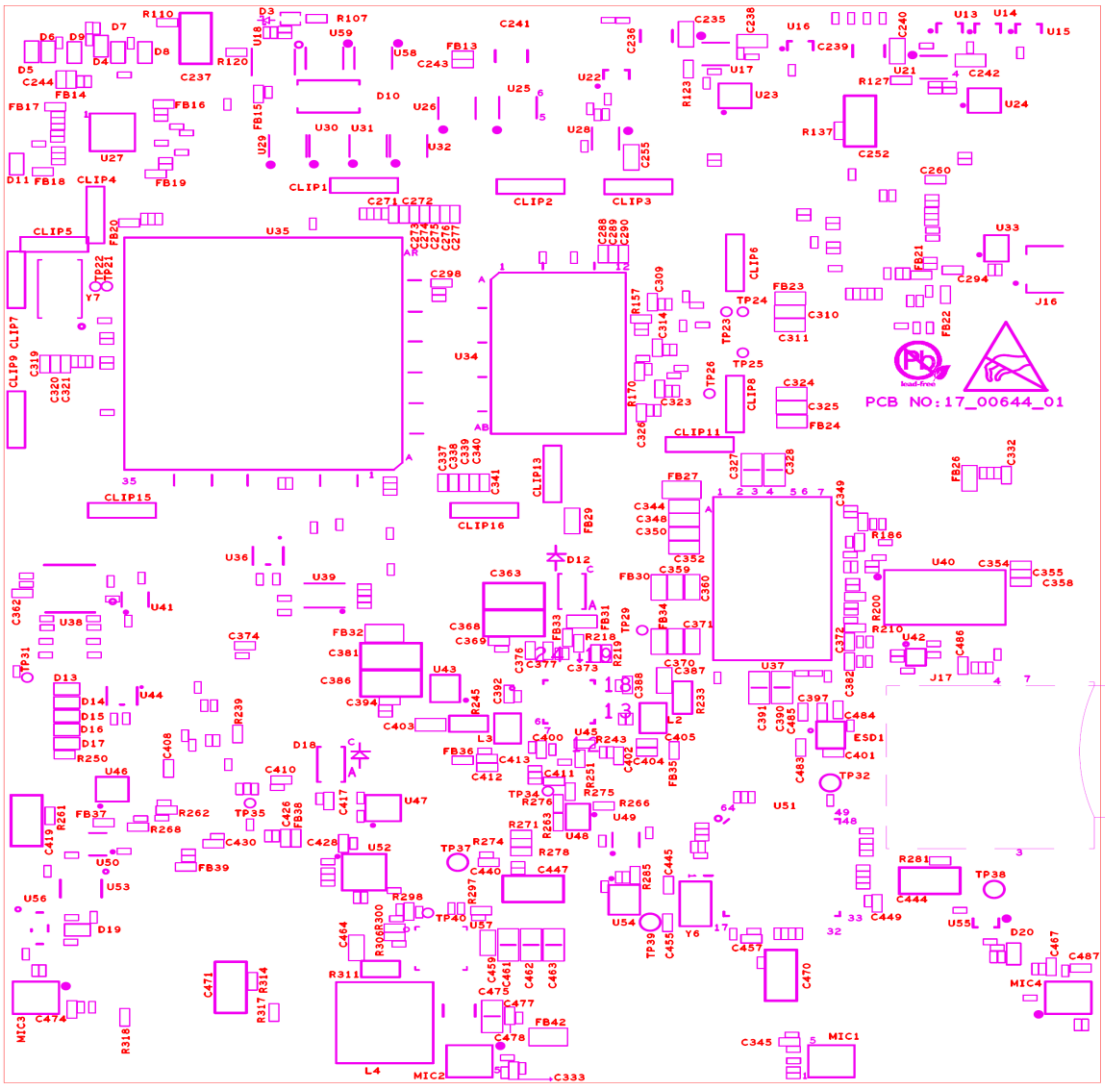


Figure 2 : iMX8XML Reference Design bottom side placement

2.1.2.2 Design Consideration

The iMX8XML Reference Design mechanical is intended to be designed to work for the temperature range of 0ºC to +55ºC
FAN provision will be used if heating issue faced during bring up activity.

2.1.2.3 Design Justification

Mechanical team has verified the STEP file of the board for the top side and bottom side component placement verification and found it OK.

SVN Path for STEP file
\13. Hardware Specific\Layout\Arrow-IMX8XML_MotherBoard\Reference Documents\3D File

Note: File not included in document due to bigger size

2.1.3 Environmental

2.1.3.1 Specifications

iMX8XML Reference Design is having operating temperature range of 0ºC to +55ºC.
Mechanical enclosure shall be designed in a way to manage the heat dissipation from the electronics parts.

2.1.3.2 Design Justification

All the components selected for iMX8XML Reference Design supports the operating temperature range more than 0ºC to +55ºC.

Refer the Bill of Material of iMX8XML_RD below that has the column with operating temperature range for all the components.

eI_Arrow_iMX8XML_RD_BOM.xls

Refer below BOM with components RoHS and EOL detail generated from Silicon Expert tool.

Report_Silicon Expert_18_00644_01

3 SYSTEM BLOCK DIAGRAM

iMX8XML_RD System level Diagram

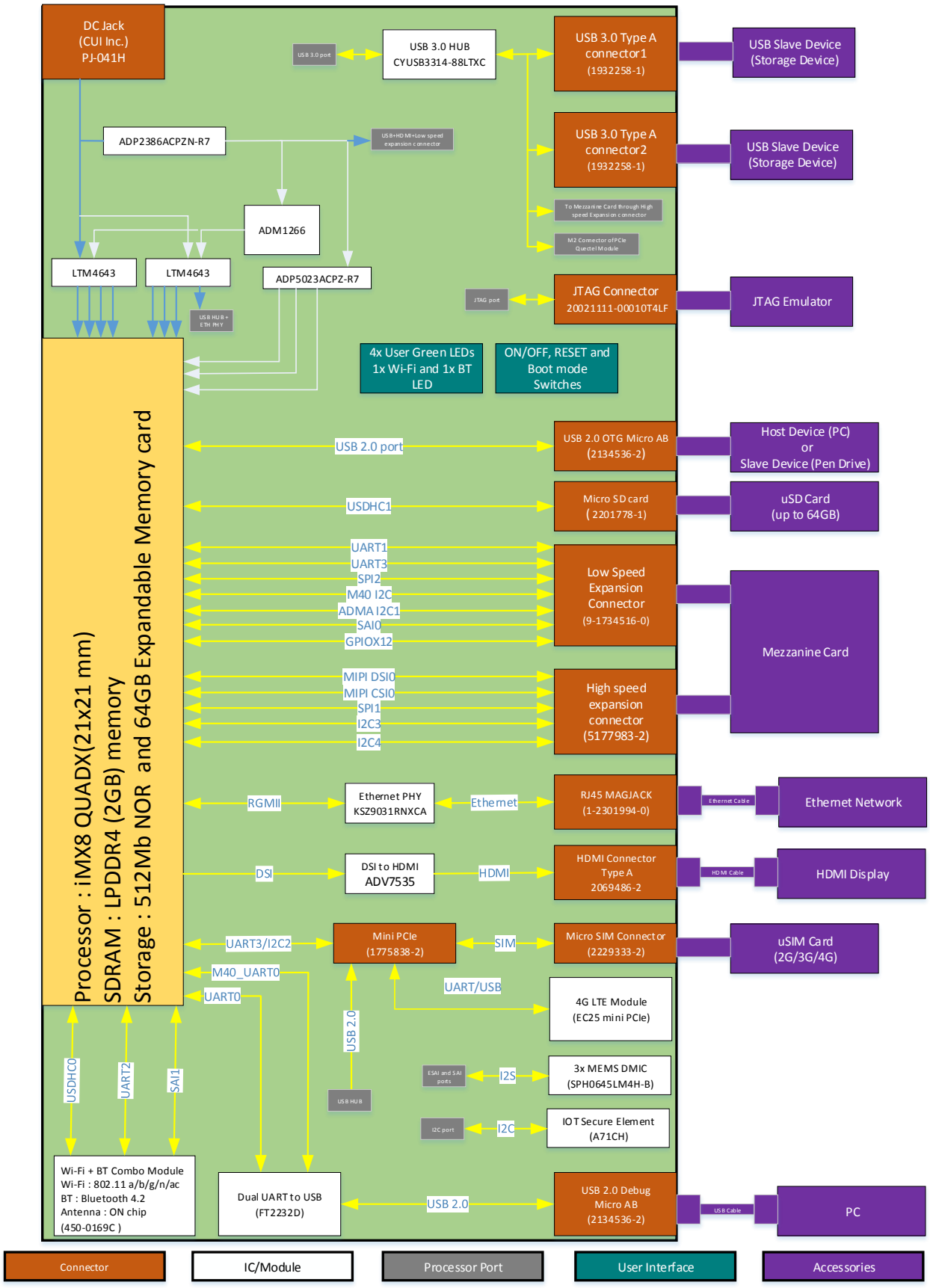


Figure 3 : High Level Design Diagram

4 HARDWARE BLOCK DIAGRAM

Arrow iMX8X ML Reference Design Block Diagram (Version 1.2)

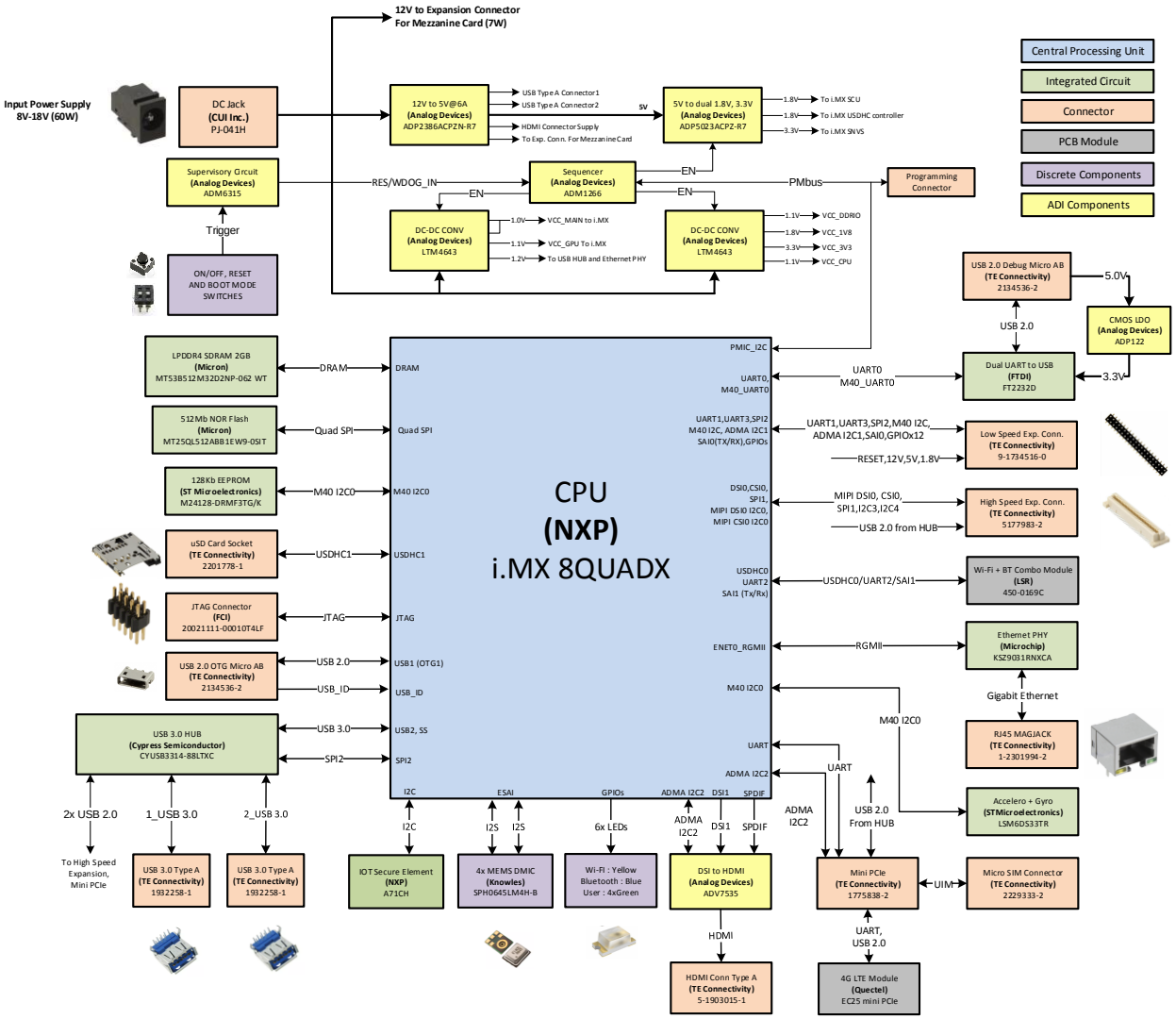


Figure 4 : Hardware Block Diagram

5 ADDRESS MAP

Memory address Map will be included in Firmware package.

6 CPU DESIGN CONSIDERATIONS

The functional specifications of the iMX8 QUADX processor are explained in the following sub-sections

6.1 CPU Power

Voltage Name	Min (V)	Typical(V)	Max (V)	Description
VDD_A35	1.05	1.10	1.15	Power supply of Cortex-A35 cluster
VDD_GPU	1.05	1.10	1.15	Power supply of GPU instance
VDD_MAIN	0.95	1.00	1.05	Power supply of remaining core logic
VDD_DDR_VDDQ	1.06	1.10	1.17	Power supplies of memory IOs
VDD_DDR_PLL_1P8	1.65	1.80	1.95	Power supplies of memory PLLs
VDD_MIPI_1P0	0.95	1.00	1.05	Power supplies of PHYs (1.0V part)
VDD_ANA0_1P8	1.65	1.80	1.95	Power supplies of IOs, analog and oscillator of the SCU
VDD_ANA1_1P8	1.65	1.80	1.95	Power supplies of IOs, analog and oscillator of the SCU
VDD_ADC_1P8	1.65	1.80	1.95	Power supplies of PHYs and GPIO operating at 1.8V
VDD_ADC_DIG_1P8	1.65	1.80	1.95	Power supplies of PHYs and GPIO operating at 1.8V
VDD_MIPI_1P8	1.65	1.80	1.95	Power supplies of PHYs and GPIO operating at 1.8V
VDD_MIPI_CSI_DIG_1P8	1.65	1.80	1.95	Power supplies of PHYs and GPIO operating at 1.8V
VDD_USB_1P8	1.65	1.80	1.95	Power supplies of PHYs and GPIO operating at 1.8V
VDD_PCIE_1P8	1.71	1.80	1.89	Power supplies of PCIE PHY (1.8 V part)
VDD_USB_3P3	3.00	3.30	3.60	Power supplies of PHYs and GPIO operating at 3.3V
VDD_CAN_UART_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_CSI_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_EMMC0_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_EMMC0_VSELECT_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_ENET_MDIO_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_MIPI_DSI_DIG_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_PCIE_DIG_1P8_3P3	3.15	3.3	3.45	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_QSPI0A_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_QSPI0B_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_SPI_MCLK_UART_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_SPI_SAI_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_TMPR_CSI_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_USDHC1_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_USDHC1_VSELECT_1P8_3P3	1.65	1.80	1.95	Power supplies of GPIO supporting both 1.8V or 3.3V
VDD_ENET0_1P8_2P5_3P3	1.65	1.80	1.95	Power supplies of Ethernet IOs
VDD_ENET0_VSELECT_1P8_2P5_3P3	1.65	1.80	1.95	Power supplies of Ethernet IOs
VDD_ESAI_SPDIF_1P8_2P5_3P3	1.65	1.80	1.95	Power supplies of Ethernet IOs
VDD_SNVS_4P2	2.40	3.30	4.20	Power supply of SNVS

6.2 CPU Clocks

Clock Name	Typical	Min	Max	Description
RTC_XTALI Oscillator	32.768KHz	-	-	RTC Clock
XTALI Oscillator	24MHz	-	-	Processor Main Clock

6.3 CPU Boot Mode settings

BOOT_CONFIG[3:1]	Boot mode description
0x0	BOOT From Fuse
0x1	Serial Download
0x2	eMMC0
0X3	SD1 boot
0x4	NAND 8-bit 128page
0x5	NAND 8-bit 32page
0x6	QSPI 3B READ
0X7	QSPI Hyperflash3.3V
0XC	SCU_PRIVATE_BOOT_I2C
0XD	Reserved
0XE	Infinite Loop Mode
0XF	TEST MODE

7 BOARD POWER AND RESET CONSIDERATIONS

Board level power requirements are mentioned here

7.1 Voltage generation diagram

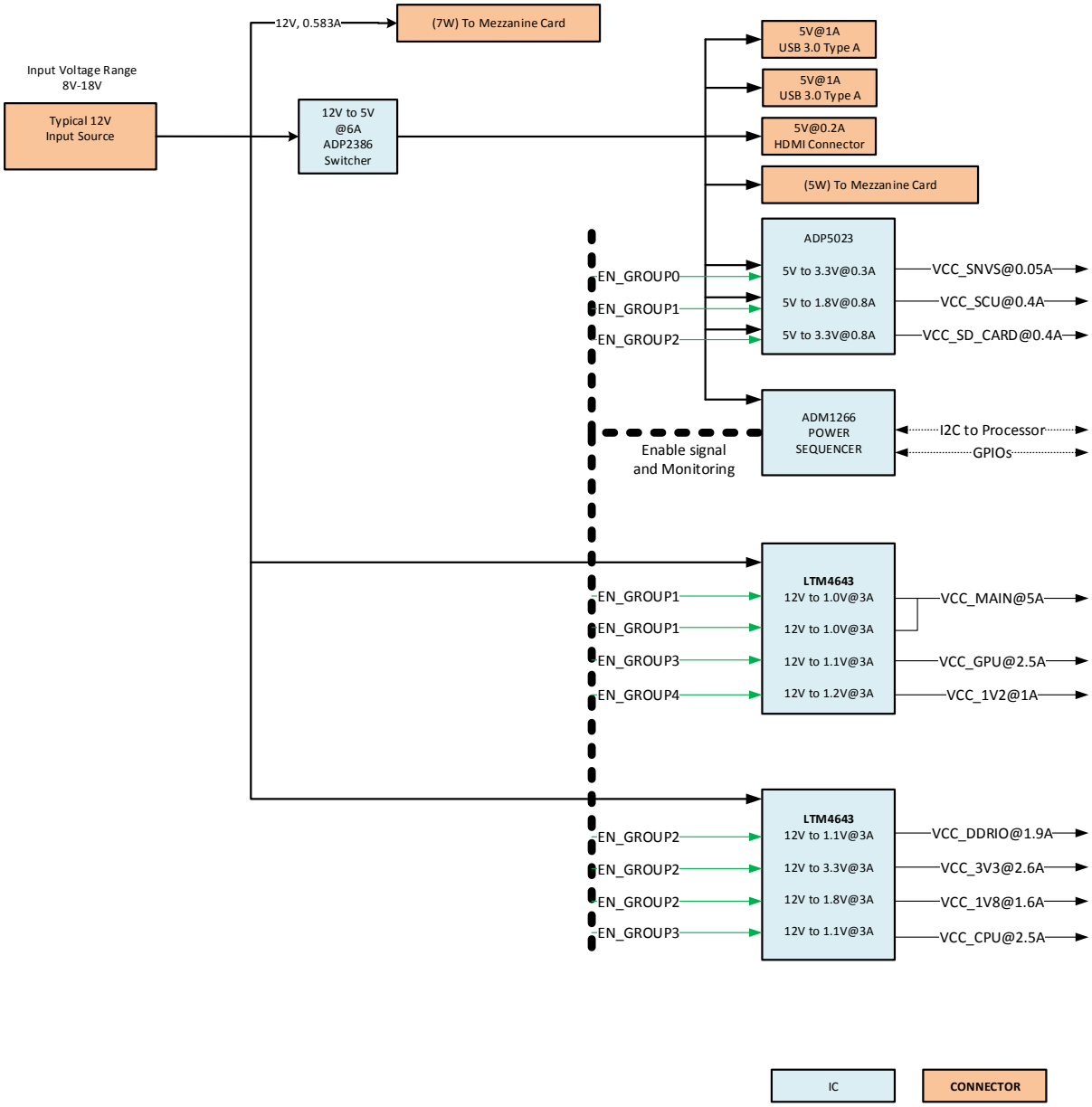


Figure 5 : System Voltage Generation

Above chart shows high-level power tree for iMX8XML Reference Design.
Refer Power Budget Analysis sheet below for more details:

eI_Arrow_iMX8XML_
RD_PowerBudgetAr

7.2 Power Sequencing

Supply Groups	Voltage				
Group 0	**2.4 - 4.2v**	**1.8v internal LDO**			
	VDD_SNVS_4P2	VDD_TMPR_CSI_1P8_3P3[1]			
Group 1	**1.0v**	**1.8v**			
	VDD_MAIN	VDD_ANAx_1P8			
	VDD_MIPI_1P0				
Group 2	**1.2 - 1.35v**	**1.8v**	**1.8v or 3.3v**	**1.8v or 3.3v switchable**	**3.3v**
	VDD_DDR_VDDQ	VDD_ADC_DIG_1P8	VDD_CAN_UART_1P8_3P3	VDD_EMMC0_1P8_3P3	VDD_USB_3P3
		VDD_ADC_1P8	VDD_CSI_1P8_3P3	VDD_USDHC1_1P8_3P3	
		VDD_DDR_PLL_1P8	VDD_EMMC0_VSELECT_1P8_3P3		
		VDD_MIPI_1P8	VDD_ENET_MDIO_1P8_3P3		
		VDD_MIPI_CSI_DIG_1P8	VDD_MIPI_DSI_DIG_1P8_3P3		
		VDD_PCIE_1P8	VDD_PCIE_DIG_1P8_3P3		
		VDD_USB_1P8	VDD_QSPI0x_1P8_3P3		
			VDD_SPI_MCLK_UART_1P8_3P3		
			VDD_SPI_SAI_1P8_3P3		
			VDD_TMPR_CSI_1P8_3P3[1]		
			VDD_USDHC1_VSELECT_1P8_3P3		
Group 3	**1.1 - 1.1v**	**1.0v internal LDO's**	**1.8v or 2.5v or 3.3v**		
	VDD_A35[2]	VDD_USB_OTG_1P0	VDD_ENET0_1P8_2P5_3P3		
	VDD_GPU[2]		VDD_ENET0_VSELECT_1P8_2P5_3P3		
			VDD_ESAI_SPDIF_1P8_2P5_3P3		

Power up
The device has the following power-up sequence requirements:

- Supply group 0 (SNVS) must be powered first. It is expected that group 0 will typically remain always on after the first power-on.
- Supply group 1 (MAIN and SCU) and group 0 must both be powered to their nominal values prior to boot. They must power up after or simultaneously with group 0.
- Supply group 2 (I/O's and DDR interface) consists of those modules required to start the boot process by accessing external storage devices. These must be fully powered prior to POR release if booting from one of these supplies interfaces. They must power up after or simultaneously with group 1.
- Supply group 3 consists of the remaining portions of the SoC. This includes non-boot I/O voltages and supplies for the major computational units. These can be sequenced in any order and as required to perform the desired functions for the intended application.

Power Down
The device processor has the following power-up sequence requirements:

- Supply group 0 must be turned off last, after all other supplies.
- Supply group 1 can be turned off just prior to group 0
- All remaining supplies can be turned off prior to group 1.

7.3 Reset Flow

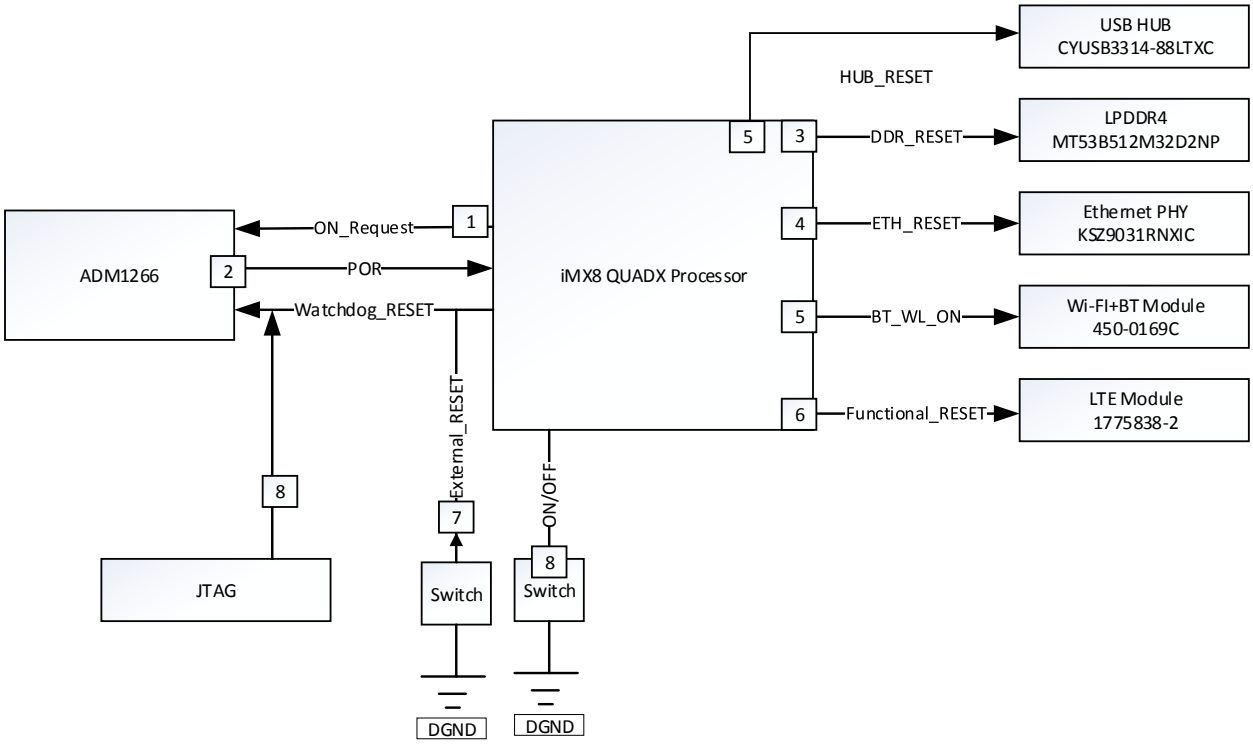


Figure 6 : RESET flow of iMX8XMK_RD

8 PIN FUNCTIONS

8.1 Processor GPIO Pin Description

GPIO BANK0

GPIO6	OUTPUT_USER LED2 CONTROL
GPIO7	OUTPUT_USER LED3 CONTROL
GPIO8	OUTPUT_USER LED4 CONTROL
GPIO29	TO LOW SPEED EXPANSION CONNECTOR
GPIO30	TO LOW SPEED EXPANSION CONNECTOR
GPIO31	TO LOW SPEED EXPANSION CONNECTOR

Figure 7 : iMX8X Processor GPIO Bank0 pin Assignment

GPIO BANK1

GPIO1	TO LOW SPEED EXPANSION CONNECTOR
GPIO2	INTERRUPT FROM ACCELEROMETER + GYRO SENSOR
GPIO3	TO LOW SPEED EXPANSION CONNECTOR
GPIO13	TO LOW SPEED EXPANSION CONNECTOR
GPIO14	TO LOW SPEED EXPANSION CONNECTOR
GPIO29	TO LOW SPEED EXPANSION CONNECTOR
GPIO30	TO LOW SPEED EXPANSION CONNECTOR

Figure 8 : iMX8X Processor GPIO Bank1 pin Assignment

GPIO BANK3

GPIO0	**POWER_CONTROL_GPIO**
GPIO1	**SLEEP CONTROL TO CELLULAR MODULE_3.3V**
GPIO2	**WATCHDOG DISABLE TO CELLULAR MODULE_3.3V**
GPIO3	**INPUT SIM CARD DETECTION_3V3**
GPIO7	TO LOW SPEED EXPANSION CONNECTOR
GPIO24	OUTPUT WLREG_BTREG_ON TO Wi-Fi+BT MODULE
GPIO13	OUTPUT NOR MEMORY CHIP DISABLE
GPIO14	TO LOW SPEED EXPANSION CONNECTOR
GPIO15	INPUT ETHERENT INTERRUPT
GPIO17	OUTPUT BT_DEV_WAKE FOR Wi-Fi+BT MODULE
GPIO18	WL_BT_GPIO1_Wi-Fi+BT MODULE
GPIO19	WL_BT_GPIO2_Wi-Fi+BT MODULE
GPIO20	OUTPUT LPO_IN TO Wi-Fi+BT MODULE
GPIO21	OUTPUT SW_CTRL TO Wi-Fi+BT MODULE
GPIO22	INPUT BT_HOST_WAKE TO Wi-Fi+BT MODULE
GPIO23	INPUT WLAN_HOST_WAKE TO Wi-Fi+BT MODULE
GPIO08	OPTIONAL CLOCK FOR HIGH SPEED CONNECTOR

Figure 9 : iMX8X Processor GPIO Bank3 pin Assignment

GPIO BANK4

GPIO1	**OUTPUT FUNCTIONAL RESET OF CELLULAR MODULE_3.3V**
GPIO2	**OUTPUT PCIE_WAKE_LTE TO CELLULAR MODULE_3.3V**
GPIO13	OUTPUT WRITE PROTECTION TO EEPROM
GPIO14	OUTPUT ETHERNET RESET
GPIO4	**OUTPUT USB HUB RESET_3.3V**
GPIO16	OUTPUT USER LED1 CONTROL
GPIO17	OUTPUT Wi-Fi LED CONTROL
GPIO18	OUTPUT BLUETOOTH LED CONTROL
GPIO19	OUTPUT BTREG_ON TO Wi-Fi+BT MODULE
GPIO21	OUTPUT BT_DEV_WAKE FOR Wi-Fi+BT MODULE
GPIO18	WL_BT_GPIO1_Wi-Fi+BT MODULE
GPIO0	**INPUT_WAKE_HOST FROM CELLULAR MODULE_3.3V**
GPIO6	**RESET_HDMI_3V3**

Figure 10 : iMX8X Processor GPIO Bank4 pin Assignment

8.2 Processor I2C Pin Description

DEVICE	DEVICE ADDRESS	I2C	IO LEVEL	BOARD
ADM1266 SEQUENCER	0x40	PMIC_I2C	1.8V/3.3V	CPU
EXPANSION CONN (LS)	NOT FIX	M40.I2C0	1.8V	MEZZANINE
EXPANSION CONN (LS)	NOT FIX	ADMA.I2C2	1.8V	MEZZANINE
EXPANSION CONN (HS)	NOT FIX	MIPI_DSI0_I2C0	1.8V	MEZZANINE
EXPANSION CONN (HS)	NOT FIX	MIPI_CSI0_I2C0	1.8V	MEZZANINE
SENSOR ACCEL+GYRO	0x6D	M40.I2C0	1.8V	CPU
EEPROM	0x50	M40.I2C0	1.8V	CPU
DSI TO HDMI BRIDGE	0x3D	ADMA_I2C1	3.3V	CPU
QUECTEL PCIe CONN	TBD	ADMA_I2C2	1.8V	MODULE
USB 3.0 HUB	0X60	ADMA_I2C1	3.3V	CPU
A71CH SECURITY IC	0X93	ADMA_I2C2	1.8V	CPU

Figure 11 : iMX8XML Reference Design I2C pin Description

iMX8XML_I2C_Topology

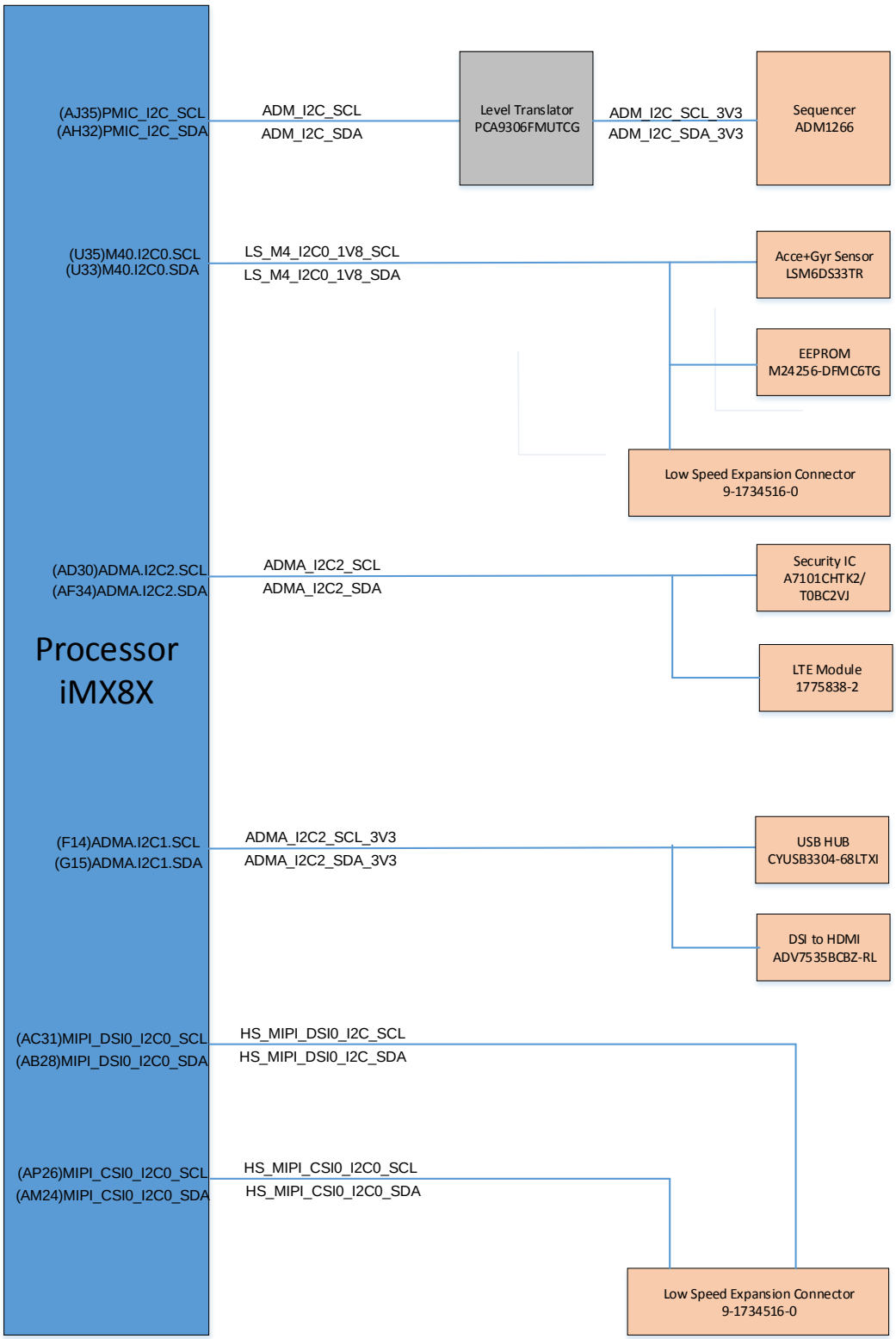


Figure 12 : iMX8XML Reference Design I2C Topology

9 TIMING REQUIREMENTS

Timing requirement and measurements of all the interfaces will be recorded in Electrical Design Validation Testing (EDVT) document.

SI Analysis performed for below high speed interface in hyperlinks tool.

1. DDR
2. MIPI CSI
3. MIPI DSI
4. USB
5. HDMI
6. QUAD SPI
7. ETHERNET
8. USDHC

SI Analysis Report

Adobe Acrobat Document

10 PRODUCT CHARACTERISTICS AND OPERATING CONDITIONS

Index	Function	Specifications
1	Input power supply	8V-18V (60W Maximum)
2	External accessories requirement	Mezzanine Cards, Adapters, USB, SD card, Debug Cable
3	Handling requirements	Mechanical Enclosure
4	Typical use cases	Machine Learning
5	Operating Temperature Range	0C to 55C
6	Storage Temperature Range	NA

Table 6: Product operating condition

11 HARDWARE INTERFACES

This section describes the interface features of the processor (iMX8 QUADX) and its peripherals used for Reference Design. Each interface is described in details with timing requirement, selected major component details and other design guidelines as recommended in datasheet of respective component

11.1 System Processor – iMX8 QUADX

IMX8 QUADX processor includes a customized 64-bit ARM Cortex-A35 compliant Quad-core application processor which targets machine learning application.

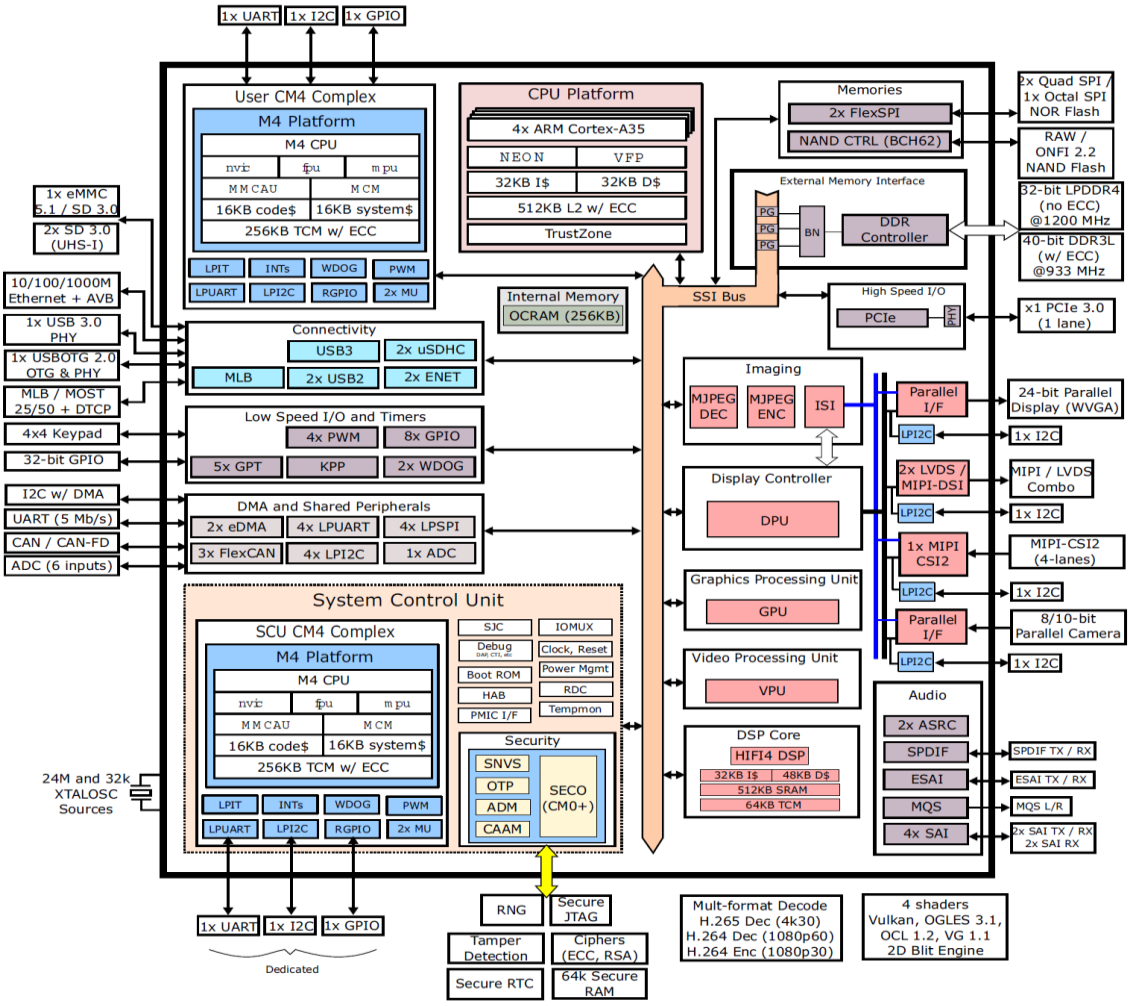


Figure 13 : iMX8 QUADX Processor Architecture

11.1.1 Interface Features

- AArch64 for 64-bit support and new architectural features
- AArch32 for full backward compatibility with ARMv7
- Cortex-A35 cores support ARM virtualization extensions.
- Cortex-M4F cores for real-time applications

- Graphics Processing Unit (GPU) and Video Processing Unit (VPU)

11.1.2 Interface Description:

IMX8 QUADX is used as main processing unit on the iMX8XML Reference Design to control overall operation of the unit. It supports two 4-lane DSI Display and also provide 4-lane CSI interface for camera related video applications. The processor support other interfaces like USB, SD card and signals for Low speed and high speed expansion connector to meet 96boards specification. Processor also supports wireless interface Module 450-0169C for Wi-Fi, Bluetooth and supports PCI LTE Module.

Part Number	Manufacturer	Description	Package
PIMX8QX6AVLFZAA	NXP Semiconductor	1.2 GHz Quad core application processor	609 pin FCPBGA

Table 7: CPU Component Details

11.1.3 PCB Layout and Mechanical Constraints

Layout guideline recommended by NXP for the processor followed in the layout design. A separate layout guideline document listing all the layout guidelines for iMX8XML Reference Design prepared and shared with layout designer.

NXP layout guideline followed for IMX8 QUADX as mentioned below:
NXP Document: IMX8_Hardware_Developers_Guide_v0.5

Package of the processor designed in way to dissipate the heat through the Metal surface of Processor.
Processor is placed at bottom side of PCB so that Heat dissipation can be taken care by Enclosure design.
Note: Mezzanine will be mounted at top side so Metal heat sink cannot be placed if kept in top side of PCB

Thermal Parameter	Test Conditions	Symbol	Value	Unit
Junction to Ambient[2]	Single-layer board (1s); natural convection[3]	$R_{\theta JA}$	27.7	°C/W
	Four-layer board (2s2p); natural convection[2]	$R_{\theta JA}$	15.2	°C/W
Junction to Ambient[1]	Single-layer board (1s); air flow 200 ft/min[4]	$R_{\theta JMA}$	17.6	°C/W
	Four-layer board (2s2p); air flow 200 ft/min[4]	$R_{\theta JMA}$	10.5	°C/W
Thermal Parameter	**Test Conditions**	**Symbol**	**Value**	**Unit**
Junction to Board[1,5]	—	$R_{\theta JB}$	2.9	°C/W
Junction to Case (top)[1,6]	—	$R_{\theta JCtop}$	0.7	°C/W

Table 8: Thermal Resistance Table for Processor

PCB stack up designed in a way to support this heat dissipation in order to comply the temperature specification.
12 Layers stack up used so that larger plane for power can be provided to the PCB.

High speed signal Length Match Report of iMX8XML_RED is at below SVN location
\13. Hardware Specific\Layout\Arrow-IMX8XML_MotherBoard\Reference Documents\Length Matching

11.2 LPDDR4 Memory Interface

Processor requires RAM for its normal functionality. 2GB LPDDR4 memory is provided on IMX8XML_RD device interfaced with processor. Higher memory part (3GB/4GB) can also be used instead of 2GB part. The processor supports high speed LPDDR4 operating at 1200 MHz clock rate

11.2.1 Interface Features

IMX8 QUADX supports Non Pop LPDDR4 SDRAM interface. It supports 32-bit LPDDR4 SDRAM.

11.2.2 Interface Description

2GB RAM is to be provided on IMX8XML_RD device.

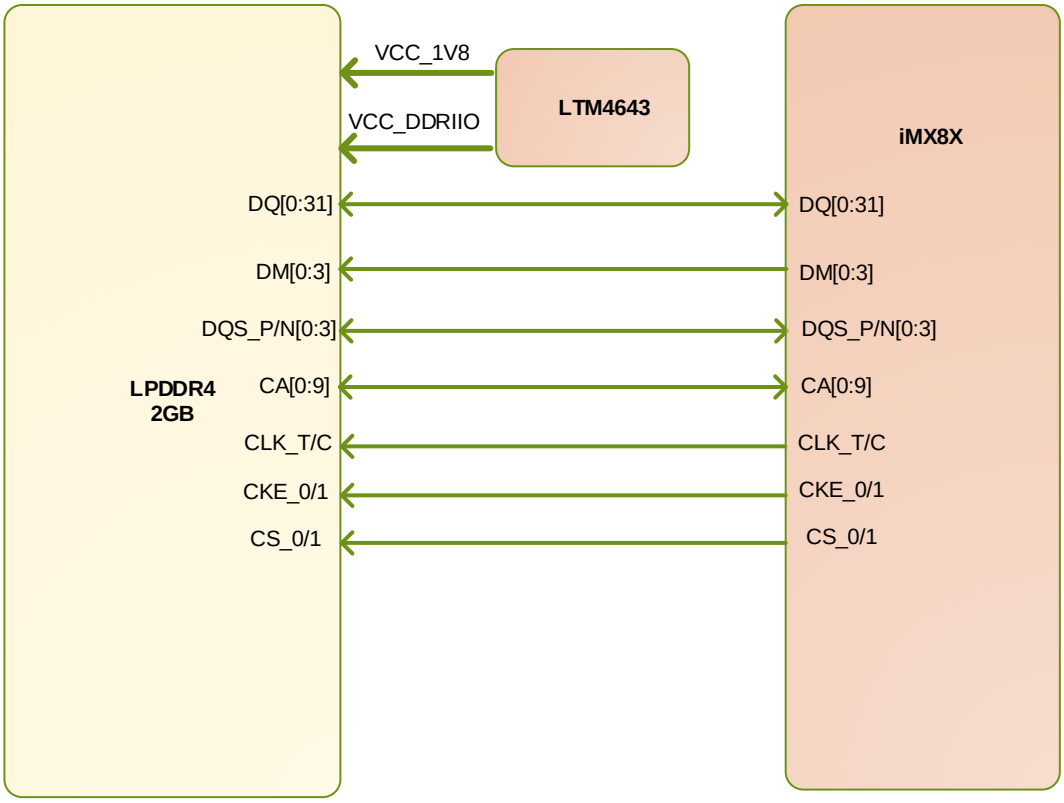


Figure 14 : LPDDR4 Interface Block Diagram

11.2.3 Component Details

Part Number	Manufacturer	Description	Package
MT53B512M32D2NP-062 WT	Micron	LPDDR4 2GB	10X14.5 mm 200 WFBGA

Table 9: LPDDR4 Component Details

11.2.4 PCB Layout Guide

For LPDDR4, layout guideline recommended by NXP for the processor followed in the layout design.
A separate layout guideline document listing all the layout guidelines for iMX8XML Reference Design prepared and shared with layout designer.

NXP layout guideline for Memory followed for IMX8 QUADX as mentioned below:
NXP Document: IMX8_Hardware_Developers_Guide_v0.5

11.3 SD card Memory Interface

SD card – Secure digital card memory provided on iMX8XML_RD as a main non-volatile memory.
It will be used for storing SW binaries, data, Android applications etc.

11.3.1 Interface Features

Processor iMX8 QUADX supports:

- Two SDIO(or USDHC) interface
- Maximum clock up to 200MHz
- Data Rage up to 400Mbit/sec per line

11.3.2 Interface Description

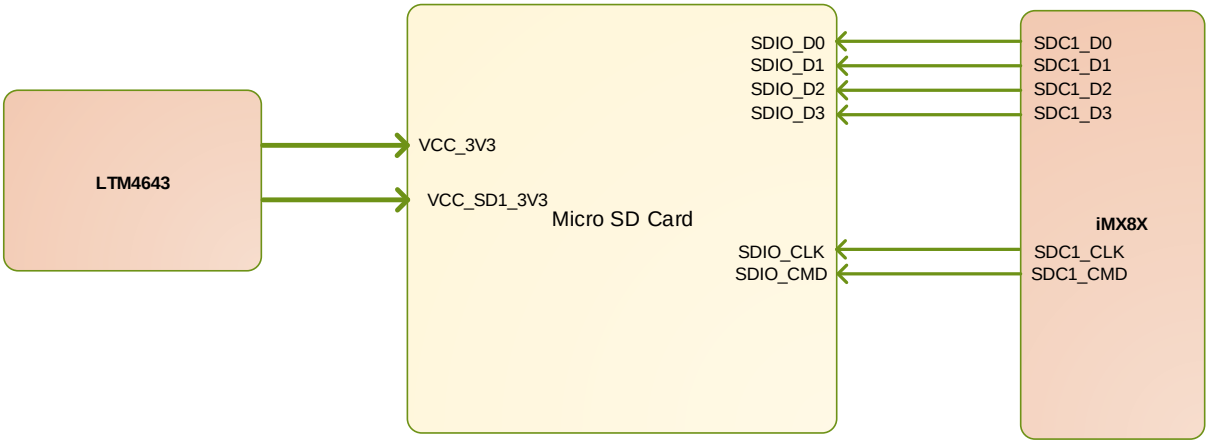


Figure 15 : SD card Interface Block Diagram

11.3.3 PCB Layout Guide for SD card

SD card connector placed as per 96board standard.
SDIO signals are 50E impedance matched as per layer stack up.

11.4 MIPI DSI Display Interface

iMX8 QUADX supports two 4-lane DSI port, which can support the display up to 1080p@60fps resolution. iMX8XML_RD used both the DSI ports.

1. DSI port connected to High speed connector
2. DSI converted to HDMI for display (through ADV7535)

11.4.1 Interface Features

Following point describes the detailed features of ADV7535 Chipset.

- Output support 24-bit RGB 4:4:4 (also support 30 and 36 bit)
- Audio inputs accept logic levels from 1.8 V to 3.3 V
- Supports up to 891 Mbps per lane
- video resolutions up to 1080p at 60 Hz
- Automatic input video format timing detection (CEA-861E)
- Supports standard S/PDIF for stereo LPCM or compressed audio up to 192 kHz
- 5 V tolerant I2C and HPD inputs/outputs (I/Os), no extra device needed
- HDMI Maximum output clock up to 148.5MHz

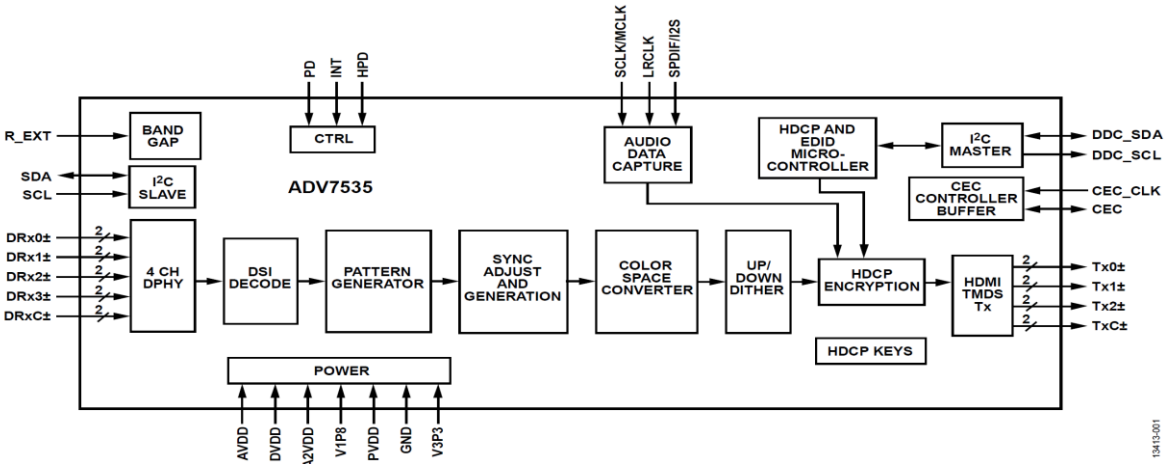


Figure 16 ADV7535 functional block diagram

11.4.2 DSI1 Interface Description

DSI1 port is mux with LVDS1 port in processor. Earlier LVDS to HDMI converter used in design but then DSI to HDMI converter used for compact size as space is very less for layout on board.

DSI to HDMI bridge chip(0.5 mm pitch) need 3 Mil trace for FAN out and fabricator support up to 3 Mil with through hole vias only. It was possible to do FAN out of DSI to HDMI bridge chip using 3 Mil traces so we opted for DSI to HDMI bridge chip over LVDS to HDMI.

iMX8XML_RD will support one 4-lane MIPI DSI1 interface to convert it into HDMI output supporting 1080P resolution via DSI to HDMI Bridge Chip.

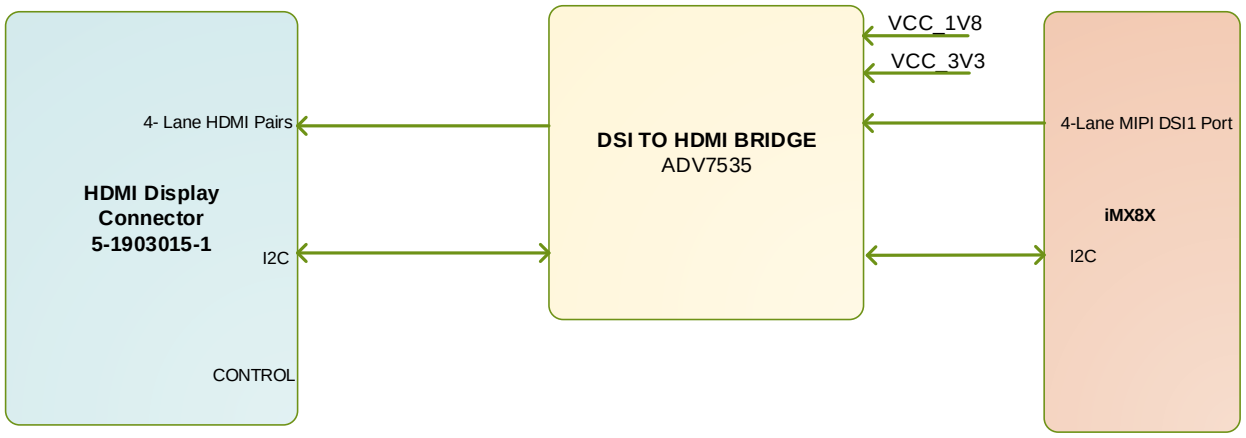


Figure 17: DSI1 Interface Diagram

11.4.3 Components for DSI1 interface

Part Number	Manufacturer	Description	Package
ADV7535	Analog Devices Inc.	DSI to HDMI Converter	49-Ball WLCSP
5-1903015-1	TE Connectivity	HDMI Connector	Through Hole, Right Angle

Table 10: DSI1 Interface Component Details

11.4.4 DSI0 Interface Description

iMX8XML_RD will support one 4-lane MIPI DSI0 interface to connect with high speed expansion connector.
Display will be at Mezzanine card which will be mounted on iMX8XML_RD

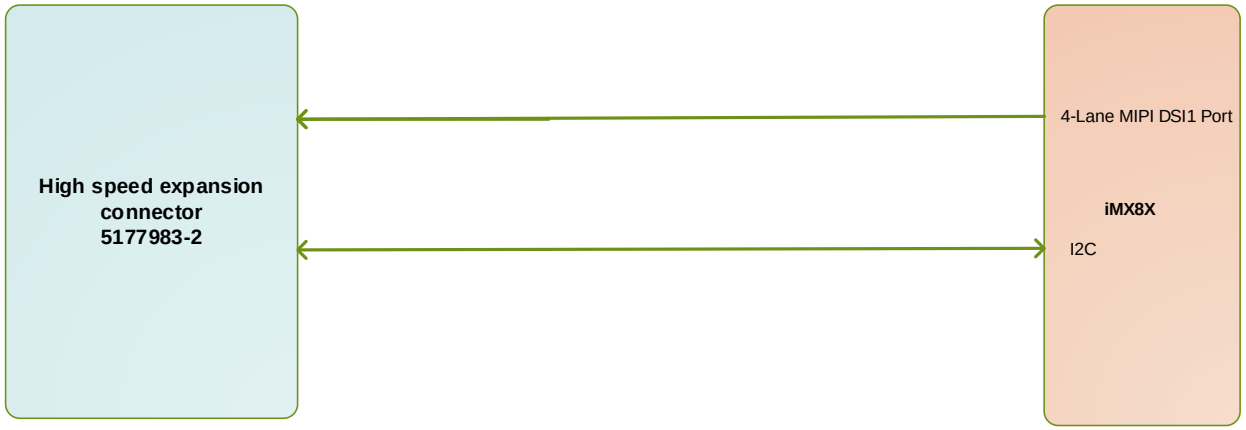


Figure 18: DSI0 Interface Diagram

11.4.5 Components for DSI0 interface

Part Number	Manufacturer	Description	Package
5177983-2	TE Connectivity	60 pin connector	SMD

Table 11: DSI0 Interface Component Details

11.4.6 Design Guidelines

1. As per recommendation if the best EMI practices followed for DSI & LVDS signals, there is no need for common mode choke filters. However, CMC provided as per design constraints.
2. Extreme care must be taken that no stubs are created.

11.4.7 PCB Layout Guidelines

1. DSI & HDMI signals are high-speed signals. Special care shall be taken for grounding of these signals.
2. Differential and signal ended impedance tolerance should not be more than 10%.
3. Intra-pair length match should be within 0.7mm (5ps).
4. Inter lane length match should be within 1.4mm (10ps).
5. There should be minimum 2.5x trace width spacing between lanes to other signals.

11.5 MIPI CSI Display Interface

iMX8 QUADX supports one 4-lane CSI port which used to connect high speed expansion connector as per 96boards standard.

11.5.1 Interface Features

MIPI CSI port is used to capture input video data from camera at Mezzanine card.

11.5.2 CSI0 Interface Description

iMX8XML_RD will support one 4-lane MIPI CSI which is connected as per below image.

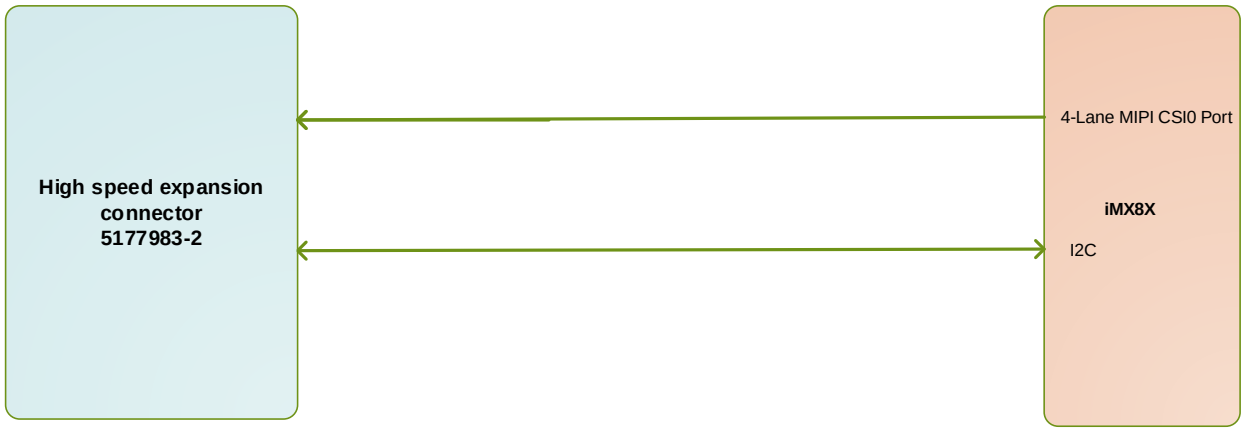


Figure 19: CSI0 Interface Diagram

11.5.3 Components for CSI0 interface

Part Number	Manufacturer	Description	Package
5177983-2	TE Connectivity	60 pin connector	SMD

Table 12: CSI0 Interface Component Details

11.5.4 Design Guidelines

1. As per recommendation if the best EMI practices followed for CSI signals, there is no need for common mode choke filters. However, CMC provided as per design constraints.
2. Extreme care must be taken that no stubs are created.

11.5.5 PCB Layout Guidelines

1. CSI signals are high-speed signals. Special care shall be taken for grounding of these signals.
2. Differential and signal ended impedance tolerance should not be more than 10%.
3. Intra-pair length match should be within 0.7mm (5ps).
4. Inter lane length match should be within 1.4mm (10ps).
5. There should be minimum 2.5x trace width spacing between lanes to other signals.

11.6 Wi-Fi/BT Interface:

iMX8XML_RD can transfer files over Wi-Fi and Bluetooth.
To meet the above requirement a combined Wi-Fi (802.11 a/b/g/n/ac, 2.4GHz and 5GHz) plus Bluetooth (BT 4.2) module 450-0169C selected.

11.6.1 Wi-Fi Interface Features

Following point describes the detailed Wi-Fi features of 450-0169C Module

- IEEE 802.11 a/b/g/n/ac (single stream n)
- Available with integrated chip antenna
- Operating temperature: -40C to +85C
- Compact design based on Cypress BCM43353 SoC
- EMC Compliance: FCC (USA), IC (Canada), & ETSI (Europe)
- REACH and RoHS compliant
-

11.6.2 BT Interface Features

Following point describes the detailed BT features of 450-0169C Module

- Bluetooth 4.2 (Bluetooth Low Energy)
- Available with integrated chip antenna
- Operating temperature: -40C to +85C
- Compact design based on Cypress BCM43353 SoC
- EMC Compliance: FCC (USA), IC (Canada), & ETSI (Europe)
- REACH and RoHS compliant

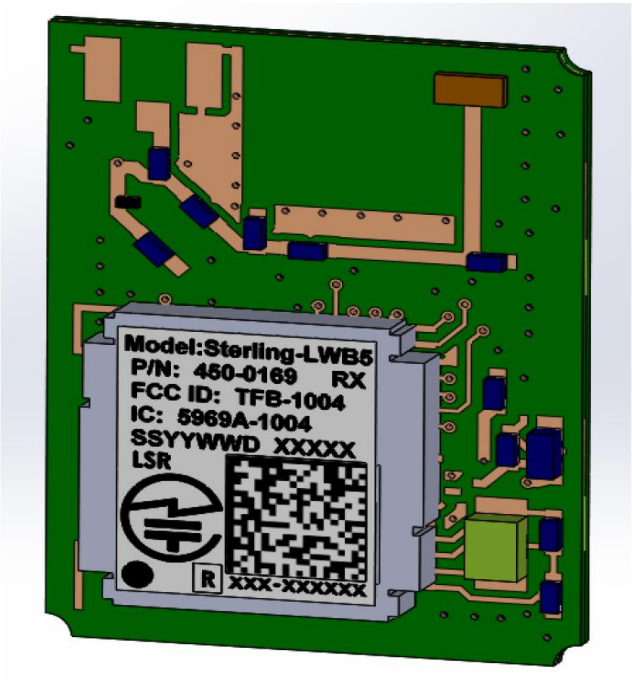


Figure 3 Sterling-LWB5 Chip Antenna Module (450-0169)

Figure 20: LSR Module with Chip Antenna

11.6.3 Interface Description

To support the Hi-speed data transfer between the Wi-Fi module and the host processor, USDHC interface of the IMX8 QUADX is used and for the Bluetooth interface, serial UART communication is used to transfer data between processor and connected Bluetooth device.

Module is having ON chip Antenna for Wi-Fi and Bluetooth.

Following figure shows the basic level interface between the processor iMX8 QUADX and the wireless Module.

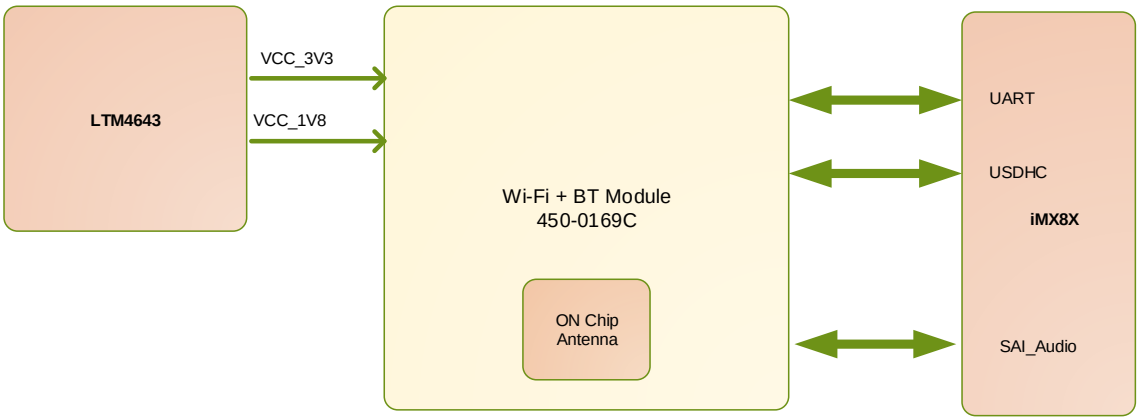


Figure 21: Wi-Fi + BT Module Interface Diagram

11.6.4 Component Details

Part Number	Manufacturer	Description	Package
450-0169C	LSR	2.4/5 GHz Wi-Fi + BT Module	SIP Module

Table 13: Wi-Fi + BT Interface Component Details

11.6.5 PCB Layout Guidelines

1. USDHC signals are high speed signals. Special care shall be taken for grounding of these signals.
2. Differential and signal ended impedance tolerance should not be more than 10%

Sr#	96boards standard Requirement	Wi-Fi + BT 450-0169C Module
1	IEEE 802.11 g/n	Yes
2	BT 4.0 LE	Yes

Table 14: Wi-Fi/BT Module Selection

11.7 DMIC Audio Interface

iMX8XML_RD device is having four DMIC for voice reorganization application.

11.7.1 Interface Features

iMX8 QuadX Processor is having one ESAI port where four I2S based Digital MIC are connected.
DMIC SPH0645LM4H-B with below features selected

- Low Current of typ. 600µA
- I2S Output: Direct attach to µP
- RF Shielded
- Omnidirectional
- Ultra-Stable Performance
- Supports Dual Microphones
- Packaged in SPH 3.50 x 2.65 x 0.98 mm

11.7.2 Interface Description

Four I2S based DMIC are interfaced with processor.

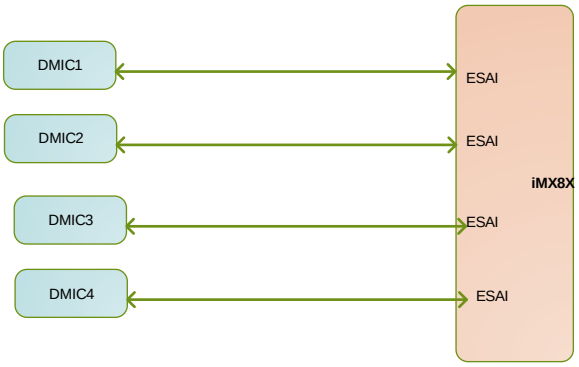


Figure 22: DMIC Interface Diagram

11.7.3 Component Details

Part Number	Manufacturer	Description	Package
SPH0645LM4H-B	Knowles	DMIC	Rectangular

Table 15: DMIC Interface Component Details

11.7.4 PCB Layout Guideline

DMIC shall be connected in daisy chain clock in layout for proper noise cancellation.
Online refer link : http://www.diva-portal.org/smash/get/diva2:940737/FULLTEXT01.pdf

Isolate DMIC signals from noise sources such as antenna, RF signals, EBI, SMPS, clocks, and other digital signals with fast transients to prevent noise from direct coupling onto the sensitive analog microphone traces.

11.8 USB Interface

iMX8 QUADX supports single USB controller with USB 3.0/2.0 support, which can be configured to Host/Device as per user application.

11.8.1 USB 3.0 Interface Description

iMX8XML_RD will have one USB3.0 HUB (CYUSB3304-68LTXI from Cypress), connected to USB3.0 port of iMX8 QUADX. Two downstream port used as USB3.0 Host port with a USB3.0 Type-A connector. Separate load switches on iMX8XML_RD will limit USB current on USB 3.0 ports as per USB specifications. This will protect iMX8XML_RD in case of short circuit. USB bandwidth will be shared between devices if more than one devices are attached to USB HUB.

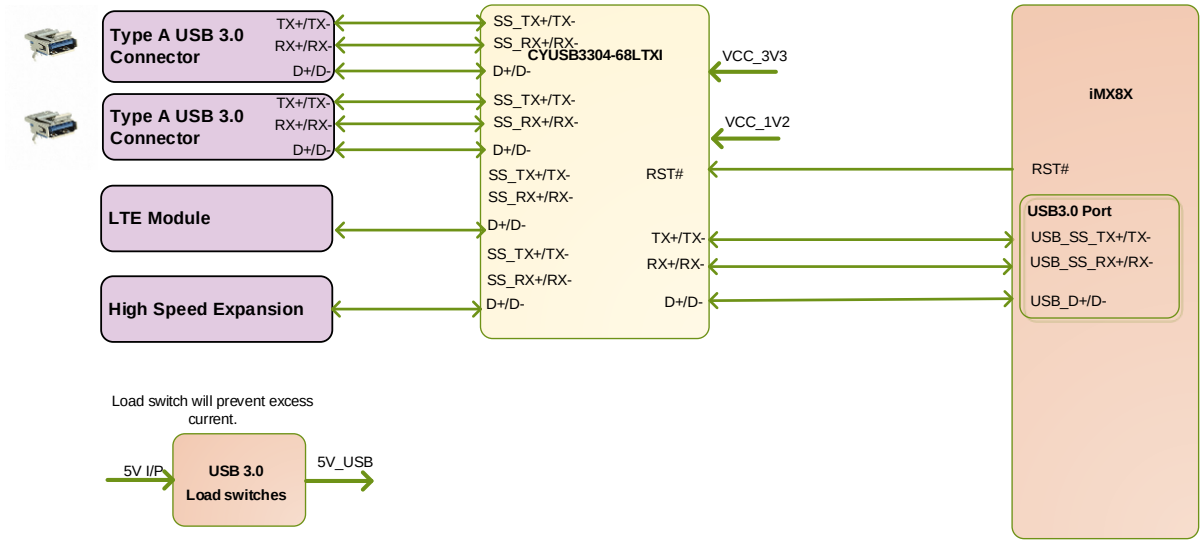


Figure 23 : USB 3.0 Top Level Interface Diagram

11.8.2 Component details

Part Number	Manufacturer	Description	Package
CYUSB3304-68LTXI	Cypress	IC 3.0 HUB	68 QFN
1932258-1 (2 Qty)	TE Connectivity	USB 3.0 Type A Connector	Through Hole, Right Angle
5177983-2	TE Connectivity	60 pin High speed expansion connector	SMD
1775838-2	TE Connectivity	LTE Connector	52pos

Table 16: USB 3.0 Interface – Component Details

11.8.3 USB 2.0 Interface Description

iMX8XML_RD will have one USB2.0 port which is used for OTG connection.

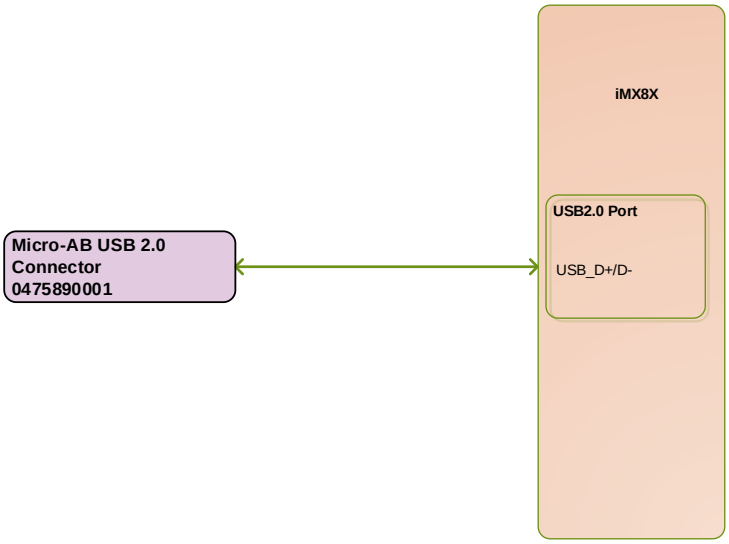


Figure 24 : USB 2.0 Top Level Interface Diagram

11.8.4 Component details

Part Number	Manufacturer	Description	Package
0475890001	TE Connectivity	USB Micro-AB OTG	5 Pin

Table 17: USB 2.0 Interface – Component Details

11.8.5 USB Design Guidelines

1. As per recommendation, capacitors on SS signals are added for HUB transmit.
2. Extreme care to be taken that no stubs are created.
3. Series capacitors for USB super-speed interface near Transmitter.
4. 900mA load current for both USB 3.0 type A connectors.

11.8.6 PCB Layout Guidelines

1. USB traces should be isolated from other high speed signals.
2. Maintain proper isolation between the USB 3.0 connector and RF antennas.
3. Place AC coupling capacitors on SS TX near the ESD diodes and connector
4. Keep isolation between the TX pair, Rx pair, and DP/DM to avoid crosstalk
5. Intra-pair length match should be within 7mm (5ps)
6. Rx to TX spacing and with other signals should be at least 4 times of USB trace width.

11.9 Switches/ Sensor/FAN/EEPROM & GPIO’s

There will be 3 switches (ON/OFF, RESET and Boot mode selection), FAN, Accelerometer-Gyroscope Sensor, Security IC and other GPIOs on iMX8XML_RD

11.9.1 Interface Description

1) ON/OFF switch is used to indicate various modes of system based on the time the switch is pressed
2) Boot mode selection switch is used to set by default booting option for processor
3) FAN is used to cool down the temperature of processor
4) Accelerometer and Gyroscope sensor and Security IC are used as per customer requirement
5) EEPROM is used to store product ID and other permanent detail

11.9.2 Component details

Part Number	Manufacturer	Description	Package
EVP-AA802Q	Panasonic	SWITCH TACTILE SPST-NO 0.02A 15V	SMD
218-4LPSTJR	CTS	SWITCH SLIDE DIP SPST 25MA 24V	SMD
LSM6DS33TR	STM	IMU ACCEL/GYRO I2C/SPI 16LGA	16-LGA
A7101CHTK2/T0BC2VJ	NXP	SECURE AUTHENTICATION	8-VDFN
1734709-2	TE	FAN Connector	2 pin SMD
M24256-DFMC6TG	STM	EEPROM	8-UFDFN

Table 18: Component Detail of Switches, EEPROM, FAN and sensors

11.10 Debug UART Interface

iMX8 QUADX is having two debug UART ports.
UART0 and UART2 of processor are used for debugging.
Two UART converted to USB through FTDI chip FT2232D-REEL.

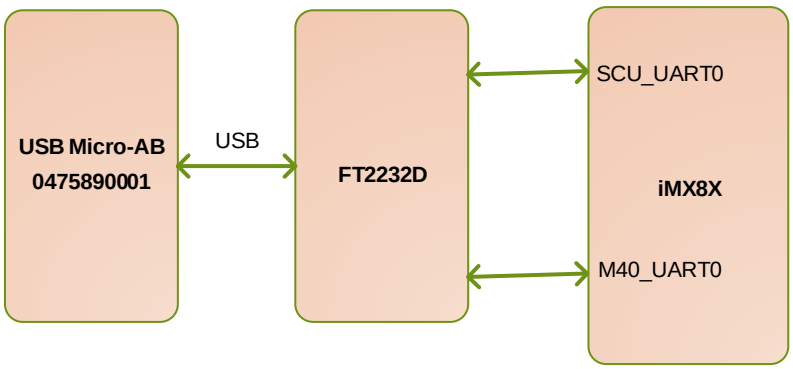


Figure 25: Debug UART to USB Interface

11.10.1 Component details

Part Number	Manufacturer	Description	Package
0475890001	TE	USB Micro-AB	Through hole
FT2232D-REEL	FTDI	UART to USB Converter	48-LQFP

Table 19: Debug UART to USB Interface – Component Details

11.11 Debug JTAG Interface

iMX8 QUADX processor can be programmed through JTAG emulator.
JTAG 10 pin connector added as per below image.

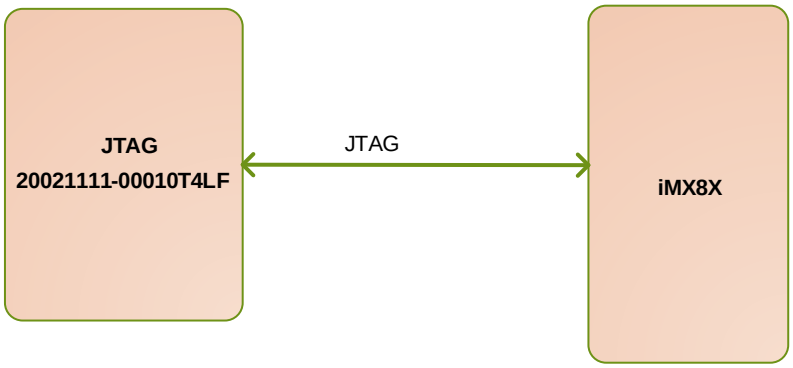


Figure 26: Debug JTAG Interface

11.11.1 Component details

Part Number	Manufacturer	Description	Package
20021111-00010T4LF	Amphenol FCI	10 pin Connector	Through hole

Table 20: Debug JTAG Interface – Component Details

11.12 Ethernet Interface:

iMX8XML_RD supports 1Gbps Ethernet connection.
MAC PHY KSZ9031RNXIC-TR from Microchip used for Ethernet.

11.12.1 Interface Features

Below are features of Ethernet PHY IC KSZ9031RNXIC-TR

- Single-Chip 10/100/1000 Mbps Ethernet Transceiver Suitable for IEEE 802.3 Applications
- RGMII with 3.3V/2.5V/1.8V Tolerant I/Os
- On-Chip Termination Resistors for the Differential Pairs
- Programmable LED Outputs for Link, Activity, and Speed
- Power-Down and Power-Saving Modes

11.12.2 Interface Description

Microchip PHY KSZ9031RNXIC-TR used between RJ45 connector and Processor as per below image.

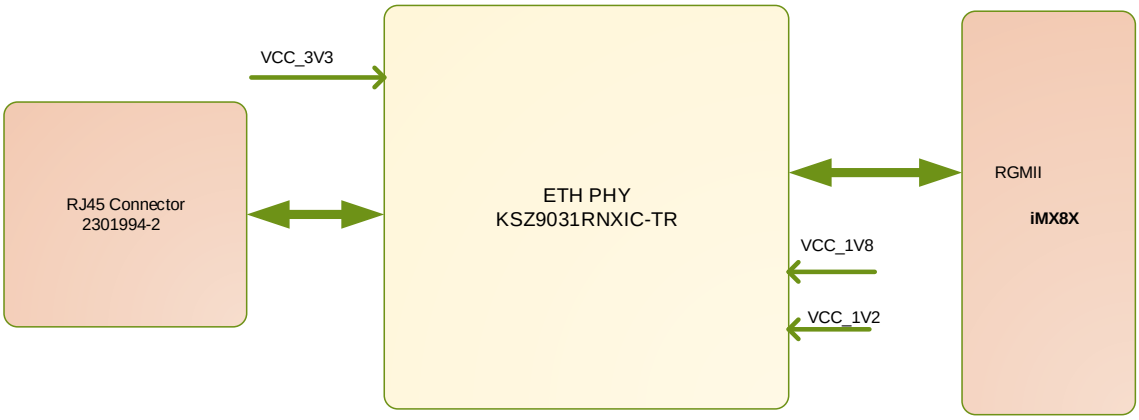


Figure 27: Ethernet Interface Diagram

11.12.3 Component Details

Part Number	Manufacturer	Description	Package
2301994-2	TE	RJ45 Connector	Through Hole

Table 21: Ethernet Interface Component Details

11.12.4 PCB Layout Guidelines

1. Ethernet signals are high speed signals.
   Special care shall be taken for grounding of these signals.
2. Differential and signal ended impedance tolerance should not be more than 10%

11.13 Power Supply

iMX8XML_RD device will have 12VDC (+8V to 18V @60W) for the input supply to power up processor and all its peripherals.

The processor and peripherals requires different voltage supplies and current for their normal functionality. The power supply section shall be designed to generate all required voltage rails with respective current requirements. The power supply section shall also suffice power sequence related requirement of each individual peripheral for its normal operation.

PMIC shall not be used for iMX8X processor.
Discrete power regulators from Analog device needs to be used. Power sequencer will be used to program power up sequence and other controlling operation.

Please find below power scheme difference.

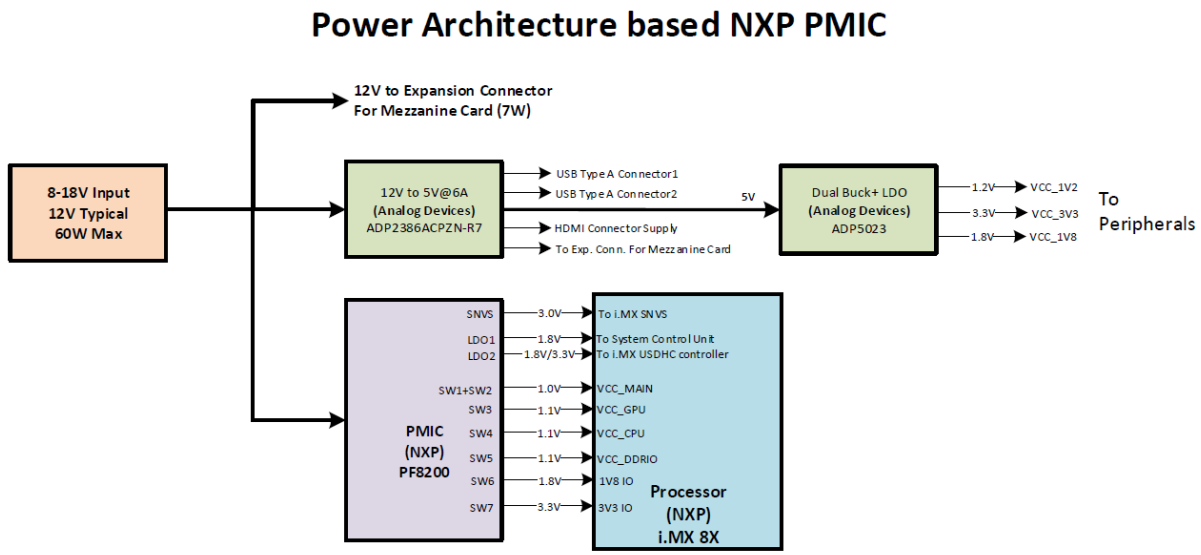


Figure 28: Power Architecture based on NXP PMIC

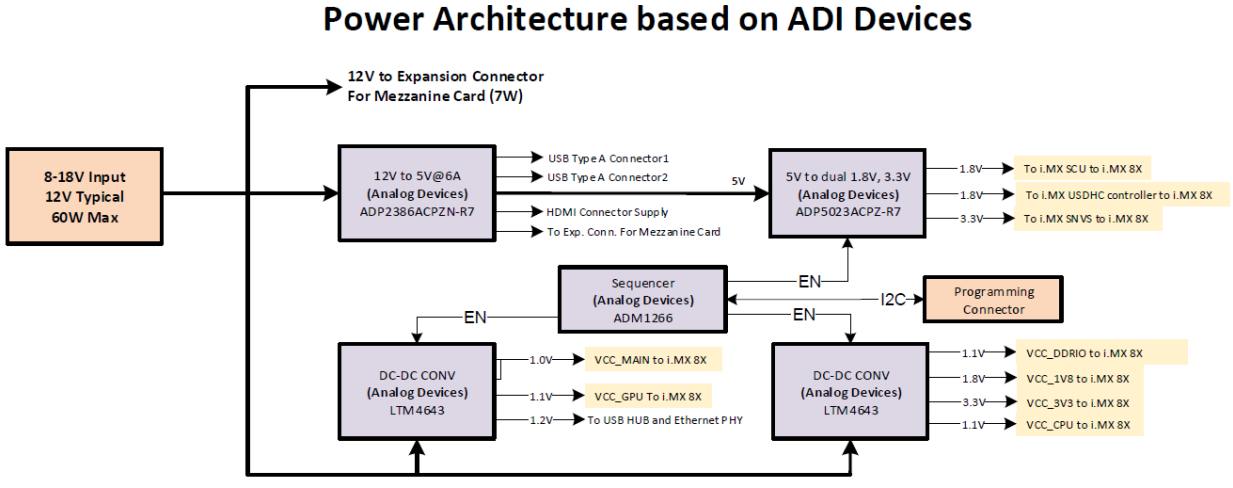


Figure 29: Power Architecture based on ADI Regulators

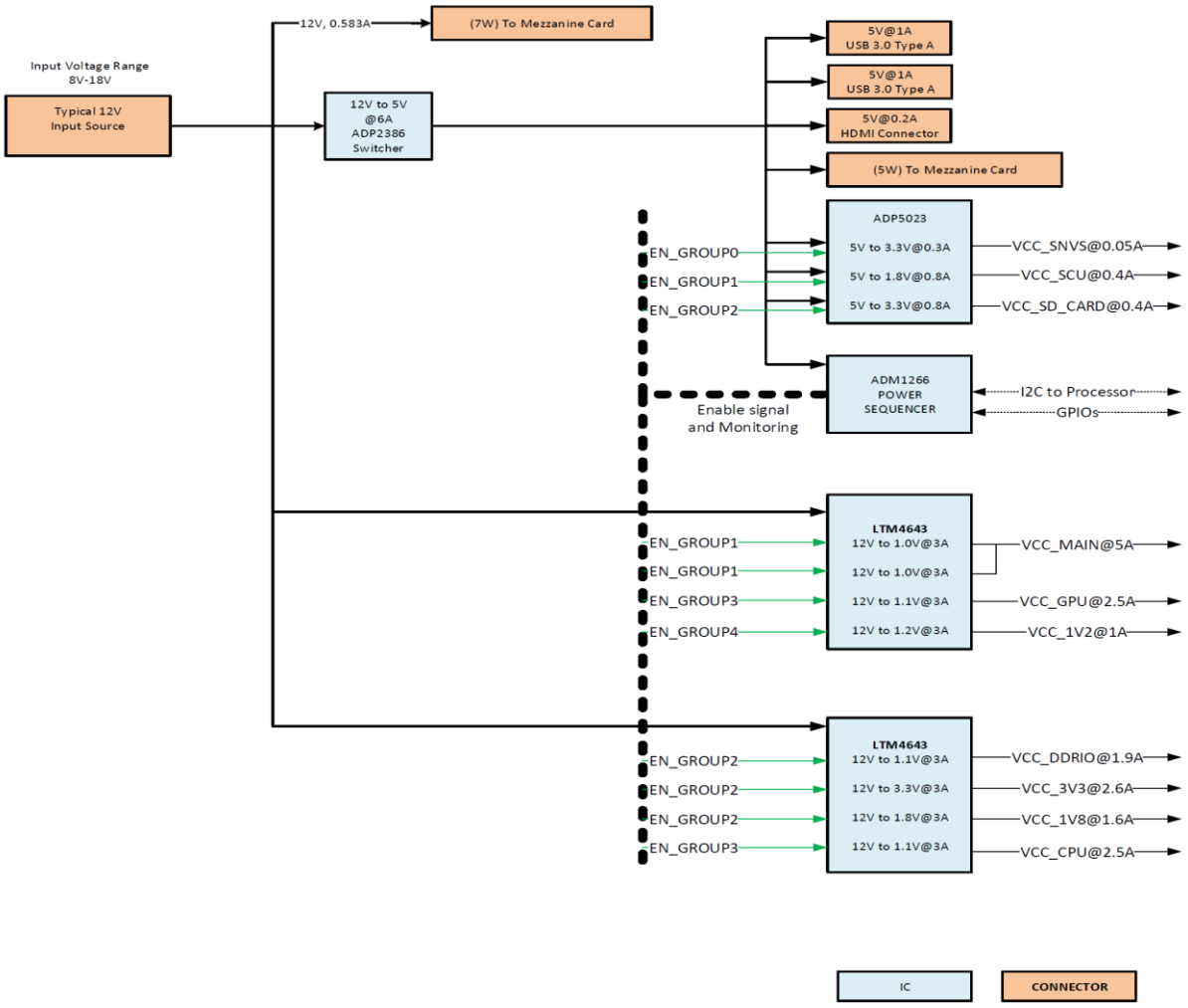


Figure 30: Finalized Power scheme

11.13.1 Input Power Supply

For protection of input power supply, below components are used

1. Fuse
2. TVS Diodes

For EMI EMC protection, below components are used

1. Common mode choke

For Input current sensing, below components are used

1. 0.01E Sense Resistor in series of input supply path
2. Two pins header across sense resistor

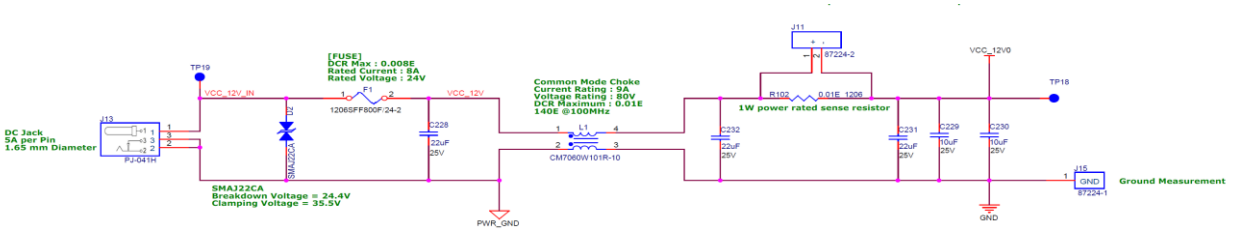


Figure 31: Input Power supply Design

11.13.2 12V to 5V@6A Regulator ADP2386ACPZN-R7

Regulator ADP2386ACPZN-R7 is selected to convert 5V from 8-18V input power supply.
This Regulator will be always in ON condition.
Regulator designed as per datasheet and get it reviewed by ADI for schematic and layout.

Design files received from ADI and added at below SVN location.
\13. Hardware Specific\Documents\Design Documents\Power Budgeting\Power Scheme Received from ADI
File Name: ADP2386_BuckDesigner_IMAX80_Revised_9am

Note: Discrete component selection for this regulator is as per the design files received from ADI.
Layout recommendation followed as per datasheet as per below image.

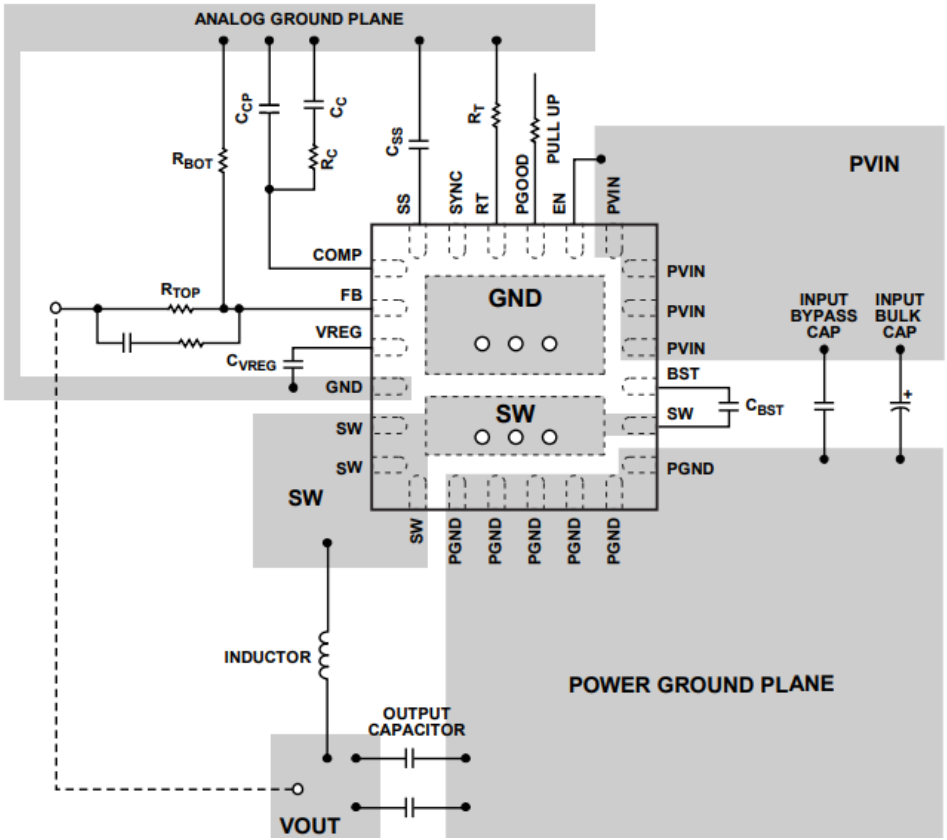


Figure 32: Layout Recommendation as per ADP2386 Regulator Datasheet

11.13.3 Regulator ADP5023ACPZ-R7

Regulator ADP5023ACPZ-R7 is selected to generate three LDO supply (low output current) for processor.
Regulator designed as per datasheet and get it reviewed by ADI for schematic and layout.
Enable of each power supply is provided by ADM1266 sequencer.

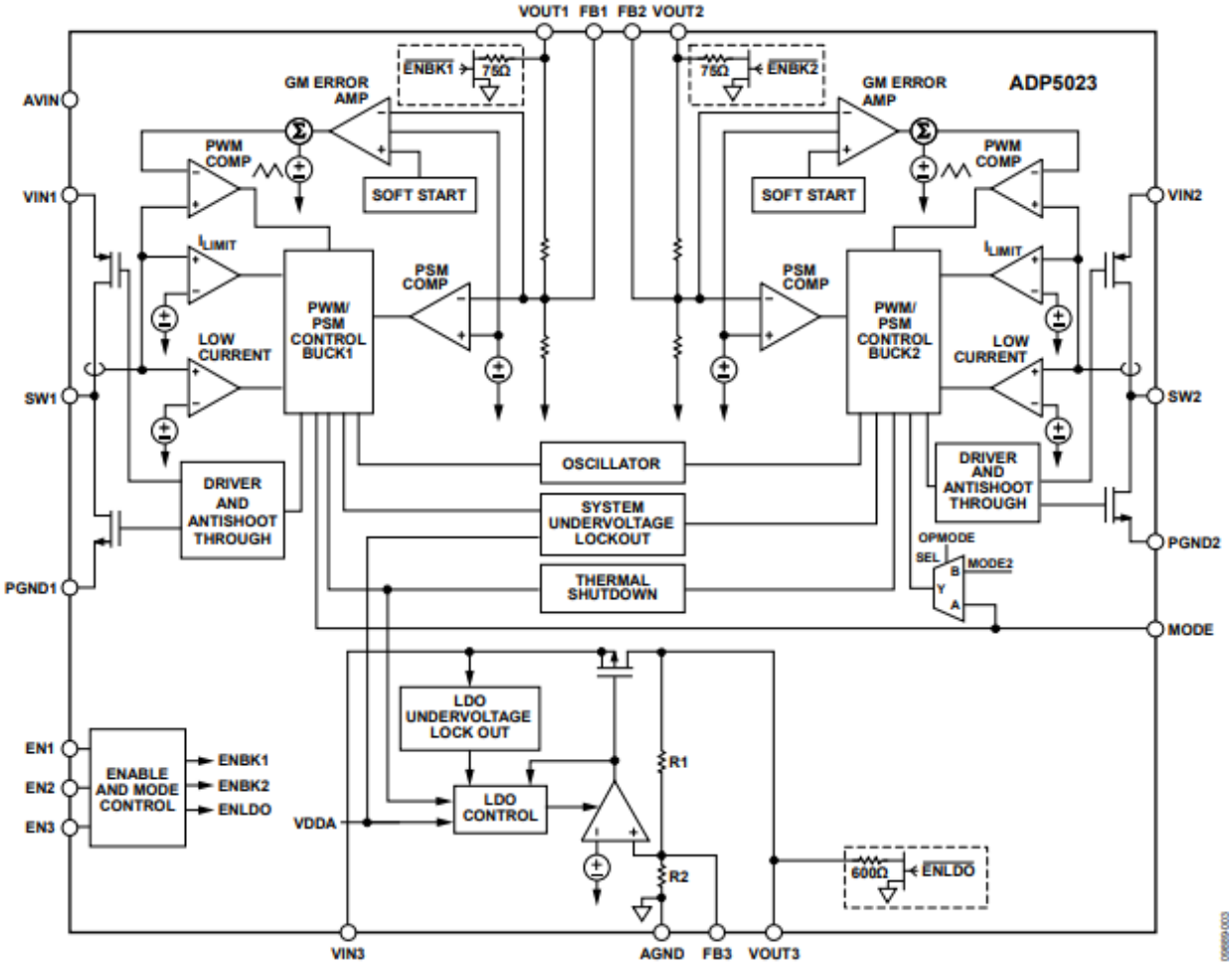


Figure 33: Internal Functional Block diagram of ADP5023

11.13.4 Two high power Regulators (LTM4643)

Two Regulators (LTM4643) are selected to generate high current supply for processor and other interfaces.
Enable of each power supply is provided by ADM1266 sequencer.

Regulator designed as per datasheet and get it reviewed by ADI for schematic and layout.

Note: LTM4643 is having inductor and discrete inside the module.

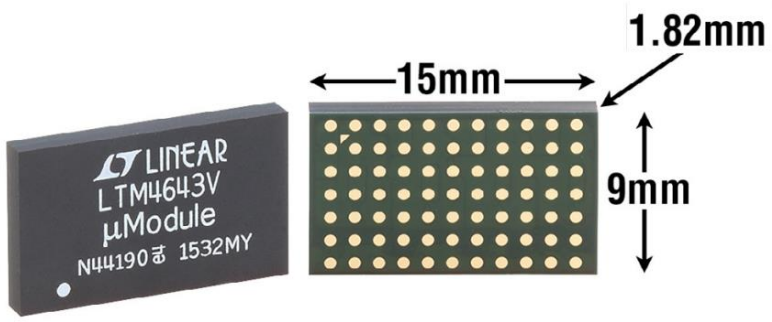


Figure 34: LTM4643 package overview

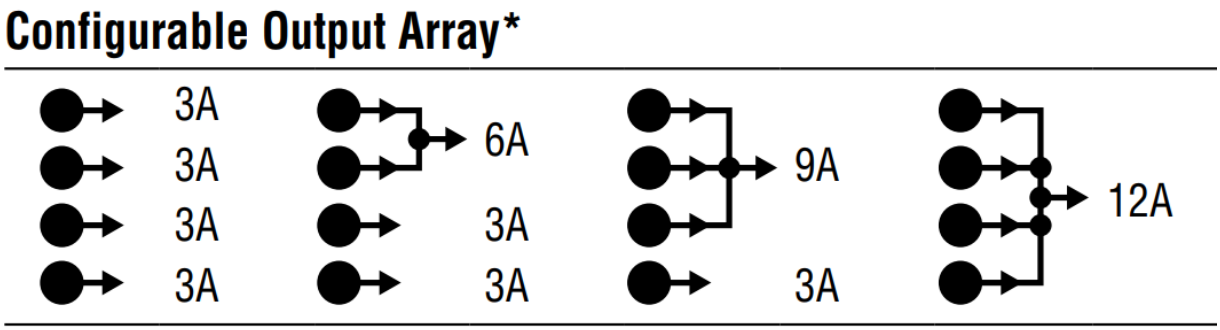


Figure 35: Configurable output as per requirement

11.13.5 Sequencer (ADM1266)

ADM1266 is used to provide power up and power down sequence to the processor.
ADM1266 will enable the other regulators as per sequence requirement.

Different product mode will be handled through GPIO between processor and AMD1266.
Sequencer designed as per datasheet and get it reviewed by ADI for schematic and layout.
I2C programmer and 3 pin header will be required on board to program ADM1266.
Generated supply will be monitored by ADM1266 by fault detector pins.

Below are the features of ADM1266

- 9 GPIOs
- 16 PDIOs
- 17 supply fault detectors enable real time supervision of supplies
- Fully programmable sequencing engine
- Industry standard PMBus interface compliant
- Available in a 9 mm × 9 mm, 64-lead package

Below is functional internal block diagram of ADM1266

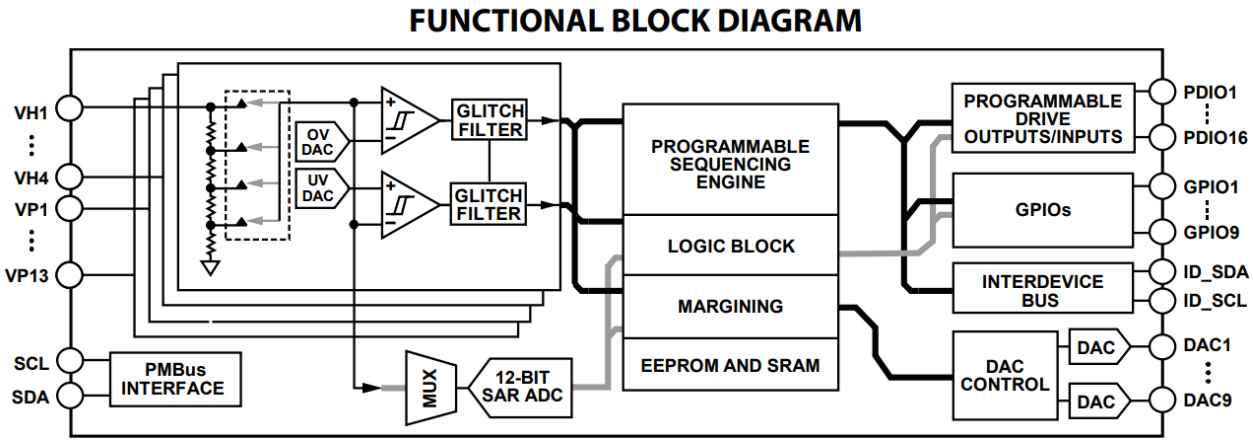


Figure 36: Internal functional block diagram of ADM1266

11.14 NOR Memory Interface

NOR memory provided on iMX8XML_RD as a secondary non-volatile memory.
It will be used for storing SW binaries, data, Android applications etc.

11.14.1 Interface Features

Processor iMX8 QUADX supports:

- Octal or Quad SPI interface

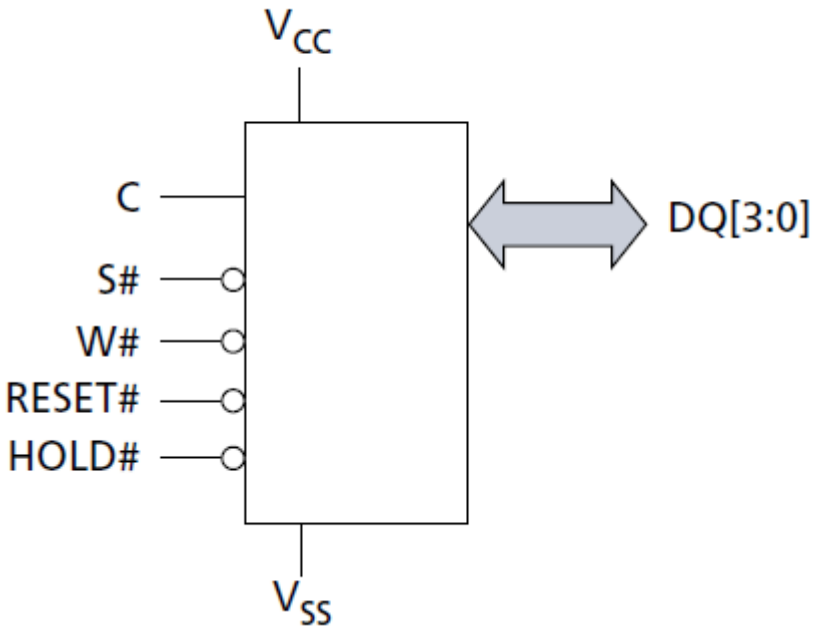


Figure 37 : NOR Memory Design

11.14.2 Interface Description

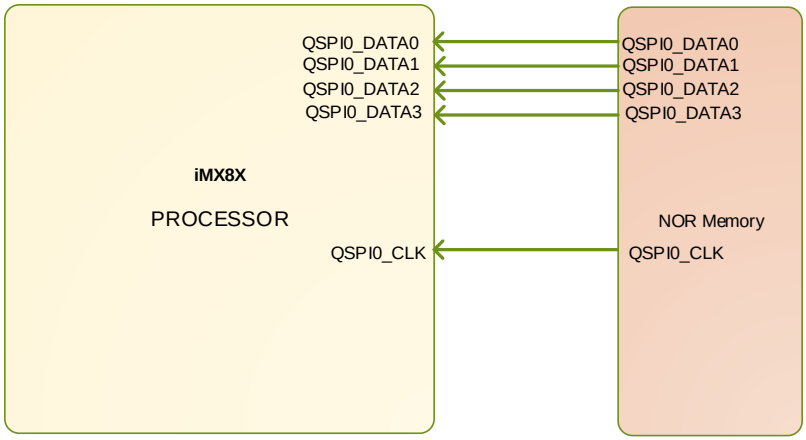


Figure 38 NOR Memory Interface Block Diagram

12 POWER SUPPLIES RAIL INFORMATION

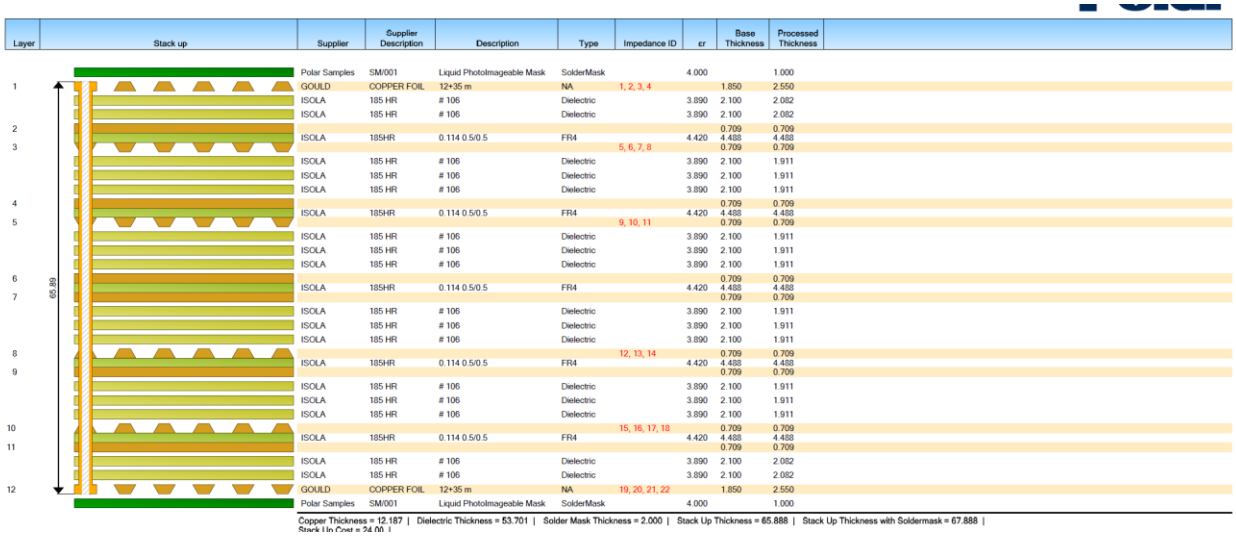
All the power supplies of Reference Design along with its current rating and voltage level are described in below table.

Sr#	Section Name	Net name	Max Current	Typical Voltage Range
1	Input power supply before common mode choke	VCC_12V_IN	5A	8V-18V
2	Input power supply after common mode choke	VCC_12V0	5A	8V-18V
3	12V to 5V	EXT_VCC_5V0	6A	5V
4	VCC_MAIN	VCC_MAIN	5A	1V
5	VCC_GPU	VCC_GPU	3A	1.1V
6	VCC_1V2	VCC_1V2	3A	1.2V
7	VCC_DDRIO	VCC_DDRIO	3A	1.1V
8	VCC_3V3	VCC_3V3	3A	3.3V
9	VCC_1V8	VCC_1V8	3A	1.8V
10	VCC_CPU	VCC_CPU	3A	1.1V
11	VCC_SNVS	VCC_SNVS	0.3A	3.3V
12	VCC_LDO_SD1	VCC_LDO_SD1	0.8A	3.3V
13	VCC_SCU_1V8	VCC_SCU_1V8	0.8A	1.8V
14	USB type A power	VUSB_1	1A	5V
15	USB type A power	VUSB_2	1A	5V
16	USB OTG power	USB_OTG1_VBUS	0.5A	5V
17	SIM supply	SIM_1V8	0.3A	1.8V
18	supply for debugging	DEBUG_VCC_5V0	0.5A	5V
19	Debug supply	DEBUG_VCC_3V3	0.2A	3.3V

13 PCB LAYER STACKUP

Below 12 Layer stack up considered for this design according to space, size and through hole via technology.

Adobe Acrobat Document



Layer	Stack up	Supplier	Supplier Description	Description	Type	Impedance ID	εr	Base Thickness	Processed Thickness
		Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask		4.000		1.000
1		GOULD	COPPER FOIL	12+35 m	NA	1, 2, 3, 4		1.850	2.550
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
2								0.709	0.709
3		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
						5, 6, 7, 8		0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
4								0.709	0.709
5		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
						9, 10, 11		0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
6								0.709	0.709
7		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
								0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
8						12, 13, 14		0.709	0.709
9		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
								0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	1.911
10						15, 16, 17, 18		0.709	0.709
11		ISOLA	185HR	0.114 0.5/0.5	FR4		4.420	4.488	4.488
								0.709	0.709
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
		ISOLA	185 HR	# 106	Dielectric		3.890	2.100	2.082
12		GOULD	COPPER FOIL	12+35 m	NA	19, 20, 21, 22		1.850	2.550
		Polar Samples	SM/001	Liquid PhotoImageable Mask	SolderMask		4.000		1.000

65.89

Copper Thickness = 12.187 | Dielectric Thickness = 53.701 | Solder Mask Thickness = 2.000 | Stack Up Thickness = 65.888 | Stack Up Thickness with Soldermask = 67.888 |

Figure 39: PCB Layer Stack up

14 MAJOR COMPONENTS - BILL OF MATERIAL

Sr #	Qty	Part Number	Manufacturer	Description
1	1	2201778-1	TE Connectivity AMP Connectors	MICRO SD PUSH PUSH LOW PROFILE T
2	2	2134536-2	TE Connectivity AMP Connectors	USB 2.0 Micro AB CONNECTOR
3	2	1932258-1	TE Connectivity	USB 3.0 RA REC TH TYPE A
4	1	2069486-2	TE Connectivity	HDMI REC SMT W/O FLANGE
5	1	1-2301994-0	TE Connectivity	CONN MAGJACK 1PORT 1000 BASE-T
6	1	5177983-2	TE Connectivity	CONN RECEPT 60POS .8MM DUAL SMD
7	1	9-1734516-0	TE Connectivity	CONN RECEPT 40POS 2MM STR DL SMD
8	1	20021111-00010T4LF	Amphenol FCI	CONN HEADER 10POS UNSHD VERT T/H
9	1	ADP2386ACPZN-R7	Analog Devices Inc.	IC REG BUCK ADJ 6A SYNC 24LFCSP
10	2	LTM4643	Analog Devices Inc.	Power Module
11	1	ADM1266	Analog Devices Inc.	Sequencer
12	1	ADP5023	Analog Devices Inc.	Buck Converter
13	1	CYUSB3304-68LTXI	Cypress	IC USB 3.0 HUB 4-PORT 88QFN
14	1	KSZ9031RNXCA	Microchip Technology	IC TXRX ETHERNET 48QFN
15	1	450-0169C	LSR (with inbuilt Cypress Chip)	Wi-Fi + BT Module
16	1	MT53B512M32D2NP-062 WT	Micron	IC DRAM 16G 1600MHZ FBGA
17	1	i.MX 8QUADX	NXP USA Inc.	I.MX 8QUADX
18	1	PJ-041H	CUI Inc.	CONN PWR JACK 1.75X4.75MM SOLDER
19	3	SPH0645LM4H-B	Knowles	DMIC with I2S interface MIC MEMS DIGITAL I2S OMNI -26DB
20	1	LSM6DS33TR	STMicroelectronics	Accelerometer + Gyroscope
21	1	IS25WP512M	ISSI	512Mb SERIAL FLASH MEMORY 133MHZ MULTI I/O SPI & QUAD I/O QPI DTR INTERFACE
22	1	M24128-DRMF3TG/K	ST Microelectronics	IC EEPROM 128K I2C 1MHZ 8MLP
23	1	IT6263	ITE Tech	LVDS to HDMI Conversion

Table 22: Major Components Bill of Material

Refer Detailed Bill of Material in the spreadsheet attached below section

eI_Arrow_iMX8XML_RD_BOM.xls

15 APPENDIX

15.1 APPENDIX A: Low Speed Expansion Connector Pinout

The signals listed in the below pinout table will be used for the Low Speed Expansion Connector, the pinouts meet the 96Boards specification and are finalized based on the available ports from the iMX 8X processor.

Pin No.	Signal	Voltage Level	Remark
1	GND		
2	GND		
3	UART0_CTS	1.8 V	
4	PWR_BTN_N	1.8 V	
5	UART0_TxD	1.8 V	
6	RST_BTN_N	1.8 V	
7	UART0_RxD	1.8 V	
8	SPI0_SCLK	1.8 V	
9	UART0_RTS	1.8 V	
10	SPI0_DIN	1.8 V	
11	UART1_TxD (Optional)	1.8 V	NC if Not Used
12	SPI0_CS	1.8 V	
13	UART1_RxD (Optional)	1.8 V	NC if Not Used
14	SPI0_DOUT	1.8 V	
15	I2C0_SCL	1.8 V	
16	PCM_FS	1.8 V	
17	I2C0_SDA	1.8 V	
18	PCM_CLK	1.8 V	
19	I2C1_SCL	1.8 V	
20	PCM_DO	1.8 V	
21	I2C1_SDA	1.8 V	
22	PCM_DI	1.8 V	
23	GPIO-A	1.8 V	Capable of waking up the SoC from sleep.
24	GPIO-B	1.8 V	
25	GPIO-C	1.8 V	
26	GPIO-D	1.8 V	
27	GPIO-E	1.8 V	
28	GPIO-F	1.8 V	DSI_BLCTL
29	GPIO-G	1.8 V	DSI_VSYNC
30	GPIO-H	1.8 V	DSI_RST
31	GPIO-I	1.8 V	CSI0_RST
32	GPIO-J	1.8 V	CSI0_PWDN
33	GPIO-K	1.8 V	CSI1_RST
34	GPIO-L	1.8 V	CSI1_PWDN

35	1V8		100 mA Max Current
36	SYS_DCIN		9-18V Input Power Supply
37	5V0		
38	SYS_DCIN		9-18V Input Power Supply
39	GND		
40	GND		

Table 23. Low Speed Expansion Connector Pinouts

15.2 APPENDIX B: High Speed Expansion Connector Pinout

The signals listed in the below pinout table will be used for the High Speed Expansion Connector, the pinouts meet the 96Boards specification and are finalized based on the available ports from the iMX 8X processor.

Pin#	Signal	Voltage Level	Remark
1	SPI1_DOUT	1.8 V	
2	CSI0_C+	1.2 V	
3	NC		NC as SDIO is not used
4	CSI0_C-	1.2 V	
5	NC		NC as SDIO is not used
6	GND		
7	SPI1_CS	1.8 V	
8	CSI0_D0+	1.2 V	
9	SPI1_SCLK	1.8 V	
10	CSI0_D0-	1.2 V	
11	SPI1_DIN	1.8 V	
12	GND		
13	GND		
14	CSI0_D1+	1.2 V	
15	CLK0/CSI0_MCLK	1.8 V	SoC Programmable CAM MCLK Clock 0
16	CSI0_D1-	1.2 V	
17	CLK1/CSI1_MCLK(Optional)	1.8 V	Optional if CSI1 is not available. NC or GPIO if not used.
18	GND		
19	GND		
20	CSI0_D2+	1.2 V	
21	DSI_CLK+	1.2 V	
22	CSI0_D2-	1.2 V	
23	DSI_CLK-	1.2 V	
24	GND		
25	GND		
26	CSI0_D3+	1.2 V	
27	DSI_D0+	1.2 V	
28	CSI0_D3-	1.2 V	
29	DSI_D0-	1.2 V	
30	GND		
31	GND		
32	I2C2_SCL		
33	DSI_D1+	1.2 V	
34	I2C2_SDA		

35	DSI_D1-	1.2 V	
36	I2C3_SCL(Optional)		Optional if CSI1 is not available. NC if not used.
37	GND		
38	I2C3_SDA(Optional)		Optional if CSI1 is not available. NC if not used.
39	DSI_D2+	1.2 V	
40	GND		
41	DSI_D2-	1.2 V	
42	CSI1_D0+(Optional)	1.2 V	NC if Not Used
43	GND		
44	CSI1_D0-(Optional)	1.2 V	NC if Not Used
45	DSI_D3+	1.2 V	
46	GND		
47	DSI_D3-	1.2 V	
48	CSI1_D1+(Optional)	1.2 V	NC if Not Used
49	GND		
50	CSI1_D1-(Optional)	1.2 V	NC if Not Used
51	USB_D+	USB	
52	GND		
53	USB_D-	USB	
54	CSI1_C+(Optional)	1.2 V	NC if Not Used
55	GND		
56	CSI1_C-(Optional)	1.2 V	NC if Not Used
57	HSIC_STR(Optional)		NC if Not Used
58	GND		
59	HSIC_DATA(Optional)		NC if Not Used
60	RESERVED		Not used, pulled up to 1.8V

Table 24. High Speed Expansion Connector Pinouts

15.3 APPENDIX C: Selection of Major Components

The critical parts identified in the architecture phase in agreement with customer is listed in below spreadsheet.

eI_Arrow_iMX8XML_
RD_Critical Parts Sele

Refer SVN for latest copy – Critical Parts List Not accessible to customer (Copy will be shared separately).

15.4 APPENDIX D: Tentative Placement as per 96Boards standard

The below image shows the board dimension with fixed placement locations of necessary connectors. The component placement and layout design of the board will meet the 96Boards Extended B criteria.

The detailed activity of placement strategy which includes all major components of the board will be carried out in document **eI_Arrow_iMX8XML_RD_PlacementDiagram.**

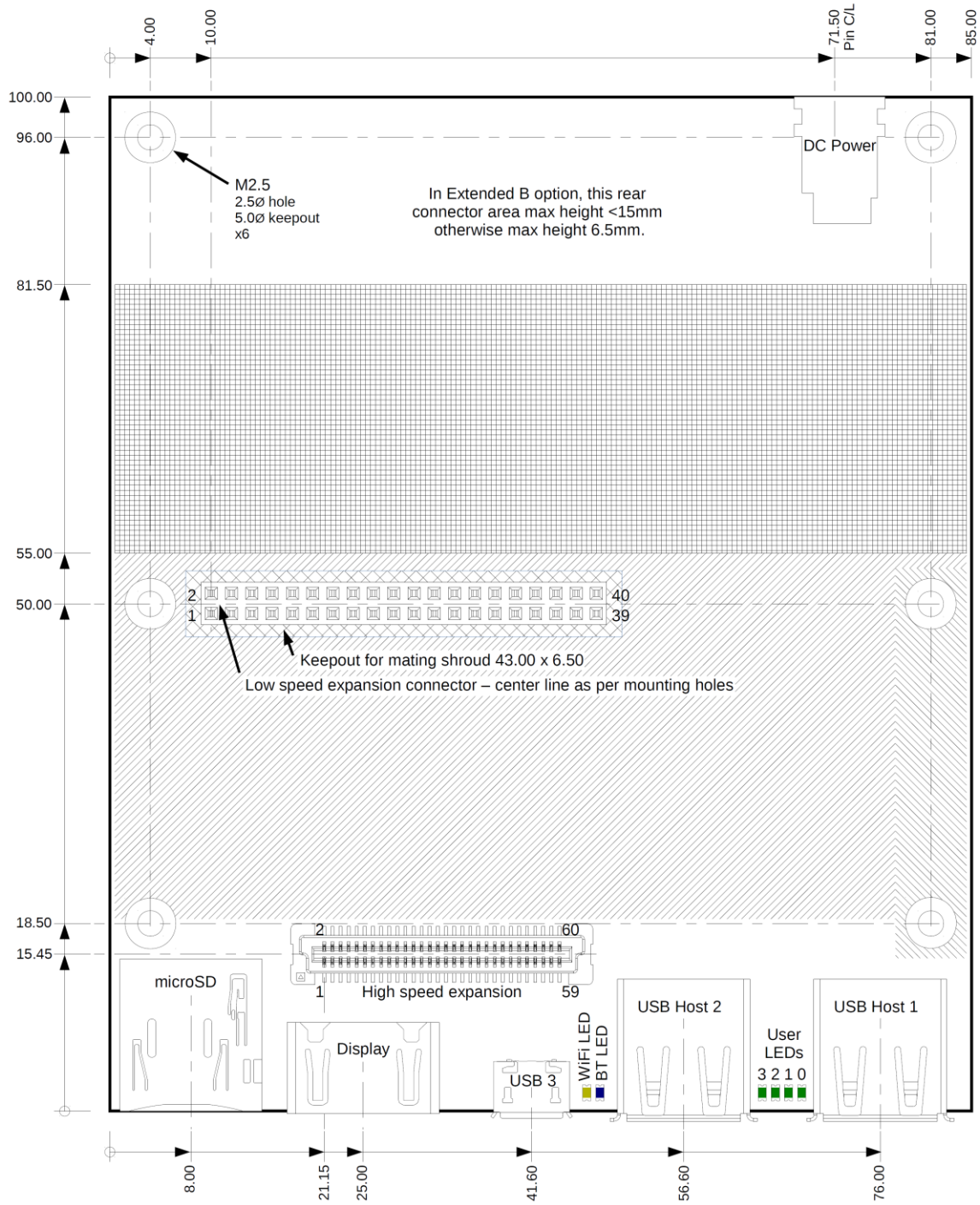


Figure 40 : 96Boards Extended B Dimensions

15.5 APPENDIX E: eI Proprietary Mezzanine Board – Block Diagram

The below block diagram show the peripherals on the eInfochips Proprietary Mezzanine Test board.

This board will be used to test the signals available on Low Speed and High Speed Expansion Connectors.

Since the eInfochips Mezzanine test board used SDIO interface and the iMX 8X ML Reference design shall use SPI interface on the same pins, the SPI interface of iMX 8X RD has to be validated by some other device/peripheral.

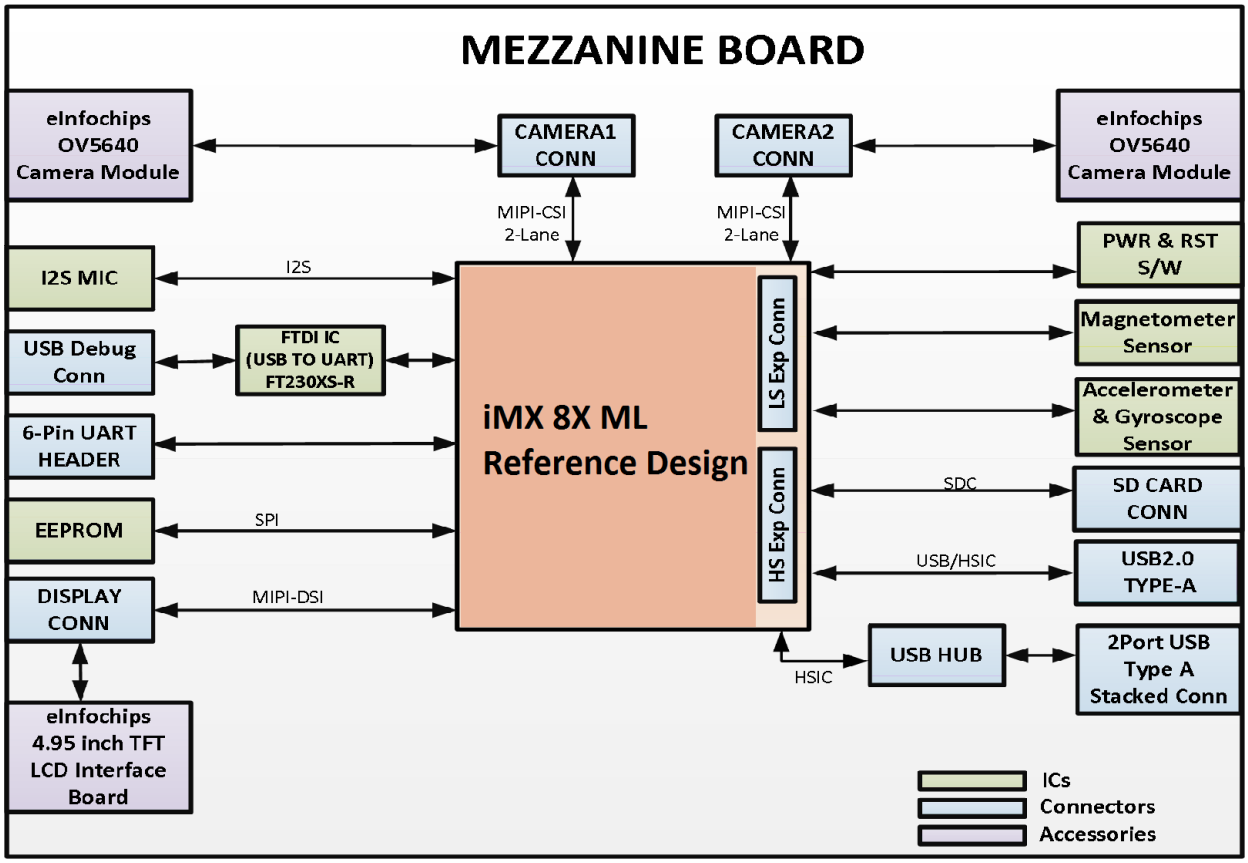


Figure 41 : EIC Mezzanine Board Block diagram

15.6 APPENDIX E: Length Match Report and Layout Guideline

Length match report generated from layout and added below

eI_Arrow_IMX8XML_RD_Lengthmatch_R

Layout guideline document added below

eI_Arrow_iMX8XML_RD_LayoutInstructic