High Precision, Impedance, and Electrochemical Front End

Preliminary Technical Data

AD5940

FEATURES

- Analog input
  - 800 kSPS, 16-bit precision ADC
  - Ultralow leakage, programmable switch matrix for custom sensor connections
  - High precision voltage, current, potentiostat, and impedance measurements
  - 6 external current measurement channels
  - Up to 24 voltage channels
  - Impedance measurement engine up to 200 kHz
  - ADC input path
    - Input buffers
    - Programmable TIA gain
    - Programmable gain amplifier with gain values of 1, 1.5, 2, 4, and 9
    - AAF
- Voltage DACs
  - Dual output voltage DAC with an output range of 0.2 V to 2.4 V (±2.2V voltage potential to sensor)
  - 12-bit V_{BIAS} output to bias Potentiostat amplifier
  - 6-bit V_{ZERO} output to bias TIA
  - Ultra low power:1 µA.
  - 1 high speed, 12-bit DAC
    - Output range: ±600 mV
    - Programmable gain amplifier on output with gain settings of 1 and 0.025
- Amplifiers, accelerators, and references
  - 1 low power, low noise Potentiostat amplifier suitable for Potentiostat bias in electrochemical sensing
  - 1 low power, low noise TIA suitable for measuring sensor current output
    - Programmable load and gain resistors for sensor output
  - Analog hardware accelerators
    - Digital waveform generator
    - Receive filters
    - Complex impedance measurement (DFT) engine
  - 1 high speed TIA to handle wide bandwidth input signals up to 200 kHz
  - Digital waveform generator for generation of sinusoid and trapezoid waveforms
  - 2.5 V and 1.82 V internal reference voltage sources
- System level power savings
  - Fast power-up and power-down analog blocks for duty cycling
  - Programmable AFE sequencer to minimize workload on host controller
  - 6 kB SRAM to preprogram AFE sequences
    - Ultra low power potentiostat channel: 6.5 µA when enabled
- Smart sensor synchronization and data collection
  - Cycle accurate control of sensor measurement
  - Sequencer controlled GPIOs
- On-chip peripherals
  - SPI serial input/output
  - Wake-up timer
  - Interrupt controller
- Power
  - 2.8 V to 3.6 V supply
  - 1.8 V input/output compliant
  - POR
  - Hibernate mode with LPDAC and potentiostat powered up to maintain sensor bias
- Package and temperature range
  - 3.6 mm × 4.2 mm, 56-ball WLCSP
  - Fully specified for –40°C to +85°C
- Applications
  - Electrochemical measurements
  - Potentiostat/amperometric/voltammetry/cyclic voltammetry
  - Bioimpedance applications
    - Skin impedance
    - Body impedance
  - Continuous glucose monitoring
  - Battery impedance

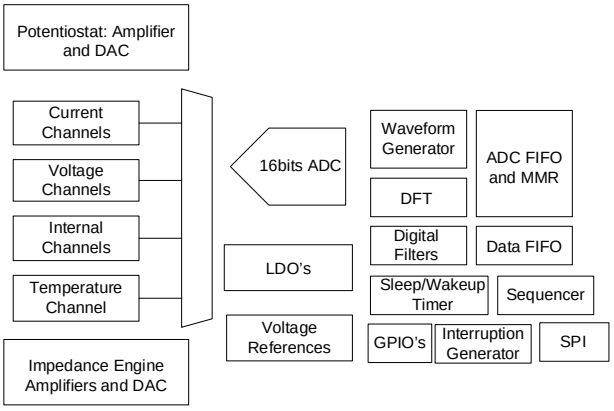

Figure 1: High Level Block Diagram

Rev. PrN Document Feedback

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FUNCTIONAL BLOCK DIAGRAM

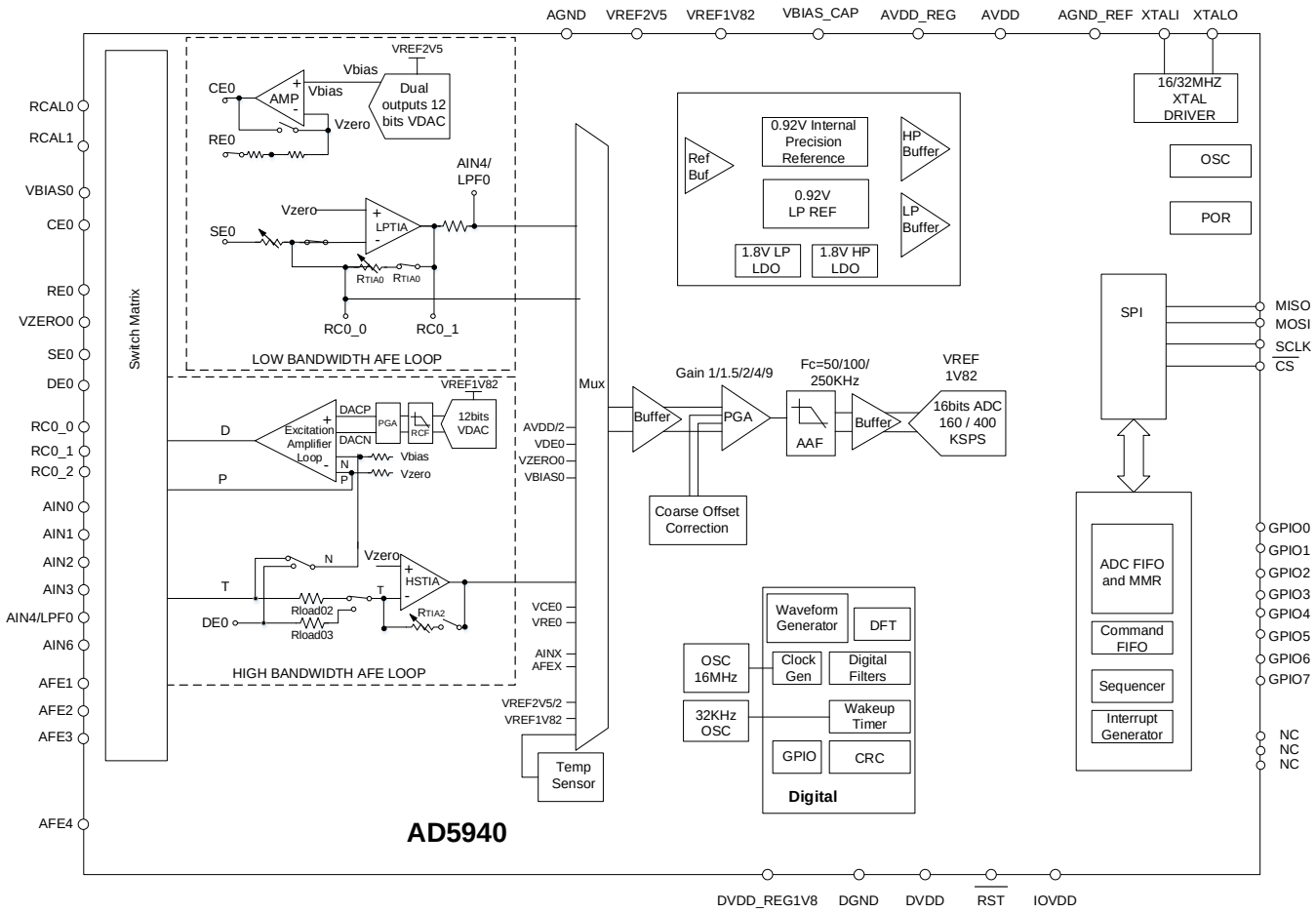

Figure 2.

GENERAL DESCRIPTION

The AD5940 is a high precision, low power analog front end (AFE) designed for portable applications requiring high precision, electrochemical-based measurement techniques, such as amperometric, voltametric, or impedance measurements. The AD5940 is designed for skin impedance and body impedance measurements, and is also designed to work with the AD8233 AFE in a complete bioelectric/biopotential measurement system.

The AD5940 consists of two high precision excitation loops and one common measurement channel, which enables a wide capability of measurements of the sensor under test. The first excitation loop consists of an ultra low power, dual output string digital-to-analog converter (DAC), and a low power, low noise potentiostat amplifier. One output of the DAC controls the noninverting input of the potentiostat amplifier, and the other output controls the noninverting input of the trans-impedance amplifier (TIA). This low power excitation loop is capable of generating signals from dc to 200 Hz.

The second excitation loop consists of a 12-bit DAC, referred to as the high speed DAC. This DAC is capable of generating high frequencies excitation signals up to 200 kHz.

The AD5940 measurement channel features a 16-bit, 800 kSPS, multichannel successive approximation register (SAR) analog-to-digital converter (ADC) with input buffers, a built in antialias filter (AAF), and a programmable gain amplifier (PGA). The ADC features an input voltage range of ±1.35 V. An input mux before the ADC allows the user to select an input channel for measurement. These input channels include multiple external current inputs, multiple external voltage inputs, and internal voltage channels. The internal channels allow diagnostic measurements of the internal supply voltages, die temperature, and reference voltages.

The current inputs include two TIAs with programmable gain and load resistors for measuring different sensor types. The first TIA, referred to as LPTIA, is designed to measure low bandwidth signals. The second TIA, referred to as the high speed TIA, is designed to measure high bandwidth signals up to 200 kHz.

An ultralow leakage, low RON programmable switch matrix connects the sensor to the internal analog excitation and measurement blocks. This matrix provides an interface for connecting external TIA gain resistors and calibration resistors. The matrix can also be used to multiplex multiple electronic measurement devices to the same measurement electrodes.

A precision 1.82 V and 2.5 V on-chip reference source is available. The internal ADC and DAC circuits use this on-chip reference source to ensure low drift performance for these peripherals.

The AD5940 measurement blocks can be controlled via direct register writes through the SPI (Serial Peripheral Interface) interface, or, alternatively, by using a preprogrammable sequencer, which provides autonomous control of the AFE chip. 6 kB of static random access memory (SRAM) is partitioned for a deep data first in, first out (FIFO) and command memory. Measurement commands are stored in the command memory and measurement results are stored in the data FIFO. A number of FIFO related interrupts are available to indicate state of the FIFO i.e. FIFO full, FIFO overflow.

8 general-purpose inputs/outputs (GPIOs) are available and can be controlled using the AFE sequencer, which allows cycle accurate control of multiple external sensor devices.

The AD5940 operates from a 2.8 V to 3.6 V supply and is specified over a temperature range of −40°C to +85°C. The AD5940 is packaged in a 56-lead, 3.6 mm × 4.2 mm WLCSP package.

SPECIFICATIONS

AVDD = DVDD = 2.8 V to 3.6 V. The maximum difference between supplies = 0.3 V. IOVDD = 1.8 V ± 10% and 2.8 V to 3.6 V. The ADC reference, excitation, and DAC and amplifier = 1.82 V, internal reference. Low power VBIAS and VZERO DAC reference = 2.5 V, internal reference. T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
BASIC ADC SPECIFICATIONS						Pseudo differential mode measured relative to ADC VBIAS, unless otherwise noted; specifications based on high speed mode, unless otherwise noted; ADC voltage channel calibrated in production with PGA gain = 1.5; AFE die ACLK = 32 MHz or 16 MHz, unless otherwise stated
Data Rate[1]	f_{SAMPLE}			400	kSPS	High speed mode; decimation factor = 4
				200	kSPS	Normal mode; decimation factor = 4
Resolution		16			Bits	Number of data bits
Integral Nonlinearity[1]	INL					
Normal Mode		−4	±2.0	+4	LSB	PGA Gain = 1.5, 1.82 V internal reference 1 LSB = 1.82 V/2^{15}
Normal Mode		−5.6	±2.0	+4.7	LSB	PGA Gain = 9, 1.82 V internal reference
Differential Nonlinearity[1]	DNL					
Normal Mode		−0.99	±0.9	+2.5	LSB	1.82 V internal reference; 1 LSB = 1.82 V/2^{15}; no missing codes
DC Code Distribution[2]			±6		LSB	PGA gain = 1.5×, low power mode, ADC input = 0.9 V; ADC output data rate = 200kSPS 1 LSB = 1.82 V/2^{15}
			±6		LSB	Input channel is LP TIA 0 = 1 µA, R_{TIA} = 512 kΩ, R_{LOAD} = 10 Ω ADC output data rate = 200kSPS
			±6		LSB	Input channel is HP TIA = 1 µA, RTIA = 10 K Ω, RLOAD = 100 Ω ADC output data rate = 200kSPS
ADC Endpoint Errors						
Offset Error		−600	±200	+600	µV	PGA gain = 1.5, LP Mode, All channels except AIN3
		-620	±200	880	µV	PGA gain = 1.5, LP Mode, AIN3 only
HP Mode[3]		-1.1	±0.5	1.4	mV	PGA gain = 1.5, HP Mode
Drift[1]			±3		µV/°C	Using 1.82 V internal reference
Offset Matching			±1		LSB	Matching compared to AIN3
Full-Scale Error		-1000	±400	800	µV	Excluding internal channels; both negative and positive full scale; error at both endpoints
HP Mode[3]		-2.2	±0.9	1.82	mV	PGA gain = 1.5x, HP Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
			0.1	0.75	% of Full Scale	AVDD/2, DVDD/2, ADCVBIAS, VREF_2.5 V, VREF_1.8 V, AVDD_REG
Gain Drift[1]		−3	±1	+3	µV/°C	Full-scale error drift minus offset error drift
Gain Error Matching			± 1.5		LSB	Mismatch from channel to channel
PGA Mismatch Error[1]						ADC offset and gain calibration with a gain value of 1.5
PGA Gain = 1 to 1.5		−0.2	+0.1	+0.3	%	
PGA Gain of 1.5 to Gain of 2		−0.2	+0.1	+0.3	%	
PGA Gain = 2 to 4		−0.3	+0.2	+0.8	%	
PGA Gain = 4 to 9		−0.35	+0.2	+0.95	%	
ADC DYNAMIC PERFORMANCE						f_{IN} = 20 kHz sine wave, f_{SAMPLE} = 200 kSPS; using AINx voltage input channels; PGA gain = 1.5×
Signal-to-Noise Ratio	SNR					Includes distortion and noise components
			80		dB	PGA Gain = 1, 1.5, and 2
			76		dB	PGA Gain = 4
			70		dB	PGA Gain = 9
Total Harmonic Distortion[1]	THD		−84		dB	
Peak Harmonic or Spurious Noise[1]			−86		dB	
Channel to Channel Crosstalk[1]			−86		dB	Measured on adjacent channels
Noise (RMS)[4]		See **Table 2**			µV (rms)	
ADC INPUT						Input to ADC mux
Input Voltage Ranges[1]		0.2		2.1	V	Voltage applied to any input pin
					V	Pseudo differential voltage between ADC VBIAS and analog input from ADC mux
		−0.9		0.9	V	Gain = 1
		−0.9		0.9	V	Gain = 1.5
		−0.6		0.6	V	Gain = 2
		−0.3		0.3	V	Gain = 4
		−0.133		0.133	V	Gain = 9
Common Mode Range[1]		0.2	1.11	2.1	V	
Leakage Current		−1.5	±0.5	+1.5	nA	AIN0, AIN1, AIN2, AIN3, AIN4, AIN6, SE0, DE0
Input Current[1]		−8	±2	+8	nA	AIN0, AIN1, AIN2, AIN3, AIN4, AIN6, SE0, DE0
Input Capacitance			40		pF	During ADC acquisition
AAF 3 dB Frequency Range						3 programmable settings
Mode 0			50		kHz	
Mode 1			100		kHz	
Mode 2			250		kHz	
ADC Channel Switch Settling Time						Time delay required after switching ADC input channel; excludes sinc3 settling time
AAF −3 dB Cutoff Frequency						
250 kHz[1]		20			µs	
100 kHz[1]		40			µs	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
50 kHz[1]		50			µs	
Sinc3 Bypassed		20			µs	800 kSPS ADC output rate
DISCRETE FOURIER TRANSFORM (DFT)-BASED IMPEDANCE MEASUREMENTS						
With High Bandwidth Loop						For Z of 1K Ω (0.02% tolerant resistor), excitation frequency = 0.1Hz to 200 kHz, sine amplitude = 10 mV rms, RTIA = 5 kΩ; R_{CAL} = 200 Ω;1% accurate tempco 5 ppm/°C Single DFT measurement; DFT using 8192 ADC samples; Hanning on; DACCON [8:1] = 0x1B for LP mode and impedance measurements ≤80 kHz; DACCON [8:1] = 0x7 for HP mode and impedance measurements > 80 kHz
Accuracy						
Magnitude		-1.25	±0.2	1.23	%	20kHz to 200kHz
Phase		-0.3	±0.1	0.3	Degrees	
Magnitude			±0.2		%	10Hz to 20kHz
Magnitude			±1		%	1 Hz to <10Hz
Three-Resistor star cell						Z=2.2 Ω connected as per Figure 3
Accuracy						0.1Hz to 200kHz
Magnitude			±0.5		%	
Phase			±0.5		Degrees	
With High Bandwidth Loop, 50 kHz, 4-Wire Isolated						For Z = 1 kΩ (0.1% tolerant resistor); excitation frequency = 50 kHz, sine amplitude = 0.6 V p-p, R_{TIA} = 1 kΩ, C_{TIA} = 32 pF, C_{ISO1} = 15 nF, C_{ISO2} = C_{ISO3} = C_{ISO4} = 470nF R_{LIMIT} = 1 kΩ;
Accuracy						Device to device repeatability for 3 devices at 50kHz.
Magnitude			TBD		%	Standard deviation as a percentage of Z
Phase			TBD		Degrees	Standard deviation of Z
With Low Bandwidth Loop						For Z = 100kΩ. Excitation frequency = 100 Hz, sine amplitude = 1.1 V p-p, R_{TIA} = 100 kΩ, C_{TIA} = 100 nF, C_{ISO1} = 15 nF, C_{ISO2} = 470 nF R_{LIMIT} = 1k;
Frequency Range		1		300	Hz	
Accuracy						Device to device repeatability for 3 devices at 100 Hz.
Magnitude			±0.3		%	Percentage Error
Phase			TBD		Degrees	Standard deviation of Z
Precision						
Magnitude			TBD		%	Standard deviation as a percentage of Z
Phase			TBD		Degrees	Standard deviation of Z
High Speed Loop						See Figure 3. Valid for Impedance Spectroscopy, Voltammetry and pulse tests.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Allowed External Load Capacitance[1]				100	pF	R2+R3 <=100Ω. R1<=100Ω
				50	pF	R2+R3 <=500Ω. R1<=100Ω
Excitation Amplifier Bandwidth			3		MHz	
LOW POWER TIA AND POTENTIOSTAT AMPLIFIER						
Input Bias Current			80	200	pA	TIA amplifier, SE0 pin
			20	150	pA	Potentiostat amplifier
Offset Voltage			50	150	µV	
Offset Voltage Drift vs. Temperature			1		µV/°C	
Noise						Unity gain mode; pk-pk voltage in 0.1 Hz to 10 Hz range
			1.6		µV	Normal mode (LPTIACON0 [2] = 0b)
			2		µV	Half power mode (LPTIACON0 [2] = 1b)
Potentiostat Source/Sink Current[1]		−750		+750	µA	Normal mode (LPTIACON0, Bits[4:3] = 00b) ; from CE0
		−3		+3	mA	High current mode (LPTIACON0, Bits[4:3] = 01/11b) ; from CE0
DC Power Supply Rejection Ratio			70		dB	At RE0 pin; RTIA = 256 KΩ, RLOAD = 10 Ω
Input Common-Mode Range		300		AVDD – 600	mV	
Output Voltage Range[1]		300		AVDD – 400	mV	Normal mode (LPTIACON0 [4 :3] = 00b), sink/source = 750 µA
		300		AVDD – 400	mV	High current mode (LPTIACON0, Bits[4:3] = 01/11b), sink/ source = 3 mA
Overcurrent Limit Protection			17		mA	Amplifiers will try to limit source/sink current to this value via internal clamp
Allowed Duration of Overcurrent Limit[1]				5	sec	User must limit duration of overcurrent condition to less than this or risk damaging amplifier
Allowed Frequency of Overcurrent Conditions				1	Per hour	
PROGRAMMABLE RESISTORS						
LPTIA Load Resistor on SE0 Input						
0 Ω R_{LOAD} Accuracy		0.01	0.08	0.15	Ω	
10 Ω R_{LOAD} Accuracy		9.8	11.7	13.5	Ω	
30 Ω R_{LOAD} Accuracy		28	33.8	39	Ω	
50 Ω R_{LOAD} Accuracy		48	55	63	Ω	
100 Ω R_{LOAD} Accuracy		88	110	130	Ω	
Drift over Temperature			±200		ppm/°C	10 Ω, 30 Ω, 100 Ω, 1500 Ω, 3000 Ω, and 3500 Ω
			±400		ppm/°C	50 Ω
0 Ω R_{LOAD} Accuracy		0.03	0.08	0.15	Ω	
LPTIA Gain Resistor on SE0 Input[1]						
Accuracy		−5		+15	%	User programmable; includes 1 kΩ, 2 kΩ, 3 kΩ, 4 kΩ, 6 kΩ, 8

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
						kΩ, 10 kΩ, 16 kΩ, 20 kΩ, 22 kΩ, 30 kΩ, 40 kΩ, 64 kΩ, 100 kΩ, 128 kΩ, 160 kΩ, 192 kΩ, 256 kΩ, and 512 kΩ
		115	120	130	Ω	200 Ω setting with R_{LOAD}=100 Ω
Drift over Temperature			±100		ppm/°C	
LPTIA RTIA Mismatch Error[1]						Error when moving up or down one RTIA value
		−0.6	+0.2	+0.6	%	512 KΩ to 2 KΩ range excluding 40 KΩ
		−3.5	+0.5	+3.5	%	40 KΩ (up to 48 KΩ, down to 32 KΩ)
			±20		%	200 Ω
High Speed TIA Gain Resistor on SE0						
Accuracy			20		%	User programmable; includes 100 Ω, 200 Ω, 1 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 40 kΩ, 80 kΩ, and 160 kΩ
Drift			±200		ppm/°C	
High Speed TIA Load Resistor on SE0 Input						User programmable; includes 10 Ω, 30 Ω, 50 Ω, and 100 Ω
Accuracy		102	110	116	Ω	Fixed 100 Ω target setting
Drift			±160		ppm/°C	
High Speed TIA Gain Resistor DE0 Inputs[1]						User programmable; includes 0.1 kΩ, 0.2 kΩ, 1.5 kΩ, 10 kΩ, 20 kΩ, 40 kΩ, 80 kΩ, and 160 kΩ
Accuracy		120	135	150	Ω	100 Ω setting
Accuracy		230	250	280	Ω	200 Ω setting
Accuracy			±20		%	1 KΩ, 5 KΩ, 10 KΩ, 20 KΩ, 40 KΩ, 80 KΩ, 160 KΩ
Drift over Temperature			±350		ppm/°C	100 Ω and 200 Ω settings
			±200		ppm/°C	1 kΩ, 5 kΩ, 10 kΩ, 20 kΩ, 40 kΩ, 80 kΩ, and 160 kΩ
High Speed TIA Gain Resistor Mismatch Error DE0[1]						Error introduced when moving up or down one RTIA value
		−3.5	+1	+3.5	%	160 KΩ to 5 KΩ range
		−25	±2	+5	%	1 KΩ, 200 Ω, and 100 Ω
High Speed TIA Load Resistor DE0 Inputs[1]						DE0RLOAD
Accuracy		0.001		0.15	Ω	0 Ω setting
		5		11	Ω	10 Ω setting
		26.5	32.6	37.6	Ω	30 Ω setting
			±15	25	%	50 Ω, and 100 Ω settings
Drift over Temperature			±0.2		%/°C	10 Ω setting
			±200		ppm/°C	Excludes R_{LOAD} = 0 Ω and 10 Ω
HIGH SPEED Trans-Impedance Amplifier						
Bias Current			1		nA	
Maximum Current Sink/Source[1]		−3		+3	mA	Ensure R_{TIA} selection generates an output voltage

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
						of < ±900 mV with PGA gain = 1
Input Common-Mode Range[1]		300		AVDD – 700	mV	
Output Voltage Range[1]		200		AVDD - 400	mV	
Overcurrent Limit Protection[1]			17		mA	Amplifier attempts to limit the source/sink current to this value via the internal clamp; tested with R_{LOAD} = 0 Ω and R_{TIA} = 100 Ω
Allowed Duration of Overcurrent Limit[1]				5	s	
Allowed Frequency of Overcurrent Conditions				1	Per hour	
LOW POWER, ON-CHIP VOLTAGE REFERENCE			2.5		V	0.47 µF from VREF_2V5 to AGND; reference is measured with low power VDAC (This just means voltage DAC, right? - Correct) and output amplifier enabled
Accuracy				±5	mV	T_A = 25°C
Noise[1]			60		µV p-p	
Reference Temperature Coefficient[1]		–25	±11	+25	ppm/°C	
DC Power Supply Rejection Ratio	PSRR		70		dB	
AC Power Supply Rejection Ratio[5]	PSRR		48		dB	Ac 1 kHz, 50 mV pk-pk ripple applied to AVDD supply
HIGH POWER, ON-CHIP VOLTAGE REFERENCE			1.82		V	0.47 µF from VREF_1.82 V to AGND; reference is measured with ADC enabled
Accuracy				±5	mV	T_A = 25 °C
Reference Temperature Coefficient[1]		–20	±5	+20	ppm/°C	
DC Power Supply Rejection Ratio	PSRR		85		dB	DC; variation due to AVDD supply changes
AC Power Supply Rejection Ratio[6]	PSRR		52		dB	AC; 1 kHz, 50 mV p-p ripple applied to AVDD supply
ADC Common-Mode Reference Source			1.11		V	470 nF from ADCVBIAS_CAP (Does this mean the voltage bias capacitor on the ADC, or something else? Bias capacitor on ADC) to AGND; reference is measured with ADC enabled
Accuracy				±5	mV	T_A = 25°C
Reference Temperature Coefficient[1]		–20		+20	ppm/°C	
DC Power Supply Rejection Ratio	PSRR		80		dB	DC variation due to AVDD supply changes
AC Power Supply Rejection Ratio	PSRR		50		dB	AC 1 kHz, 50 mV pk-pk ripple applied to AVDD supply
LOW POWER, DUAL OUTPUT DAC (V_{BIAS} AND V_{ZERO})						VBIAS specifications derived from measurements taken with potentiostat amplifier in unity gain mode and measured at CE0; VZERO specifications derived from measurements at VZERO0; dual output low power DAC
Resolution[1]						Number of data bits

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
12-Bit Mode		12			Bits	
6-Bit Mode		6			Bits	
Relative Accuracy[1,9]	INL					
12-Bit Mode		-3.5	±1	3	LSB	1 LSB = 2.2 V/(2^{12} − 1)
6-Bit Mode		-3.5	±0.1	2	LSB	1 LSB = 2.2 V/2^6
Differential Nonlinearity[1,9]	DNL					
12-Bit Mode		−0.99		+2.5	LSB	Guaranteed monotonic, 1 LSB = 2.2 V/(2^{12} − 1)
6-Bit Mode		−0.5		+0.5	LSB	Guaranteed monotonic, 1 LSB = 2.2 V/2^6
Offset Error[1]		−7	±3.9	+7	mV	V_{BIAS0}/V_{ZERO0} in 12-bit mode; 2.5 V internal reference, DAC output code = 0x000; Target 0x000 code = 200 mV
		−2	±0.2	+2.6	mV	Differential offset voltage of VBIAS referred to VZERO
Drift			±5		µV/°C	V_{BIAS0} or V_{ZERO0} referred to AGND
Differential Offset VBIAS to VZERO ≈ 0 V[1]				4	µV/°C	Differential offset voltage of VBIAS referred to VZERO, −40°C to +60°C range; LPDACDAT0 = 0x1A680
Differential offset VBIAS to VZERO ≈ ±600 mV[1]				10	µV/°C	Differential offset voltage of VBIAS referred to VZERO, −40°C to +60°C range; LPDACDAT0 = 0x1AAE0
Gain Error[1]			±0.2	±0.5	%	12-bit mode, DAC code = 0xFFF with target voltage of 2.4 V
Drift			10		ppm/°C	Using internal low power reference
Analog Outputs						
Output Voltage Range[1]						LSB size = 2.2/(2^{12} − 1); the input common-mode voltage of the low power potentiostat and LPTIA = AVDD − 600 mV
12-Bit Outputs		0.2		2.4	V	AVDD ≥ 2.8 V
6-Bit Outputs						LSB size is 2.2/2^6; the input common-mode voltage of the low power potentiostat and LPTIA = AVDD − 600 mV
		0.2		2.366	V	AVDD ≥ 2.8 V
		0.2		2.3	V	AVDD < 2.8V
AVDD to VBIAS/VZERO Headroom Voltage[1]		400			mV	A minimum headroom between AVDD and VBIAS/VZERO output voltage, increases to 600 mV if connected to LPTIA or LP potentiostat amplifiers
Output Impedance[1]			1.65		MΩ	
DAC AC Characteristics						
Output Settling Time			1.5		s	Settled to ±2 LSB_{12} with 0.1 µF load for ¼ of full scale to ¾ of full scale
Output Settling Time			500		µs	Settled to ±2 LSB_{12}; no load
Glitch Energy			±5		nV/sec	1 LSB change when the maximum number of bits changes simultaneously in the LPDACDAT0 register.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
						Switch to external caps on V_{BIAS0}/V_{ZERO0} opened. No caps on CE0/RC0_x pins.
EXCITATION DAC/PGA/ RECONSTRUCTION FILTER (RCF)						Use HSDACDAT range 0x200 to 0xE00. Specified for gain = 2, (HSDACCON[12] & [0] = 0) and Gain =0.05, (HSDACCON[12] & [0] = 1)
DAC						
Common mode voltage range[1]		0.2		AVDD-0.6	V	Set by excitation amplifiers N-node
Resolution[1]		12			Bits	1 LSB = 293 µV × programmable gain
Differential Nonlinearity	DNL	−0.99		+1.25	LSB	Gain = 2
	DNL		±7	±20	LSB	G = 0.05
Relative Accuracy[1]	INL		±2	±3	LSB	Gain = 2
			±8	±20	LSD	Gain = 0.05
Full-Scale Error[7]						
Positive		595	607	620	mV	Gain = 2, DAC code = 0xE00
		14	15.1	16	mV	Gain = 0.05, DAC code = 0xE00
Negative		-620	-607	-595	mV	Gain = 2, DAC code = 0x200
		-16	-15.1	-14	mV	Gain = 0.05, DAC code = 0x200
Gain error drift						
G=1			11.5		µV /°C	
G=0.05			0.33		µV/°C	
Offset Error (Midscale)						Measured at an output of the excitation loop across RCAL. DAC Code = 0x800
			±1	±5	mV	G=2
			±0.2	±0.9	mV	G=0.05
Offset error drift						
G=2			TBD		µV/°C	
G=0.05			5		µV/°C	
DC Power Supply Rejection Ratio	PSRR		70		dB	DC variation due to AVDD supply changes
PGA, Programmable Gain		0.05		2		
RCF						
3 dB Corner Frequency Accuracy			+/-5		%	Programmable to 50 kHz, 100 kHz, and 250 kHz
Allowed External Load Capacitance						SE0, DE0, AINx, and RCALx pins
<80 kHz (Low Power Mode)				30	pF	
>80 kHz (High Power Mode)				30	pF	
Overcurrent Limit Protection[1]			5		mA	Amplifier attempts to limit the source/sink current to this value via the internal clamp
Allowed Duration of Overcurrent Limit[1]				5	s	
Allowed Frequency of Overcurrent Conditions[1]				1	Per hour	
SWITCH MATRIX						Switches on analog front end before ADC mux

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
On Resistance[1]	R_{ON}					Characterized with a voltage sweep from 0 V to AVDD; production tested at 1.82 V
Current Carrying Switches			40	80	Ω	T switches, except T5 and T7
			30	52	Ω	T5 and T7 only
			35	70		D switches
Noncurrent Carrying Switches			1	5	kΩ	N and P switches
DC Off Leakage			370		pA	Analog input pin used for test driven to 0.2 V
DC On Leakage[1]			530	2000	pA	Analog input pin used for test driven to 0.2 V
TEMPERATURE SENSOR						
Resolution			0.3		°C	
Accuracy			±2		°C	Measurement taken immediately after exiting hibernate mode; user single-point calibration required
POWER-ON RESET	POR					Refers to voltage on DVDD pin
POR Trip Level						
Power-On		1.59	1.62	1.67	V	Power-on level
Power-Down		1.799	1.8	1.801	V	Power-down level
POR Hysteresis[1]			10		mV	
Delay Between POR Power-On and Power-Down Trip Levels		110			ms	After DVDD passes POR power-on trip level, DVDD must remain at or above power down level for this period
External Reset						
Minimum Pulse Width[1]		1			µs	Minimum pulse width required on external reset pin to trigger a reset
WAKE-UP TIMER						
Shortest Duration			31.25		µs	
Longest Duration			32		s	
DIGITAL INPUTS						
Input Leakage Current[1]						
Logic 1 GPIO			1	±5	nA	$V_{IH} = V_{DD}$, pull-up resistor disabled
Logic 0 GPIO			1	±10	nA	$V_{IL} = 0$ V, pull-up resistor disabled
Input Capacitance			10		pF	
Pin Capacitance						
XTALI			10		pF	
XTALO			10		pF	
GPIO Input Voltage						
Low	V_{INL}			0.25 × IOVDD	V	
High	V_{INH}	0.57 × IOVDD			V	
XTALI Input Voltage						
Low	V_{INL}		1.1		V	
High	V_{INH}		1.7		V	
LOGIC INPUTS						
GPIO Input Voltage						

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Low	V_{INL}			0.25 × IOVDD	V	
High	V_{INH}	0.57 × IOVDD			V	
Pull-Up Current[1]		30		130	µA	V_{IN} = 0 V; DVDD = 3.6 V
LOGIC OUTPUTS						All digital outputs, excluding XTALO
GPIO Output Voltage[8]						
High	V_{OH}	IOVDD – 0.4			V	I_{SOURCE} = 2 mA
Low	V_{OL}			0.3	V	I_{SINK} = 2 mA
Pull-Down Current[1]		30		100	µA	V_{IN} = 3.3 V
GPIO Short-Circuit Current			11.5		mA	
PIN SUPPLY RANGE FOR 1.8 V INPUT/OUTPUT		1.62	1.8	1.98	V	
Input Voltage						
Low	V_{INL}		0.3 × pin supply		V	
High	V_{INH}		0.7 × pin supply		V	
Output Voltage						
Low	V_{OL}		0.45		V	I_{SINK} = 1.0 mA
High	V_{OH}		Pin supply – 0.5		V	I_{SOURCE} = 1.0 mA
OSCILLATORS						
Internal System Oscillator			16 or 32		MHz	
Accuracy						
16 MHz Mode			±0.5	±3	%	
32 MHz Mode			±0.5	±4	%	
Switching Time[1]		4			µs	Time delay required after switching system clock source from 16 MHz or 32 MHz before communication
External Crystal Oscillator			16	32	MHz	Can be selected in place of the internal oscillator
Leakage			500	540	nA	XTALI/XTAO pins
Logic Inputs, XTALI Only						
Input Low Voltage (V_{INL})			1.1		V	
Input High Voltage (V_{INH})			1.7		V	
XTALI Input Capacitance			8		pF	
XTALO Output Capacitance			8		pF	
32 kHz Internal Oscillators			32.768		kHz	Used for watchdog timers and wake-up timers
Accuracy			±5	±15	%	
EXTERNAL INTERRUPTS						
Pulse Width[1]						
Level Triggered		7			ns	
Edge Triggered		1			ns	
POWER REQUIREMENTS[9]						
Power Supply Voltage Range (AVDD to AGND, DVDD to DGND, and IOVDD to DGND)		2.8	3.3	3.6	V	
IOVDD[10]		1.62	1.8	1.98	V	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
AVDD Current			0.56	0.64	mA	Analog Peripheral in idle mode
Hibernate Mode			8.5		µA	Only low power DAC, potentiostat amplifier, LP reference, LPTIA and 32 kHz oscillator active
			6.5		µA	Only low power DACs, potentiostat amplifiers, LP reference, and 32 kHz oscillator active; potentiostat and TIA in half power mode
			1.8		µA	Lowest power mode; only wake-up timer active. All Analog peripherals powered down
Impedance Measurement Modes						
Impedance Spectroscopy Mode			9.1		mA	When AC impedance engine, ADC and Sequencer are active.
50 kHz Impedance Measurement			106		µA	50 kHz excitation signal; DFT enabled with N = 2048; 1 Hz output data rate (ODR)
100 Hz Impedance Measurement			65		µA	When LP Loop creates sine wave at 100 Hz and the receive channel + DFT engine is duty cycled, with N = 16,to give 4 Hz ODR
Additional Power Supply Currents						
ADC			0.75	0.8	mA	f_{ADC} = 200 kSPS
			1.1	1.15	mA	f_{ADC} = 400 kSPS
High Speed TIA			0.3	0.42	mA	Low power mode
Low Power Reference			1.65		µA	
Low Power DACs for V_{ZERO} and V_{BIAS}			2.3		µA	LPDAC powered up excluding load current
Potentiostat Amplifier			2.1		µA	Potentiostat amplifier powered up
Low Power TIA			2	4.2	µA	Normal Mode
			1	3.2	µA	Half power mode
START-UP TIME						Processor clock = 16 MHz
AFE Wake Up			30	50	ms	Wake-up time to allow communication on SPI bus
ADC Wake Up			80	180	µs	Time delay required on exiting hibernate mode before starting ADC conversions.

[1] Guaranteed by design, not production tested.
[2] Code distribution can be reduced if ADC output rate is reduced by using SINC2 filter option.
[3] ADC offset and gain not calibrated for HP mode in production. User calibration can eliminate this error
[4] Noise can be reduced if ADC sample rate is reduced using the SINC2 filter
[5] See Figure 9. Low Power 2.5 V Voltage Reference DC PSRR for more details
[6] See Figure 7. ADC 1.82 V Voltage Reference AC PSRR for more details
[7] HSDAC Offset calibration can remove this error. See High Speed DAC Calibration Options for details.
[8] Code distribution can be reduced if ADC output rate is reduced by using SINC2 filter option.
[9] DAC linearity is calculated using a reduced code range of TBD lower limit to TBD upper limit
[10] IOVDD can optionally be powered from 1.8V supply rail

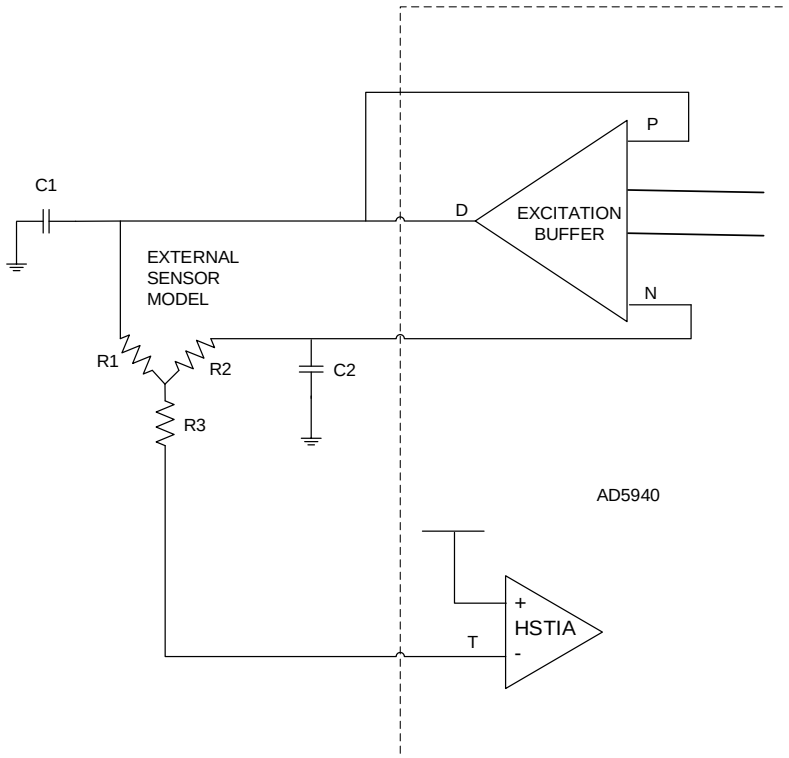

Figure 3: High Speed Loop Connected to Sensor (R1, R2 & R3). C1 and C2 represent total external capacitance to Ground

RMS NOISE RESOLUTION OF ADC

Table 2 ADC RMS Noise

Table 2 shows the rms noise specifications for the ADC with different ADC digital filter settings. The internal 1.82 V reference was used for all measurements. Table 3 shows the RMS and pk-pk effective number of bits based on the noise results in **Table 2** for various PGA gain settings. (Peak-peak ENOB results are shown in parentheses.). RMS bits are calculated as follows: log2 ((2 × *Input Range*)/*RMS Noise*); peak-to-peak (p-p) bits are calculated as follows: log2 ((2 × *Input Range*)/(6.6 × *RMS Noise*)).

Table 2 ADC RMS Noise

Update Rate (Hz)	**Sinc3 Over Sampling Rate**	**SINC2 Over Sampling Rate**	**Gain = 1** RMS Noise (uV)	**Gain = 1.5** RMS Noise (uV)	**Gain = 2** RMS Noise (uV)	**Gain = 4** RMS Noise (uV)	**Gain = 9** RMS Noise (uV)
200000	**4**	**NA**	72.43	49.732	37.83	18.93	8.62
9090	**4**	**22**	29.29	19.59	10.4	6.687	4.42
900	**5**	**178**	24.0	17.11	12.832	6.416	1.018

Table 3 ADC ENOB based on RMS Noise Effective Number of Bits (ENOB)

Update Rate (Hz)	**Sinc3 OSR**	**SINC2 OSR**	**Gain = 1**	**Gain = 1.5**	**Gain = 2**	**Gain = 4**	**Gain = 9**
200000	**4**	**NA**	14.6 (11.9 p-p)	15 (12.4 p-p)	14.95 (12.23 p-p)	14.95 (12.23 p-p)	14.9 (12.15 p-p)

9090	**4**	**22**	15 (13.18 p-p)	15 (13.8 p-p)	15 (14.09 p-p)	15 (13.73 p-p)	15 (13.15 p-p)
900	**5**	**178**	15 (13.47 p-p)	15 (13.96 p-p)	15 (13.8 p-p)	15 (13.79 p-p)	15 (15 p-p)

SPI TIMING SPECIFICATIONS

Table 4.

Parameter	Limit	Unit	Description
t_1	152	ns max	Falling edge to MISO setup time
t_2	40	ns min	$\overline{CS}$ low to SCLK setup time
t_3	40	ns min	SCLK high time
t_4	40	ns min	SCLK low time
t_5	42.1	ns min	SCLK period
t_6	14	ns max	SCLK falling edge to MISO delay
t_7	0.5	ns min	MOSI to SCLK rising edge setup time
t_8	5	ns min	MOSI to SCLK rising edge hold time
t_9	19	ns min	SCLK falling edge to hold time $\overline{CS}$
t_{10}	53	ns min	$\overline{CS}$ high time
t_{11}	62	ns min	High time $\overline{CS}$
t_{12}	310	µs typ	Low to MISO high wake-up time.

SPI Timing Diagrams

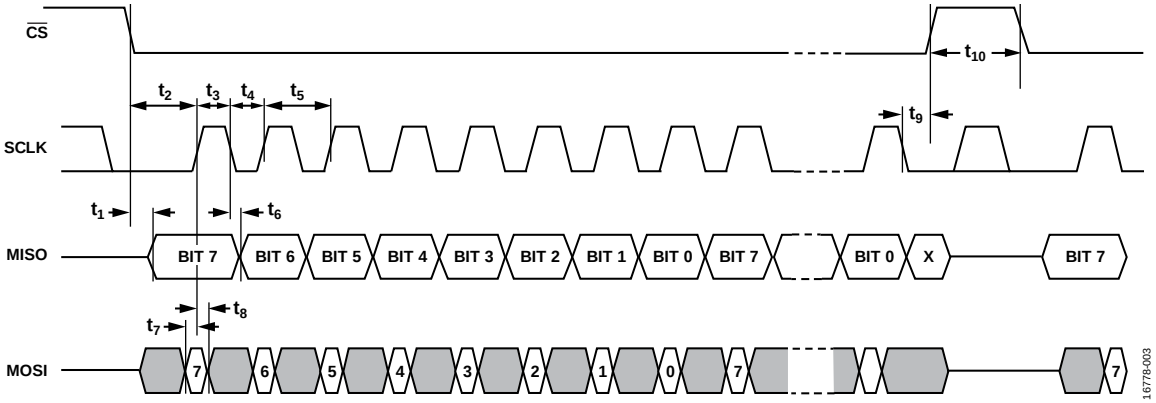

Figure 4. SPI Interface Timing Diagram

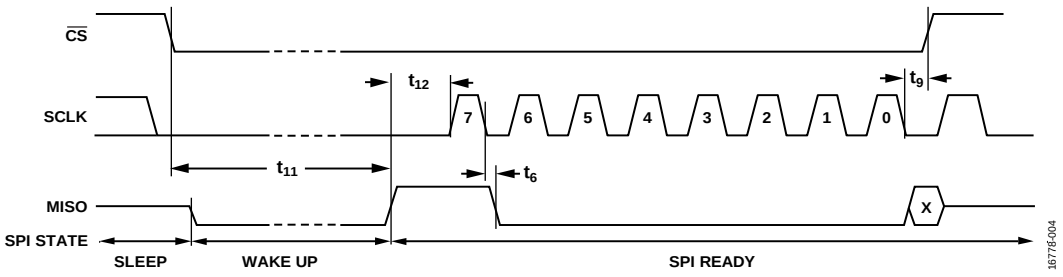

Figure 5. SPI Wake Up to Ready State Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
AVDD to AGND	−0.3 V to +3.6 V
DVDD to DGND	−0.3 V to +3.6 V
IOVDD to DGND	−0.3 V to +3.6 V
Analog Input Voltage to AGND	−0.3 V to AVDD +0.3V
Digital Input Voltage to DGND	−0.3 V to DVDD +0.3V
Digital Output Voltage to DGND	−0.3 V to DVDD +0.3V
AGND to DGND	−0.3 V to +0.3 V
Total GPIOx Pins Current	
Positive	0 mA to 30 mA
Negative	−30 mA to 0 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Reflow Profile	J-STD 020E (JEDEC)
Junction Temperature	150°C max
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	2 kV
Field Induced Charged Device Model (FICDM)	1 kV
Machine Model (MM)	100 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 6. Thermal Resistance[1]

Air Flow	θ_{JA}	Ψ_{JT}	Ψ_{JB}	θ_{JC}	θ_{JB}	Unit
Still Air	33.0702	0	15.105	0.0642	11.5904	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD51.

PACKAGE INFORMATION

Table 8 provides information about the package branding.

Table 7. Package Branding Information

Line	Branding Key	Field Description
1	AD5940	Part identifier.
2	BCBZ-Ux	Model and RoHS-compliant designation. Prerelease branding includes Ux. U indicates sample material. x indicates the silicon revision.
3	#yyww	Lead free, date code, year, and week.
4	Lot ID	Assembly lot code.
5		Country of origin.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8
A	AFE4	AFE3	AIN2	AVDD	VREF_1V82	SE0	CE0	RE0
B	RCAL1	AFE1	AIN1	LPF0	AIN3 /BUF_VREF1V8	DE0	VZERO0	RC0_1
C	RCAL0	AFE2	NC	AGND	AIN6	RC0_2	VBIAS0	RC0_0
D	VBIAS_CAP	AIN0	NC	NC	AGND_REF	GP1	VREF_2V5	AVDD_REG
E	GP2	GP3	AGND	DGND	DGND	DGND	MOSI	MISO
F	/RESET	AVDD	DVDD	GP6	GP0	GP5	CS	CLK
G	NC	IOVDD	DVDD_REG1V8	GP7	XTALI	XTALO	GP4	NC

Figure 6. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output Supply	Description
A1	AFE4	Analog	Uncommitted Analog Pin 4. Voltage input to the ADC
A2	AFE3	Analog	Uncommitted Analog Pin 3. Connects to switch matrix.
A3	AIN2	Analog	Uncommitted AFE Pin 2. This pin connects to the switch matrix and ADC mux
A4	AVDD	Supply	Analog Circuit Power. Short this pin to Pin F2.
A5	VREF_1V82	Analog	1.82 V Reference Decoupling Capacitor Pin.
A6	SE0	Analog	Sense Electrode Input Pin for Both High and Low Bandwidth Loop Circuits. This pin connects to the switch matrix.
A7	CE0	Analog	Counter Electrode Input Pin for Both High and Low Bandwidth Loop Circuits. This pin connects to the switch matrix.
A8	RE0	Analog	Reference Electrode Input Pin for Both High and Low Bandwidth Loop Circuits. This pin connects to positive node (P node) of the switch matrix.
B1	RCAL1	Analog	Terminal B of Calibration Resistor. Connect RCAL1 to the switch matrix.
B2	AFE1	Analog	Uncommitted Analog Pin 1.
B3	AIN1	Analog	Uncommitted AFE Pin 1. This pin connects to the switch matrix.
B4	AIN4/LPF0	Analog	Low Power TIA Output Low-pass filter capacitor Pin.
B5	AIN3/BUF_VREF1V8	Analog	Uncommitted AFE Pin 3 (AIN3)/1.82 V reference buffered output (BUF_VREF1V8). This pin connects to the switch matrix. This is a dual function pin.
B6	DE0	Analog	Analog Input Pin. This pin connects to the input and output of the high speed TIA.
B7	V_{ZERO0}	Analog	Low Power, Dual Output DAC V_{ZERO0} Output.
B8	RC0_1	Analog	Low Power TIA Feedback Pin.
C1	RCAL0	Analog	Terminal A of Calibration Resistor. Connect RCAL0 to the switch matrix.

Pin No.	Mnemonic	Input/Output Supply	Description
C2	AFE2	Analog	Uncommitted Analog Pin 2.
C3	NC	Analog	Not Connected.
C4	AGND	Ground	Analog Ground. Short this pin to Pin E3.
C5	AIN6	Analog	Uncommitted analog pin. Can be used as an auxiliary voltage channel to the ADC.
C6	RC0_2	Analog	Filter Pin. It is possible to leave this pin open (optional).
C7	V_{BIAS0}	Analog	Low Power, Dual Output DAC V_{BIAS0} Output.
C8	RC0_0	Analog	Low Power TIA Feedback Pin.
D1	VBIAS_CAP	Analog	VBIAS Decoupling Capacitor Pin.
D2	AIN0	Analog	Uncommitted AFE Pin 0. This pin connects to the switch matrix.
D3	NC	Analog	Not Connected
D4	NC	Not applicable	Not Connected.
D5	AGND_REF	Ground	Analog Reference Ground.
D6	GPIO1	Digital input/output	General-Purpose Input/Output Pin 1.
D7	VREF_2V5	Analog	2.5 V Analog Reference Decoupling Capacitor Pin.
D8	AVDD_REG	Supply	Analog Regulator Decoupling Capacitor Pin.
E1	GPIO2	Digital input/output	General-Purpose Input/Output Pin 2.
E2	GPIO3	Digital input/output	General-Purpose Input/Output Pin 3.
E3	AGND	Ground	Analog Ground. Short this pin to Pin C4.
E4	DGND	Digital input	Digital Ground
E5	DGND	Ground	Digital Input/Output Ground Pin.
E6	DGND	Ground	Digital Ground.
E7	MOSI	Digital input	SPI MOSI.
E8	MISO	Digital output	SPI MISO.
F1	$\overline{\text{RESET}}$	Digital input	Reset Pin, Active Low.
F2	AVDD	Supply	Analog 3.3 V Circuit Power.
F3	DVDD	Supply	Digital Circuit Power.
F4	GPIO6	Digital input/output	General-Purpose Input/Output Pin 6.
F5	GPIO0	Digital input/output	General-Purpose Input/Output Pin 0.
F6	GPIO5	Digital input/output	General-Purpose Input/Output Pin 5.
F7	$\overline{\text{CS}}$	Digital input/output	SPI Chip Select.
F8	SCLK	Digital input	SPI Clock.
G1	NC	Not applicable	Not Connected.
G2	IOVDD	Supply	Digital Input/Output Supply Pin. DVDD must be driven before IOVDD is enabled.
G3	DVDD_REG1V8	Analog	1.8 V Digital Regulator Decoupling Capacitor Pin.
G4	GPIO7	Digital input/output	General-Purpose Input/Output Pin 7.
G5	XTALI	Analog	16 MHz External Crystal Pin.
G6	XTALO	Analog	16 MHz External Crystal Pin.
G7	GPIO4	Digital input/output	General-Purpose Input/Output Pin 4.
G8	NC	Not applicable	Not Connected.

TYPICAL PERFORMANCE CHARACTERISTICS

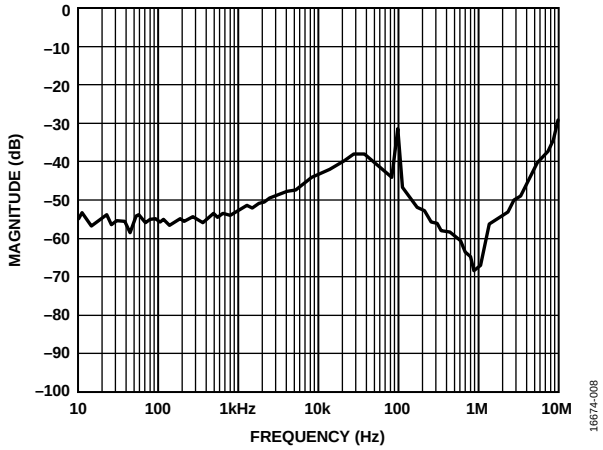

Figure 7. ADC 1.82 V Voltage Reference AC PSRR

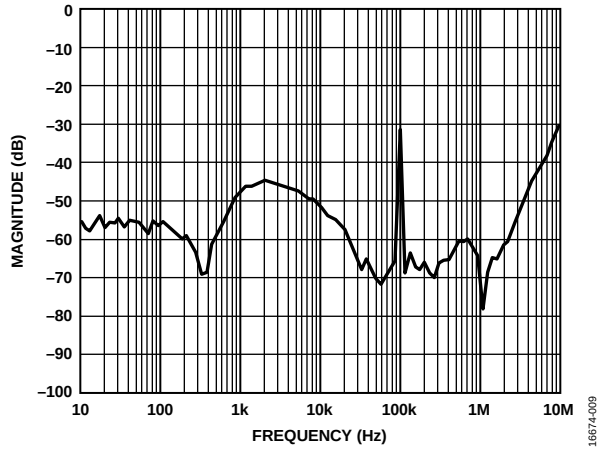

Figure 8. Low Power 2.5 V Voltage Reference AC PSRR

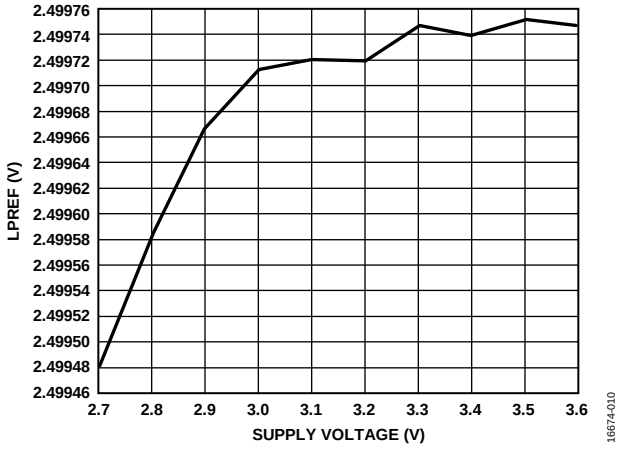

Figure 9. Low Power 2.5 V Voltage Reference DC PSRR

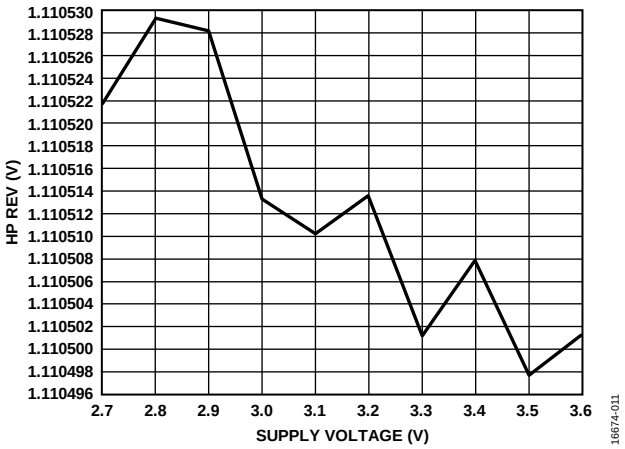

Figure 10. 1.11 V Voltage Reference DC PSRR

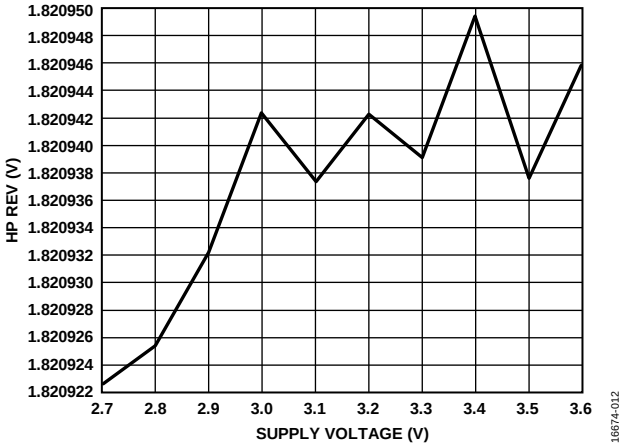

Figure 11. ADC 1.82 V Voltage Reference DC PSRR

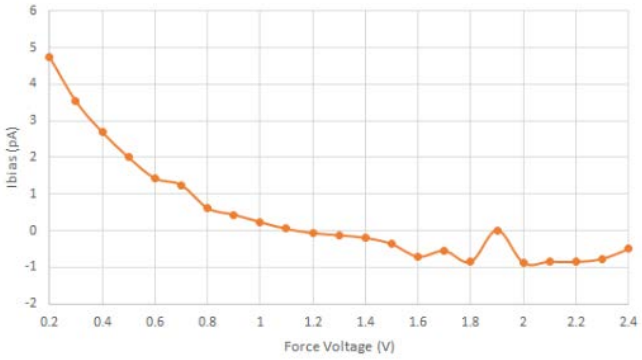

Figure 12. Potentiostat Amplifier Input Bias Current vs. RE0 Pin Voltage

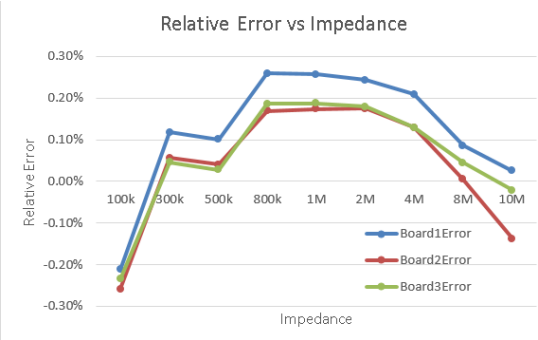

Figure 13: EDA Measurement Relative Error vs Impedance

THEORY OF OPERATION

The main blocks of the AD5940 are as follows (each block is covered in more detail in the subsequent sections):

- A low power, dual output string DAC used to set the sensor bias voltage and low frequency excitation. Supports chrono-amperometric and voltammetry electrochemical techniques (see Low Power DAC section).
- A low power potentiostat amplifier that controls the voltage on the sensor (see Low Power Potentiostat Amplifier section).
- A low power TIA that performs low bandwidth current measurements (see Low Power TIA section).
- A high speed DAC and amplifier designed to generate excitation signals for impedance measurements up to 200 kHz (see High Speed DAC Circuits section).
- A high speed TIA that supports wider signal bandwidth measurements (see High Speed TIA Circuits section).
- A high performance ADC circuit (see the High Performance ADC Circuit section).
- A programmable switch matrix. The input switching of the AD5940 allows full configurability in the connections of the external sensors (see the Programmable Switch Matrix section).
- A programmable sequencer (see the Sequencer section).
- An SPI interface.
- A waveform generator designed to create sinusoid and trapezoid waveforms up to 200 kHz (see the Waveform Generator section).
- Interrupt sources that output to a GPIOx pin to alert the host controller that an interrupt event occurred (see the Interrupts).
- Digital inputs/outputs (see the Digital Inputs/Outputs section).

CONFIGURATION REGISTERS

Configuration Register—AFECON

Address: 0x00002000, Reset: 0x00080000, Name: AFECON

Table 9. Bit Descriptions for AFECON

Bits	Bit Name	Settings	Description	Reset	Access
[31:22]	Reserved		Reserved.	0x0	R
21	DACBUFEN		Enables the dc DAC buffer. This bit enables the buffer for the high impedance output of the dc DAC.	0x0	R/W
		0	Disable the dc DAC buffer.		
		1	Enable the dc DAC buffer.		
20	DACREFEN		High speed DAC reference enable.	0x0	R/W
		0	Reference disable. Clear to 0 to disable the high speed DAC reference.		
		1	Reference enable. Set to 1 to enable the high speed DAC reference.		
19	ALDOILIMITEN		Analog low dropout regulator (LDO) current limiting. This bit enables AFE analog LDO buffer current limiting. If enabled, this feature limits the current drawn from the battery while charging the capacitor on AVDD_REG.	0x1	R/W
		0	Analog LDO buffer current limiting enabled.		
		1	Analog LDO buffer current limiting disabled.		
[18:17]	Reserved		Reserved	0x0	R
16	SUPPLYLPFEN		ADC output 50 Hz/60 Hz filter enable. This bit enables the 50 Hz/60 Hz supply rejection filter.	0x0	R/W
		0	Supply rejection filter disabled. Disables sinc2, the 50 Hz/60 Hz digital filter. Disable this bit for impedance measurements.		
		1	Supply rejection filter enabled. Enables sinc2, the 50 Hz/60 Hz digital filter.		
15	DFTEN		DFT hardware accelerator enable. This bit enables the DFT hardware acceleration block.	0x0	R/W
		0	DFT hardware accelerator disabled.		
		1	DFT hardware accelerator enabled.		
14	WAVEGENEN		Waveform generator enable. This bit enables the waveform generator.	0x0	R/W
		0	Waveform generator disabled. The waveform generator includes a sinusoid wave and a trapezoid wave.		
		1	Waveform generator enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
13	TEMPCONVEN		ADC temperature sensor convert enable. This bit enables the temperature reading. If this bit is set to 1, a temperature reading is initiated. When the temperature conversion is complete and the result available in the AFE_ TEMP_SENSOR_RESULT register, this bit is reset to 0.	0x0	R/W
		0	Temperature reading disabled.		
		1	Temperature reading enabled.		
12	TEMPSENSEN		ADC temperature sensor channel enable. This bit enables the temperature sensor.	0x0	R/W
		0	Temperature sensor disabled. The temperature sensor is powered down.		
		1	Temperature sensor enabled. The temperature sensor is powered up; however, no temperature readings are performed unless TEMPCONVEN = 1.		
11	TIAEN		High speed TIA enable. This bit enables the high speed TIA.	0x0	R/W
		0	High speed TIA disabled.		
		1	High speed TIA enabled.		
10	INAMPEN		Excitation instrumentation amplifier enable. This bit enables the instrumentation amplifier.	0x0	R/W
		0	Programmable instrumentation amplifier disabled.		
		1	Programmable instrumentation amplifier enabled.		
9	EXBUFEN		Excitation buffer enable. This bit enables the excitation buffer to drive the resistance under measurement.	0x0	R/W
		0	Excitation buffer disabled.		
		1	Excitation buffer enabled.		
8	ADCCONVEN		ADC conversion start enable.	0x0	R/W
		0	ADC idle. The ADC is powered on, but is not converting.		
		1	ADC conversions enabled.		
7	ADCEN		ADC power enable. This bit enables the ADC.	0x0	R/W
		0	ADC disabled. The ADC is powered off.		
		1	ADC enabled. The ADC is powered on. ADCCONVEN must be set to start conversions.		
6	DACEN		High speed DAC enable. This bit enables the high speed DAC, the corresponding reconstruction filter, and the attenuator. This bit only enables the analog block and does not include the DAC waveform generator.	0x0	R/W
		0	High speed DAC disabled.		
		1	High speed DAC enabled.		
5	HSREFDIS		High Speed reference disable. This bit is the power-down signal of the high power reference. Set this bit to 1 to power down the reference.	0x0	R/W
		0	High power reference enabled.		
		1	High power reference disabled.		
[4:0]	Reserved		Reserved.	0x0	R

Power Mode Configuration Register—PMBW

Address: 0x000022F0, Reset: 0x00088800, Name: PMBW

The power mode configuration register, PMBW, configures the high and low power system modes for the high speed DAC and ADC circuits.

Table 10. Bit Descriptions for PMBW

Bits	Bit Name	Settings	Description	Reset	Access
[31:4]	Reserved		Reserved	0x8880	R
[3:2]	SYSBW		System bandwidth configure. The RCF of the high speed DAC and the AAF bandwidth configuration of the ADC are configured by a single register.	0x0	R/W
		00	No action for system configuration. The RCF and AAF are automatically configured according to the waveform generator frequency.		
		01	50 kHz, −3 dB bandwidth.		
		10	100 kHz, −3 dB bandwidth.		
		11	250 kHz ,−3 dB bandwidth.		
1	Reserved		Reserved.	0x0	R
0	SYSHS		Sets the high speed DAC and ADC in high power mode.	0x0	R/W
		0	Low power mode. Clear this bit for impedance measurements of <80 kHz.		
		1	High speed mode. Set this bit for impedance measurements of >80 kHz.		

SILICON IDENTIFICATION

The AD5940 contains a chip ID register and a hardware revision register.

These registers can be read by software to allow users to determine the revision of the silicon currently in use. ADIID is always equal to 0x4144. The CHIPID contains the device identifier (CHIPID [14:4] and silicon revision number (CHIPID [3:0]). The device identifier changes with silicon revision.

IDENTIFICATION REGISTERS

Analog Devices, Inc., Identification Register—ADIID

Address: 0x00000400, Reset: 0x0000, Name: ADIID

Table 11. Bit Descriptions for ADIID

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ADIID		Analog Devices identifier. Always equal to 0x4144.	0x0	R

Chip Identification Register—CHIPID

Address: 0x00000404, Reset: 0x0000, Name: CHIPID

Address 0x00000404 is the chip identification (ID) register.

Table 12. Bit Descriptions for CHIPID

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Part ID		Device identifier	0x0	R
[3:0]	Revision		Silicon revision number	0x0	R

LOW POWER DAC

The ultra low power DAC is a dual output string DAC and is designed to set the bias voltage of the sensor. There are two output resolution formats: 12-bit resolution (V_{BIAS0}) and 6-bit resolution (V_{ZERO0}).

In normal operation, the 12-bit output sets the voltage on the reference/counter electrode pins, RE0 and CE0, via the potentiostat circuit. This voltage can also be sent to the V_{BIAS0} pin by configuring SW12 (see Figure 21). An external filtering capacitor can be connected to the V_{BIAS0} pin.

The 6-bit output sets the voltage to the positive LPTIA pin. The voltage on the sense electrode is equal to the voltage on the LPTIA positive pin. This voltage is referred to as V_{ZERO} and can be connected to the V_{ZERO0} pin by configuring SW13 (see Figure 21). In diagnostic mode, the V_{ZERO} output can also be connected to the high speed TIA by setting Bit 5 in the LPDACCON register to 1.

The low power DAC reference source is a low power, 2.5 V reference.

The low power DACs are made up of two 6-bit string DACs. The main 6-bit string DAC provides the V_{ZERO0} DAC output, and is made up of 63 resistors. Each resistor is the same value.

The main 6-bit string with the 6-bit sub-DAC provides the V_{BIAS0} DAC output. In 12-bit mode, the MSBs select a resistor from the main string DAC. The top end of this resistor is selected as the top of the 6-bit sub-DAC, and the bottom end of the selected resistor is connected to the bottom of the 6-bit sub-DAC string as in Figure 17.

The resistor matching between the 12-bit and 6-bit means 64 LSB12 (V_{BIAS0}) is equal to one LSB6 (V_{ZERO0}).

The output voltage range is not rail-to-rail, but ranges from 0.2 V to 2.4 V for the 12-bit output of the low power DAC. Therefore, the LSB value of the 12-bit output is

$$12\text{-}BIT\_DAC\_LSB = \frac{2.2\ V}{2^{12}-1} = 537.2\ \mu V$$

The 6-bit output range is from 0.2 V to 2.366 V. This range is not 0.2 V to 2.4 V because there is a voltage drop across R1 in the resistor string (see Figure 17). The LSB value of the 6-bit output is

$$6\text{-}BIT\_DAC\_LSB = 12\text{-}BIT\_DAC\_LSB \times 64 = 34.38mV$$

To set the output voltage of the 12-bit DAC, write to Bits[11:0] of the LPDACDAT0 register. To set the 6-bit DAC output voltage, write to Bits[17:12] of the LPDACDAT0 register.

If the system clock is 16 MHz, LPDACDAT0 takes 10 clock cycles to update. If system clock is 32 kHz, LPDACDAT0 takes one clock cycle to update. Take these values into consideration when using the sequencer. The following code demonstrates how to correctly set the LPDACDAT0 value:

```
SEQ_WR(REG_AFE_LPDACDAT0, 0x1234);
SEQ_WAIT(10); // Wait 10 clocks for
LPDADAT0 to update
SEQ_SLP();
```

Optionally, the waveform generator described in the Waveform Generator section can be used as the DAC codes source for the low power DAC. When using the waveform generator with the low power DAC, ensure that the settling time specification of the low power DAC is not violated. The system clock source must be the 32 kHz oscillator. This feature is provided for ultra low power, always on, low frequency measurements, such as skin impedance measurements where the excitation signal is roughly 100 Hz and system power consumption needs to be <100uA.

LPDAC SWITCH OPTIONS

There are a number of switch options available that allow the user to configure the LPDAC for various modes of operation. These switches facilitate different use cases, such as electro-chemical impedance spectroscopy. Figure 16 shows the available switches, labeled SW0 to SW4. These switches are controlled either automatically via Bit 5 in the LPDACCON register, or individually via the LPDACSW0 register

When LPDACCON, Bit 5, is cleared, the switches are configured for normal mode. SW2 and SW3 are closed and SW0, SW1, and SW4 are open. When LPDACCON, Bit 5, is set, the switches are configured for diagnostic mode. SW0 and SW4 are closed and the remaining switches are open. This feature is designed for electrochemical use cases, such as continuous glucose measure-ment where, in normal mode, the low power TIA measures the sense electrode. Then, in diagnostic mode, the high speed TIA measures the sense electrode. By switching the V_{ZERO} output from the LPTIA to the HSTIA, the effective bias on the sensor, $V_{BIAS} - V_{ZERO}$, is unaffected. Using the HSTIA facilitates high band-width measurements, such as impedance, ramp, and cyclic voltammetry.

Use the LPDACSWO register to control the switches individually. LPDACSW0, Bit 5, must be set to 1; then, each switch can be individually controlled via LPDACSW0, Bits[0:4].

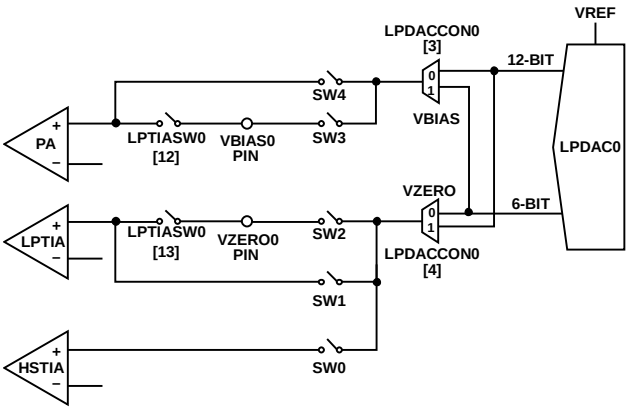

Figure 14. Low Power DAC Switches

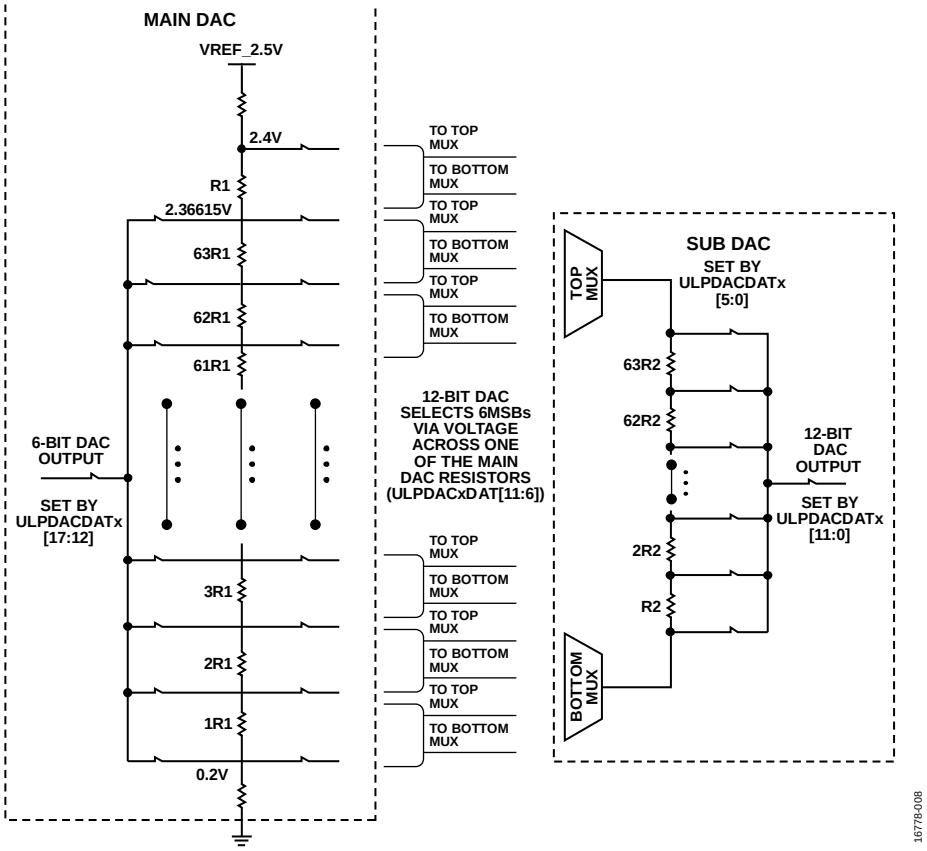

Figure 15. Low Power DAC Resistor String

RELATIONSHIP BETWEEN THE 12-BIT AND 6-BIT OUTPUTS

The 12-bit and 6-bit outputs are mostly independent. However, the selected 12-bit value does have a loading effect on the 6-bit output that must be compensated for in user code, particularly when the 12-bit output level is greater than the 6-bit output.

When the 12-bit output is less than the 6-bit output,

12-Bit DAC Output Voltage = 0.2 V + (*LPDACDAT, Bits[11:0]* × *12-BIT_LSB_DAC*)

6-Bit DAC Output Voltage = 0.2 V + (*LPDACDAT, Bits[17:12]* × *6-BIT_LSB_DAC*) – *12-BIT_LSB_DAC*)

When the 12-bit output is ≥ the 6-bit output,

12-Bit DAC Output Voltage = 0.2 V + (LPDACDAT, Bits[11:0] × *12-BIT_LSB_DAC*)

6-Bit DAC Output Voltage = 0.2 V + (*LPDACDAT, Bits[17:12]* × *6-BIT_LSB_DAC*)

Therefore, in user code, it is recommended to add the following:

```
12BITCODE = LPDACDAT0 [11:0];
6BITCODE = LPDACDAT0 [17:12];
if (12BITCODE < (6BITCODE *64))
LPDACDAT [11:0] = (12BITCODE – 1);
```

This code ensures that the 12-bit output voltage is equal to the 6-bit output voltage when LPDACDAT0, Bits[11:0] = 64 × LPDACDAT0, Bits[17:12].

LOW POWER DAC USE CASES

Electrochemical Amperometric Measurement

In an electrochemical measurement, the 12-bit output sets the voltage on the reference electrode pin via the potentiostat circuit shown in Figure 18. The voltage on the CE0 pin and RE0 pin is referred to as V_{BIAS}. The 6-bit output sets the bias voltage on the LPTIA positive pin; this sets the voltage on the sense electrode pin, SE0. This voltage is referred to as V_{ZERO}. The bias voltage on the sensor effectively becomes the difference between the 12-bit output and the 6-bit output.

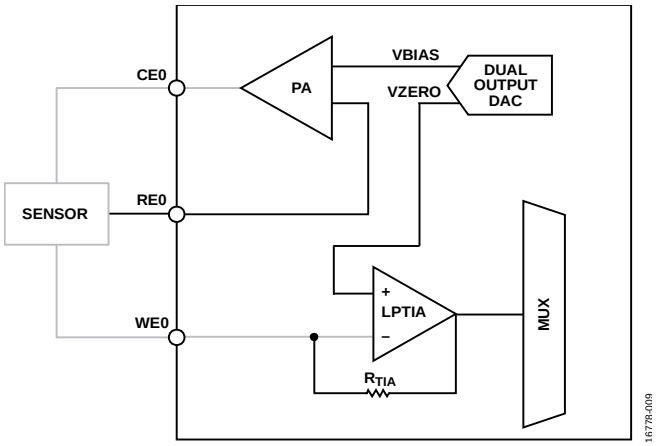

Figure 16. Electrochemical Standard Configuration

Electrochemical Impedance Spectroscopy

In many electrochemical applications, there is significant value in carrying out a diagnostic measurement. A typical diagnostic technique is carrying out an impedance measurement on the sensor. For some sensor types, the dc bias on the sensor must be maintained while carrying out the impedance measurement; the AD5940 facilitates this. To perform this action, LPDACCON, Bit 5 = 1. V_{ZERO} is set to the input of the high speed TIA and the high speed DAC generates an ac signal. The level of the ac signal is set via the V_{BIAS} output of the low power DAC, and the voltage on SE0 is maintained by V_{ZERO}. The high speed DAC dc buffers must also be enabled by setting AFECON, Bit 1.

Low Power DAC in 4-Wire Isolated Impedance Measurements

For 4-wire isolated impedance measurements, such as body impedance measurements, a high frequency sinusoid waveform is applied to the sensor via the high speed DAC. There is also a common-mode voltage set across the sensor using the LPDAC 6-bit output, V_{ZERO}, and the LPTIA. This configuration sets the common-mode voltage between AIN2 and AIN3 (see Figure 19). To enable this common-mode voltage setup, SWMUX, Bit 3, must be set to 1. The V_{BIAS} output of the low power DAC also sets the common-mode voltage for the high speed DAC excitation buffer.

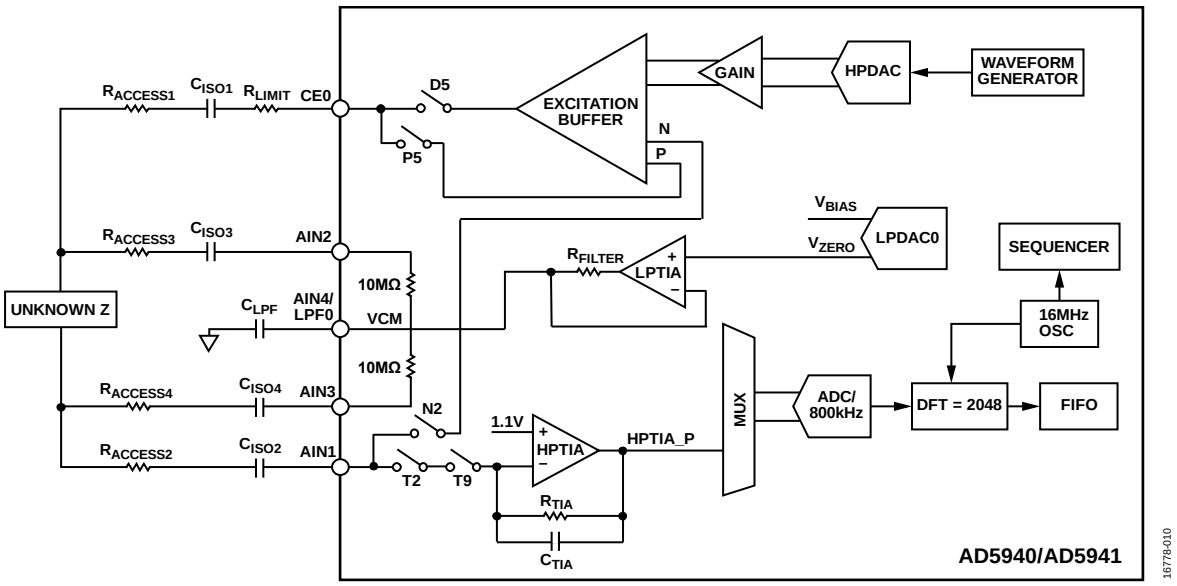

Figure 17. Low Power DACs Used in a 4-Wire Impedance Measurement

LOW POWER DAC CIRCUIT REGISTERS

Table 13. LPTIA and DAC Registers Summary

Address	Name	Description	Reset	Access
0x00002120	LPDACDAT0	Low power DAC data output	0x00000000	R/W
0x00002128	LPDACCON0	Low power DAC configuration register	0x00000002	R/W
0x00000124	LPDACCSW0	Low power DAC switch control	0x00000000	R/W
0x00002050	LPREFBUFCON	Low power reference configuration	0x00000000	R/W

LPDACCON0 Register—LPDACCON0

Address: 0x00002128, Reset: 0x00000002, Name: LPDACCON0

Table 14. Bit Descriptions for LPDACCON0

Bits	Bit Name	Settings	Description	Reset	Access
[31:7]	Reserved		Reserved.	0x0	R
6	WAVETYPE		Low power DAC data source. This bit determines the DAC waveform type.	0x0	R/W
		0	Direct from LPDACDAT0.		
		1	Waveform generator.		
5	DACMDE		Low power DAC0 switch settings. This bit is the control bit for the low power DAC output switches.	0x0	R/W
		0	Low power DAC0 switches set for normal mode (default). Clear this bit to 0 for normal output switch operation. See the Low Power DAC section for more information.		
		1	Low power DAC0 switches set for diagnostic mode. Set this bit to 1 for diagnostic mode switch settings. See the Low Power DAC section for more information.		
4	VZEROMUX		V_{ZERO} mux select. This bit selects the DAC output that connects to the V_{ZERO0} node. Ensure that the same value is written to the VBIASMUX bit.	0x0	R/W
		0	V_{ZERO}, 6-bit (default). Clear this bit to 0 for the V_{ZERO} output to be 6-bit.		
		1	V_{ZERO}, 12-bit. Set this bit to 1 for the V_{ZERO} output to be 12-bit.		

Bits	Bit Name	Settings	Description	Reset	Access
3	VBIASMUX		V_{BIAS} mux select. This bit selects the DAC0 output that connects to the V_{BIAS0} node. Ensure that the same value is written to the VZEROMUX bit.	0x0	R/W
		0	Output, 12-bit (default). The 12-bit DAC is connected to V_{BIAS0}.		
		1	Output, 6-bit. The 6-bit DAC is connected to V_{BIAS0}.		
2	REFSEL		Low power DAC reference select.	0x0	R/W
		0	Selects the low power 2.5 V reference as the low power DAC reference source.		
		1	Selects AVDD as the low power DAC reference source.		
1	PWDEN		Low Power DAC0 power-down. This bit powers down the control bit for the low power DAC.	0x1	R/W
		0	Low Power DAC0 powered on. Clear this bit to 0 to power on the low power DAC.		
		1	Low Power DAC0 powered off (default). Powers down the low power DAC and opens all switches on the low power DAC0 output.		
0	RSTEN		Enable writes to Low Power DAC0. Enables writes to LPDACDAT0 register.	0x0	R/W
		0	Disables Low Power DAC0 writes (default). If this bit is cleared to 0, LPDACDAT0 is always 0. Writes to LPDACDAT0 are disabled.		
		1	Enables Low Power DAC0 writes. Set this bit to 1 to enable writes to LPDACDAT0.		

LPDAC Switch Control Register—LPDACSW0

Address: 0x00002124, Reset: 0x00000000, Name: LPDACSW0

Table 15. Bit Descriptions for LPDACSW0

Bits	Bit Name	Settings	Description	Reset	Access
[31:6]	Reserved		Reserved.	0x0	R
5	LPMODEDIS		Switch control. LPDACSW0, Bit 5, controls the switches connected to the output of the low power DAC.	0x0	R/W
		0	Low power DAC switch controlled by LPDACCON0, Bit 5 (default). Clear this bit to 0 to control the switches connected to the output of the low power DAC via LPDACCON0, Bit 5.		
		1	LPDAC switches override. Set this bit to 1 to overrides LPDACCON0, Bit 5. The switches connected to the low power DAC0 output are controlled via LPDACSW00, Bits[4:0].		
4	SW4		Low Power DAC0 SW4 control	0x0	R/W
		0	Disconnects the direct connection of the V_{BIAS0} DAC output to positive input of Low Power Amplifier 0 (default).		
		1	Connects the V_{BIAS0} DAC output directly to the positive input of Low Power Amplifier 0.		
3	SW3		Low Power DAC0 SW3 control.	0x1	
		0	Disconnects the V_{BIAS0} DAC output from the low-pass filter/V_{BIAS0} pin.		R/W
		1	Connects the V_{BIAS0} DAC output to the low-pass filter/V_{BIAS0} pin (default).		
2	SW2		Low Power DAC0 SW2 control.		
		0	Disconnects the V_{ZERO} DAC output from the low-pass filter/V_{ZERO} pin.	0x1	R/W
		1	Connects the V_{ZERO} DAC output to the low-pass filter/V_{ZERO} pin (default).		
1	SW1		Low Power DAC0 SW1 control.	0x0	
		0	Disconnects the direct connection of the V_{ZERO} DAC output to the Low Power TIA0 positive input (default).		R/W
		1	Connects the V_{ZERO} DAC output directly to the Low Power TIA0 positive input.		
0	SW0		Low Power DAC0 SW0 control.	0x0	
		0	Disconnects the V_{ZERO} DAC output from the high speed TIA positive input (default).		R/W
		1	Connects the V_{ZERO} DAC output to the high speed TIA positive input.		

Low Power DAC Data Output Register—LPDACDAT0

Address: 0x00002120, Reset: 0x00000000, Name: LPDACDAT0

Table 16. Bit Descriptions for LPDACDAT0

Bits	Bit Name	Settings	Description	Reset	Access
[31:18]	Reserved		Reserved.	0x0	R
[17:12]	DACIN6		Low Power DAC0 6-bit output data register (1 LSB = 34.375 mV). A value between 0 and 0x3F sets the 6-bit output voltage.	0x0	R/W
		0	0.2 V.		
		111111	2.366 V.		
[11:0]	DACIN12		Low Power DAC0 12-bit output data register (1 LSB = 537 µV). A value between 0 and 0xFFF sets the 12-bit output voltage.	0x0	R/W
		0	0.2 V.		
		0xFFF	2.4 V.		

Low Power Reference Control Register—LPREFBUFCON

Address: 0x00002050, Reset: 0x00000000, Name: LPREFBUFCON

Table 17. Bit Descriptions for LPREFBUFCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:2]	Reserved		Reserved.	0x0	R
1	LPBUF2P5DIS		Low power output band gap buffer. This bit is normally cleared to enable the low power reference buffer.	0x0	R/W
		0	Enables the low power 2.5 V buffer.		
		1	Powers down the low power 2.5 V buffer.		
0	LPREFDIS		Low power band gap power-down bit. This bit is normally cleared to enable the low power reference.	0x0	R/W
		0	Low power reference enabled.		
		1	Low power reference powered down		

Switch Mux Register—SWMUX

Address: 0x0000235C, Reset: 0x00000000, Name: SWMUX

Table 18. Bit Descriptions for SWMUX

Bits	Bit Name	Settings	Description	Reset	Access
[31:4]	Reserved		Reserved.	0x0	R
3	CMMUX		Common-mode resistor select for AIN2 and AIN3.	0x0	R/W
		0	Common-mode switch off.		
		1	Enables the common-mode switches with a 10 MΩ resistor to set up the common-mode voltage on the AINx pins. The voltage is driven by the low power TIA and the LPF0 pin.		
[2:0]	SWMUX		AFE switch mux control.	0x0	R/W
		0	AFE switch mux off.		
		1	Short AFE1 and AFE2.		
		10	Short AFE3 and AFE4.		

LOW POWER POTENTIOSTAT AMPLIFIER

The AD5940 has a low power potentiostat amplifier that sets and controls the bias voltage of an electrochemical sensor. Typically the output of the potentiostat is connected to CE0. The non-inverting input is connected to V_{BIASO} and the inverting input is connected to RE0 as in Figure 20. For an electrochemical cell the potentiostat maintains the bias voltage on the reference electrode (RE0) by sourcing or sinking current through the counter electrode (CE0).

The output of the potentiostat can be connected to various package pins through the switch matrix (see the Programmable Switch Matrix section for details). There are a number of configurable switch options around the potentiostat to provide numerous configuration options (see Figure 21).

The potentiostat can also be used a standard buffer output to output V_{BIAS0} onto CE0. TO do this the inverting input is connected to the output of the potentiostat by closing sw10 in Figure 21.

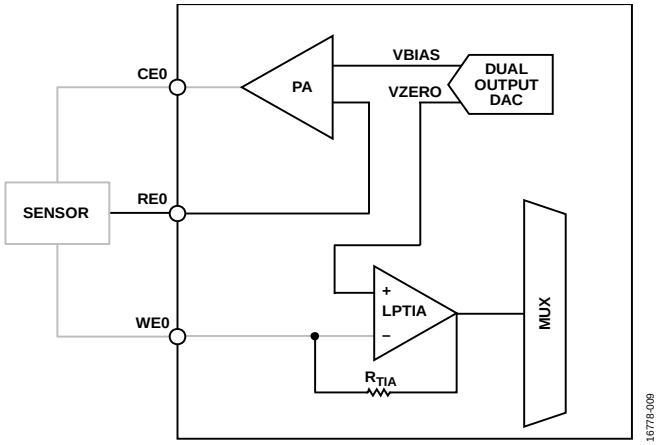

Figure 18. Potentiostat Connected to Sensor

LOW POWER TIA

The AD5940 has a low power TIA channel used to amplify small current inputs to voltages to be measured by the ADC. The load resistor and gain resistor are internal and programmable. Select the TIA gain resistor that maximizes the ADC input range of ±900 mV.

To calculate the required gain resistor, use the following equation:

$$I_{MAX} = \frac{0.9}{R_{TIA}}$$

where:
I_{MAX} is the expected full-scale input current.
R_{TIA} is the required gain resistor.

There are a number of switches available around the LPTIA circuitry. Figure 21 shows the available switches. These switches are configured in the LPTIASW0 register. The switches labeled as F/S in Figure 21 indicate a force and sense circuit. When the TIAGAIN bit in the LPTIACON0 register is set, these switches are closed automatically. When these switches are closed, there is a force/sense circuit with R_{LPF} and a capacitor on AIN4/LPF0 acting as a resistor-capacitor (RC) delay circuit. Analog Devices recommends that the LPTIA0_P_LPF mux option is selected as the ADC input when using the LPTIA. It is also recommended to connect a 100 nF capacitor between RC0_0 and RC0_1 to stabilize the amplifier.

LOW POWER TIA PROTECTION DIODES

Back to back protection diodes are connected in parallel with the R_{TIA} gain resistor. These diodes are connected or disconnected by closing or opening SW0, controlled by LPTIASW0, Bit 1.These diodes are intended for use when switching R_{TIA} gain settings to amplify small currents to prevent saturation of the TIA. These diodes have a leakage current specification dependent on the voltage across the diodes. If the differential voltage across the diodes is >200 mV, leakage can be >1 nA; if the voltage is >500 mV, leakage can be >1 µA.

LPTIA and Potentiostat Amplifiers Current Limit Feature

In addition to the protection diode, the LPTIA also has a built in current limiting feature. If the current sourced or sunk from the LPTIA is greater than the overcurrent limit protection specified in the Specifications section, the amplifiers clamp the current to this limit. If a sensor on start-up attempts to source or sink more than the overcurrent limit, the amplifier clamps the output current. Do not use this feature more frequently or for longer than specified in the Specifications section.

LPTIA Force/Sense Feature

The LPTIACON0[9:5] bits select different gain resistor values for the LPTIA, labeled as R_{TIA} in **Error! Reference source not found.**. The force and sense connections shown on the feedback path of the LPTIA are used to avoid voltage (I × R) drops on the switches used to select different R_{TIA} settings for the internal R_{TIA}.

USING AN EXTERNAL R_{TIA}

To use an external R_{TIA} gain resistor, follow this process:

- Connect external R_{TIA} gain resistor across the RC0_0 and RC0_1 pins.
- Clear LPTIACON0 [9:5] = 00000b to disconnect the internal R_{TIA} resistor from the TIA output terminal.
- Close the SW9 switch by setting LPTIASW0 [9] = 1. When using the internal R_{TIA}, open SW9.
- An external capacitor should also be connected in parallel with an external R_{TIA} to maintain loop stability. The recommended value of this external capacitor is 100 nF.

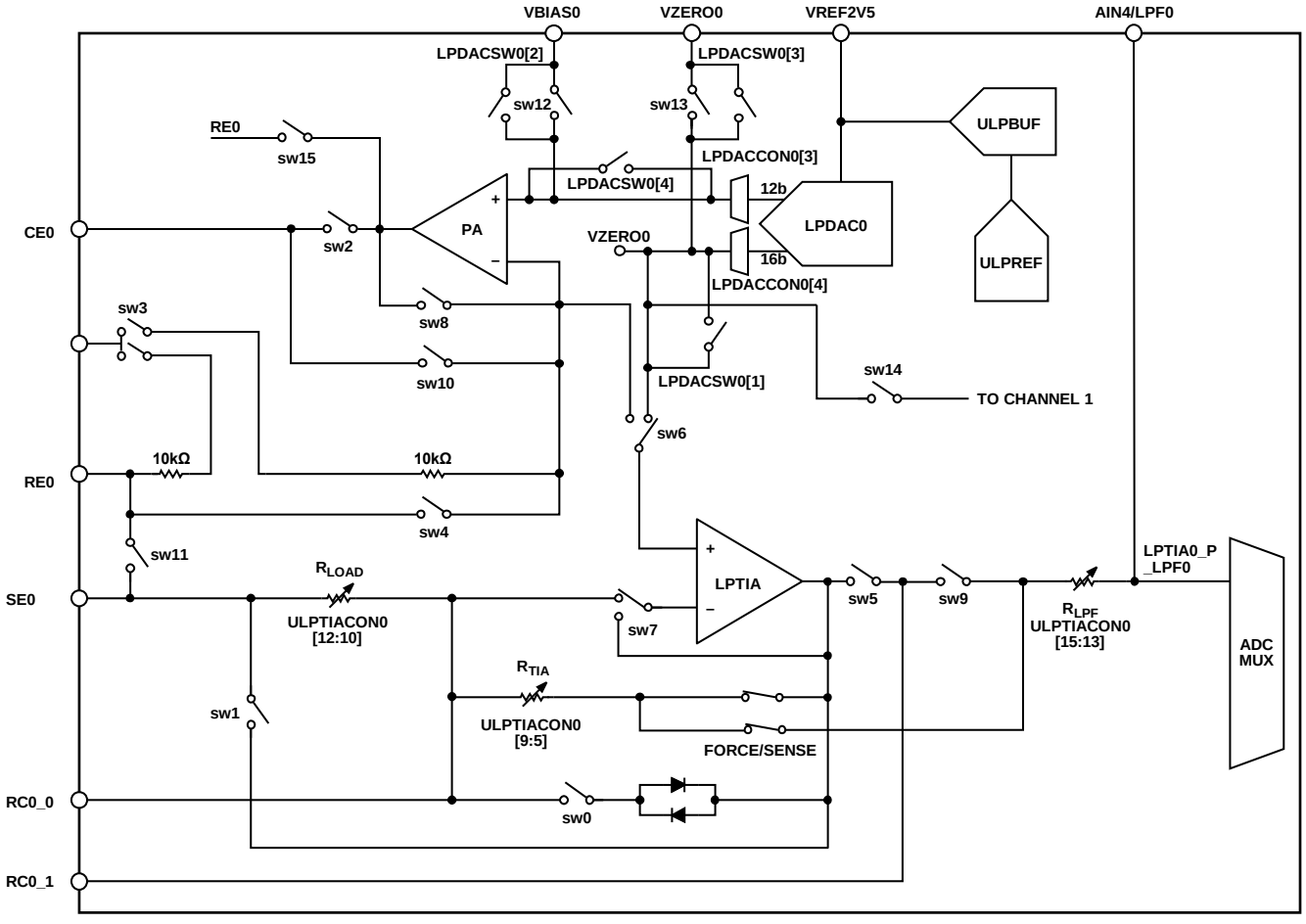

Figure 19. Low Bandwidth Loop Switches

LOW POWER TIA CIRCUITS REGISTERS

Table 19. Low Power TIA and DAC Registers Summary

Address	Name	Description	Reset	Access
0x000020E4	LPTIASW0	Low power TIA switch configuration	0x00000000	R/W
0x000020EC	LPTIACON0	Low power TIA control bits	0x00000003	R/W

Low Power TIA Switch Configuration Register—LPTIASW0

Address: 0x000020E4, Reset: 0x00000000, Name: LPTIASW0

Table 20. Bit Descriptions for LPTIASW0

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
15	RECAL		TIA SW15 control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
14	Reserved		Reserved.	0x0	R/W
13	SW13		SW13 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		

Bits	Bit Name	Settings	Description	Reset	Access
12	SW12		SW12 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
11	SW11		SW11 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
10	SW10		SW10 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
9	SW9		SW9 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
8	SW8		SW8 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
7	SW7		SW7 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
6	SW6		SW6 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
5	SW5		SW5 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
4	SW4		SW4 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
3	SW3		SW3 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
2	SW2		SW2 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
1	SW1		SW1 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		
0	SW0		SW0 switch control, active high.	0x0	R/W
		0	Opens switch.		
		1	Closes switch.		

Low Power TIA Control Bits, Channel 0 Register—LPTIACON0

Address: 0x000020EC, Reset: 0x00000003, Name: LPTIACON0

Table 21. Bit Descriptions for LPTIACON0

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:13]	TIARF		These bits set the low-pass filter resistor and configure the TIA output low-pass filter cutoff frequency.	0x0	R/W
		0	Disconnects the TIA output from the low-pass filter pin (LPF0), which is useful for diagnostics where a fast response is required from the ADC. This setting disconnects the LPTIA output from the low-pass filter capacitor.		
		1	Bypass resistor; 0 Ω option.		
		10	20 kΩ.		

Bits	Bit Name	Settings	Description	Reset	Access
		11	100 kΩ.		
		100	200 kΩ.		
		101	400 kΩ.		
		110	600 kΩ.		
		111	1 MΩ; recommended value for best dc current measurement performance. This setting is the lowest cutoff frequency setting for the low-pass filter.		
[12:10]	TIARL		These bits set R_{LOAD}.	0x0	R/W
		0	0 Ω.		
		1	10 Ω.		
		10	30 Ω.		
		11	50 Ω.		
		100	100 Ω.		
		101	1.6 kΩ; TIA gain resistor must be ≥ 2 kΩ.		
		110	3.1 kΩ; TIA gain resistor must be ≥ 4 kΩ.		
		111	3.6 kΩ; TIA gain resistor must be ≥ 4 kΩ.		
[9:5]	TIAGAIN		These bits set R_{TIA}.	0x0	R/W
		0	Disconnects the TIA gain resistor.		
		1	200 Ω. The TIA gain resistor is combination of R_{LOAD} and a fixed series 110 Ω. Assumes R_{LOAD} = 10 Ω. Set by TIARL. $R_{TIAGAIN}$ section = 100 Ω − R_{LOAD} + 110 Ω. The fixed overall TIA gain = 200.		
		10	1 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 1 kΩ. If R_{LOAD} >100 Ω, $R_{TIAGAIN}$ = 1 kΩ − (R_{LOAD} − 100 Ω).		
		11	2 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 2 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 2 kΩ − (R_{LOAD} − 100 Ω).		
		100	3 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 3 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 3 kΩ − (R_{LOAD} − 100 Ω).		
		101	4 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 4 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 4 kΩ − (R_{LOAD} − 100 Ω).		
		110	6 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 6 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 6 kΩ − (R_{LOAD} − 100 Ω).		
		111	8 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 8 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 8 kΩ − (R_{LOAD} − 100 Ω).		
		1000	10 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 10 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 10 kΩ − (R_{LOAD} − 100 Ω).		
		1001	12 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 12 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 12 kΩ − (R_{LOAD} − 100 Ω).		
		1010	16 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 16 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 16 kΩ − (R_{LOAD} − 100 Ω).		
		1011	20 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 20 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 20 kΩ − (R_{LOAD} − 100 Ω).		
		1100	24 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 24 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 24 kΩ − (R_{LOAD} − 100 Ω).		
		1101	30 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 30 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 30 kΩ − (R_{LOAD} − 100 Ω).		
		1110	32 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 32 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 32 kΩ − (R_{LOAD} − 100 Ω).		
		1111	40 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 40 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 40 kΩ − (R_{LOAD} − 100 Ω).		
		10000	48 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 48 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 48 kΩ − (R_{LOAD} − 100 Ω).		
		10001	64 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 64 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 64 kΩ − (R_{LOAD} − 100 Ω).		
		10010	85 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 85 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 85 kΩ − (R_{LOAD} − 100 Ω).		
		10011	96 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 96 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 96 kΩ − (R_{LOAD} − 100 Ω).		

Bits	Bit Name	Settings	Description	Reset	Access
		10100	100 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 100 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 100 kΩ − (R_{LOAD} − 100 Ω)		
		10101	120 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 120 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 120 kΩ − (R_{LOAD} − 100 Ω)		
		10110	128 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 128 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 128 kΩ − (R_{LOAD} − 100 Ω)		
		10111	160 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 160 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 160 kΩ − (R_{LOAD} − 100 Ω)		
		11000	196 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 196 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 196 kΩ − (R_{LOAD} − 100 Ω)		
		11001	256 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 256 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 256 kΩ − (R_{LOAD} − 100 Ω)		
		11010	512 kΩ. If R_{LOAD} ≤ 100 Ω, $R_{TIAGAIN}$ = (100 Ω − R_{LOAD}) + 512 kΩ. If R_{LOAD} >100 Ω. $R_{TIAGAIN}$ = 512 kΩ − (R_{LOAD} − 100 Ω)		
[4:3]	IBOOST		Current boost control.	0x0	R/W
		00	Normal mode.		
		01	Increase amplifier output stage current to quickly charge external capacitor load. This setting is intended for use with high current sensors.		
		10	Double TIA and PA overall quiescent current; increases amplifier bandwidth. This setting is useful for diagnostic tests.		
		11	Double TIA and PA overall quiescent current and increase output stage current. This setting increases amplifier bandwidth and output current capability.		
2	HALFPWR		Half power mode select. This control bit reduces the active power consumption of the TIA and potentiostat amplifiers for Sensor Channel 0.	0x0	R/W
		0	Normal mode (default).		
		1	Reduces PA and TIA current by half.		
1	PAPDEN		PA power-down. Low Power Potentiostat Amplifier 0 power-down control bit.	0x1	R/W
		0	Power up.		
		1	Power down.		
0	TIAPDEN		TIA power-down. Low Power TIA0 power-down control bit.	0x1	R/W
		0	Power up.		
		1	Power down.		

HIGH SPEED DAC CIRCUITS

The 12-bit high speed DAC generates an ac excitation signal when measuring the impedance of an external sensor. Control the DAC output signal directly by writing to a data register or by using the automated waveform generator block. The high speed DAC signal is fed to an excitation amplifier designed specifically to couple the ac signal on top of the normal dc
bias voltage of a sensor.

HIGH SPEED DAC OUTPUT SIGNAL GENERATION

There are two ways of setting the output voltage of the high speed DAC:

- A direct write to the DAC code register, WGDACCODE. This is a 12-bit register where the most significant bit (MSB) is a sign bit. Writing 0x800 results in a 0 V output. Writing 0x200 results in negative full scale, and writing 0xE00 results in positive full scale.
- Use the automatic waveform generator. The waveform generator can be programmed to generate fixed frequency, fixed amplitude signals including, sine, trapezoid and square wave signals. If the user selects the sine wave, options exist to adjust the offset and phase of the output signal.

POWER MODES OF THE HIGH SPEED DAC CORE

The reference source of the high speed DAC is an internal 1.82V precision reference voltage. There are three basic modes of operation for the high speed DAC that trade off between power consumption vs. output speed: low power mode and high power mode. The high speed DAC can also be placed into hibernate mode when inactive. The following sections describes these modes.

Low Power Mode

Low power mode is used when the high speed DAC output signal frequency is less than 80 kHz. Note these steps when configuring the HSDAC for low power mode:

- Clear PMBW [0] = 0.
- In this mode, the system clock to the DAC and the ADC is 16 MHz.
- Ensure CLKSEL [SYSCLK] selects a 16 MHz clock source. For example, internal high speed oscillator is CLKSEL[SYSCLK] = 00. Ensure the system clock divide ratio is 1 (CLKCON0 [5:0] = 0 or 1).
- If the internal high speed oscillator is selected as the system clock source, ensure the 16 MHz option is selected. Set HPOSCCON[2] = 1.

High Power Mode

High power mode increases the bandwidth supported by the high speed DAC amplifiers. Use high power mode when the high speed DAC frequency is greater than 80 kHz. To enter high power mode, a number of register writes are required. Note these steps when configuring the HS DAC for high power mode:

- Set PMBW[0] = 1. Power consumption is increased, but the output signal bandwidth increases to a maximum of 200 kHz.
- In this mode, the system clock to the DAC and the ADC is 32 MHz.
- Ensure CLKSEL [SYSCLKSEL] selects a 32 MHz clock source. For example, internal high speed oscillator is CLKSEL[1:0] (SYSCLKSEL) = 00. Ensure the system clock divide ratio is 1. CLKCON0[5:0] = 0 or 1.
- If the internal high speed oscillator is selected as the system clock source, ensure the 32 MHz option is selected. Clear HPOSCCON[2] = 0.

Hibernate Mode

When the AD5940 enters hibernate mode, the clocks to the high speed DAC circuits are clock gated to save power. When in active mode and the high speed DAC is not in use, disable the clocks to save power.

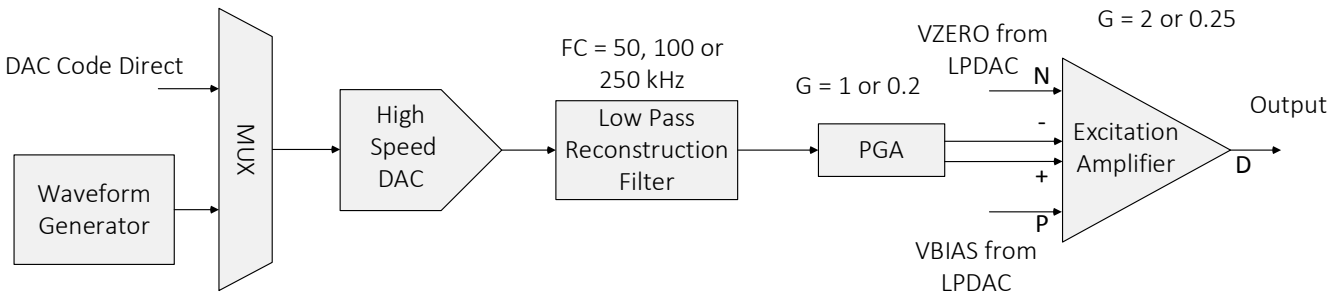

Figure 20. High Speed DAC Block

HIGH SPEED DAC FILTER OPTIONS

The output stage of the high speed DAC features a configurable reconstruction filter. Depending on the output signal frequency of the DAC, it is important that this filter is configured correctly.

Bits[3:2] in the PMBW register configure the 3 dB cutoff frequency of the reconstruction filter. Ensure that the cutoff frequency is higher than the required DAC output frequency:

- PMBW, Bits[3:2] = 01b for optimal performance if the DAC update rate is <50 kHz.
- PMBW, Bits[3:2] = 10b for optimal performance if the DAC update rate is <100 kHz.
- PMBW, Bits[3:2] = 11b for optimal performance if the DAC update rate is up to 200 kHz.

HIGH SPEED DAC OUTPUT ATTENUATION OPTIONS

Scaling options to the high speed DAC output exist to modify the output signal amplitude to the sensor. The output of the 12-bit DAC string before any attenuation or gain is ±300 mV. At the DAC output, there is a ×1 or ×0.2 gain stage. At the PGA stage, there are ×2 or ×0.25 gain options. Table 23 shows the available gain options and the corresponding output voltage ranges.

HIGH SPEED DAC EXCITATION AMPLIFIER

Figure 23 shows how the excitation amplifier works and its connection to the switch matrix. There are four inputs to the excitation amplifier: DACP, DACN, P, and N. The high speed DAC is a differential output DAC where the positive and negative inputs feed directly to the excitation amplifier. The voltage difference between these two outputs sets the peak-to-peak voltage on the output waveform. The P and N inputs serve two purposes: they maintain the stability of the excitation amplifier by providing a feedback path from the sensor, and they set the common mode for the high speed DAC output. Under normal circumstances, the common mode is set by the V_{ZERO} output connected to the N input. There is also an option to apply a dc bias voltage to the sensor and couple an ac signal onto this bias as in Figure 24. This is described in the next paragraph.

However, there is an option available if the sensor requires a bias voltage between the counter and sense electrode. V_{BIAS} sets the voltage on the counter electrode (the common-mode voltage of the high speed DAC) and V_{ZERO} sets the voltage on the sense electrode. V_{ZERO} must be connected to the positive terminal on the high speed TIA (HSTIACON, Bits[1:0] = 0x1) The DAC dc buffers must also be enabled by setting AFECON, Bit 21. With this configuration, a waveform, such as what is shown in Figure 24, can be achieved. The bias across the sensor is effectively the difference between V_{BIAS} and V_{ZERO}.

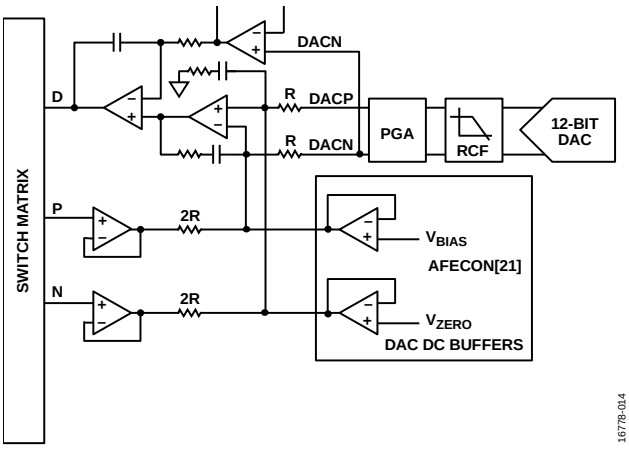

Figure 21. High Speed DAC Excitation Amplifier

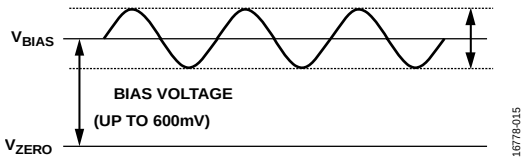

Figure 22. Sensor Excitation Signal

HOW TO COUPLE AN AC SIGNAL FROM THE HIGH SPEED DAC TO THE DC LEVEL SET BY THE LOW POWER DAC

The AD5940 contains a low power potentiostat channel to configure an electrochemical sensor. In normal operation, the bias voltage of the sensor between the RE0 and SE0 electrodes is set by the low power DAC outputs, V_{BIAS} and V_{ZERO} where V_{BIAS0} sets the bias to the potentiostat amplifier and ultimately the voltage on CE0. V_{ZERO0} sets the bias voltage on the LPTIA and hence SE0. The high speed DAC circuit is not used. However, for ac impedance measurements the output of the excitation amplifier must be connected to CE0. The potentiostat amplifier must be disconnected so the entire signal comes from the excitation amplifier output. The HSTIA is connected to the SE0 pin and the LPTIA is disconnected. The sensor bias must then

be set by HSTIA and the excitation amplifier. This is achieved by the following:

- The LPDAC's V_{ZERO} output must be connected to the. HSTIA non-inverting input (HSTIACON [1:0] = 0x1). This will set the voltage on SE0 (or whatever pin is connected to the HSTIA inverting input via the switch matrix).
- The DAC DC buffers must be enabled, AFECON [21] = 1. Figure 23 shows how the DC buffers are connected to the excitation amplifier. These buffers enable the LPDAC outputs to drive the required bias voltage to the excitation amplifier and HSTIA.
- The DC bias is then the difference between V_{BIAS0} and V_{ZERO0}.

AVOIDING INCOHERENCY ERRORS BETWEEN EXCITATION AND MEASUREMENT FREQUENCIES DURING IMPEDANCE MEASUREMENTS

The following settings are recommended to avoid incoherency errors between excitation and measurement frequencies during impedance measurements:

- The Hanningwindow is always on (DFTCON, Bit 0 = 1).
- In low power mode, the high speed DAC update rate is 16 MHz/27 MHz (DACCON, Bits[8:1] = 0x1B). In high power mode, the high speed DAC update rate is 32 MHz/7 MHz (DACCON, Bits[8:1] = 0x7).
- In low power mode, the ADC sampling rate is 800 kSPS (high frequency oscillator = 16 MHz). In high power mode, the ADC sampling rate is 1.6 MSPS (high frequency oscillator = 32 MHz).

Disabling the Hanning window may result in degraded performance.

HIGH SPEED DAC CALIBRATION OPTIONS

The high speed DAC is not calibrated during production testing by Analog Devices. This section describes the steps to calibrate the high speed DAC for all gain settings and in both high power and low power modes.

Calibrate the high speed DAC if it is intended to generate an excitation signal to a sensor. If an offset error exists on the excitation signal, and a current or voltage output is to be measured, the excitation signal may exceed the headroom of the selected TIA or ADC input buffer/PGA setting.

Figure 26 shows the circuit diagram for high speed DAC calibration. A precision external resistor is required between the RCAL0 pin and the RCAL1 pin. To calibrate the offset, the differential voltage measured across R_{CAL} must be 0 V.

Calibrate the high speed DAC with the required bit settings (DACCON, Bit 12 and Bit 0). For example, if the DAC is calibrated with DACCON, Bit 12 and Bit 0 = 0, and the user changes DACCON, Bit 12 to 1, an offset error is introduced if either the DACOFFSET register or DACOFFSETHS registers is recalibrated for the new output range.

The gain calibration is optional and adjusts the peak-to-peak voltage swing. Alternatively, adjust the voltage swing by changing the maximum/minimum DAC code.

The high speed DAC transfer function is shown in Figure 25. Figure 26 shows how the common-mode voltage is set by the noninverting input of the HSTIA. This voltage must be set by the low power DAC V_{ZERO} output or by the internal 1.11 V ADC VBIAS voltage.

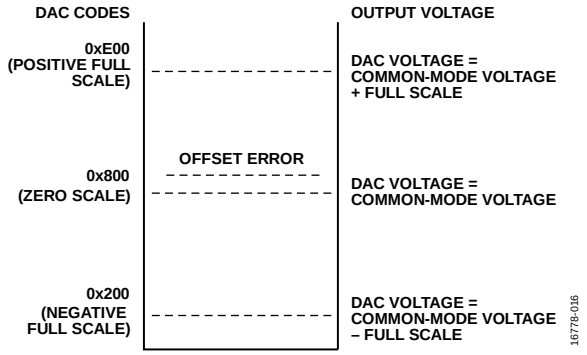

Figure 23. High Speed DAC Transfer Function

The AD5940 Software Development Kit includes sample functions that demonstrate how to use the ADC to measure the differential voltage across R_{CAL} resistor and how to adjust the appropriate calibration register until the differential voltage is ~0 V.

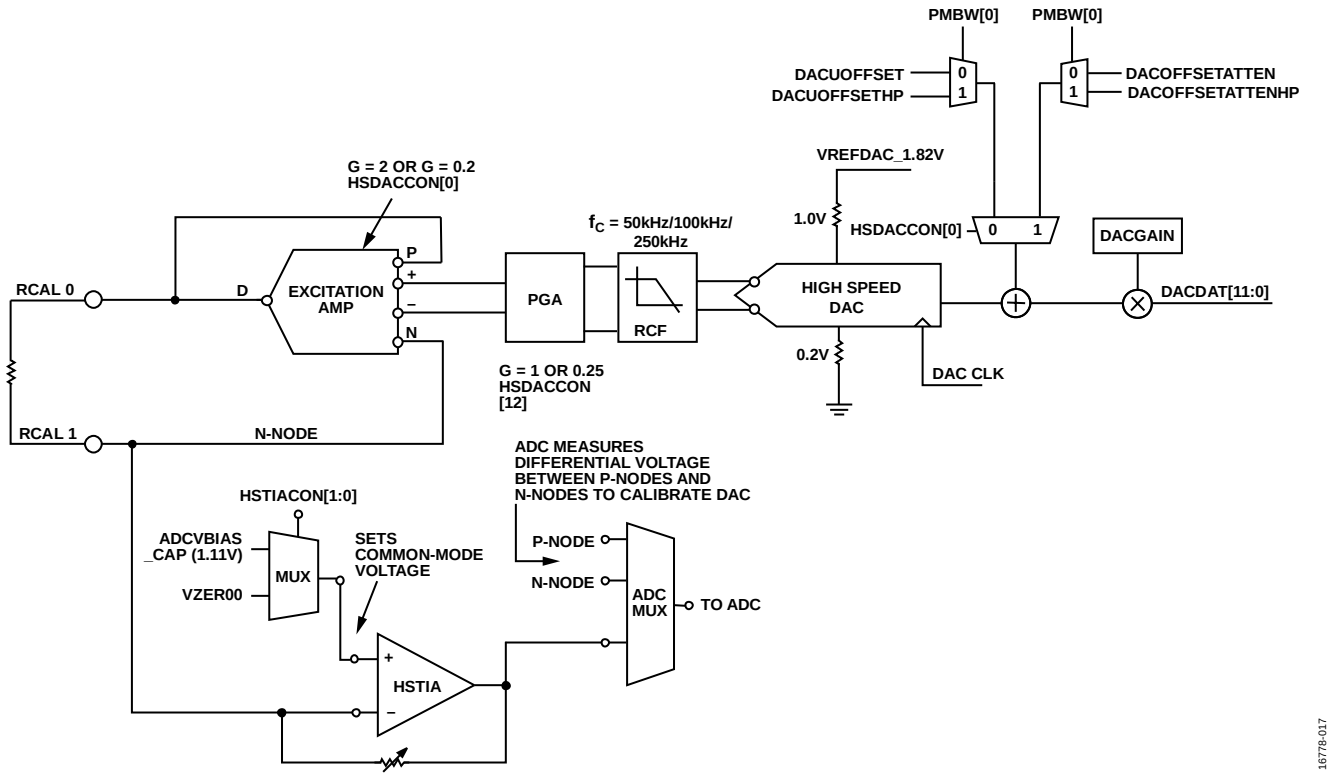

Figure 24. High Speed DAC Calibration

Table 22. High Speed DAC Calibration Register Assignment

DACCON Bit Settings	Typical Output Range (mV), Code 0x200 to Code 0xE00	Relevant Calibration Registers		
		Low Power Mode	High Speed Mode	Low Power Mode and High Speed Mode
Bit 12 = 0 and Bit 0 = 0	±607	DACOFFSET	DACOFFSETHS	DACGAIN
Bit 12 = 1 and Bit 0 = 0	±75	DACOFFSET	DACOFFSETHS	DACGAIN
Bit 12 = 1 and Bit 0 = 1	±15.14	DACOFFSETATTEN	DACOFFSETATTENHS	DACGAIN
Bit 12 = 0 and Bit 0 = 1	±121.2	DACOFFSETATTEN	DACOFFSETATTENHS	DACGAIN

HIGH SPEED DAC CIRCUIT REGISTERS

Table 23. High Speed DAC Control Register Summary

Address	Name	Description	Reset	Access
0x00002000	AFECON	AFE configuration	0x00080000	R/W
0x00002010	HSDACCON	High speed DAC configuration	0x0000001E	R/W
0x00002048	HSDACDAT	Direct write to DAC output control value	0x00000800	R/W

Table 24. High Speed DAC Calibration Register Summary

Address	Name	Description	Reset	Access
0x00002230	CALDATLOCK	Calibration data lock register	0x00000000	R/W
0x00002260	DACGAIN	DAC gain	0x00000800	R/W
0x00002264	DACOFFSETATTEN	DAC offset with attenuator enabled (low power mode)	0x00000000	R/W
0x00002268	DACOFFSET	DAC offset with attenuator disabled (low power mode)	0x00000000	R/W
0x000022B8	DACOFFSETATTENHS	DAC offset with attenuator enabled (high speed mode)	0x00000000	R/W
0x000022BC	DACOFFSETHS	DAC offset with attenuator disabled (high speed mode)	0x00000000	R/W

High Speed DAC Configuration Register—HSDACCON

Address: 0x00002010, Reset: 0x0000001E, Name: HSDACCON

Table 25. Bit Descriptions for HSDACCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:13]	Reserved		Reserved.	0x0	R
12	INAMPGNMDE		Excitation amplifier gain control. This bit selects the gain of the excitation amplifier.	0x0	R/W
		0	Gain = 2.		
		1	Gain = 0.25.		
[11:9]	Reserved		Reserved.	0x0	R/W
[8:1]	Rate		DAC update rate. The DAC update rate = ACLK/DACCON, Bits[8:1]. ACLK can be a high speed 16 MHz/32 MHz oscillator or a low power 32 kHz oscillator.	0xF	R/W
0	ATTENEN		PGA stage gain attenuation. Enable the PGA attenuator at the output of the DAC.	0x0	R/W
		0	DAC attenuator disabled. Gain of 1 mode.		
		1	DAC attenuator enabled. Gain of 0.2x mode.		

High Speed DAC Code Register—HSDACDAT

Address: 0x00002048, Reset: 0x00000800, Name: HSDACDAT

Table 26. Bit Descriptions for HSDACDAT

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:0]	DACDAT		DAC code, written directly to the DAC. The minimum code is 0x200 and the maximum code is 0xE00. Midscale (0x800) corresponds to an output voltage of 0 V.	0x800	R/W

Calibration Data Lock Register—CALDATLOCK

Address: 0x00002230, Reset: 0x00000000, Name: CALDATLOCK

Table 27. Bit Descriptions for CALDATLOCK

Bits	Bit Name	Settings	Description	Reset	Access
[31:0]	Key		Password for the calibration data registers. This password prevents the overwriting of data after the calibration phase.	0x0	R/W
		0xDE87A5AF	Write this value to unlock the calibration registers.		

DAC GAIN REGISTER

Address: 0x00002260, Reset: 0x00000800, Name: DACGAIN

Protected by CALDATLOCK. Valid for all settings of HSDACCON [12] and HSDACCON[0].

Table 28. Bit Descriptions for DACGAIN

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:0]	VALUE		HP DAC Gain Correction Factor. Unsigned number.	0x800	R/W
		0x000	Maximum negative gain adjustment occurs.		
		0x800	No gain adjustment.		
		0xFFF	Maximum positive gain adjustment occurs.		

DAC Offset with Attenuator Enabled (Low Power Mode) Register—DACOFFSETATTEN

Address: 0x00002264, Reset: 0x00000000, Name: DACOFFSETATTEN

The LSB adjustment is typically 4.9 µV for HSDACCON [12] = 1 and HSDACCON[0] = 1. The LSB adjustment is typically 24.7 µV for HSDACCON [12] = 1 and HSDACCON [0] = 0.

Table 29. Bit Descriptions for DACOFFSETATTEN

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:0]	Value		DAC offset correction factor. This value is a signed number represented in twos complement format with 0.5 LSB precision. Used when attenuator is enabled.	0x0	R/W
		0x7FF	$2^{10-0.5}$. Maximum positive adjustment that results in a positive full-scale/2 – 0.5 LSB adjustment.		
		0x001	+0.5, results in a +0.5 LSB adjustment.		
		0x000	0, no offset adjustment.		
		0xFFF	−0.5, results in a −0.5 LSB adjustment.		
		0x800	-2^{10}, maximum negative adjustment that results in negative full-scale/2 adjustment.		

DAC Offset with Attenuator Disabled (Low Power Mode Register)—DACOFFSET

Address: 0x00002268, Reset: 0x00000000, Name: DACOFFSET

The LSB adjustment is typically 197.7 µV for HSDACCON [12] = 0 and HSDACCON [0] = 0. The LSB adjustment is typically 39.5 µV for HSDACCON [12] = 0 and HSDACCON [0] = 1.

Table 30. Bit Descriptions for DACOFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:0]	Value		DAC offset correction factor. This value is a signed number represented in twos complement format with 0.5 LSB precision. Used when attenuator is disabled.	0x0	R/W
		0x7FF	$2^{10-0.5}$. Maximum positive adjustment that results in a positive full-scale/2 – 0.5 LSB adjustment.		
		0x001	+0.5, results in a +0.5 LSB adjustment.		
		0x000	0, no offset adjustment.		
		0xFFF	−0.5, results in a −0.5 LSB adjustment.		
		0x800	-2^{10}, maximum negative adjustment that results in negative full-scale/2 adjustment.		

DAC Offset with Attenuator Enabled (High Speed Mode Register)—DACOFFSETATTENHS

Address: 0x000022B8, Reset: 0x00000000, Name: DACOFFSETATTENHS

Protected by CALDATLOCK. The LSB adjustment is typically 4.9 µV for HSDACCON [12] = 1 and HSDACCON [0] = 1. The LSB adjustment is typically 24.7 µV for HSDACCON [12] = 1 and HSDACCON [0] = 0.

Table 31. Bit Descriptions for DACOFFSETATTENHS

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:0]	Value		DAC offset correction factor. This value is a signed number represented in twos complement format with 0.5 LSB precision. Used when attenuator is enabled.	0x0	R/W
		0x7FF	$2^{10-0.5}$. Maximum positive adjustment that results in a positive full-scale/2 – 0.5 LSB adjustment.		
		0x001	+0.5, results in a +0.5 LSB adjustment.		
		0x000	0, no offset adjustment.		
		0xFFF	−0.5, results in a −0.5 LSB adjustment.		
		0x800	-2^{10}, maximum negative adjustment that results in negative full-scale/2 adjustment.		

DAC Offset with Attenuator Disabled (High Speed Mode Register)—DACOFFSETHS

Address: 0x000022BC, Reset: 0x00000000, Name: DACOFFSETHS

Protected by CALDATLOCK. The LSB adjustment is typically 197.7 µV for HSDACCON [12] = 0 and HSDACCON[0] = 0. The LSB adjustment is typically 39.5 µV for HSDACCON [12] = 0 and HSDACCON[0] = 1.

Table 32. Bit Descriptions for DACOFFSETHS

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:0]	Value		DAC offset correction factor. This value is a signed number represented in twos complement format with 0.5 LSB precision. Used when attenuator is disabled.	0x0	R/W
		0x7FF	$2^{10-0.5}$. Maximum positive adjustment that results in a positive full-scale/2 − 0.5 LSB adjustment.		
		0x001	+0.5, results in a +0.5 LSB adjustment.		
		0x000	0, no offset adjustment.		
		0xFFF	−0.5, results in a −0.5 LSB adjustment.		
		0x800	-2^{10}, maximum negative adjustment that results in negative full-scale/2 adjustment.		

HIGH SPEED TIA CIRCUITS

The high speed TIA measures wide bandwidth input signals up to 200 kHz.

The output of the high speed TIA is connected to the main ADC mux, where it can be programmed as the ADC input channel.

This block is designed for impedance measurements in conjunction with the high speed DAC and excitation amplifier.

HIGH SPEED TIA CONFIGURATION

The high speed TIA is disabled by default and is turned on by setting AFECON [11] = 1. The high speed TIA has programmable flexibility built in to the input signal selection, gain resistor selection, input load resistor selection, and common-mode voltage source.

Input Signal Selection

The input signal options are as follows:

- The SE0 input pin.
- The AIN0, AIN1, AIN2, and AIN3/BUF_VREF1V8 input pins.
- The DE0 input pin, which has its own R_{LOAD}/R_{TIA} options and is user programmable.

Gain Resistor Selection

The gain resistor (R_{TIA}) options are 50 Ω to 160 kΩ for the DE0 input, and 200 Ω to 160 kΩ for all other input pins.

Load Resistor Selection

The load resistor, R_{LOAD}, options are as follows:

- R_{LOAD02} and R_{LOAD04} are fixed 100 Ω for SE0 and AFE3.
- For DE0, R_{LOAD} is programmable. The user can select values from 0 Ω, 10 Ω, 30 Ω, 50 Ω, and 100 Ω.

Common-Mode Voltage Selection

The high speed TIA common-mode voltage setting, on the positive input to the high speed TIA amplifier, is configurable. The options are as follows:

- Internal 1.11 V reference source, which is the same as the VBIAS_CAP pin voltage.
- Low power DAC output (V_{ZERO0}).

Figure 27 shows the high speed TIA connections to the switch matrix and external pins. Note also the extra load and gain resistors, DE0RLOAD and DE0RTIA, available on DE0 pin.

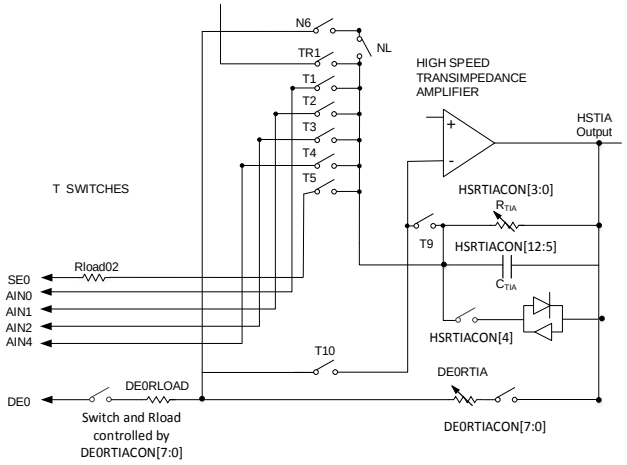

Figure 25. High Speed TIA Switches

Table 33. High Speed TIA Resistor Options on the DE0 Input

DE0RESCON[7:0]	RLOAD03 (Ω)	RTIA03 (Ω)
0x00	0	50 Ω
0x18	0	100 Ω
0x38	0	200 Ω
0x58	0	1.1 kΩ
0x60	0	5.1 kΩ
0x68	0	10.1 kΩ
0x70	0	20.1 kΩ
0x78	0	40.1 kΩ
0x80	0	80.1 kΩ
0x88	0	160.1 kΩ
0x9	10	50 Ω
0x21	10	100 Ω
0x39	10	190 Ω
0x59	10	1.09 kΩ
0x61	10	5.09 kΩ
0x69	10	10.09 kΩ
0x71	10	20.09 kΩ
0x79	10	40.09 kΩ
0x81	10	80.09 kΩ
0x89	10	160.09 kΩ
0x12	30	50 Ω
0x2A	30	100 Ω
0x4A	30	210 Ω
0x5A	30	1.07 kΩ
0x62	30	5.07 kΩ
0x6A	30	10.07 kΩ
0x72	30	20.07 kΩ
0x7A	30	40.07 kΩ
0x82	30	80.07 kΩ
0x8A	30	160.07 kΩ
0x1B	50	50 Ω
0x33	50	100 Ω
0x4B	50	190 Ω
0x5B	50	1.05 kΩ
0x63	50	5.05 kΩ
0x6B	50	10.05 kΩ
0x73	50	20.05 kΩ
0x7B	50	40.05 kΩ
0x83	50	80.05 kΩ
0x8B	50	160.05 kΩ
0x34	100	50 Ω
0x3C	100	100 Ω
0x54	100	200 Ω
0x5C	100	1 kΩ
0x64	100	5 kΩ
0x6C	100	10 kΩ
0x74	100	20 kΩ
0x7C	100	40 kΩ
0x84	100	80 kΩ
0x8C	100	160 kΩ

External R_{TIA} Selection

The high speed TIA has the option of selecting an external gain resistor instead of the internal R_{TIA} gain option. To do perform this selection, connect one end of the resistor to the DE0 pin and connect the other end to AIN0, AIN1, AIN2, or AIN3_BUF_VREF1V8. DE0 must be connected to the output of the high speed TIA.

To use DE0 for external R_{TIA} set the following register values:

- DE0RESCON = 0x97.
- HSRTIACON, Bits[3:0] = 0xF.

AIN0, AIN1, AIN2, or AIN3_BUF_VREF1V8 (whichever pin the resistor is connected to) must be connected to the inverting input of the high speed TIA (see the Programmable Switch Matrix section).

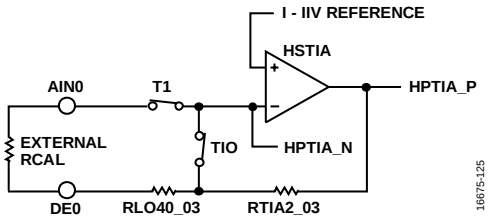

Figure 26: Connecting External Gain Resistor to HSTIA

HIGH SPEED TIA CIRCUIT REGISTERS

Table 34. High Speed TIA Register Summary

Address	Name	Description	Reset	Access
0x000020F0	HSRTIACON	High speed R_{TIA} configuration	0x0000000F	R/W
0x000020F8	DE0RESCON	DE0 HSTIA resistors configuration	0x000000FF	R/W
0x000020FC	HSTIACON	HSTIA amplifier configuration	0x00000000	R/W

High Speed R_{TIA} Configuration Register—HSRTIACON

Address: 0x000020F0, Reset: 0x0000000F, Name: HSRTIACON

This register controls the high speed TIA gain resistor, current protection diode, and feedback capacitor

Table 35. Bit Descriptions for HSRTIACON

Bits	Bit Name	Settings	Description	Reset	Access
[31:13]	Reserved		Reserved.	0x0	R
[12:5]	CTIACON		Configure capacitor in parallel with R_{TIA}. This capacitor stabilizes the amplifier loop. When this bit is set, the capacitor is added in parallel with the R_{TIA}.	0x0	R/W
		0	1 pF.		
		1	2 pF.		
		10	4 pF.		
		100	8 pF.		
		1000	16 pF.		
		10000	2 pF.		
		100000	Not used.		
		1000000	Not used.		
4	TIASW6CON		SW6 control. Use SW6 to select whether or not to use the diode in parallel with R_{TIA}.	0x0	R/W
		0	SW6 off, diode is not in parallel with R_{TIA}.		
		1	SW6 on, diode is in parallel with R_{TIA}.		
[3:0]	RTIACON		Configure general R_{TIA} value. To use this R_{TIA}, close Switch T9 and open Switch T10 (SWCON, Bits[18:17]).	0xF	R/W
		0000	R_{TIA} = 200 Ω.		
		0001	R_{TIA} = 1 kΩ.		
		0010	R_{TIA} = 5 kΩ.		
		0011	R_{TIA} = 10 kΩ.		
		0100	R_{TIA} = 20 kΩ.		
		0101	R_{TIA} = 40 kΩ.		
		0110	R_{TIA} = 80 kΩ.		
		0111	R_{TIA} = 160 kΩ.		
		1000 to 1111	R_{TIA} is open.		

DE0 High Speed TIA Resistors Configuration Register—DE0RTIACON

Address: 0x000020F8, Reset: 0x000000FF, Name: DE0RTIACON

Table 36. Bit Descriptions for DE0RTIACON

Bits	Bit Name	Settings	Description	Reset	Access
[31:8]	Reserved		Reserved.	0x0	R
[7:0]	DE0RCON		DE0 R_{LOAD} R_{TIA} setting. To use this R_{LOAD}/R_{TIA}, open Switch T9 and close Switch T10 and the R_{TIA} resistor values (see Table 34).	0xFF	R/W

High Speed TIA Configuration Register—HSTIACON

Address: 0x000020FC, Reset: 0x00000000, Name: HSTIACON

Table 37. Bit Descriptions for HSTIACON

Bits	Bit Name	Settings	Description	Reset	Access
[31:2]	Reserved		Reserved.	0x0	R
[1:0]	VBIASSEL		Select HSTIA positive input.	0x0	R/W
		00	ADCVBIAS_CAP. 1.11 V voltage source.		
		01	V_{ZERO} output from Low Power DAC0.		
		10	Reserved.		
		11	Reserved.		

HIGH PERFORMANCE ADC CIRCUIT

ADC CIRCUIT OVERVIEW

The AD5940 implements a 16-bit, 800 kSPS, multichannel SAR ADC. The ADC operates from a 2.8 V to 3.6 V power supply. The host microcontroller interfaces to the ADC via the sequencer or directly through the SPI interface.

An ultralow leakage switch matrix is used for sensor connection and can also be used to multiplex multiple electronic measurement devices to the same wearable electrodes.

The ADC uses a precision, low drift, factory calibrated 1.82 V reference. An external reference source can also be connected to the VREF_1V8 pin.

ADC conversions are triggered by writing directly to the ADC control register via the SPI interface, or by writing to the ADC control register via the sequencer.

ADC CIRCUIT DIAGRAM

Figure 29 shows the ADC core architecture. Figure 29 excludes input buffering, gain stages, and output post processing.

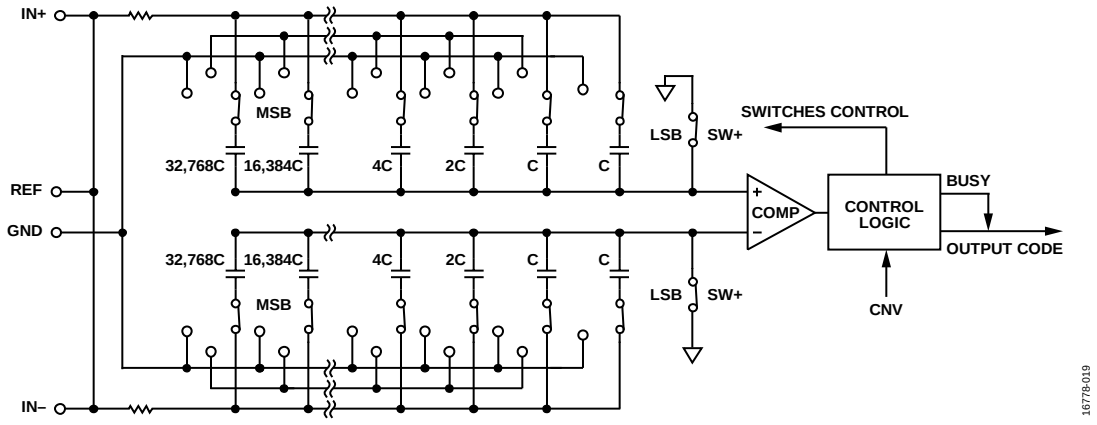

Figure 27: ADC Core Block Diagram

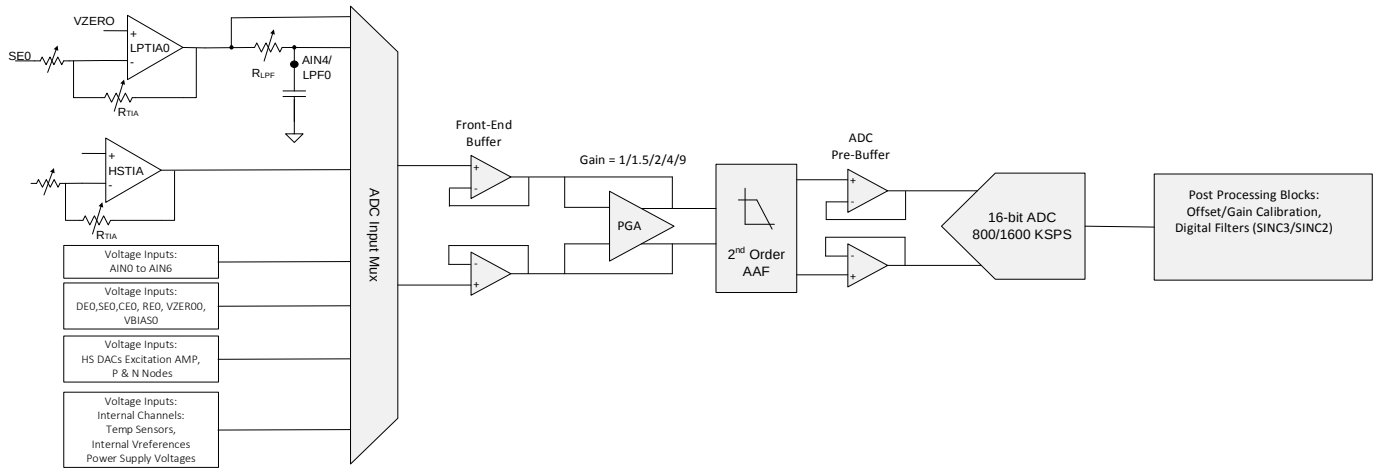

Figure 28. Basic Diagram of ADC Input Channel

ADC CIRCUIT FEATURES

An input multiplexer, located in front of the fast, multichannel, 16-bit ADC, enables the measurement of a number of external and internal channels. These channels include

- Two low power current measurement channels. These channels measure the low current outputs of the connected sensor through SE0 or DE0.
  - The current channels feed into a programmable load resistor.

    - There is one low power TIA (LPTIA). The LPTIA has its own programmable gain resistor to convert very small currents to a voltage signal that can be measured by the ADC.
        - The low power current channel can be configured to sample with or without a low-pass filter in place.
- One high speed current input channel for performing impedance measurements up to 200 kHz.
    - The high speed current channel has a dedicated HSTIA with a programmable gain resistor.
- Multiple external voltage inputs.
    - Six dedicated voltage input channels: AIN0, AIN1, AIN2, AIN3/BUF_VREF1V8, AIN4/LPF0, and AIN6.
    - The sensor electrode pins, SE0, DE0, RE0, and CE0, can also be measured as ADC voltage pins. Divide by 2 options are available on the CE0 pin.
- Internal ADC channels.
    - AVDD, DVDD, and AVDD_REG power supply measurement channels.
    - ADC, high speed DAC, and low power reference voltage sources.
    - Internal die temperature sensor.
    - Two low power DAC output voltages, V_{BIAS0} and V_{ZERO0}.
- ADC result post processing features.
    - Digital filters (sinc2 and sinc3) and 50 Hz/60 Hz power supply rejection. The sinc2 and sinc3 filters have programmable oversampling rates to allow the user to trade off conversion speed vs. noise performance.
    - Discrete Fourier transform (DFT), used with impedance measurements to automatically calculate magnitude and phase values.
    - Programmable averaging of ADC results to separate the sincx filters.
    - Programmable statistics option for calculating mean and variance automatically.
- Multiple calibration options to support system calibration of the current, voltage, and temperature channels.

The ADC input stage provides an input buffer to support low input current leakage specifications on all channels.

To support a range of current and voltage based input ranges, the ADC front end provides a PGA and TIA. The PGA supports gains of 1×, 1.5×, 2×, 4×, and 9×. The low power TIA supports programmable gain resistors ranging from 200 Ω to 512 kΩ. The high speed TIA used for impedance measurement supports programmable gain resistors ranging from 200 Ω to 160 kΩ.

By default, the reference source of the ADC is a precision, low drift, internal 1.82 V reference source. Optionally, an external reference can be connected to the VREF_1.82V pin and the AGND_REF pin.

The ADC supports averaging and digital filtering options. The user can trade off speed vs. precision by using these options. The highest ADC update rate is 800 kHz in normal mode and 1.6 MHz in high speed mode, with no digital filtering. The ADC filtering options also include a 50 Hz/60 Hz mains power supply filter; with this filter enabled, the ADC update rate is typically 900 Hz.

The ADC supports a number of post processing features, including a DFT engine intended for impedance measurements to remove the processing requirements from the host microcontroller. Minimum, maximum, and mean value detection is also supported.

ADC CIRCUIT OPERATION

The SAR ADC is based on a charge redistribution DAC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the two inputs of the comparator.

The ADC block operates from the 16 MHz clock in normal operation.; this ensures a maximum DAC update rate of 800 kSPS.

For high power mode, the 32 MHz oscillator must be selected as the ADC clock source. The ADC maximum update rate is 1.6 MSPS with higher power consumption, which is only required for impedance measurements in the >80 kHz range.

ADC TRANSFER FUNCTION

The transfer function in Figure 31 shows the ADC output codes on the y-axis vs. the differential voltage into the ADC.

In Figure 31, the ADC negative input channel is the 1.11 V voltage source.

The positive input channel is any voltage input to the ADC after the TIA/PGA and/or input buffer stages.

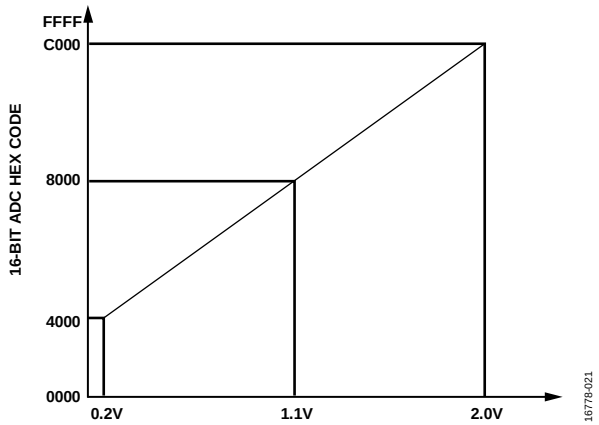

Figure 29. Ideal ADC Transfer Function—Voltage Input vs. Output

Codes

Calculate the input voltage, V_{IN}, with the following equation:

$$V_{IN} = \frac{V_{REF}}{PGA\_G} \times \left(\frac{ADCDAT - 0x8000}{2^{15}} \right) + VBIAS\_CAP$$

where:
V_{REF} = 1.835
PGA_G is the PGA gain and is selectable as 1, 1.5, 2, 4, or 9.
VBIAS_CAP is typically 1.11 V.

ADC LOW POWER CURRENT INPUT CHANNEL

Figure 32 shows the low power TIA input current channel. The ADC measures the output voltage of the low power TIA.

The positive inputs can be selected via ADCCON, Bits[5:0]. The negative input is nominally selected to be the 1.11 V reference source. Perform this selection by setting ADCCON, Bits[12:8] = 01000b for ADCVBIAS_CAP.

An optional programmable gain stage can be selected to amplify the positive voltage input. The instrumentation amplifier is enabled via AFECON, Bit 10. The gain setting is configured via ADCCON, Bits[18:16].

The output of the gain stage goes through an antialias filter (AAF). The cutoff frequency of the AAF is set by ADCCON, Bits[21:20] or PMBW, Bits[3:2]. Set the cutoff frequency to suit the input signal bandwidth.

The ADC output code is calibrated with an offset and gain correction factor. This digital adjustment factor happens automatically. The offset and gain correction register used depends on the ADC input channel selected. See Calibration section for more details.

See the Low Power TIA section for details on how to configure the R_{LOAD}, R_{TIA}, and R_{FILTER} resistor values. The LPTIA output has a low-pass filter consisting of R_{FILTER} and an external capacitor connected to the AIN4/LPF0 pin. R_{FILTER} is typically 1 MΩ and the external capacitor is recommended to be 1 µF, which provides a low cutoff frequency.

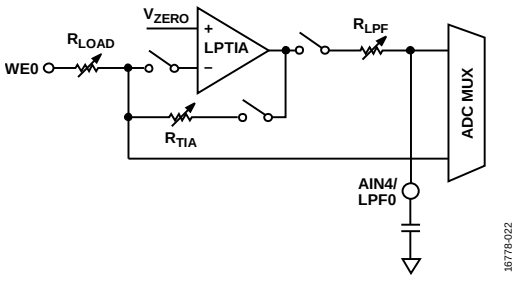

Figure 30. Low Power TIA Current Input Channel to the ADC

SELECTING INPUTS TO ADC MUX

For optimum ADC operation, the following are the recommended MUX inputs based on measurement type:

1. Voltage Measurement
   - MUXSEL_P = CE0, RE0, SE0, DE0, AINx
   - MUXSEL_N = VREF1V11
2. DC Current Measurement on LTPIA
   - MUXSEL_P = LPTIA0_LPF
   - MUXSEL_N =LPTIA0_N
3. AC or higher bandwidth current measurements on LPTIA
   - MUXSEL_P = LPTIA0_P
   - MUXSEL_N = LPTIA0_N
4. Current and Impedance Measurement on HSTIA
   - MUXSEL_P = HSTIA_P
   - MUXSEL_N = HSTIA_N

ADC POST PROCESSING

The AD5940 provides many digital filtering and averaging options to improve signal-to-noise performance and overall measurement accuracy. Figure 33 shows an overview of the post processing filter options.

The processing filter options include

- Digital filtering (sinc2/sinc3) and 50 Hz/60 Hz power supply rejection.
- DFT used with impedance measurements to automatically calculate magnitude
  and phase values
- Programmable averaging of ADC results.
- Programmable statistics option for calculating mean and variance automatically.

Sinc3 Filter

The input to the sinc3 filter is the raw ADC codes at a rate of 800 kHz (if the 16 MHz oscillator is selected) or 1.6 MHz (if the 32 MHz oscillator is selected). To enable the sinc3 filter, ensure that ADCFILTERCON, Bit 6 = 0. The filter decimation rate is programmable with options of 2, 4, or 5. It is recommended to use a decimation rate of 4.

The gain correction block is enabled by default and is not user programmable.

INTERNAL TEMPERATURE SENSOR CHANNEL

The AD5940 contains an internal temperature sensor channel.

The temperature sensor outputs a voltage proportional to the die temperature. This voltage is linear, relative to temperature.

For improved accuracy, the temperature sensor can be configured in chop mode via TEMPSENS, Bits[3:1]. If chopping is selected, the user must ensure an even number of ADC conversions take

place on the temperature sensor channel; these results must be averaged.

Dedicated calibration registers for the temperature sensor channel are also available, which the ADC uses automatically.

POWER SUPPLY REJECTION FILTER (50 HZ OR 60 HZ MAINS FILTER)

To enable the 50 or 60 notch filter for filtering mains noise, clear ADCFILTERCON [4] = 0 and set AFECON[16] = 1. The input is the sinc2 filter output. The input rate is dependent on the sinc3 and sinc2 settings. If selected, the power supply rejection filter output can be read via the SINC2DAT register. The following table shows the digital filter settings that support simultaneous 50/60Hz mains rejection.

Table 38: Digital filter settings to support simultaneous 50/60Hz mains rejection

ADCFILTERCON[13:8] Value	*Power Mode (PMBW[0])*	*SINC3 Oversampling setting*	*SINC2 Oversampling setting*	*Final ADC output update rate in samples per second*
010111_b	0 (LP Mode)	2	667	600 SPS
011011_b	0 (LP Mode)	2	1333	300SPS
011011_b	1 (HP Mode)	2	1333	600SPS

ADC CALIBRATION

Because of the multiple input types on the AD5940 (current, voltage, temperature, and so on), there are multiple offset and gain calibration options. A built in self calibration system is provided to aid the user when calibrating different ADC input channels. This is included in the AD5940 software development kit.

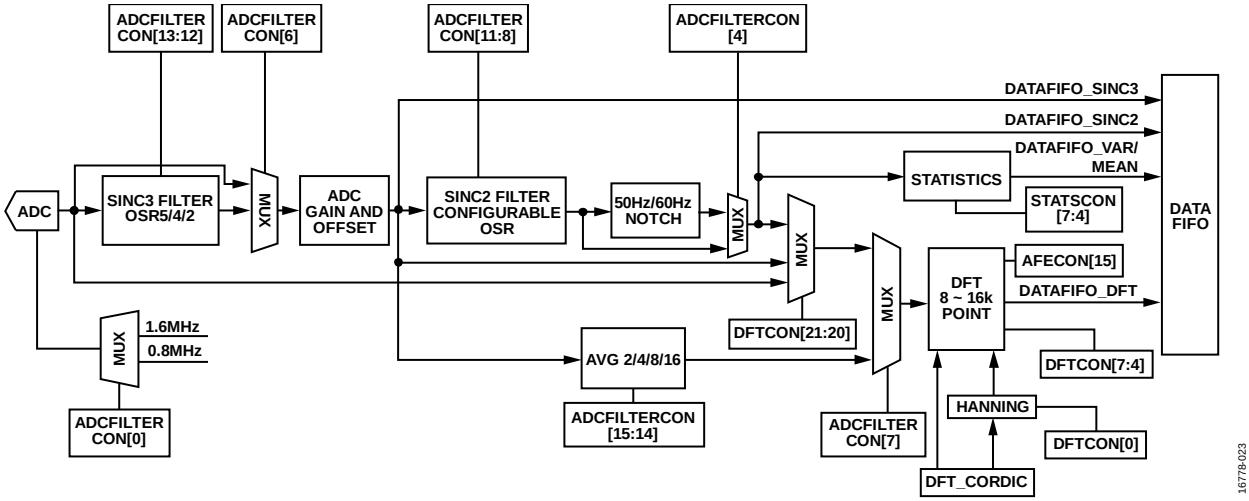

Figure 31. Post Processing Filter Options

ADC CIRCUIT REGISTERS

Table 39. ADC Control Register Summary

Address	Name	Description	Reset	Access
0x00002044	ADCFILTERCON	ADC output filters configuration	0x00000301	R/W
0x00002074	ADCDAT	ADC raw result	0x00000000	R/W
0x00002078	DFTRESULTREAL	DFT result, real part	0x00000000	R/W
0x0000207C	DFTIMAGVAL	DFT result, imaginary part	0x00000000	R/W
0x00002080	SUPPLYLPFRESULT	Supply rejection filter result	0x00000000	R/W
0x00002084	TEMPSENSDAT	Temperature sensor result	0x00000000	R/W

0x00002180	BUFSENCON	High speed and low power buffer control	0x00000037	R/W
0x000021A8	ADCCON	ADC configuration	0x00000000	R/W
0x000021F0	REPEATADCCNV	Repeat ADC conversion control register	0x00000160	R/W
0x0000238C	ADCBUFCON	ADC buffer configuration register	0x005F3D00	R/W

Table 40. ADC Calibration Register Summary

Address	Name	Description	Reset	Access
0x00002230	CALDATLOCK	ADC calibration lock	0x00000000	R/W
0x00002288	ADCOFFSETLPTIA	ADC offset calibration on the low power TIA0 channel	0x00000000	R/W
0x0000228C	ADCGNLPTIA	ADC gain calibration for the low power TIA0 channel	0x00004000	R/W
0x00002234	ADCOFFSETHSTIA	ADC offset calibration on the high speed TIA channel	0x00000000	R/W
0x00002284	ADCGAINHSTIA	ADC gain calibration for the high speed TIA channel	0x00004000	R/W
0x00002244	ADCOFFSETAUX	ADC offset calibration auxiliary channel (PGA gain = 1)	0x00000000	R/W
0x00002240	ADCGAINAUX	ADC gain calibration auxiliary input channel (PGA gain = 1)	0x00004000	R/W
0x000022CC	ADCOFFSET1P5	ADC offset calibration auxiliary input channel (PGA gain = 1.5)	0x00000000	R/W
0x00002270	ADCPGAGN1P5	ADC gain calibration auxiliary input channel (PGA gain = 1.5)	0x00004000	R/W
0x000022C8	ADCOFFSET2	ADC offset calibration auxiliary input channel (PGA gain = 2)	0x00000000	R/W
0x00002274	ADCPGAGN2	ADC gain calibration auxiliary input channel (PGA gain = 2)	0x00004000	R/W
0x000022D4	ADCOFFSET4	ADC offset calibration auxiliary input channel (PGA gain = 4)	0x00000000	R/W
0x00002278	ADCPGAGN4	ADC gain calibration auxiliary input channel (PGA gain = 4)	0x00004000	R/W
0x000022D0	ADCOFFSET9	ADC offset calibration auxiliary input channel (PGA gain = 9)	0x00000000	R/W
0x00002298	ADCPGAGN9	ADC gain calibration auxiliary input channel (PGA gain = 9)	0x00004000	R/W
0x0000223C	ADCOFFSETTEMPSENS	ADC offset calibration temperature sensor channel.	0x00000000	R/W
0x00002238	ADCGAINTEMPSENS	ADC gain calibration temperature sensor channel	0x00004000	R/W
0x00002280	ADCPGAOFFSETCANCEL	ADC offset cancellation, optional calibration	0x00000000	R/W
0x00002294	ADCPGAGN4OFCAL	ADC gain cancellation, optional calibration; calibration with dc cancellation (PGA gain = 4)	0x00004000	R/W
0x000023E4	ADCBISCCON	ADC built in self check (BISC) control, optional self calibration	0x00000000	R/W
0x000023E8	ADCBISCTARGETVAL	ADC BISC target value.	0x00000000	R/W
0x000023EC	ADCBISCDAT	ADC BISC target value	0x00000000	R/W

Table 41. ADC Digital Post Processing Register Summary (Optional)

Address	Name	Description	Reset	Access
0x000020A8	ADCMIN	ADC minimum value check	0x00000000	R/W
0x000020AC	ADCMINSM	ADC minimum Hysteresis	0x00000000	R/W
0x000020B0	ADCMAX	ADC maximum value check	0x00000000	R/W
0x000020B4	ADCMAXSMEN	ADC maximum Hysteresis	0x00000000	R/W
0x000020B8	ADCDELTA	ADC delta check	0x00000000	R/W

Table 42. ADC Statistics Register Summary (Optional)

Address	Name	Description	Reset	Access
0x000021C0	STATSVAR	Variance output	0x00000000	R
0x000021C4	STATSCON	Statistics module configuration, including mean, variance, and outlier detection blocks	0x00000000	R/W
0x000021C8	STATSMEAN	Mean output	0x00000000	R

ADC Output Filters Configuration Register—ADCFILTERCON

Address: 0x00002044, Reset: 0x00000300, Name: ADCFILTERCON

Table 43. Bit Descriptions for ADCFILTERCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:19]	Reserved		Reserved.	0x0	R
18	DFTCLKENB		DFT clock enable.	0x0	
		0	Enable.		
		1	Disable.		
17	DACWAVECLKENB		DAC wave clock enable.	0x0	
		0	Enable.		
		1	Disable.		
16	SINC2CLKENB		Sinc2 filter clock enable.	0x0	
		0	Enable.		
		1	Disable.		
[15:14]	AVRGNUM		These bits set the number of samples used by the averaging function. The average output is fed directly to DFT block and the DFT source is automatically changed to the average output. The AVRGEN bit must be set to 1 to use these bits.	0x0	R/W
		0	2 ADC samples used for the average function.		
		1	4 ADC samples used for the average function.		
		10	8 ADC samples used for the average function.		
		11	16 ADC samples used for the average function.		
[13:12]	SINC3OSR		Sinc3 filter oversampling rate.	0x0	R/W
		0	Oversampling rate of 5. Use this setting for the 160 kHz sinc3 filter output update rate and when the ADC update rate is 800 kSPS (default).		
		1	Oversampling rate of 4. Use this setting for the 400 kHz sinc3 filter output update rate and when the ADC update rate is 1.6 MSPS. High power option.		
		10	Oversampling rate of 2. Use this setting for the 400 kHz sinc3 filter output update rate and when the ADC update rate is 800 kSPS.		
		11	Oversampling rate of 5. Use this setting for the 160 kHz sinc3 filter output update rate and when the ADC update rate is 800 kSPS.		
[11:8]	SINC2OSR		Sinc2 oversampling rate (OSR).	0x3	R/W
		0	22 samples for this OSR setting.		
		1	44 samples for this OSR setting.		
		10	89 samples for this OSR setting.		
		11	178 samples for this OSR setting.		
		100	267 samples for this OSR setting.		
		101	533 samples for this OSR setting.		
		110	640 samples for this OSR setting.		
		111	667 samples for this OSR setting.		
		1000	800 samples for this OSR setting.		
		1001	889 samples for this OSR setting.		
		1010	1067 samples for this OSR setting.		
		1011	1333 samples for this OSR setting.		
7	AVRGEN		ADC average function enable. The average output feeds directly to the DFT block and, when this bit is set, the DFT source automatically changes to the average output.	0x0	R/W
		0	Disable average.		
		1	Enable average to feed to the DFT block.		
6	SINC3BYP		Sinc3 filter bypass. This bit bypasses the sinc3 filter.	0x0	R/W
		0	Sinc3 filter enable.		
		1	Bypasses the sinc3 filter. Raw 800 kHz/1.6 MHz ADC output data is fed directly to the gain offset adjustment stage. If the sinc3 filter is bypassed, the 200 kHz sine wave can be handled directly by the DFT block without amplitude attenuation. If the sinc3 filter is bypassed and the ADC raw data rate is 800 kHz, the gain offset block output is used as the DFT input.		
5	Reserved		Reserved	0x0	R
4	LPFBYPEN		50 Hz/60 Hz low-pass filter.	0x0	R/W

Bits	Bit Name	Settings	Description	Reset	Access
		0	Enables the 50 Hz/60 Hz notch filter. The ADC result is written to the SUPPLYLPFRESULT register.		
		1	Bypasses both the 50 Hz notch and 60 Hz notch filters.		
[3:1]	Reserved		Reserved.	0x0	R
0	ADCSAMPLERATE		ADC data rate. Unfiltered ADC output rate.	0x0	R/W
		1	800 kHz.		
		0	1.6 MHz. If the ADC sample rate = 1.6 MHz, the ACLK frequency to analog must be 32 MHz (refer to the clock configuration).		

ADC Raw Result Register—ADCDAT

Address: 0x00002074, Reset: 0x00000000, Name: ADCDAT

The ADCDAT register is the ADC result register for the raw ADC output or when the sinc3 and/or sinc2 filter options are selected.

Table 44. Bit Descriptions for ADCDAT

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	Data		ADC result. This register contains the ADC conversion result. Depending on the user configuration, this result can reflect raw, sinc3, or sinc2 filter outputs. This result is a 16-bit unsigned number.	0x0	R/W

DFT Result, Real Part Register—DFTREAL

Address: 0x00002078, Reset: 0x00000000, Name: DFTREAL

Table 45. Bit Descriptions for DFTREAL

Bits	Bit Name	Settings	Description	Reset	Access
[31:18]	Reserved		Reserved.	0x0	R
[17:0]	Data		DFT, real. The DFT hardware accelerator returns a complex number. This register returns the 18-bit real part of the complex number representing the magnitude part of the DFT result. The DFT result is represented in twos complement format.	0x0	R/W

DFT Result, Imaginary Part Register—DFTIMAG

Address: 0x0000207C, Reset: 0x00000000, Name: DFTIMAG

Table 46. Bit Descriptions for DFTIMAG

Bits	Bit Name	Settings	Description	Reset	Access
[31:18]	Reserved		Reserved.	0x0	R
[17:0]	Data		DFT, imaginary. The DFT hardware accelerator returns a complex number. This register returns the 18-bit imaginary part of the complex number representing the phase part of the DFT result. The DFT result is represented in twos complement format.	0x0	R/W

Supply Rejection Filter Result Register—SINC2DAT

Address: 0x00002080, Reset: 0x00000000, Name: SINC2DAT

Table 47. Bit Descriptions for SINC2DAT

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	Data		LPF result. Power supply rejection filter, ADC output result. This data is output from the 50 Hz/60 Hz rejection filter. When new data is available, the INTCFLAGx (Bit 2) interrupt bit is set to 1.	0x0	R/W

Temperature Sensor Result Register—TEMPSENSDAT

Address: 0x00002084, Reset: 0x00000000, Name: TEMPSENSDAT

Table 48. Bit Descriptions for TEMPSENSDAT

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	Data		ADC temperature sensor channel result.	0x0	R/W

AFE DSP Configuration Register—DFTCON

Address: 0x000020D0, Reset: 0x00000090, Name: DFTCON

Table 49. Bit Descriptions for DFTCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:22]	Reserved		Reserved.	0x0	R
[21:20]	DFTINSEL		DFT input select. The AVRGEN bit (Bit 7 in the ADCFILTERCON register) is of the highest priority; if this bit = 1, the output of the average block is used as the DFT input, regardless of the SELDFTIN setting.	0x0	R/W
		00	Supply filter output. Select the output from the low-pass supply filter.		
		01	Gain offset output with or without sinc3. This setting selects the output from the ADC gain and offset correction stage. If the sinc3 filter is bypassed (the SINC3BYP bit in the ADCFILTERCON register = 1), ADC raw data through gain/offset correction is the DFT input. If sinc3 is not bypassed(the SINC3BYP bit in the ADCFILTERCON register = 0), the sinc3 output through gain/offset correction is the DFT input.		
		10	ADC raw data. Selects the output direct from the ADC; no offset/gain correction. Only supported for an ADC sample rate of 800 kHz.		
		11	Supply filter output. Selects the output from the low-pass supply filter. Same as 00.		
[19:8]	Reserved		Reserved.	0x0	R
[7:4]	DFTNUM		ADC samples used. DFT number ranges from 4 up to 16,384.	0x9	R/W
		0	DFT point number is 4. DFT uses 4 ADC samples.		
		1	DFT point number is 8. DFT uses 8 ADC samples.		
		10	DFT point number is 16. DFT uses 16 ADC samples.		
		11	DFT point number is 32. DFT uses 32 ADC samples.		
		100	DFT point number is 64. DFT uses 64 ADC samples.		
		101	DFT point number is 128. DFT uses 128 ADC samples.		
		110	DFT point number is 256. DFT uses 256 ADC samples.		
		111	DFT point number is 512. DFT uses 512 ADC samples.		
		1000	DFT point number is 1024. DFT uses 1024 ADC samples.		
		1001	DFT point number is 2048. DFT uses 2048 ADC samples.		
		1010	DFT point number is 4096. DFT uses 4096 ADC samples.		
		1011	DFT point number is 8192. DFT uses 8192 ADC samples.		
		1100	DFT point number is 16384. DFT uses 16,384 ADC samples.		
[3:1]	Reserved		Reserved.	0x0	R
0	HANNINGEN		Hanning window enable.	0x0	R/W
		0	Disable Hanning window.		
		1	Enable Hanning window.		

Temperature Sensor Configuration Register—TEMPSENS

Address: 0x00002174, Reset: 0x00000000, Name: TEMPSENS

Table 50. Bit Descriptions for TEMPSENS

Bits	Bit Name	Settings	Description	Reset	Access
[31:4]	Reserved		Reserved.	0x0	R
[3:2]	CHOPFRESEL		Chop mode frequency setting. These bits set the frequency of the chop mode switching.	0x0	R/W
		00	Chop switch frequency = 6.25 kHz.		

		01 10 11	Chop switch frequency = 25 kHz. Chop switch frequency = 100 kHz. Chop switch frequency = 200 kHz.		
1	CHOPCON	 0 1	Temperature sensor chop mode. Temperature sensor channel chop control signal. Disables chop. Enables chop. If chopping is enabled, take 2× consecutive samples and average the results to obtain a final temperature sensor channel reading. Chopping reduces the offset error associated with this channel.	0x0	R/W
0	Enable	 0 1	Unused. Temperature sensor enable. AFECON, Bit 12 overrides this bit. Disable temperature sensor. Enable temperature sensor. Temperature sensor enable. AFECON, Bit 12 overrides this bit.	0x0	R/W

ADC Configuration Register—ADCCON

Address: 0x000021A8, Reset: 0x00000000, Name: ADCCON

Table 51. Bit Descriptions for ADCCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:29]	Reserved		Reserved.	0x0	R
[18:16]	GNPGA	 0 1 10 11 100 101 1xx	PGA gain setup. Gain = 1. Gain = 1.5. Gain = 2. Gain = 4. Gain = 9. Gain = 9. All 1xx values refer to gain = 9.	0x0	R/W
15	GNOFSELPGA	 0 1	Internal offset/gain cancellation. DC offset cancellation disabled. Enables dc offset cancellation. When the PGA is enabled, only a gain value of 4 is supported.	0x0	R/W
[14:13]	Reserved		Reserved.	0x0	R/W
[12:8]	MUXSELN	 00000 00001 00010 00011 00100 00101 00110 00111 01000 01001 01010 01011 01100 01101 01110 01111 10000 10001 10010 10011 10100	Select signals for the ADC input multiplexor as positive input. Floating input. High speed TIA negative input Low power TIA negative input Reserved. AIN0. AIN1. AIN2. AIN3. ADCVBIAS_CAP. Reserved. Reserved. TEMPSEN_N. AIN4/LPF0. Reserved. AIN6. Reserved. V_{ZERO0}. V_{BIAS0}. Reserved. Reserved. N (negative – labelled N in diagrams) node of excitation amplifier.	0x0	R/W

Bits	Bit Name	Settings	Description	Reset	Access
		10101	Reserved.		
		10110	Reserved.		
[7:6]	Reserved		Reserved.	0x0	R
[5:0]	MUXSELP		Select signals for the ADC input multiplexor as N input.	0x0	R/W
		00000	Floating input.		
		00001	HSTIA_P.		
		00010	LPTIA0_P_LPF.		
		00011	Reserved.		
		00100	AIN0.		
		00101	AIN1.		
		00110	AIN2.		
		00111	AIN3.		
		01000	AVDD/2.		
		01001	DVDD/2.		
		01010	AVDD_REG/2.		
		01011	Internal temperature sensor.		
		01100	ADCVBIAS_CAP.		
		01101	DE0.		
		01110	SE0.		
		01111	Reserved.		
		010000	VREF_2V5/2.		
		010001	Reserved.		
		010010	VREF1V8_DAC.		
		010011	TEMPSENS_N.		
		010100	AIN4/LPF0.		
		010101	Reserved.		
		010110	AIN6.		
		010111	V_{ZERO0}.		
		011000	V_{BIAS0}.		
		011001	V_{CE0}.		
		011010	V_{RE0}.		
		011011	Reserved.		
		011100	Reserved.		
		011101	Reserved.		
		011110	Reserved.		
		011111	VCE0/2.		
		100000	Reserved.		
		100001	LPTIA0_P.		
		100010	Reserved.		
		100011	AGND_REF.		
		100100	P node of excitation amplifier.		

Repeat ADC Conversions Register—REPEATADCCNV

Address: 0x000021F0, Reset: 0x00000160, Name: REPEATADCCNV

Table 52. Bit Descriptions for REPEATADCCNV

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:4]	NUM		Repeat value. Writing 0 to these bits causes unpredictable operation.	0x16	R/W
		1	1 conversion.		
		0xFF	256 conversions.		
[3:1]	Reserved		Reserved.	0x0	R

0	EN_P enable		Enable repeat ADC conversions.	0x0	R/W
		0	Disable repeat ADC conversions.		
		1	Enable repeat ADC conversions.		

ADC Buffer Configuration Register—ADCBUFCON

Address: 0x0000038C, Reset: 0x005F3D00, Name: ADCBUFCON

Recommended value is 0x005F3D0F in HP mode.

Recommended value is 0x005F3D04 in LP mode.

Table 53. Bit Descriptions for ADCBUFCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:9]	Reserved		Reserved.	0x0	R
[8:4]	AMPDIS		Set these bits to 1 to disable the op amp. Set these bits to 0 to enable the op amp. AMPDIS [0] controls the n (negative) front-end buffer. AMPDIS [1] controls the p (positive) front-end buffer. AMPDIS [2] controls the PGA. AMPDIS [3] controls the ADC buffers. AMPDIS [4] controls the offset cancellation buffers.	0x10	R/W
[3:0]	CHOPDIS		Set these bits to 1 to disable chop. Set these bits to 0 to enable chop. Clear these bits when measuring signals <80 kHz. Set these bits when measuring signals >80 kHz. CHOPDIS [0] controls the front-end buffers. CHOPDIS [1] controls the PGA. CHOPDIS [2] controls the ADC buffers. CHOPDIS [3] controls the offset cancellation buffers.	0x0	R/W

ADC CALIBRATION REGISTERS

Calibration Data Lock Register—CALDATLOCK

Address: 0x00002230, Reset: 0x00000000, Name: CALDATLOCK

Table 54. Bit Descriptions for CALDATLOCK

Bits	Bit Name	Settings	Description	Reset	Access
[31:0]	Key		Password for calibration data registers. These bits prevent the overwriting of data after the calibration phase.	0x0	R/W
		0xDE87A5AF	Write this value to unlock the calibration registers.		

ADC Offset Calibration LPTIA Channel Register—ADCOFFSETLPTIA

Address: 0x00002288, Reset: 0x00000000, Name: ADCOFFSETLPTIA

LPTIA Channel Offset Calibration Register

Table 55. Bit descriptions for ADCOFFSETLPTIA

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Offset calibration for the LPTIA. The ADC offset correction for the LPTIA channel is represented as a twos complement number. The calibration resolution is 0.25 LSBs of the ADCDAT LSB size.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0; no offset adjustment.		
		0x7FFF	−0.25. Minimum negative offset calibration value.		

		0x4000	−4096.0. Maximum negative offset calibration value.		

ADC Gain Calibration for the LPTIA Channel Register—ADCGNLPTIA

Address: 0x0000228C, Reset: 0x00004000, Name: ADCGNLPTIA

Table 56. Bit Descriptions for ADCGNLPTIA

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Gain error calibration for the LPTIA.	0x4000	R/W
		0x7FFF	2. Maximum positive gain adjustment.		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default).		
		0x3FFF	0.999939. Minimum negative gain adjustment.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x0000	0. Illegal value; results in an ADC result of 0.		

ADC Offset Calibration HSTIA Channel Register—ADCOFFSETHSTIA

Address: 0x00002234, Reset: 0x00000000, Name: ADCOFFSETHSTIA

Table 57. Bit Descriptions for ADCOFFSETTIA

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		HSTIA offset calibration. ADC offset correction for high speed TIA measurement mode, represented as a twos complement number. The calibration resolution is 0.25 LSBs of the ADCDAT LSB size.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0. No offset correction.		
		0x7FFF	−0.25. Minimum negative offset correction.		
		0x4000	−4096.0. Maximum negative offset correction.		

ADC Gain Calibration for HSTIA Channel Register

Address: 0x00002284, Reset: 0x00004000, Name: ADCGNHSTIA

Table 58. Bit Descriptions for ADCGAINHSTIA

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Gain error calibration on the high speed TIA channel.	0x4000	R/W
		0x7FFF	2. Maximum positive gain adjustment.		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default).		
		0x3FFF	0.999939. Minimum negative gain adjustment.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x0000	0. Illegal value; results in an ADC result of 0.		

ADC Offset Calibration Auxiliary Channel PGA Gain = 1 Register—ADCOFFSETGN1

Address: 0x00002244, Reset: 0x00000000, Name: ADCOFFSETGN1

Table 59. Bit Descriptions for ADCOFFSETAUX

Bits	Bit Name	Settings	Description	Reset	Access

[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Offset Calibration Gain 1. ADC offset correction for the auxiliary channel with gain = 1, represented as a twos complement number. The calibration resolution is 0.25 LSBs of the ADCDAT LSB size; therefore, the calibration resolution is $\pm V_{REF}/2^{18}$. If V_{REF} = 1.82 V, the calibration resolution is $1.82/2^{17}$ = 13.885 µV.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0. No offset adjustment.		
		0x7FFF	−0.25. Minimum negative offset calibration value.		
		0x4000	−4096. Maximum negative offset calibration value.		

ADC Gain Calibration Auxiliary Input Channel Register—ADCGAINGN1

Address: 0x00002240, Reset: 0x00004000, Name: ADCGAINGN1

The ADCGAINGN1 register provides gain calibration for the voltage input channels to the ADC, including the AINx channels.

Table 60. Bit Descriptions for ADCGAINAUX

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Gain calibration PGA gain = 1×; ADC gain correction for auxiliary input channels. These bits are used for all channels, except the TIA and temperature sensor channels when PGA gain = 1. This value is stored as a signed number. Bit 14 is the sign bit, and Bits[13:0] represent the fractional part.	0x4000	R/W
		0x0000	0. Illegal value; results in an ADC result of 0x8000.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default).		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x7FFF	2. Maximum positive gain adjustment.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x3FFF	0.999939. Minimum negative gain adjustment.		

Offset Calibration Auxiliary Channel PGA Gain =1.5 Register—ADCOFFSETGN1P5

Address: 0x00002270, Reset: 0x00000000, Name: ADCOFFSETGN1P5

The ADCOFFSETGN1P5 register provides ADC input offset calibration with PGA gain =1.5.

Table 61. Bit Descriptions for ADCOFFSETGN1P5

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Offset calibration gain = 1.5; ADC offset correction with PGA gain = 1.5.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0. No offset adjustment.		
		0x7FFF	−0.25. Minimum negative offset calibration value.		
		0x4000	−4096. Maximum negative offset calibration value.		

ADC Gain Calibration Auxiliary Input Channel Register—ADCGAINGN1P5

Address: 0x00002240, Reset: 0x00004000, Name: ADCGAINGN1P5

The ADCGAINGN1P5 register provides gain calibration for the voltage input channels to the ADC, including the AINx channels.

Table 62. Bit Descriptions for ADCPGAGN1P5

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R

[14:0]	Value		Gain calibration for PGA gain = 1.5×. These bits provide ADC gain correction for the auxiliary input channels. These bits are used for all channels except the TIA and temperature sensor channels when PGA gain =1.5. This value is stored as a signed number. Bit 14 is the sign bit and Bits[13:0] represent the fractional part.	0x4000	R/W
		0x0000	0. Illegal value resulting in an ADC result of 0.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default value).		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x7FFF	2. Maximum positive gain adjustment.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x3FFF	0.999939. Minimum negative gain adjustment.		

Offset Calibration Auxiliary Channel PGA Gain =2 Register—ADCOFFSETGN2

Address: 0x000022C8, Reset: 0x00000000, Name: ADCOFFSETGN1P5

The ADCOFFSETGN2 register provides ADC input offset calibration with PGA gain =2

Table 63. Bit Descriptions for ADCOFFSETGN2

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Offset calibration auxiliary channel (PGA gain = 2). These bits provide ADC offset correction for inputs using PGA gain = 2, represented as a twos complement number. The calibration resolution is 0.25 LSB of the ADCDAT LSB size. Therefore, the calibration resolution is $\pm V_{REF}/2^{18}$. If V_{REF} = 1.82 V, the calibration resolution is $1.8/2^{17}$ = 13.73 µV.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0. No offset adjustment.		
		0x7FFF	−0.25. Minimum negative offset calibration value.		
		0x4000	−4096. Maximum negative offset calibration value.		

ADC Gain Calibration Auxiliary Input Channel PGA Gain = 2 Register—ADCGAINGN2

Address: 0x00002274, Reset: 0x00004000, Name: ADCGAINGN2

The ADCGAINGN2 register provides gain calibration for the voltage input channels to the ADC, including the AINx channels, when the PGA is enabled with gain = 2×.

Table 64. Bit Descriptions for ADCGAINGN2

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Gain calibration PGA gain = 2. These bits provide ADC gain correction for the auxiliary input channels. These bits are used for all channels except the TIA and the temperature sensor channels when PGA gain = 2. This value is stored as a signed number. Bit 14 is the sign bit and Bits[13:0] represent the fractional part.	0x4000	R/W
		0x0000	0. Illegal value resulting in an ADC result of 0.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default value).		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x7FFF	2. Maximum positive gain adjustment.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x3FFF	0.999939. Minimum negative gain adjustment.		

Offset Calibration Auxiliary Channel PGA Gain = 4 Register—ADCOFFSETGN4

Address: 0x000022D4, Reset: 0x00000000, Name: ADCOFFSETGN4

The ADCOFFSETGN4 register provides ADC input offset calibration with PGA gain = 4.

Table 65. Bit Descriptions for ADCOFFSETGN4

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Offset calibration gain = 4. ADC offset correction with PGA gain = 4.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0. No offset adjustment.		
		0x7FFF	−0.25. Minimum negative offset calibration value.		
		0x4000	−4096. Maximum negative offset calibration value.		

ADC Gain Calibration Auxiliary Input Channel PGA Gain = 4 Register—ADCGAINGN4

Address: 0x00002278, Reset: 0x00004000, Name: ADCGAINGN4

The ADCGAINGN4 register provides gain calibration for the voltage input channels to the ADC, including the AINx channels, when PGA is enabled with gain = 4.

Table 66. Bit Descriptions for ADCPGAGN4

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Gain calibration for PGA gain = 4. These bits provide ADC gain correction for the auxiliary input channels. These bits are used for all channels except the TIA and temperature sensor channels when PGA gain = 4. This value is stored as a signed number. Bit 14 is the sign bit and Bits[13:0] represent the fractional part.	0x4000	R/W
		0x0000	0. Illegal value resulting in an ADC result of 0.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default value).		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x7FFF	2. Maximum positive gain adjustment.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x3FFF	0.999939. Minimum negative gain adjustment.		

Offset Calibration Auxiliary Channel PGA Gain = 9 Register—ADCOFFSETGN9

Address: 0x000022D0, Reset: 0x00000000, Name: ADCOFFSETGN9

The ADCOFFSETGN9 register provides ADC input offset calibration with PGA gain = 9.

Table 67. Bit Descriptions for ADCOFFSETGN9

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Offset calibration gain = 9. ADC offset correction with PGA gain = 9.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0. No offset adjustment.		
		0x7FFF	−0.25. Minimum Negative Offset calibration value.		
		0x4000	−4096. Maximum Negative Offset calibration value.		

ADC Gain Calibration Auxiliary Input Channel PGA Gain = 9 Register—ADCFAINGN9

Address: 0x00002298, Reset: 0x00004000, Name: ADCGAINGN9

The ADCFAINGN9 register provides gain calibration for the voltage input channels to the ADC, including the AINx channels, when the PGA is enabled with gain = 9.

Table 68. Bit Descriptions for ADCGAINGN9

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R

[14:0]	Value		Gain calibration for PGA gain = 9. These bits provide ADC gain correction for the auxiliary input channels. These bits are used for all channels except the TIA and temperature sensor channels when PGA gain = 9. This value is stored as a signed number. Bit 14 is the sign bit and Bits[13:0] represent the fractional part.	0x4000	R/W
		0x0000	0. Illegal value resulting in an ADC result of 0.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default value).		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x7FFF	2. Maximum positive gain adjustment.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x3FFF	0.999939. Minimum negative gain adjustment.		

ADC Offset Calibration Temperature Sensor Channel Register—ADCOFFSETTEMPSENS

Address: 0x0000223C, Reset: 0x00000000, Name: ADCOFFSETTEMPSENS

Table 69. Bit Descriptions for ADCOFFSETTEMPSENS

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	Value		Offset calibration for the temperature sensor. These bits provide ADC offset correction for the temperature sensor channel, represented as a twos complement number. The calibration resolution is 0.25 LSB of the ADCDAT LSB size. Therefore, the calibration resolution is $\pm V_{REF}/2^{18}$. If V_{REF} = 1.82 V, the calibration resolution is: $1.82/2^{17}$ = 13.73 µV.	0x0	R/W
		0x3FFF	+4095.75. Maximum positive offset calibration value.		
		0x0001	+0.25. Minimum positive offset calibration value.		
		0x0000	0. No offset adjustment.		
		0x7FFF	−0.25. Minimum negative offset calibration value.		
		0x4000	−4096. Maximum negative offset calibration value.		

ADC Gain Calibration Temperature Sensor Channel Register—ADCGAINTEMPSENS

Address: 0x00002238, Reset: 0x00004000, Name: ADCGAINTEMPSENS

The ADCGAINTEMPSENS register provides the ADC gain calibration value used when measuring the internal temperature sensor.

Table 70. Bit Descriptions for ADCGAINTEMPSENS

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	GAINTEMPSENS		Gain calibration for the temperature sensor channel. These bits provide ADC gain correction for the temperature sensor channel. This value is stored as a signed number. Bit 14 is the sign bit and Bits[13:0] represent the fractional part.	0x4000	R/W
		0x0000	0. Illegal value resulting in an ADC result of 0.		
		0x2000	0.5. ADC result multiplied by 0.5.		
		0x4000	1.0. ADC result multiplied by 1. No gain adjustment (default value).		
		0x4001	1.000 061. Minimum positive gain adjustment.		
		0x7FFF	2. Maximum positive gain adjustment.		
		0x0001	0.000061. Maximum negative gain adjustment.		
		0x3FFF	0.999939. Minimum negative gain adjustment.		

ADC Offset Cancellation Register—ADCPGAOFFSETCANCEL

Address: 0x00002280, Reset: 0x00000000, Name: ADCPGAOFFSETCANCEL

The ADCPGAOFFSETCANCEL register provides PGA offset cancellation for gain = 4. This register is used to cancel large system offset errors and is only valid for gain = 4.

Table 71. Bit Descriptions for ADCPGAOFFSETCANCEL

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	OFFSETCANCEL		Offset cancellation. These bits provide ADC offset correction in auxiliary channel measurement mode. This value is represented as a twos complement number and allows a ±5% correction range with a resolution of 0.25 LSB at a 16-bit level.	0x0	R/W
		0x3FFF	+4095.75.		
		0x0001	+0.25.		
		0x0000	0.		
		0x7FFF	−0.25.		
		0x4000	−4096.		

ADC Gain Calibration with DC Cancellation (PGA Gain = 4) Register—ADCPGAGN4OFCAL

Address: 0x00002294, Reset: 0x00004000, Name: ADCPGAGN4OFCAL

PGA dc gain cancellation is used to remove large dc offsets and is only valid when PGA gain = 4.

Table 72. Bit Descriptions for ADCPGAGN4OFCAL

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
[14:0]	ADCGAINAUX		DC calibration gain = 4. Optional dc calibration register.	0x4000	R/W

ADC DIGITAL POST PROCESSING REGISTERS

ADC Minimum Value Check Register—ADCMIN

Address: 0x000020A8, Reset: 0x00000000, Name: ADCMIN

Table 73. Bit Descriptions for ADCMIN

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	MINVAL		ADC minimum value threshold. This value is a low ADCDAT threshold value. If a value less than ADCMIN is measured by the ADC, the INTCFLAGx bit (Bit 4) is set to 1.	0x0	R/W

ADCMIN Hysteresis Value Register—ADCMINSM

Address: 0x000020AC, Reset: 0x00000000, Name: ADCMINSM

Table 74. Bit Descriptions for ADCMINSM

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	MINCLRVAL		ADCMIN hysteresis value. If a value less than ADCMIN is measured by the ADC, the ADCMINERR bit is set. The ADCMINERR bit is set until ADCDAT is greater than ADCMIN + ADCMINSM, Bits[15:0].	0x0	R/W

ADC Maximum Value Check Register—ADCMAX

Address: 0x000020B0, Reset: 0x00000000, Name: ADCMAX

Table 75. Bit Descriptions for ADCMAX

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	MAXVAL		ADC maximum threshold. These bits form the optional maximum ADCDAT threshold. If a value less than ADCMAX is measured by the ADC, the INTCFLAGx bit (Bit 5) is set to 1.	0x0	R/W

ADCMAX Hysteresis Value Register—ADCMAXSMEN

Address: 0x000020B4, Reset: 0x00000000, Name: ADCMAXSMEN

Table 76. Bit Descriptions for ADCMAXSMEN

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	MAXSWEN		ADCMAX hysteresis value. If a value greater than ADCMAX is measured by the ADC, the ADCMAXERR bit is set. The ADCMAXERR bit remains set until ADCDAT is less than ADCMAX – ADCMAXSMEN, Bits[15:0].	0x0	R/W

ADC Delta Value Register—ADCDELTA

Address: 0x000020B8, Reset: 0x00000000, Name: ADCDELTA

Table 77. Bit Descriptions for ADCDELTA

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	DELTAVAL		ADCDAT code differences limit option. If two consecutive ADCDAT results have a difference greater than ADCDELTA, Bits[15:0], an error flag is set via INTCFLAGx, Bit 6.	0x0	R/W

ADC STATISTICS REGISTERS (OPTIONAL)

Statistics Control Register—STATSCON

Address: 0x000021C4, Reset: 0x00000000, Name: STATSCON

Table 78. Bit Descriptions for STATSCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:7]	STDDEV		Standard deviation configuration.	0x0	R/W
[6:4]	SAMPLENUM		Sample size. These bits set the number of ADC samples used for each statistic calculation.	0x0	R/W
		0	128 samples.		
		1	64 samples.		
		10	32 samples.		
		11	16 samples.		
		100	8 samples.		
[3:1]	Reserved		Reserved.	0x0	R/W
0	STATSEN		Statistics enable.	0x0	R/W
		0	Disable statistics.		
		1	Enable statistics.		

Statistics Mean Output Register—STATSMEAN

Address: 0x000021C8, Reset: 0x00000000, Name: STATSMEAN

Table 79. Bit Descriptions for STATSMEAN

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	Mean		Mean output. These bits form the mean value calculated for the number of ADC samples set by STATSCON, Bits[6:4].	0x0	R

Variance Output Register—STATSVAR

Address: 0x000021C0, Reset: 0x00000000, Name: STATSVAR

Table 80. Bit Descriptions for STATSVAR

Bits	Bit Name	Settings	Description	Reset	Access
31	Reserved		Reserved.	0x0	R
[30:0]	Variance		Statistical variance value. This value indicates the spread from the mean value.	0x0	R

PROGRAMMABLE SWITCH MATRIX

The AD5940 provides flexibility for connecting external pins to the high speed DAC excitation amplifier and to the high speed TIA inverting input. This flexibility supports options for impedance measurements of different sensor types and allows an ac signal to be coupled to the dc bias voltage of a sensor.

When configuring the switches, take the switch settings on the output of the low power amplifiers into account.

On power-up, all switches are open to disconnect the sensor.

Figure 34 shows a high level diagram of how each of the switch matrix nodes, D, P, N and T connect to the internal circuitry of the AD5940. Figure 35 shows a detailed diagram of every switch on the matrix.

SWITCH DESCRIPTIONS

D Switches

The D switches select the pin to connect to the excitation amplifier output of the high speed DAC. For an impedance measurement, this pin is CE0. The output of the excitation amplifier can be connected to an external calibration resistor via the RCAL0 pin if Switch DR0 is closed.

P Switches

The P switches select the pin to connect to the excitation amplifier P input of the high speed DAC's excitation amplifier. For most applications, this pin is RE0. The negative input of the excitation amplifier can be connected to an external calibration resistor via the RCAL0 pin if Switch PR0 is closed.

N Switches

The N switches select the pin to connect to the excitation amplifier N input of the high speed DAC. The inverting input of the HSTIA can be connected to an external calibration resistor via the RCAL1 pin if Switch NR1 is closed.

T Switches

The T switches select the pin to connect to the inverting input of the high speed TIA. The inverting input of the HSTIA can be connected to an external calibration resistor via the RCAL1 pin if Switch TR1 is closed.

AFEx Switches

The AFE1, AFE2, and AFE3 switches are only intended for use as switches. These switches are not ADC inputs. In a multi-measurement system, these switches provide a method to switch sensor electrodes; this is useful in, for example, bioelectric system applications.

RECOMMENDED CONFIGURATION IN HIBERNATE MODE

To minimize leakage on the switches connecting to the excitation amplifier P and N terminals, and to minimize leakage on the high speed TIA, it is recommended to tie the switches to the internal 1.82 V LDO generated voltage by closing the PL, PL2, NL, and NL2 switches.

In hibernate mode, it is assumed that only the dc bias voltage from the low power amplifiers is required for the sensor.

OPTIONS FOR CONTROLLING ALL SWITCHES

Figure 34 shows all switches connected to the high speed DAC excitation amplifier and to the inverting input of the high speed TIA.

The register map proved the user with two options to control the programmable switches in the high speed DAC excitation amplifier and the inverting input of the high speed TIA. These options are as follows:

- Control the T, N, P, and D switches as a group in the SWCON register.
- Individual control of each switch within the switch matrix using the xSWFULLCON registers.

If controlling the switches using the xSWFULLCON registers, follow this sequence:

1. Write to the specific bit in the register.
2. Set the SOURCESEL bit. If this bit is not set after writing to the register, the changes do not take effect.

In addition, status registers are available to read back the open or closed status of each switch.

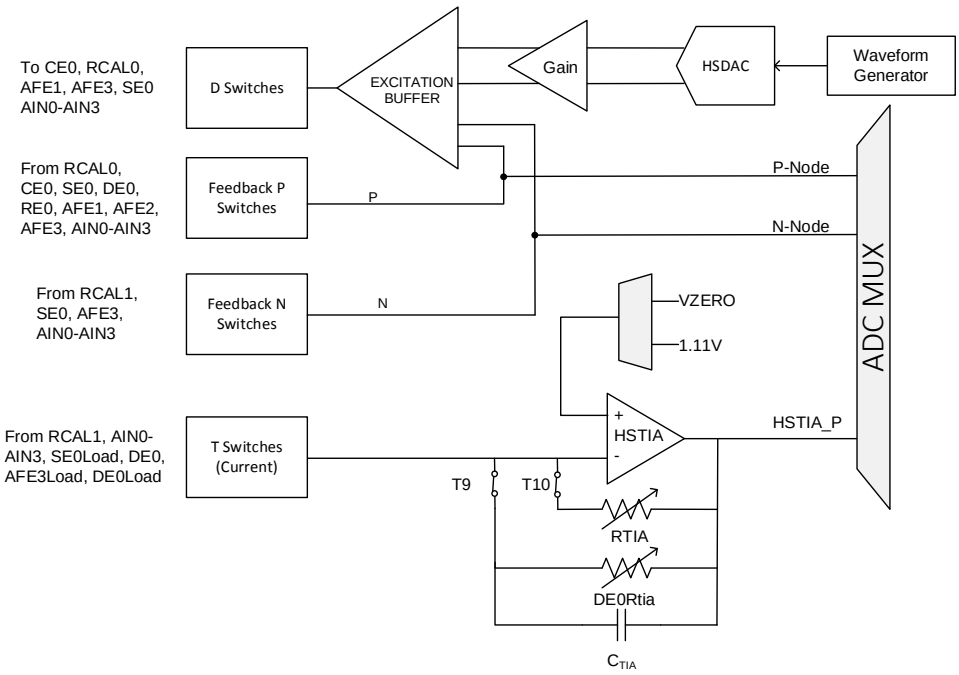

Figure 32: Switch Matrix High Level Diagram

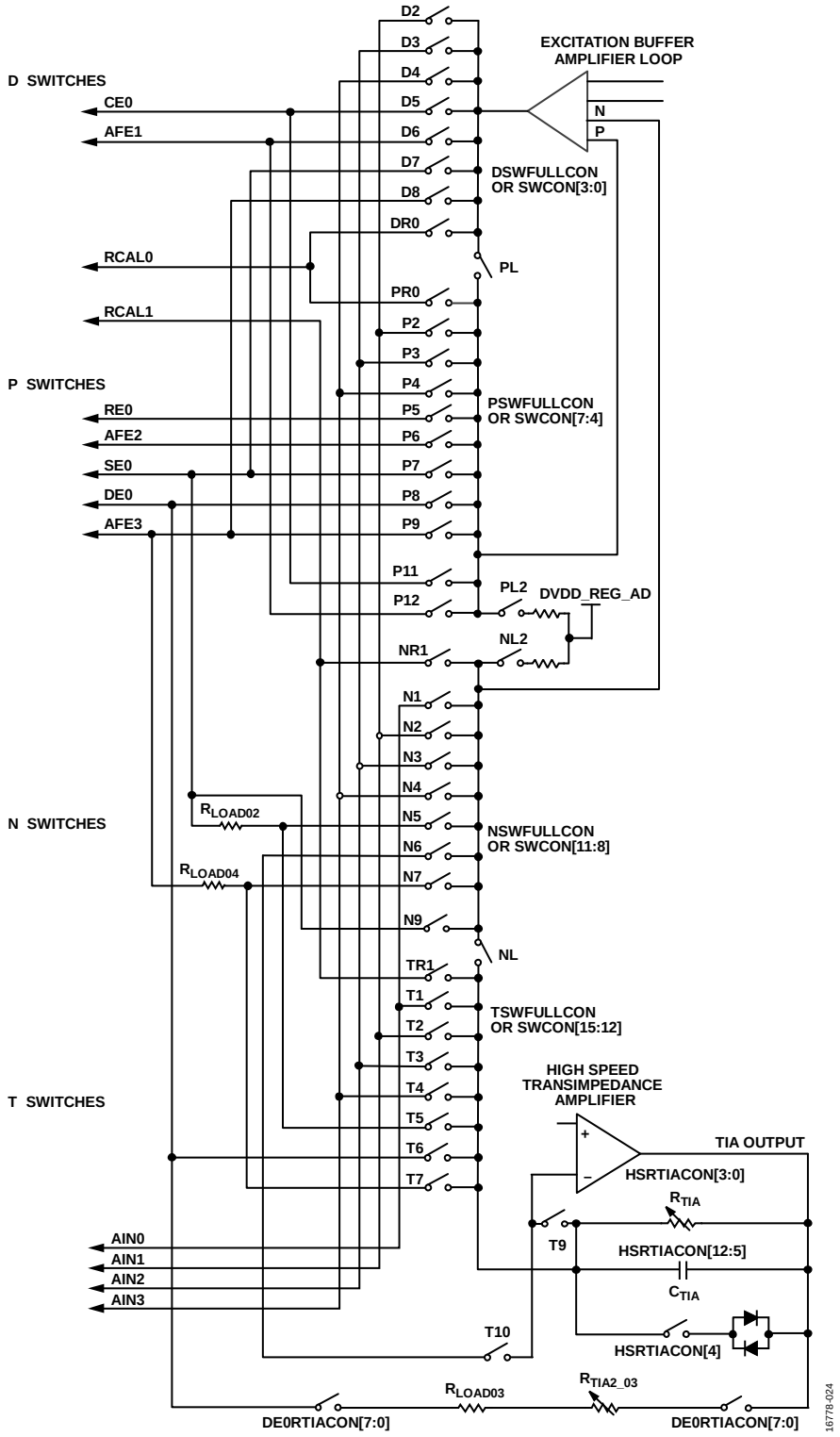

Figure 33. Switch Matrix Block Diagram—Switches Connecting to the High Speed DAC and High Speed TIA

PROGRAMMABLE SWITCHES REGISTERS

Table 81. Programmable Switch Matrix Register List

Address	Name	Description	Reset	Access
0x0000200C	SWCON	Switch matrix configuration	0x0000FFFF	R/W
0x00002150	DSWFULLCON	Switch matrix full configuration (D)	0x00000000	R/W
0x00002154	NSWFULLCON	Switch matrix full configuration (N)	0x00000000	R/W
0x00002158	PSWFULLCON	Switch matrix full configuration (P)	0x00000000	R/W
0x0000215C	TSWFULLCON	Switch matrix full configuration (T)	0x00000000	R/W
0x000021B0	DSWSTAT	Switch matrix status (D)	0x00000000	R
0x000021B4	SWPSTA	Switch matrix status (P)	0x00006000	R
0x000021B8	SWNSTA	Switch matrix status (N)	0x00000C00	R
0x000021BC	TSWSTA	Switch matrix status (T)	0x00000000	R

Switch Matrix Configuration Register Details—SWCON

Address: 0x0000200C, Reset: 0x0000FFFF, Name: SWCON

Table 82. Bit Descriptions for SWCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:19]	Reserved		Reserved.	0x0	R
18	T10CON		Control of T10.	0x0	R/W
		1	T10 closed.		
		0	T10 open.		
17	T9CON		Control of T9.	0x0	R/W
		1	T9 closed.		
		0	T9 open.		
16	SWSOURCESEL		Switch control select. This bit selects the registers to control the programmable switches.	0x0	R/W
		1	Switch control source. Switches controlled by DSWFULLCON, TSWFULLCON, PSWFULLCON, and NSWFULLCON.		
		0	D, T, P, and N switches controlled as groups. Switches controlled as groups via SWCON.		
[15:12]	TMUXCON		Control of the T switch mux. Does not include control of T9 or T10.	0xF	R/W
		0000	All switches open.		
		0001	T1 closed, remaining switches open.		
		0010	T2 closed, remaining switches open.		
		0011	T3 closed, remaining switches open.		
		0100	T4 closed, remaining switches open.		
		0101	T5 closed, remaining switches open.		
		0110	T6 closed, remaining switches open		
		0111	Reserved.		
		1000	TR1 closed, remaining switches open.		
		1001	All switches closed.		
		1010 to 1111	All switches open.		

Bits	Bit Name	Settings	Description	Reset	Access
[11:8]	NMUXCON		Control of N switch mux.	0xF	R/W
		0000	NL closed, remaining switches open.		
		0001	N1 closed, remaining switches open.		
		0010	N2 closed, remaining switches open.		
		0011	N3 closed, remaining switches open.		
		0100	N4 closed, remaining switches open.		
		0101	N5 closed, remaining switches open.		
		0110	N6 closed, remaining switches open.		
		0111	Reserved.		
		1000	Reserved.		
		1001	N9 closed, remaining switches open.		
		1010	NR1 closed, remaining switches open.		
		1011-1110	NL closed, remaining switches open.		
		1111	All switches open.		
[7:4]	PMUXCON		Control of P switch mux.	0xF	R/W
		0000	PL closed, remaining switches open.		
		0001	PR0 closed, remaining switches open.		
		0010	P2 closed, remaining switches open.		
		0011	P3 closed, remaining switches open.		
		0100	P4 closed, remaining switches open.		
		0101	P5 closed, remaining switches open.		
		0110	Reserved		
		0111	P7 closed, remaining switches open.		
		1000	P8 closed, remaining switches open.		
		1001	Reserved.		
		1010	Reserved.		
		1011	P11 closed, remaining switches open.		
		1100	Reserved.		
		1101-1110	PL closed, remaining switches open.		
		1111	All switches open.		
[3:0]	DMUXCON		Control of D switch mux.	0xF	R/W
		0000	All switches open.		
		0001	DR0 closed, remaining switches open.		
		0010	D2 closed, remaining switches open.		
		0011	D3 closed, remaining switches open.		
		0100	D4 closed, remaining switches open.		
		0101	D5 closed, remaining switches open.		
		0110	Reserved.		
		0111	D7 closed, remaining switches open.		
		1000	Reserved		
		1001	All switches closed.		
		1010-1111	All switches open.		

Switch Matrix Full Configuration D Register—DSWFULLCON

Address: 0x00002150, Reset: 0x00000000, Name: DSWFULLCON

The DSWFULLCON register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram.

Table 83. Bit Descriptions for DSWFULLCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:7]	Reserved		Reserved.	0x0	R
6	D7		Control of D7 switch. This bit connects the D node of the excitation amplifier to SE0.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
5	Reserved		Reserved.	0x0	R/W
4	D5		Control of D5 Switch. This bit connects the D node of the excitation amplifier to CE0.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
3	D4		Control of D4 Switch. This bit connects the D node of the excitation amplifier to AIN3.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
2	D3		Control of D3 Switch. This bit connects the D node of the excitation amplifier to AIN2.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
1	D2		Control of D2 Switch. This bit connects the D node of the excitation amplifier to AIN1.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
0	DR0		Control of Dr0 Switch. This bit connects the D node of the excitation amplifier to RCAL0.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		

Switch Matrix Full Configuration N Register—NSWFULLCON

Address: 0x00002154, Reset: 0x00000000, Name: NSWFULLCON

The NSWFULLCON register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram.

Table 84. Bit Descriptions for NSWFULLCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
11	NL2		Control of the NL2 Switch. If this bit is set, Nl2 is closed. If this bit is not set, Nl2 is open.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
10	NL		Control of the NL switch. If this bit is set, NL is closed. If this bit is not set, NL is open. This bit shorts the N node of the excitation amplifier to the inverting input of the high speed TIA.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
9	NR1		Control of the NR1 switch. If this bit is set, NR1 is closed. If this bit is not set, NR1 is open. This bit connects the N node of the excitation amplifier to the RCAL1 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
8	N9		Control of the N9 switch. If this bit is set, N9 is closed. If this bit is not set, N9 is open. This bit connects the N node of the excitation amplifier directly to SE0, bypassing RLOAD02.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	Reserved		Reserved.	0x0	R/W
5	N6		Control of the N6 switch. If this bit is set, N6 is closed. If this bit is not set, N6 is open. This bit connects the N node of the excitation amplifier to RLOAD03/T10.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
4	N5		Control of the N5 switch. If this bit is set, N5 is closed. If this bit is not set, N5 is open. This bit connects the N node of the excitation amplifier to SE0 via RLOAD02.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
3	N4		Control of the N4 switch. If this bit is set, N4 is closed. If this bit is not set, N4 is open. This bit connects the N node of the excitation amplifier to AIN3.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
2	N3		Control of the N3 switch. If this bit is set, N3 is closed. If this bit is not set, N3 is open. This bit connects the N node of the excitation amplifier to AIN2.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
1	N2		Control of the N2 switch. If this bit is set, N2 is closed. If this bit is not set, N2 is open. This bit connects the N node of the excitation amplifier to AIN1.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
0	N1		Control of the N1 switch. If this bit is set, N1 is closed. If this bit is not set, N1 is open. This bit connects the N node of the excitation amplifier to AIN0.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		

Switch Matrix Full Configuration P Register—PSWFULLCON

Address: 0x00002158, Reset: 0x00000000, Name: PSWFULLCON

The PSWFULLCON register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram.

Table 85. Bit Descriptions for PSWFULLCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
14	PL2		PL2 switch control.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
13	PL		PL switch control. This bit shorts the D and P nodes of the excitation amplifier together.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
[12:11]	Reserved		Reserved.	0x0	R/W
10	P11		Control of the P11 switch. Setting this bit closes P11. P11 is open if this bit is not set. This bit connects the P node of the excitation amplifier to the CE0 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
[9:8]	Reserved		Reserved.	0x0	R/W
7	P8		Control of the P8 switch. Setting this bit closes P8. P8 is open if this bit is not set. This bit connects the P node of the excitation amplifier to the DE0 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
[6:5]	Reserved		Reserved.	0x0	R/W
4	P5		Control of the P5 switch. Setting this bit closes P5. P5 is open if this bit is not set. This bit connects the P node of the excitation amplifier to the RE0 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		

Bits	Bit Name	Settings	Description	Reset	Access
3	P4		Control of the P4 switch. Setting this bit closes P4. P4 is open if this bit is not set. This bit connects the P node of the excitation amplifier to the AIN3 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
2	P3		Control of the P3 switch. Setting this bit closes P3. P3 is open if this bit is not set. This bit connects the P node of the excitation amplifier to the AIN2 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
1	P2		Control of the P2 switch. Setting this bit closes P2. P2 is open if this bit is not set. This bit connects the P node of the excitation amplifier to the AIN1 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
0	PR0		PR0 switch control. This bit connects the P node of the excitation amplifier to the RCAL0 pin.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		

Switch Matrix Full Configuration T Register—TSWFULLCON

Address: 0x0000215C, Reset: 0x00000000, Name: TSWFULLCON

The TSWFULLCON register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram.

Table 86. Bit Descriptions for TSWFULLCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
11	TR1		Control of the TR1 switch. Setting this bit closes TR1. TR1 is open if this bit is not set. This bit connects the RCAL1 pin to the inverting input of the high speed TIA.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
10	Reserved		Reserved.	0x0	R/W
9	T10		Control of the T10 switch. Setting this bit closes T10. T10 is open if this bit is not set. This bit connects the DE0 pin to the inverting input of the high speed TIA.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
8	T9		Control of the T9 switch. Setting this bit closes T9. T9 is open if this bit is not set. This switch is used in conjunction with T10.	0x0	R/W
		0	Switch open. When open, the inverting input of the high speed TIA can be DE0 via the T10 switch.		
		1	Switch closed. Ensure that T10 is open. The inverting input of the high speed TIA is decided by T1, T2, T3, T4, T5, and T6.		
7	Reserved		Reserved.	0x0	R/W
6	T7		Control of the T7 switch. This bit connects the inverting input of the high speed TIA to AFE3 pin via T9 and Rload04.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
5	T6		Control of the T6 switch. Setting this bit closes T6. T6 is open if this bit is not set. This bit allows connection of the RCAL path to the DE0 input to calibrate the RLOAD03 and RTIA2_03 resistors.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
4	T5		Control of the T5 switch. Setting this bit closes T5. T5 is open if this bit is not set. This bit connects the inverting input of the high speed TIA to the SE0 pin via T9 and RLOAD02.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		

Bits	Bit Name	Settings	Description	Reset	Access
3	T4		Control of the T4 switch. Setting this bit closes T4. T4 is open if this bit is not set. This bit connects the inverting input of the high speed TIA to the AIN3 pin via T9.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
2	T3		Control of the T3 switch. Setting this bit closes T3. T3 is open if this bit is not set. This bit connects the inverting input of the high speed TIA to the AIN2 pin via T9.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
1	T2		Control of the T2 switch. Setting this bit closes T2. T2 is open if this bit is not set. This bit connects the inverting input of the high speed TIA to the AIN1 pin via T9.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		
0	T1		Control of the T1 switch. Setting this bit closes T1. T1 is open if this bit is not set. This bit connects the inverting input of the high speed TIA to the AIN0 pin via T9.	0x0	R/W
		0	Switch open.		
		1	Switch closed.		

Switch Matrix Status D Register—DSWSTA

Address: 0x000021B0, Reset: 0x00000000, Name: DSWSTA

The DSWSTA register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram.

Table 87. Bit Descriptions for DSWSTA

Bits	Bit Name	Settings	Description	Reset	Access
[31:7]	Reserved		Reserved.	0x0	R
6	D7STA		Status of the D7 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
5	Reserved		Reserved.	0x0	R
4	D5STA		Status of the D5 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
3	D4STA		Status of the D4 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
2	D3STA		Status of the D3 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
1	D2STA		Status of the D2 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
0	D1STA		Status of the DR0 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		

Switch Matrix Status P Register—PSWSTA

Address: 0x000021B4, Reset: 0x00006000, Name: PSWSTA

The PSWSTA register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram.

Table 88. Bit Descriptions for PSWSTA

Bits	Bit Name	Settings	Description	Reset	Access
[31:15]	Reserved		Reserved.	0x0	R
14	PL2STA		PL switch control.	0x1	R
		0	Switch open.		
		1	Switch closed.		
13	PLSTA		PL switch control.	0x1	R
		0	Switch open.		
		1	Switch closed.		
12	P13STA		Status of the P13 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
11	Reserved		Reserved	0x0	R
10	P11STA		Status of the P11 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
9	Reserved		Reserved	0x0	R
7	P8STA		Status of the P8 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
6	P7STA		Status of the P7 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
5	Reserved		Reserved	0x0	R
4	P5STA		Status of the P5 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
3	P4STA		Status of the P4 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
2	P3STA		Status of the P3 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
1	P2STA		Status of the P2 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
0	PR0STA		PR0 switch control.	0x0	R
		0	Switch open.		
		1	Switch closed.		

Switch Matrix Status N Register—NSWSTA

Address: 0x000021B8, Reset: 0x00000C00, Name: NSWSTA

The NSWSTA register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram.

Table 89. Bit Descriptions for NSWSTA

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
11	NL2STA		Status of the NL2 switch.	0x1	R
		0	Switch open.		
		1	Switch closed.		
10	NLSTA		Status of the NL switch.	0x1	R
		0	Switch open.		
		1	Switch closed.		
9	NR1STA		Status of the NR1 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
8	N9STA		Status of the N9 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
[7:6]	Reserved		Reserved	0x0	R
5	N6STA		Status of the N6 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
4	N5STA		Status of the N5 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
3	N4STA		Status of the N4 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
2	N3STA		Status of the N3 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
1	N2STA		Status of the N2 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
0	N1STA		Status of the N1 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		

Switch Matrix Status T Register—TSWSTA

Address: 0x000021BC, Reset: 0x00000000, Name: TSWSTA

The TSWSTA register allows individual control of the AFE switches. The bit names are the same as the switch names in the AFE diagram

Table 90. Bit Descriptions for TSWSTA

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
11	TR1STA		Status of the TR1 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
10	Reserved		Reserved	0x0	R
9	T10STA		Status of the T10 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		

Bits	Bit Name	Settings	Description	Reset	Access
8	T9STA		Status of the T9 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
7	RESERVED		Reserved.	0x0	R
6	T7STA		Status of the T7 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
5	T6STA		Status of the T6 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
4	T5STA		Status of the T5 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
3	T4STA		Status of the T4 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
2	T3STA		Status of the T3 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
1	T2STA		Status of the T2 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		
0	T1STA		Status of the T1 switch.	0x0	R
		0	Switch open.		
		1	Switch closed.		

PRECISION VOLTAGE REFERENCES

This section describes the integrated voltage references options available on the AD5940. The AD5940 is capable of generating accurate voltage references for the ADC and DAC. There is a 1.82 V reference for the ADC and DAC, and a 2.5 V reference for the potentiostat. The 2.5 V reference must be decoupled via the VREF_2V5 pin and the 1.82 V reference must be decoupled via the VREF_1V82 pin.

Figure 35 shows the various voltage reference options available and the register and bits that control these options.

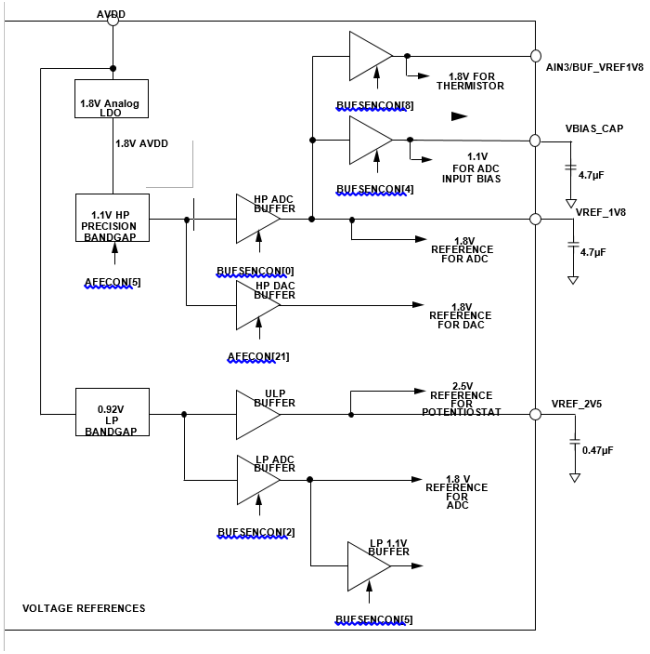

Figure 34. Precision Voltage References

High Power and Low Power Buffer Control Register—BUFSENCON

Address: 0x00002180, Reset: 0x00000000, Name: BUFSENCON

Table 91. Bit Descriptions for BUFSENCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:9]	Reserved		Reserved.	0x0	R
8	V1P8THERMSTEN		Buffered reference output. Buffered output to the AIN3/BUF_VREF1V82 pin.	0x0	R/W
		0	Disable 1.82 V buffered reference output.		
		1	Enable 1.82 V Buffered reference output.		
7	Reserved		Reserved.	0x0	R
6	V1P1LPADCCHGDIS		Control of the decoupling capacitor discharge switch. This switch connects the 1.11 V internal reference for the ADC common-mode voltage to an internal discharging circuit. Leave this bit open for normal operation to maintain the reference voltage on the external 1.11 V decoupling capacitor.	0x0	R/W
		0	Open switch (recommended value). Leave the switch open to maintain charge on external decoupling capacitor for the 1.11 V reference.		
		1	Close switch. Close this switch to connect the 1.11 V reference to the discharging circuit.		
5	V1P1LPADCEN		ADC 1, 1 V low power common-mode buffer (optional). Use Either the high speed or low power reference buffer.	0x0	R/W
		0	Disable the ADC 1, 1 V low power reference buffer.		
		1	Enable the ADC 1, 1 V low power reference buffer.		

Bits	Bit Name	Settings	Description	Reset	Access
4	V1P1HSADCEN		Enable the 1.11 V high speed common-mode buffer. This bit controls the buffer for the 1.11 V common-mode voltage source to the ADC input stage.	0x0	R/W
		0	Disable the 1.11 V high speed common-mode buffer.		
		1	Enable the 1.11 V high speed common-mode buffer (recommended value for normal ADC operation).		
3	V1P8HSADCCHGDIS		Controls the decoupling capacitor discharge switch. This switch connects the 1.82 V internal ADC reference to an internal discharging circuit. Leave this bit open for normal operation to maintain the reference voltage on the external decoupling capacitor.	0x0	R/W
		0	Open switch. If opened, the voltage on the external decoupling capacitor for the reference is maintained (recommended value).		
		1	Close switch. Close this switch to connect the reference to the discharge circuit.		
2	V1P8LPADCEN		ADC 1.82 V low power reference buffer.	0x0	R/W
		0	Disable the low power 1.82 V reference buffer.		
		1	Enable the low power 1.82 V reference buffer (recommended value). This setting speeds up the settling time when exiting a power-down state.		
1	V1P8HSADCILIMITEN		High speed ADC input current limit. This bit protects the ADC input buffer.	0x0	R/W
		0	Disable buffer current limit.		
		1	Enable buffer current limit (recommended value).		
0	V1P8HSADCEN		High speed 1.82 V reference buffer. Enable the reference buffer for normal ADC conversions.	0x0	R/W
		0	Disable 1.82 V high speed ADC reference buffer.		
		1	Enable 1.82 V high speed ADC reference buffer.		

SEQUENCER

FEATURES

The features of the AD5940 sequencer are as follows:

- Programmable for cycle accurate applications.
- Four separate command sequences.
- Large 6 kB SRAM to store sequences.
- FIFO for storing measurement results.
- Control via the wake-up timer, SPI command, or GPIO toggle.
- Various interrupts from user maskable sources.

OVERVIEW

The role of the sequencer is to allow offloading of the low level AFE operations from the external microcontroller and to provide cyclic accurate control over the analog DSP blocks. The sequencer handles timing critical operations without being subject to system load.

In the AD5940, four sequences are supported by hardware. These sequences can be stored in SRAM to easily switch between different measurement procedures. Only one sequence can be executed by the sequencer at a time. However, the user can configure which sequences the sequencer executes and the order in which they are executed.

The sequencer reads commands from the sequence stored in the command memory and, depending on the command, either waits a certain amount of time or writes a value to a memory map register. The execution is sequential, with no branching. The sequencer cannot read MMR values or signals from the analog/DSP blocks.

To enable the sequencer, set the SEQEN bit in the SEQCON register. Writing 0 to this bit disables the sequencer.

The rate at which the sequencer commands are executed is provided in the SEQWRTMR bits in the SEQCON register. When a write command is executed by the sequencer, the sequencer performs the MMR write and then waits SEQWRTMR clock cycles before fetching the next command in the sequence. The effect is the same as a write command followed by a wait command. The main purpose of this setup is to reduce code size when generating arbitrary waveforms. The SEQWRTMR bits do not have any effect following a wait or timeout command.

In addition to a single write command being followed by a wait command, multiple write commands can be executed in succession followed by a wait command. Therefore, any configuration can be set up rapidly by the sequencer, regardless of the number of register writes followed by a precisely executed delay.

The sequencer can also be paused by setting the SEQHALT bit in the SEQCON register. This option applies to each function, including FIFO operations, internal timers, and waveform generation. Reads from the MMRs are allowed when the sequencer is paused. This mode is intended for debugging during software development.

The number of commands executed by the sequencer can be read from the SEQCNT register. Each time a command is read from command memory and executed, the counter is incremented by 1. Performing a write to the SEQCNT register resets the counter.

The sequencer calculates the cyclic redundancy check (CRC) of all commands it executes. The algorithm used is the CRC-8, using the polynomial $x^8 + x^2 + x + 1$. The CRC-8 algorithm performs on 32-bit input data (sequencer instructions). Each 32-bit input is processed in one clock cycle, and the result is available immediately for reading by the host controller. The CRC value can be read from the SEQCRC register. This register is reset by the same mechanism as the command count, by writing to the SEQCNT register. The SEQCRC resets to a seed value of 0x01. The SEQCRC is a read only register.

SEQUENCER COMMANDS

There are two types of commands that can be executed by the sequencer: write commands and timer commands, which includes wait commands and timeout commands.

Write Command

Use a write instruction to write data into a register. Figure 36 shows the format of the instruction. The MSB is equal to 1, which indicates a write command.

ADDR is the write address and DATA is the write data to be written to the MMR. All write instructions finish within one cycle.

The address field is 7 bits wide, allowing access to registers from Address 0x0 to address 0x1FC in the AFE register block. All MMR accesses are 32 bits only. Byte and half word accessed are forbidden. All accesses are implied write only. There is a direct mapping between the address field and the MMR address. ADDR corresponds to Bits [8:2] of the 16-bit MMR address.

For example, when writing to WGCON directly through the SPI interface, the address used is 0x2014. To write to the same register using the sequencer, the address field must be 0b0000101 (Bits [8:2] of the address used by the external controller).

The data field is 24 bits wide and only allows writing to the MMR bits, Bits [23:0]. It is not possible to write to the full 32 bits of the MMRs via the sequencer. However, Bits [31:24] are not used by any of the MMRs; therefore, all assigned MMR bits can be written by the sequencer.

Timer Command

There are two, timer commands in the sequencer, with a separate hardware counter for each.

The wait command introduces wait states in the sequencer execution. After the programmed counter reaches 0, the execution is resumed by reading the next command from command memory.

The timeout command starts a counter that operates independent of the sequencer flow. When the timer elapses, one of two interrupts is generated: a sequence timeout error interrupt,

INTSEL15, or a sequence timeout finished interrupts, INTSEL16; both interrupts are configured in the INTCSELx registers. The sequence timeout finished interrupt is asserted at the end of the timeout period. The sequence timeout error interrupt is asserted if, at the end of the timeout period, the sequencer does not reach the end of execution. These interrupts are cleared by writing to the corresponding bits in the INTCCLRx registers. The current value of the counter can be read by the host controller at any time through the SEQTIMEOUT register

The timeout counter is not reset when the sequencer execution is stopped as a result of a sequencer write command. However, it is reset if the host controller writes a 0 to the SEQEN bit in the SEQCON register; this applies to situations when the host must abort the sequence.

The time unit for both timer commands is one ACLK period. For a clock frequency of 16 MHz, the timer resolution is 62.5 ns, and the maximum timeout is 67.1 sec. These values are true even if the SEQWRTMR bits in SEQCON register are nonzero.

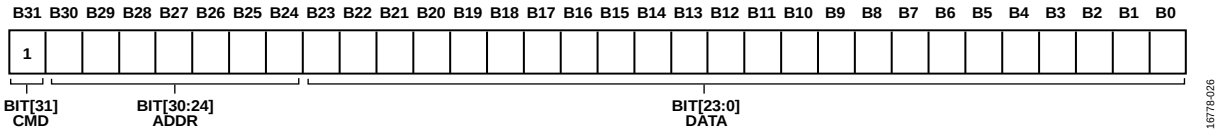

Figure 35. Sequencer Write Command

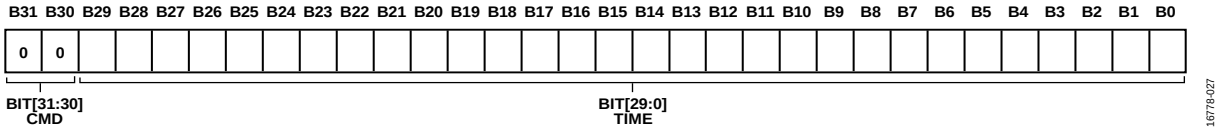

Figure 36. Sequencer Timer Command

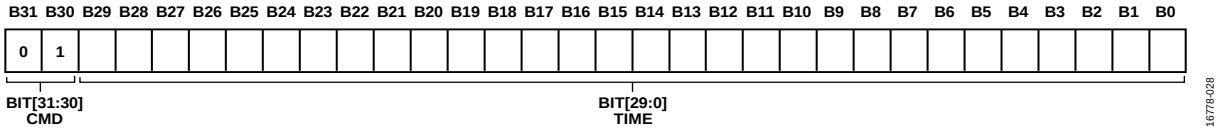

Figure 37. Sequencer Wait Command

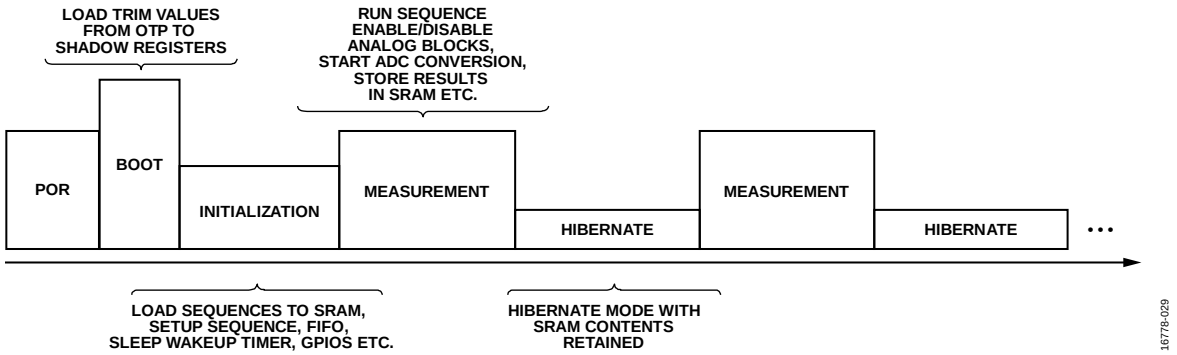

Figure 38. Run Sequence

SEQUENCER OPERATION

Figure 39 shows the typical steps required to set up the sequencer to take measurements. After the device is booted, the sequencer, command memory, and data FIFO must be configured. The following steps are required for this configuration:

1. Configure the command memory.
2. Load the sequences into SRAM.
3. Set the SEQ0 to SEQ3 information.
4. Configure the data FIFO.
5. Configure the sleep wake-up timer.
6. Configure the GPIO pin mux.
7. Configure the interrupts.
8. Configure the sleep and wake-up method.

Command Memory

The command memory stores the sequence commands and provides a link between the external microcontroller and the sequencer. The command memory can be configured to use the following memory sizes, which are selected using CMDDATACO, Bits[2:0]:

- 2 kB of SRAM.
- 4 kB of SRAM.
- 6 kB of SRAM.

The large amount of memory available for the command memory facilitates the creation of larger, more complex sequences.

Determine the number of commands in a sequence by reading SEQxINFO, Bits[26:16].

The command memory is unidirectional. The host microcontroller specifies the destination address of the command by writing to the CMDFIFOWADDR register and writes the command contents to the CMDFIFOWRITE register. The sequencer reads the commands from memory for execution.

There are a number of interrupts associated with the command FIFO, including the FIFO threshold interrupt, the FIFO empty interrupt, and the FIFO full interrupt. Refer to the Interrupts section for more information.

Loading Sequences

The sequence commands are written to SRAM by writing to two registers. The address in SRAM for the command is written to CMDFIFOWADDR. The command content is written to CMDFIFOWRITE. After all the commands are written to SRAM, the SEQ0 to SEQ3 information is set.

Each sequence from SEQ0 to SEQ3 requires a start address in SRAM and a total number or commands for that sequence. The number of commands is written to SEQxINFO, Bits[26:16]. The start address is written to SEQxINFO, Bits[10:0]. Ensure there is no overlap between the four sequences. There is no hardware mechanism in place to warn the user of overlapping sequences.

There are a number of interrupt sources associated with the sequencer, including

- Sequence timeout error.
- Sequencer timeout command finished.
- End of sequence interrupt. For this interrupt to be asserted, SEQCON, Bit 0, must be cleared at the end of the sequencer command.

Refer to the Interrupts section for more information.

Data FIFO

The data FIFO provides a buffer for the output of the analog/DSP blocks before it is read by the external controller.

The memory available for the data FIFO can be selected in the DATAMEMSEL bits in the CMDDATACON register. The available options are 32B, 2K, 4K, and 6K. The data FIFO and command memory share the same block of 8K SRAM; therefore, ensure there is no overlap between the command memory and data FIFO.

The data FIFO can be configured in FIFO mode or stream mode via CMDDATACON, Bits[11:9]. In stream mode, when the FIFO is full, old data is discarded to make room for new data. In FIFO mode, when the FIFO is full, new data is discarded.

The data FIFO is always unidirectional. A selectable source in the AFE block writes data and the external microcontroller reads data from DATAFIFORD.

Select the data source for the data FIFO in DATAFIFOSRCSEL. The available options are

- ADC data.
- DFT result.
- LPF result.
- Mean.
- Variance.

There a number of interrupt flags associated with the data FIFO, including

- Empty.
- Full.
- Overflow.
- Underflow.
- Threshold.

These interrupts are user readable using the INTCFLAGx registers (see the Interrupts for more details). Each flag has an associated maskable interrupt.

The overflow and underflow flags only activate for one clock period.

The data FIFO is enabled by writing a 1 to FIFOCON [11]. The data FIFO threshold value is set by writing to the DATAFIFOTHRES register. At any time, the host microcontroller can read the number of words in the data FIFO by reading FIFOCNTSTA, Bits[26:16].

Reading data from the data FIFO when empty returns 0x00000000. In addition, the underflow flag, FLAG27, in the INTCFLAG register is asserted.

Data FIFO Word Format

The format of data FIFO words is shown in Figure 40. Each word in the data FIFO is 32 bits. The 7 MSBs are the Error Correction Code (ECC) required for functional safety applications. Bits [24:23] form the sequence ID and indicate which sequence, from SEQ0 to SEQ3, is currently running.

Bits [22:16] contain the channel ID and indicate the source for the data.

Table 92: Channel ID Description

Bits [22:16]	Meaning
11111_xx	DFT Result
11110_xx	Mean from statistics block
11101_xx	Variance from statistics block
1xxxx_xx	SINC2 filter result. xxxx_xx is the ADC Mux P setting (ADCCON [5:0])
0xxxx_xx	SINC3 filter result. xxxx_xx is the ADC Mux P setting (ADCCON [5:0])

The 16 LSBs are the actual data (see Figure 40).

When the data source is the DFT result, the data is 18 bits wide. The extra two bits are due to the results being in twos complement format. The format is shown in Figure 41. The channel ID is 5 bits wide, with 5'b11111 indicating the DFT results

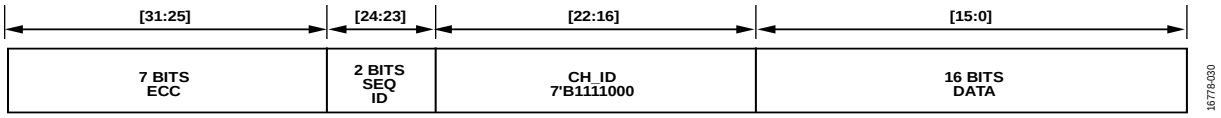

Figure 39. Data FIFO Word Format

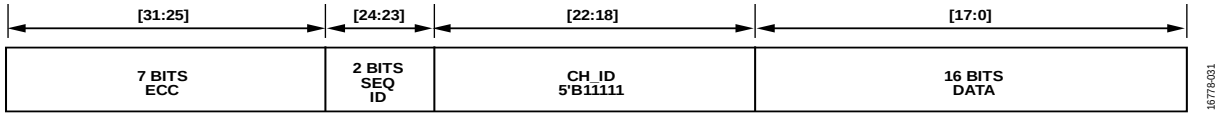

Figure 40. Data FIFO DFT Word Format

Sequencer and the Sleep and Wake-Up Timer

See the Sleep and Wake-Up Timer section for more information.

Configuring the GPIOx Pin Mux

Each of the eight GPIOx pins can be configured to trigger a sequence. The GPIOx pin must first be configured as an input in the GP0OEN register. Then, the pin must be configured to TRIGx in the GP0CON register. After a GPIO event is detected, the corresponding sequence begins to run. The sequencer can also access the GPIO while running. The main purpose this access serves is to synchronize external devices, such as the ADXL362 or the AD8233. To perform this synchronization, the corresponding GPIOx functionality must be set to synchronize in the GP0CON register and the direction of data must be set to output in the GP0OEN register. The sequencer can then write to the SYNCEXTDEVICE register to toggle the corresponding GPIOx pin, which is a very useful debugging feature when programming the sequencer.

Sequencer Conflicts

If a conflict between sequences arises—for example, when SEQ0 is running and the SEQ1 request arrives—SEQ1 is ignored and SEQ0 completes. An interrupt is generated to indicate that SEQ1 is ignored.

Reading back registers does not cause resource conflicts. Writes to MMRs by the host controller are allowed while the sequencer is enabled. There may be some conflicts. If conflicts arise, the sequencer has the priority. If sequencer and host controller write at the same time, the host controller is ignored. There is no error report for this conflict. The user must ensure they do not write to a register when the sequencer is running. However, there are exceptions, which can be written freely without any conflict. The SEQCON register allows ending sequence execution (SEQEN) and halting a sequence (SEQHALT).

SEQUENCER AND FIFOS REGISTERS

Table 93. Sequence and FIFO Register Summary

Address	Name	Description	Reset	Access
0x00002004	SEQCON	Sequencer configuration	0x00000002	R/W
0x00002008	FIFOCON	FIFO configuration	0x00001010	R/W
0x00002060	SEQCRC	Sequencer CRC value	0x00000001	R
0x00002064	SEQCNT	Sequencer command count	0x00000000	R/W
0x00002068	SEQTIMEOUT	Sequencer timeout counter	0x00000000	R
0x0000206C	DATAFIFORD	Data FIFO read	0x00000000	R
0x00002070	CMDFIFOWRITE	Command FIFO write	0x00000000	W
0x00002118	SEQSLPLOCK	Sequencer sleep control lock	0x00000000	R/W
0x0000211C	SEQTRGSLP	Sequencer trigger sleep	0x00000000	R/W
0x000021CC	SEQ0INFO	Sequence 0 information	0x00000000	R/W
0x000021D0	SEQ2INFO	Sequence 2 information	0x00000000	R/W
0x000021D4	CMDFIFOWADDR	Command FIFO write address	0x00000000	R/W
0x000021D8	CMDDATACON	Command data control	0x00000410	R/W
0x000021E0	DATAFIFOTHRES	Data FIFO threshold	0x00000000	R/W
0x000021E4	SEQ3INFO	Sequence 3 information	0x00000000	R/W

0x000021E8	SEQ1INFO	Sequence 1 information	0x00000000	R/W
0x00002200	FIFOCNTSTA	Command and data FIFO internal data count	0x00000000	R

Sequencer Configuration Register—SEQCON

Address: 0x00002004, Reset: 0x00000002, Name: SEQCON

Table 94. Bit Descriptions for SEQCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:8]	SEQWRTMR		Timer for sequencer write commands. These bits act as a clock divider affecting the write commands, but not the wait commands. This divider is useful to reduce the code size when generating arbitrary waveforms. The clock source for the timer is ACLK.	0x0	R/W
[7:5]	Reserved		Reserved.	0x0	R
4	SEQHALT		Halt sequence debugging feature. This bit provides a way to halt the AFE interface, including the sequencer, DSP hardware accelerators, FIFOs, and so on.	0x0	R/W
		0	Normal execution.		
		1	Execution halted.		
[3:2]	Reserved		Reserved	0x0	R
1	SEQHALTFIFOEMPTY		Halt sequencer, if empty. This bit controls if the sequencer stops when attempting to read when the command FIFO is empty (in an underflow condition).	0x1	R/W
		1	Sequencer stops if command FIFO is empty and sequencer attempts to read (in an underflow condition).		
		0	Sequencer continues to attempt to read, even if the FIFO is empty.		
0	SEQEN		Enable sequencer. If this bit is set to 1, the sequencer reads from the command FIFO and executes the commands.	0x0	R/W
		0	Sequencer disabled (default).		
		1	Sequencer enabled.		

FIFOs Configuration Register—FIFOCON

Address: 0x00002008, Reset: 0x00001010, Name: FIFOCON

Table 95. Bit Descriptions for FIFOCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	RESERVED		Reserved	0x0	R
[15:13]	DATAFIFOSRCSEL		Selects the source for the data FIFO.	0x0	R/W
		000/001	ADC data. ADC data is output of gain/offset calibration through the sinc3 filter.		
		110/111			
		010	DFT data. Real part is 18 bits and the imaginary part is 18 bits. The lowest 2 bits are fractional because the ADC is 16 bits.		
		011	Supply rejection filter output. Supply rejection is 16 bits.		
		100	Variance. Variance is 30-bit data, which uses two addresses.		
		101	Mean result. Mean is 16 bits of data.		
12	Reserved		Reserved	0x1	R/W
11	DATAFIFOEN		Data FIFO enable.	0x0	R/W
		0	FIFO is reset. No data transfers can take place. This setting sets the read and write pointers to the default values (empty FIFO). The status indicates that the FIFO is empty.		
		1	Normal operation. The FIFO is not reset.		
[10:0]	Reserved		Reserved.	0x0	R/W

Sequencer CRC Value Register—SEQCRC

Address: 0x00002060, Reset: 0x00000001, Name: SEQCRC

The SEQCRC register forms the checksum value calculated from all the commands executed by the sequencer.

Table 96. Bit Descriptions for SEQCRC

Bits	Bit Name	Settings	Description	Reset	Access
[31:8]	Reserved		Reserved.	0x0	R
[7:0]	CRC		Sequencer command CRC value. The algorithm used is CRC-8.	0x1	R

Sequencer Command Count Register—SEQCNT

Address: 0x00002064, Reset: 0x00000000, Name: SEQCNT

The SEQCNT register forms the command count, which is incremented by 1 each time the sequencer executes a command. This register is not key protected.

Table 97. Bit Descriptions for SEQCNT

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	Count		Sequencer command count. This count is incremented by 1 each time the sequencer executes a command. Reset to 0 by writing 1 to this register. Write 1 to this register also to clear the SEQCRC register	0x0	R/W1

Sequencer Timeout Counter Register—SEQTIMEOUT

Address: 0x00002068, Reset: 0x00000000, Name: SEQTIMEOUT

Table 98. Bit Descriptions for SEQTIMEOUT

Bits	Bit Name	Settings	Description	Reset	Access
[31:30]	Reserved		Reserved.	0x0	R
[29:0]	Timeout		Current value of the sequencer timeout counter.	0x0	R

Data FIFO Read Register—DATAFIFORD

Address: 0x0000206C, Reset: 0x00000000, Name: DATAFIFORD

Table 99. Bit Descriptions for DATAFIFORD

Bits	Bit Name	Settings	Description	Reset	Access
[31:16]	Reserved		Reserved.	0x0	R
[15:0]	DATAFIFOOUT		Data FIFO read. If the data FIFO is empty, a read of this register returns 0x00000000.	0x0	R

Command FIFO Write Register—CMDFIFOWRITE

Address: 0x00002070, Reset: 0x00000000, Name: CMDFIFOWRITE

Table 100. Bit Descriptions for CMDFIFOWRITE

Bits	Bit Name	Settings	Description	Reset	Access
[31:0]	CMDFIFOIN		Command FIFO write. If the command FIFO is written while full, the write is ignored and all current commands are not affected.	0x0	W

Sequencer Sleep Control Lock Register—SEQSLPLOCK

Address: 0x00002118, Reset: 0x00000000, Name: SEQSLPLOCK

The SEQSLPLOCK register protects the SEQTRGSLP register.

Table 101. Bit Descriptions for SEQSLPLOCK

Bits	Bit Name	Settings	Description	Reset	Access
[31:20]	Reserved		Reserved.	0x0	R
[19:0]	SEQ_SLP_PW		Password for the SLPBYSEQ register. These bits prevent the sequencer from accidentally triggering a sleep state.	0x0	R/W
		0x0000	Write any value other than 0xA47E5 to lock SEQTRGSLP		
		0xA47E5	Write 0xA47E5 to this register to unlock SEQTRGSLP.		

Sequencer Trigger Sleep Register—SEQTRGSLP

Address: 0x0000211C, Reset: 0x00000000, Name: SEQTRGSLP

The SEQTRGSLP register is protected by the SEQSLPLOCK register.

Table 102. Bit Descriptions for SEQTRGSLP

Bits	Bit Name	Settings	Description	Reset	Access
[31:1]	Reserved		Reserved.	0x0	R
0	TRGSLP		Trigger sleep by sequencer. Write to SEQSLPLOCK first. Put this command at the end of a sequence. Set this command to 1 if entering sleep at the end of a sequence.	0x0	R/W

Sequence 0 Information Register—SEQ0INFO

Address: 0x000021CC, Reset: 0x00000000, Name: SEQ0INFO

Table 103. Bit Descriptions for SEQ0INFO

Bits	Bit Name	Settings	Description	Reset	Access
[31:27]	Reserved		Reserved.	0x0	R
[26:16]	SEQ0INSTNUM		SEQ0 instruction number.	0x0	R/W
[15:11]	Reserved		Reserved.	0x0	R
[10:0]	SEQ0STARTADDR		SEQ0 start address.	0x0	R/W

Sequence 2 Information Register—SEQ2INFO

Address: 0x000021D0, Reset: 0x00000000, Name: SEQ2INFO

Table 104. Bit Descriptions for SEQ2INFO

Bits	Bit Name	Settings	Description	Reset	Access
[31:27]	Reserved		Reserved.	0x0	R
[26:16]	SEQ2INSTNUM		SEQ2 instruction number.	0x0	R/W
[15:11]	Reserved		Reserved.	0x0	R
[10:0]	SEQ2STARTADDR		SEQ2 start address.	0x0	R/W

Command FIFO Write Address Register—CMDFIFOWADDR

Address: 0x000021D4, Reset: 0x00000000, Name: CMDFIFOWADDR

Table 105. Bit Descriptions for CMDFIFOWADDR

Bits	Bit Name	Settings	Description	Reset	Access
[31:11]	Reserved		Reserved.	0x0	R
[10:0]	WADDR		Write address. These bits are the address in SRAM in which to store the command.	0x0	R/W

Command Data Control Register—CMDDATACON

Address: 0x000021D8, Reset: 0x00000410, Name: CMDDATACON

Table 106. Bit Descriptions for CMDDATACON

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:9]	DATAMEMMDE		Data FIFO mode select.	0x2	R/W
		10	FIFO mode.		
		11	Stream mode.		
[8:6]	DATA_MEM_SEL		Data FIFO size select.	0x0	R/W
		000	Reserved.		
		001	2kB SRAM.		
		010	4kB SRAM.		
		011	6kB SRAM.		
[5:3]	CMDMEMMDE		Command FIFO mode.	0x2	R/W
		01	Memory mode.		
		10	Reserved.		
		11	Reserved.		
[2:0]	CMD_MEM_SEL		Command memory select.	0x0	R/W
		0x0	Reserved.		
		0x1	2kB SRAM.		
		0x2	4kB SRAM.		
		0x3	6kB SRAM.		

Data FIFO Threshold Register—DATAFIFOTHRES

Address: 0x000021E0, Reset: 0x00000000, Name: DATAFIFOTHRES

Table 107. Bit Descriptions for DATAFIFOTHRES

Bits	Bit Name	Settings	Description	Reset	Access
[31:27]	Reserved		Reserved	0x0	R
[26:16]	HIGHTHRES		High threshold	0x0	R/W
[15:0]	Reserved		Reserved	0x0	R

Sequence 3 Information Register—SEQ3INFO

Address: 0x000021E4, Reset: 0x00000000, Name: SEQ3INFO

Table 108. Bit Descriptions for SEQ3INFO

Bits	Bit Name	Settings	Description	Reset	Access
[31:27]	Reserved		Reserved	0x0	R
[26:16]	INSTNUM		SEQ3 instruction number	0x0	R/W
[15:11]	Reserved		Reserved	0x0	R
[10:0]	STARTADDR		SEQ3 start address	0x0	R/W

Sequence 1 Information Register—SEQ1INFO

Address: 0x000021E8, Reset: 0x00000000, Name: SEQ1INFO

Table 109. Bit Descriptions for SEQ1INFO

Bits	Bit Name	Settings	Description	Reset	Access
[31:27]	Reserved		Reserved	0x0	R
[26:16]	SEQ1INSTNUM		SEQ1 instruction number	0x0	R/W
[15:11]	Reserved		Reserved	0x0	R
[10:0]	SEQ1STARTADDR		SEQ1 start address	0x0	R/W

Command and Data FIFO Internal Data Count Register—FIFOCNTSTA

Address: 0x00002200, Reset: 0x00000000, Name: FIFOCNTSTA

Table 110. Bit Descriptions for FIFOCNTSTA

Bits	Bit Name	Settings	Description	Reset	Access
[31:27]	Reserved		Reserved	0x0	R
[26:16]	DATAFIFOCNTSTA[10:0]		Current number of words in the data FIFO	0x0	R
[15:0]	Reserved		Reserved	0x0	R

SYNC External Devices Register—SYNCEXTDEVICE

Address: 0x00002054, Reset: 0x00000000, Name: SYNCEXTDEVICE

Table 111. Bit Descriptions for SYNCEXTDEVICE

Bits	Bit Name	Settings	Description	Reset	Access
[31:8]	Reserved		Reserved.	0x0	R
[7:0]	SYNC		Output data of the GPIOx. Refer to the GPCON register to understand the GPIOx to be controlled. Writing 1 to the corresponding bit sets the corresponding GPIOs high. Writing 0 sets the corresponding GPIOx to 0.	0x0	R/W

Trigger Sequence Register—TRIGSEQ

Address: 0x00000430, Reset: 0x0000, Name: TRIGSEQ.

Table 112. Bit Descriptions for TRIGSEQ

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Reserved		Reserved	0x0	R
3	TRIG3		Trigger Sequence 3	0x0	R/W
2	TRIG2		Trigger Sequence 2	0x0	R/W
1	TRIG1		Trigger Sequence 1	0x0	R/W
0	TRIG0		Trigger Sequence 0	0x0	R/WS

WAVEFORM GENERATOR

The AD5940 implements a digital waveform generator for generating sinusoid, trapezoid, and square waveforms. This section describes how to use the waveform generator.

WAVEFORM GENERATOR FEATURES

The waveform generator features sine wave, trapezoid, and square wave capabilities and can be used with the high speed DAC or the low power DAC.

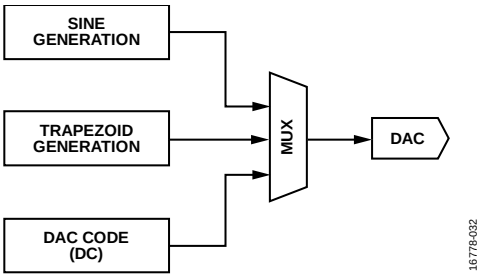

Figure 41. Simplified Waveform Generator Block Diagram

WAVEFORM GENERATOR OPERATION

To enable the waveform generator block, set the WAVEGENEN bit in the AFECON register to 1. When this bit is enabled, the selected waveform source starts and loops until either the block is disabled (WAVEGENEN = 0), or another source is selected. When the block is disabled, the DAC output maintains the voltage until a different waveform is selected by writing to the TYPESEL bit in the WGCON register, or if the waveform is reset.

Sinusoid Generator

The block diagram for the sinusoid generator is shown in Figure 43.

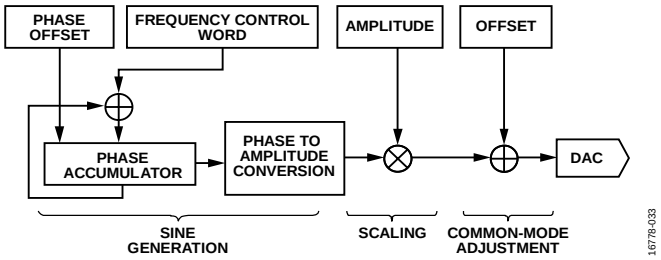

Figure 42. Sinusoid Generator

The output frequency is adjusted using the frequency control word (WGFCW, Bits[30:0]) with the following formula:

$$f_{OUT} = f_{ACLK} \times SINEFCW/2^{30}$$

where:

f_{ACLK} is the frequency of ACLK, 16 MHz.

SINEFCW is WGFCW, Bits[30:0].

The sinusoid generator includes a programmable phase offset controlled by the WGOFFSET register. When enabled, the phase accumulator is initialized with the contents of the phase offset register. After the sinusoid generator starts, the phase increment is always positive.

Trapezoid Generator

The definition of the trapezoid waveform is shown in Figure 44

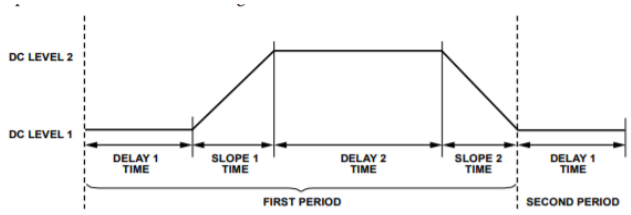

Figure 43. Trapezoid Waveform Definition

The six parameters shown in Figure 44 are user programmable through the WGDCLEVEL1, WGDCLEVEL2, WGDELAY1, WGDELAY2, WDSLOPE1, and WGSLOPE2 registers. These variables define the trapezoid waveform. By setting the WGSLOPEx register to 0x00000, a square wave is generated. The times are expressed in the number of periods of the DAC update clock, which is set to 320 kHz for the trapezoid function. A period of the trapezoid waveform begins at the start of WGDELAY1 and completes and the end of WGSLOPE2. The trapezoid continues to loop until it is disabled by the user.

USING THE WAVEFORM GENERATOR WITH THE LOW POWER DAC

Although the waveform generator is primarily designed for use with the high speed DAC, it can also be used with the low power DAC for ultra low power and low bandwidth applications. To configure the low power DAC for generating waveforms, set Bit 6 in the LPDACCON register to 1. Trapezoid or sinusoid can be selected as described previously The 32 kHz oscillator must be selected as the system clock when using the waveform generator with the low power DAC, which limits the bandwidth of the signal.

WAVEFORM GENERATOR REGISTERS

Table 113. Waveform Generator for High Speed DAC Register List

Address	Name	Description	Reset	Access
0x00002014	WGCON	Waveform generator configuration.	0x00000030	R/W
0x00002018	WGDCLEVEL1	Waveform generator. Trapezoid DC Level 1.	0x00000000	R/W
0x0000201C	WGDCLEVEL2	Waveform generator. Trapezoid DC Level 2.	0x00000000	R/W
0x00002020	WGDELAY1	Waveform generator. Trapezoid Delay 1 time.	0x00000000	R/W
0x00002024	WGSLOPE1	Waveform generator. Trapezoid Slope 1 time.	0x00000000	R/W

0x00002028	WGDELAY2	Waveform generator. Trapezoid Delay 2 time.	0x00000000	R/W
0x0000202C	WGSLOPE2	Waveform generator. Trapezoid Slope 2 time.	0x00000000	R/W
0x00002030	WGFCW	Waveform generator. Sinusoid frequency control word.	0x00000000	R/W
0x00002034	WGPHASE	Waveform generator. Sinusoid phase offset.	0x00000000	R/W
0x00002038	WGOFFSET	Waveform generator. Sinusoid offset.	0x00000000	R/W
0x0000203C	WGAMPLITUDE	Waveform generator. Sinusoid amplitude.	0x00000000	R/W

Waveform Generator Configuration Register—WGCON

Address: 0x00002014, Reset: 0x00000030, Name: WGCON

Table 114. Bit Descriptions for WGCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:6]	Reserved		Reserved	0x0	R
5	DACGAINCAL		Bypass DAC gain. Use the DAC gain calculated during the Analog Devices factory trim and stored in DACGAIN.	0x1	R/W
		0	Bypass DAC gain correction.		
		1	Perform DAC gain correction.		
4	DACOFFSETCAL		Bypass DAC Offset. Use the DAC offset calculated during the calibration routine.	0x1	R/W
		0	Bypass DAC offset correction.		
		1	Perform DAC offset correction. The offset value is in DACUOFFSET and DACUOFFSETHS for low power and high power mode, respectively, when DACCON, Bit 0 = 0. The offset value is in DACUOFFSETATTEN and DACUOFFSETATTENHS for low power and high power mode, respectively, when DACCON, Bit 0 = 1.		
3	Reserved		Reserved.	0x0	R
[2:1]	TYPESEL		These bits select the type of waveform.	0x0	R/W
		00	Direct write to the DAC. User code writes to the WGADACCODE register directly.		
		10	Sinusoid. Sets the WAVEGENEN bit in the AFECON register to 1 and sets TYPESEL to 2'b10. The DAC outputs a sine wave.		
		11	Trapezoid. Sets the WAVEGENEN bit in the AFECON register to 1 and sets TYPESEL to 2'b11. The DAC outputs a trapezoid wave.		
0	TRAPRSTEN		Resets the trapezoid waveform generator. The output restarts from the beginning of the Delay 1 period, with an output corresponding to DC Level 1. The reset takes effect immediately. After the trapezoid generator is reset, the bit value returns to 0.	0x0	W
		0	Disable reset of the trapezoid waveform generator.		
		1	Enable reset of the trapezoid waveform generator.		

Waveform Generator, Trapezoid DC Level 1 Register—WGDCLEVEL1

Address: 0x00002018, Reset: 0x00000000, Name: WGDCLEVEL1

Table 115. Bit Descriptions for WGDCLEVEL1

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved	0x0	R
[11:0]	TRAPDCLEVEL1		DC Level 1 value for trapezoid waveform generation	0x0	R/W

Waveform Generator, Trapezoid DC Level 2 Register—WGDCLEVEL2

Address: 0x0000201C, Reset: 0x00000000, Name: WGDCLEVEL2

Table 116. Bit Descriptions for WGDCLEVEL2

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved	0x0	R
[11:0]	TRAPDCLEVEL2		DC Level 2 value for trapezoid waveform generation	0x0	R/W

Waveform Generator, Trapezoid Delay 1 Time Register—WGDELAY1

Address: 0x00002020, Reset: 0x00000000, Name: WGDELAY1

Table 117. Bit Descriptions for WGDELAY1

Bits	Bit Name	Settings	Description	Reset	Access
[31:20]	Reserved		Reserved.	0x0	R
[19:0]	DELAY1		Delay 1 value for trapezoid waveform generation. The unit of time is the DAC update rate.	0x0	R/W

Waveform Generator, Trapezoid Slope 1 Time Register—WGSLOPE1

Address: 0x00002024, Reset: 0x00000000, Name: WGSLOPE1

Table 118. Bit Descriptions for WGSLOPE1

Bits	Bit Name	Settings	Description	Reset	Access
[31:20]	Reserved		Reserved.	0x0	R
[19:0]	SLOPE1		Slope 1 value for trapezoid waveform generation. The unit of time is the DAC update rate. For trapezoid generation, the DAC update rate is fixed to 320 kHz.	0x0	R/W

Waveform Generator, Trapezoid Delay 2 Time Register—WGDELAY2

Address: 0x00002028, Reset: 0x00000000, Name: WGDELAY2

Table 119. Bit Descriptions for WGDELAY2

Bits	Bit Name	Settings	Description	Reset	Access
[31:20]	Reserved		Reserved.	0x0	R
[19:0]	DELAY2		Delay 2 value for trapezoid waveform generation. The unit of time is the DAC update rate. For trapezoid generation, the DAC update rate is fixed to 320 kHz.	0x0	R/W

Waveform Generator, Trapezoid Slope 2 Time Register—WGSLOPE2

Address: 0x0000202C, Reset: 0x00000000, Name: WGSLOPE2

Table 120. Bit Descriptions for WGSLOPE2

Bits	Bit Name	Settings	Description	Reset	Access
[31:20]	Reserved		Reserved.	0x0	R
[19:0]	SLOPE2		Slope 2 value for trapezoid waveform generation. The unit of time is the DAC update rate. For trapezoid generation, the DAC update rate is fixed to 320 kHz.	0x0	R/W

Waveform Generator, Sinusoid Frequency Control Word Register—WGFCW

Address: 0x00002030, Reset: 0x00000000, Name: WGFCW

Table 121. Bit Descriptions for WGFCW

Bits	Bit Name	Settings	Description	Reset	Access
[31:24]	Reserved		Reserved.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[30:0]	SINEFCW		Sinusoid generator frequency control word. These bits select the output frequency of the sinusoid waveform. The output frequency (f_{OUT}) = f_{ACLK} × (SINEFCW/2^{30}). To obtain accurate DFT results and to avoid spectral leakage, f_{OUT}/(DFT input data rate/N) must be an integer. (where N is input data number of DFT (refer to the DFTNUM bit in the DFTCON register). The DFT input data rate can be different due to different input data sources (refer to the DFTINSEL bit in the DFTCON register.) Sinc3 is output as input data of DFT. The DFT input data rate = ADC output data rate(1.6 MHz or 800 kHz)/ SINC3_OSR (refer to the SINC3OSR bit in the ADCFILTERCON register). For the sinc3 bypass, refer to the SINC3BYP bit in the ADCFILTERCON register. If the DFT input data rate = 800 kHz, the ADC output data rate must be set to 800 kHz (the ADCSAMPLERATE bit in the ADCFILTERCON register = 1). The general formula is ADC_FS/SINC3_OSR/ SINC2_OSR (refer to the SINC2OSR bit in the ADCFILTERCON register). For more information, refer to the digital filter options in the High Performance ADC Circuit section.	0x0	R/W

Waveform Generator, Sinusoid Phase Offset Register—WGPHASE

Address: 0x00002034, Reset: 0x00000000, Name: WGPHASE

Table 122. Bit Descriptions for WGPHASE

Bits	Bit Name	Settings	Description	Reset	Access
[31:20]	Reserved		Reserved.	0x0	R
[19:0]	SINEOFFSET		Sinusoid phase offset. SINOFFSET, Bits[19:0] = Phase (Degrees)/360 × 2^{20}. For example, to obtain a 45° phase offset, SINOFFSET, Bits[19:0] = 45/360 × 2^{20}. This register must be set before setting the TYPESEL bit in the WGCON register and the WAVEGENEN bit in the AFECON register.	0x0	R/W

Waveform Generator, Sinusoid Offset Register—WGOFFSET

Address: 0x00002038, Reset: 0x00000000, Name: WGOFFSET

Table 123. Bit Descriptions for WGOFFSET

Bits	Bit Name	Settings	Description	Reset	Access
[31:12]	Reserved		Reserved.	0x0	R
[11:0]	SINEOFFSET		Sinusoid offset. This offset is added to the waveform generator output in sinusoid mode. This value is a signed number represented in twos complement format. This register must be set before setting the TYPESEL bit in the WGCON register and the WAVEGENEN bit in the AFECON register.	0x0	R/W

Waveform Generator - Sinusoid Amplitude Register—WGAMPLITUDE

Address: 0x0000203C, Reset: 0x00000000, Name: WGAMPLITUDE

Table 124. Bit Descriptions for WGAMPLITUDE

Bits	Bit Name	Settings	Description	Reset	Access
[31:11]	Reserved		Reserved.	0x0	R
[10:0]	SINEAMPLITUDE		Sinusoid amplitude, unsigned number. This amplitude scales the waveform generator in sinusoid mode. The DAC output voltage is determined by this value, as well as the ATTEN bit and the INAMPGNMDE bit in the DACCON register. This register must be set before setting the TYPESEL bit in the WGCON register and the WAVEGENEN bit in the AFECON register.	0x0	R/W

SPI INTERFACE

OVERVIEW

The AD5940 provides an SPI interface to facilitate configuration and control by a host microcontroller. The host controller uses the SPI to read from and write to memory, registers, and FIFOs. The AD5940 operate as a slave SPI device.

SPI PINS

The SPI connections between the host and the AD5940 are

- $\overline{CS}$—chip select.
- SCLK—serial clock.
- MOSI—serial data from the SPI master to the AD5940.
- MISO—serial data from the AD5940 to the SPI master.

Chip Select Enable

The host must connect the SPI slave enable signal to the $\overline{CS}$ input of the AD5940. To initiate an SPI transaction, the host drives $\overline{CS}$ low before the first SCLK rising edge and drives it high again after the last SCLK falling edge. The AD5940 ignores the SPI SCLK and MOSI signals while the $\overline{CS}$ input is high.

SCLK

SCLK is the serial clock driven by the host to the AD5940. The maximum clock speed is 16Mhz.

MOSI/MISO

MOSI is the data input line driven from the host to the AD5940, and MISO is the data output from the AD5940 to the host. MOSI and MISO are launched on the falling edge of SCLK and sampled on the rising edge of SCLK by the host and the AD5940, respectively. MOSI carries the data from the host to the AD5940. MISO carries the returning read data fields from the AD5940 to the host during a read transaction.

SPI OPERATION

The host is the master of the SPI. The following are the features and requirements of SPI operation:

- SCLK is always slower than the system clock on the AD5940 which is 16Mhz.
- When $\overline{CS}$ is brought low, a multiple of eight clock cycles must be generated by the host.
- Transfers over the SPI slave are always byte aligned.
- In every octet, the most significant bit (Bit 7) is transmitted and received first.
- If the $\overline{CS}$ line is brought high at any time by the host, the AD5940 is ready to accept new SPI transactions when $\overline{CS}$ is brought low again by the host. The minimum time between $\overline{CS}$ going high and going low again is t_{10}, which is specified in Table 4.

COMMAND BYTE

The first byte sent from host to the AD5940 in an SPI transaction is the command byte. The command byte specifies the SPI protocol used for the SPI transaction. The available commands are detailed in Table 126.

Table 125: SPI Commands

Command	Value	Description
SPICMD_SETADDR	0x20	Set register address for SPI transaction
SPICMD_READREG	0x6D	Specifies SPI transaction is a read transaction
SPICMD_WRITEREG	0x2D	Specifies SPI transaction is a write transaction
SPICMD_READFIFO	0x5F	Command to read FIFO.

There are two main SPI transaction protocols available on the AD5940:

1. Writing to and reading from registers
2. Reading data from the data FIFO.

WRITING TO AND READING FROM REGISTERS

Writing to and reading from a register requires two SPI transactions. The first transaction sets the register address. The second transaction is the actual read or write to the required register. The following are the steps to write to a register:

Write Command Byte and Configure address

1. Drive CS low
2. Send 8 bit command byte: SPICMD_SETADDR
3. Send 16-bit address of register to read to or write from.
4. Pull CS high

Write Data to register

1. Drive CS low
2. Send 8 bit command byte: SPICMD_WRITEREG
3. Write either 16-bit or 32-bit data to register.
4. Bring CS high

Read Data from Register

1. Drive CS low
2. Send 8 bit command byte: SPICMD_READREG
3. Transmit a dummy byte on the SPI bus to initiate a read.
4. Read returning 16-bit or 32-bit data
5. Bring CS high

READING DATA FROM THE DATA FIFO

There are two methods to read back data from the data FIFO:

1. Read DATAFIFORD register as outlined in the previous paragraph.
2. Implement a fast FIFOREAD protocol

If there are less than three results in the data FIFO, the data should be read as outlined in point 1 above. However, if there are more than three results in the FIFO a much more efficient SPI transaction protocol is implemented. The protocol is outlined below and illustrated in Figure 45

Read Data from data FIFO

1. Drive CS low
2. Send 8 bit command byte: SPICMD_READFIFO
3. Transmit six dummy bytes on SPI bus before valid data can be read back.
4. Continuously read DATAFIFORD register until only two results are left.
5. Read back last two data points using a non-zero offset.
6. Pull CS high.

The transaction protocol is shown in Figure 45. Six dummy reads are needed before valid data is returned on the APB (Arm Peripheral Bus). The diagram also shows why the last two FIFO results are read back with a non-zero offset. Note APB read C. The APB will read data C while the SPI bus is transferring data B. So assuming Read B is the last data in FIFO, ROFFSETC is set to non–zero value. Then the APB will read a different register to the DATAFIFORD. If it continues to read DATAFIFORD register, the data FIFO will underflow causing an underflow error.

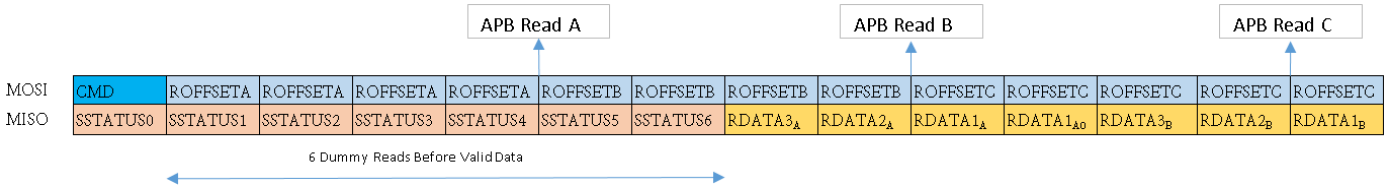

Figure 44: Data FIFO Read Protocol

SLEEP AND WAKE-UP TIMER

SLEEP AND WAKE-UP TIMER FEATURES

The AD5940 integrates a 20-bit sleep and wake-up timer. The sleep and wake-up timer provides automated control of the sequencer and can run up to eight sequences sequentially in any order from SEQ0 to SEQ3.The timer is clocked from either the internal 32 kHz oscillator clock source.

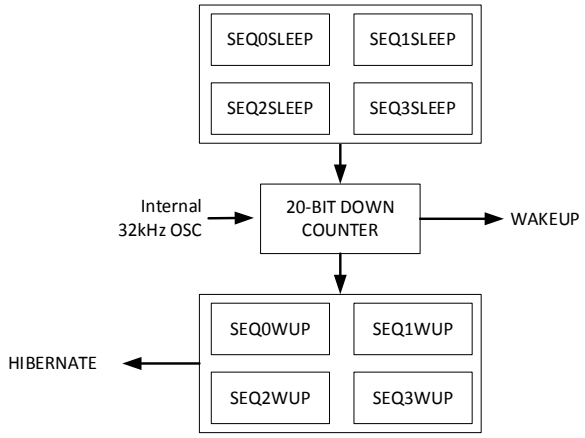

Figure 45. Sleep and Wake-Up Timer Block Diagram

SLEEP AND WAKE-UP TIMER OVERVIEW

The sleep and wake-up timer block consists of a 20-bit timer that counts down. The source clock is the 32kHz internal low frequency oscillator.

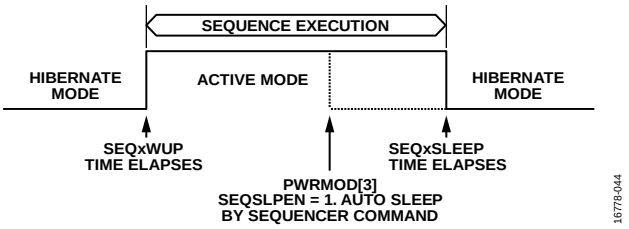

Figure 46. Sleep/Wake-Up Timing Diagram

Once the timer elapses, the device wakes up runs a sequence automatically. Up to eight sequences can be run sequentially.

When the timer elapses, the device returns to sleep. If the timer elapses before the sequence completes execution, remaining commands in the sequence are ignored. Therefore, user code must ensure that the values in the SEQxSLEEP registers are large enough to allow sequences to execute all commands.

The recommended way to use the wakeup-timer is to disable the timer sleep function PWRMOD [2] = 0 and use the sequencer to go to hibernate mode. Set PWRMOD [3] = 1 to enable the sequencer to put the part in hibernate mode.

CONFIGURING A DEFINED SEQUENCE ORDER

The sleep-wakeup timer provides a feature whereby a specific order of sequences can be executed periodically. The order in which the sequences are executed is defined in SEQORDER register. There are 8 available slots in this register, A to H. Each slot can be configured with any one of the four sequences.

Figure 49 shows an example of this feature. There are three defined sequences SEQ1, SEQ3 and SEQ4 executed according to the diagram. To configure the AD5940 to implement this the following register settings are implemented:

- SEQORDER [SEQA] = 1 (SEQ1)
- SEQORDER [SEQB] = 2 (SEQ2)
- SEQORDER [SEQC] = 3 (SEQ3)
- SEQORDER [SEQD] = 1 (SEQ1)
- CON [ENDSEQ] = 3 (End on sequence D)

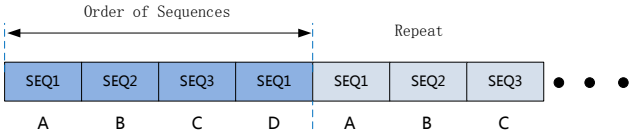

Figure 47: Sequence Order Diagram

RECOMMENDED SLEEP AND WAKE-UP TIMER OPERATION

ADI recommends to use the following procedure when using the sleep-wakeup timer to optimize performance and power consumption:

1. Disable the timer sleep function by setting PWRMOD, Bit 2 to 0. This means the sleep-wakeup timer will not put the part into hibernate. Instead, place the device in sleep mode by writing to SEQTRGSLEEP register at the end of the sequence. This optimizes power consumption.
2. Enable the timer wakeup function by setting TMRCON , Bit 0 to 1.
3. Enable the sequencer to trigger sleep by setting PWRMOD, Bit 3 to 1 and SEQSLPLOCK to 0xA47E5.
4. Set the final sequence in CON, Bits[3:1]. If only one sequence is used, select that sequence.
5. Write the sleep time and wake-up time to the SEQxSLEEPH, SEQxSLEEPL, SEQxWUPH, and SEQxWUPL registers.
6. Configure the order in which sequences are triggered by using the SEQORDER register.
7. Enable the timer by writing to CON, Bit 0 = 1.

When CON [0] = 1, the timer loads the values from the SEQxWUPH and SEQxWUPL registers and begins counting down. When the timer reaches zero, the device wakes up and begins executing sequences in the order specified in SEQORDER, Bits[1:0]. The timer loads the values from the SEQxSLEEPH and SEQxSLEEPL registers and begins counting down again while the sequencer is running. When the timer elapses, the AD5840 returns to sleep if TMRCON, Bit 0 = 1. If PWRMOD, Bit 3 = 1 the AD5940 returns to sleep at the end of the last sequence.

The maximum hibernate time is 32 sec when using the internal 32 kHz oscillator.

To calculate the code for SEQxWUPx registers use the following equation:

$$Code = ClkFreq \times Sleep\ Time$$

SLEEP AND WAKE-UP TIMER REGISTERS

Table 126. WUPTMR Register Summary

Address	Name	Description	Reset	Access
0x00000800	CON	Timer control	0x0000	R/W
0x00000804	SEQORDER	Order control	0x0000	R/W
0x00000808	SEQ0WUPL	Sequence 0 wake-up time, low (Lowest 16 bits)	0xFFFF	R/W
0x0000080C	SEQ0WUPH	Sequence 0 wake-up time, high (Highest 4 bits)	0x000F	R/W
0x00000810	SEQ0SLEEPL	Sequence 0 sleep time, low (Lowest 16 bits)	0xFFFF	R/W
0x00000814	SEQ0SLEEPH	Sequence 0 sleep time, high (Highest 4 bits)	0x000F	R/W
0x00000818	SEQ1WUPL	Sequence 1 wake-up time, low (Lowest 16 bits)	0xFFFF	R/W
0x0000081C	SEQ1WUPH	Sequence 1 wake-up time, high (Highest 4 bits)	0x000F	R/W
0x00000820	SEQ1SLEEPL	Sequence 1 sleep time, low (Lowest 16 bits)	0xFFFF	R/W
0x00000824	SEQ1SLEEPH	Sequence 1 sleep time, high (Highest 4 bits)	0x000F	R/W
0x00000828	SEQ2WUPL	Sequence 2 wake-up time, low (Lowest 16 bits)	0xFFFF	R/W
0x0000082C	SEQ2WUPH	Sequence 2 wake-up time, high (Highest 4 bits)	0x000F	R/W
0x00000830	SEQ2SLEEPL	Sequence 2 sleep time, low (Lowest 16 bits)	0xFFFF	R/W
0x00000834	SEQ2SLEEPH	Sequence 2 sleep time, high (Highest 4 bits)	0x000F	R/W
0x00000838	SEQ3WUPL	Sequence 3 wake-up time, low (Lowest 16 bits)	0xFFFF	R/W
0x0000083C	SEQ3WUPH	Sequence 3 wake-up time, high (Highest 4 bits)	0x000F	R/W
0x00000840	SEQ3SLEEPL	Sequence 3 sleep time, low (Lowest 16 bits)	0xFFFF	R/W
0x00000844	SEQ3SLEEPH	Sequence 3 sleep time, high (Highest 4 bits)	0x000F	R/W
0x00000A1C	TMRCON	Timer wake-up configuration	0x0000	R/W

Timer Control Register—CON

Address: 0x00000800, Reset: 0x0000, Name: CON

The CON register is the wake-up timer control register.

Table 127. Bit Descriptions for CON

Bits	Bit Name	Settings	Description	Reset	Access
[15:7]	Reserved		Reserved.	0x0	R
6	MSKTRG		Mark sequence trigger from the sleep and wake-up timer. This bit masks the sequence trigger from the sleep and wake-up timer. After the trigger is masked, it does not go to the sequencer.	0x0	R/W
[5:4]	RESERVED		Reserved.	0x0	R
[3:1]	ENDSEQ		End sequence. These bits select one of SEQORDER bits to end the timing sequence.	0x0	R/W
		0	The sleep and wake-up timer stops at Sequence A and then goes back to Sequence A.		
		1	The sleep and wake-up timer stops at Sequence B and then goes back to Sequence A.		
		10	The sleep and wake-up timer stops at Sequence C and then goes back to Sequence A.		
		11	The sleep and wake-up timer stops at Sequence D and then goes back to Sequence A.		
		100	The sleep and wake-up timer stops at Sequence E and then goes back to Sequence A.		
		101	The sleep and wake-up timer stops at Sequence F and then goes back to Sequence A.		
		110	The sleep and wake-up timer stops at Sequence G and then goes back to Sequence A.		
		111	The sleep and wake-up timer stops at Sequence H and then goes back to Sequence A.		
0	EN		Sleep and wake-up timer enable bit.	0x0	R/W
		0	Enables the sleep and wake-up timer.		
		1	Disables the sleep and wake-up timer.		

Order Control Register—SEQORDER

Address: 0x00000804, Reset: 0x0000, Name: SEQORDER

The SEQORDER register controls the command sequence execution order.

Table 128. Bit Descriptions for SEQORDER

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	SEQH		Sequence H configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for Timer Sequence H.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		
[13:12]	SEQG		Sequence G Configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for timer Sequence G.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		
[11:10]	SEQF		Sequence F Configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for timer Sequence F.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		
[9:8]	SEQE		Sequence E Configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for timer Sequence E.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		
[7:6]	SEQD		Sequence D Configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for timer Sequence D.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		
[5:4]	SEQC		Sequence C Configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for timer Sequence C.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		
[3:2]	SEQB		Sequence B Configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for timer Sequence B.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		

Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	SEQA		Sequence A Configuration. These bits select Command Sequence 0, Command Sequence 1, Command Sequence 2, or Command Sequence 3 for timer Sequence A.	0x0	R/W
		0	Fills in Sequence 0.		
		1	Fills in Sequence 1.		
		10	Fills in Sequence 2.		
		11	Fills in Sequence 3.		

Sequence x WTimeL (LSB Register)— SEQxWUPL

Address: 0x00000808, Reset: 0xFFFF, Name: SEQ0WUPL

Address: 0x00000818, Reset: 0xFFFF, Name: SEQ1WUPL

Address: 0x00000828, Reset: 0xFFFF, Name: SEQ2WUPL

Address: 0x00000838, Reset: 0xFFFF, Name: SEQ3WUPL

Sequence x sleep time Low period

Table 129. Bit Descriptions for SEQxWUPL

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	WAKEUPTIME0[15:0]		Sequence xsleep period. This register defines the length of time in which the device stays in sleep mode. When this time elapses, the device wakes up.	0xFFFF	R/W

Sequence x WTimeH (MSB Register)—SEQxWUPH

Address: 0x0000080C, Reset: 0x000F, Name: SEQ0WUPH

Address: 0x0000081C, Reset: 0x000F, Name: SEQ1WUPH

Address: 0x0000082C, Reset: 0x000F, Name: SEQ2WUPH

Address: 0x0000083C, Reset: 0x000F, Name: SEQ3WUPH

Sequence x sleep time High period

Table 130. Bit Descriptions for SEQxWUPH

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Reserved		Reserved.	0x0	R
[3:0]	WAKEUPTIME0[19:16]		Sequence x sleep period. This register defines the length of time in which the device stays in sleep mode. When this time elapses, the device wakes up.	0xF	R/W

Sequence x STimeL (LSB Register)—SEQxSLEEPL

Address: 0x00000810, Reset: 0xFFFF, Name: SEQ0SLEEPL

Address: 0x00000820, Reset: 0xFFFF, Name: SEQ1SLEEPL

Address: 0x00000830, Reset: 0xFFFF, Name: SEQ2SLEEPL

Address: 0x00000840, Reset: 0xFFFF, Name: SEQ3SLEEPL

The SEQxSLEEPL registers define the active time low period for Sequence 0 to Sequence 3.

Table 131. Bit Descriptions for SEQxSLEEPL

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	SLEEPTIME0[15:0]		Sequence x active period. This register defines the length of time in which the device stays in active mode. When this time elapses, the device returns to sleep.	0xFFFF	R/W

Sequence x STimeH (MSB Register)—SEQxSLEEPH

Address: 0x00000814, Reset: 0x000F, Name: SEQ0SLEEPH

Address: 0x00000824, Reset: 0x000F, Name: SEQ1SLEEPH

Address: 0x00000834, Reset: 0x000F, Name: SEQ2SLEEPH

Address: 0x00000844, Reset: 0x000F, Name: SEQ3SLEEPH

Sequence x active time high period

Table 132. Bit Descriptions for SEQxSLEEPH

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Reserved		Reserved.	0x0	R
[3:0]	SLEEPTIME0[19:16]		Sequence x active period. This register defines the length of time in which the device stays in active mode. When this time elapses, the device returns to sleep.	0xF	R/W

Wake-Up Timer Configuration Register—TMRCON

Address: 0x00000A1C, Reset: 0x0000, Name: TMRCON

Table 133. Bit Descriptions for TMRCON

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	Reserved		Reserved.	0x0	R
0	TMRINTEN		Wake-up timer enable. Set this bit before entering hibernate mode to enable the ability of the sleep and wake-up timer to wake up the chip.	0x0	R/W
		0	Wake-up timer disabled.		
		1	Wake-up timer enabled.		

INTERRUPTS

There are a number of interrupt options available on the AD5940. These interrupts can be configured to toggle a GPIOx pin in response to an interrupt event.

INTC INTERUPTS

The interrupt controller is divided into two blocks. Each block consists of an INTCSELx register and an INTCFLAGx register. The INTCPOL and INTCCLR registers are common to both blocks. After an interrupt is enabled in the INTCSELx register, the corresponding bit in the INTCFLAGx register is set. The available interrupt sources are shown in Table 135. The INTC interrupts can be configured to toggle a GPIOx pin in response to an interrupt event.

HOW TO CONFIGURE THE INTC INTERRUPTS

Before configuring the interrupt sources, the GPIOx pin must be configured as the interrupt output. GPIO0, GPIO3, and GPIO6 can be configured for the INT0 output. GPIO4 and GPIO7 can be configured for the INT1 output. Refer to the Digital Port Multiplex section for more details. The user can program the polarity of the interrupt (rising or falling edge) in the INTCPOL register. When an interrupt is triggered, the selected GPIOx pin toggles to alert the host microcontroller that an interrupt event occurred. To clear an interrupt source, write to the corresponding bit in the INTCCLR register.

INTC CUSTOM INTERRUPTS

There are four custom interrupt sources selectable by the user in INTCSELx, Bits[12:9]). These custom interrupts can generate an interrupt event by writing to the corresponding bit in the AFEGENINTSTA register. It is only possible to write to this register via the sequencer. Writing to the AFEGENINTSTA register using the SPI has no effect.

EXTERNAL INTERRUPT CONFIGURATION

Eight external interrupts are implemented on the AD5940. These external interrupts can be configured to detect any combination of the following types of events:

- Rising edge. The logic detects a transition from low to high and generates a pulse.
- Falling edge. The logic detects a transition from high to low and generates a pulse.
- Rising or falling edge. The logic detects a transition from lot to high or high to low and generates a pulse
- High level. The logic detects a high level. The interrupt line is held asserted until the external deasserts.
- Low level. The logic detects a low level. The interrupt line is held asserted until the external source deasserts.

The external interrupt detection unit block allows an external event to wake up the AD5940 when it is in hibernate mode.

Table 134. Interrupt Sources

INTCFLAGx	Interrupt Source
FLAG0	ADC result ready interrupt.
FLAG1	DFT result ready interrupt.
FLAG2	Supply rejection filter result ready interrupt.
FLAG3	Temperature measurement result ready interrupt.
FLAG4	ADC minimum value check fail interrupt.
FLAG5	ADC maximum value check fail interrupt.
FLAG6	ADC delta value check fail interrupt.
FLAG7	Mean result ready interrupt.
FLAG8	Variance result ready interrupt.
FLAG13	Boot loading done interrupt.
FLAG15	End of sequence interrupt.
FLAG16	Sequencer timeout command finished. See the Timer Command section.
FLAG17	Sequencer timeout command error interrupt. See the Timer Command section.
FLAG23	Data FIFO full interrupt.
FLAG24	Data FIFO empty interrupt.
FLAG25	Data FIFO threshold interrupt. Threshold value set in DATAFIFOTHRES register.
FLAG26	Data FIFO overflow interrupt.
FLAG27	Data FIFO underflow interrupt.
FLAG29	Outlier IRQ. Detects when an outlier is detected.
FLAG31	Tried_to_Break IRQ. Interrupt generate if a sequence B request comes in while Sequence A is running. It indicates that sequence B will be ignored

INTERRUPT REGISTERS, EXTERNAL INTERRUPT CONFIGURATION REGISTERS, AND INTERRUPT CONTROLLER

REGISTERS

Table 135. INTC Register Summary

Address	Name	Description	Reset	Access
0x00003000	INTCPOL	Interrupt polarity register	0x00000000	R/W
0x00003004	INTCCLR	Interrupt clear register	0x00000000	W
0x00003008	INTCSEL0	INT0 select register	0x00002000	R/W
0x0000300C	INTCSEL1	INT1 select register	0x00000000	R/W
0x00003010	INTCFLAG0	INT0 flag register	0x00000000	R
0x00003014	INTCFLAG1	INT1 flag register	0x00000000	R
0x0000209C	AFEGENINTSTA	Analog generation interrupt	0x00000000	R/W

Table 136. External Interrupt Register Summary

Address	Name	Description	Reset	Access
0x00000A20	EI0CON	External Interrupt Configuration 0	0x0000	R/W
0x00000A24	EI1CON	External Interrupt Configuration 1	0x0000	R/W
0x00000A28	EI2CON	External Interrupt Configuration 2	0x0000	R/W
0x00000A30	EICLR	External interrupt clear	0xC000	R/W

Interrupt Polarity Register—INTCPOL

Address: 0x00003000, Reset: 0x00000000, Name: INTCPOL

Table 137. Bit Descriptions for INTCPOL

Bits	Bit Name	Settings	Description	Reset	Access
[31:1]	Reserved		Reserved.	0x0	R
0	INTPOL		Interrupt polarity	0x0	R/W
		0	Output negative edge interrupt		
		1	Output positive edge interrupt		

Interrupt Clear Register—INTCCLR

Address: 0x00003004, Reset: 0x00000000, Name: INTCCLR

Table 138. Bit Descriptions for INTCCLR

Bits	Bit Name	Settings	Description	Reset	Access
31	INTCLR31		Attempt to break IRQ. Write 1 to clear.	0x0	W
30	Reserved		Reserved.	0x0	W
29	INTCLR29		Outlier IRQ. Write 1 to clear.	0x0	W
28	Reserved		Reserved.	0x0	W
27	INTCLR27		Data FIFO underflow IRQ. Write 1 to clear.	0x0	W
26	INTCLR26		Data FIFO overflow IRQ. Write 1 to clear.	0x0	W
25	INTCLR25		Data FIFO threshold IRQ. Write 1 to clear.	0x0	W
24	INTCLR24		Data FIFO empty IRQ. Write 1 to clear.	0x0	W
23	INTCLR23		Data FIFO full IRQ. Write 1 to clear.	0x0	W
22	Reserved		Reserved.	0x0	W
17	INTCLR17		Sequencer timeout error IRQ. Write 1 to clear.	0x0	W
16	INTCLR16		Sequencer timeout finished IRQ. Write 1 to clear.	0x0	W
15	INTCLR15		End of sequence IRQ. Write 1 to clear.	0x0	W
14	Reserved		Reserved.	0x0	W
13	INTCLR13		Boot load done IRQ. Write 1 to clear.	0x0	W
12	INTCLR12		Custom IRQ 3. Write 1 to clear.		
11	INTCLR11		Custom IRQ 2. Write 1 to clear.		
10	INTCLR10		Custom IRQ 1. Write 1 to clear.		

Bits	Bit Name	Settings	Description	Reset	Access
9	INTCLR9		Custom IRQ 0. Write 1 to clear.		
8	INTCLR8		Variance IRQ. Write 1 to clear.	0x0	W
7	INTCLR7		Mean IRQ. Write 1 to clear.	0x0	W
6	INTCLR6		ADC delta fail IRQ. Write 1 to clear.	0x0	W
5	INTCLR5		ADC max fail IRQ. Write 1 to clear.	0x0	W
4	INTCLR4		ADC min fail IRQ. Write 1 to clear.	0x0	W
3	INTCLR3		Temperature result IRQ. Write 1 to clear.	0x0	W
2	INTCLR2		Supply rejection filter result ready IRQ. Write 1 to clear.	0x0	W
1	INTCLR1		DFT result IRQ. Write 1 to clear.	0x0	W
0	INTCLR0		ADC result IRQ. Write 1 to clear.	0x0	W

INTx Select Registers—INTCSELx

Address: 0x00003008, Reset: 0x00002000, Name: INTCSEL0

Address: 0x0000300C, Reset: 0x00002000, Name: INTCSEL1

Table 139. Bit Descriptions for INTCSELx

Bits	Bit Name	Settings	Description	Reset	Access
31	INTSEL31		Attempt to break IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
30	Reserved		Reserved.	0x0	R/W
29	INTSEL29		Outlier IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
28	Reserved.		Reserved.	0x0	R/W
27	INTSEL27		Data FIFO underflow IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
26	INTSEL26		Data FIFO overflow IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
25	INTSEL25		Data FIFO Threshold IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
24	INTSEL24		Data FIFO empty IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
23	INTSEL23		Data FIFO full IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
[22:18]	Reserved.		Reserved.	0x0	R/W
17	INTSEL17		Sequencer timeout error IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
16	INTSEL16		Sequencer timeout finished IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
15	INTSEL15		End of sequence IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
14	Reserved.		Reserved.	0x0	R/W
13	INTSEL13		Bootloader done IRQ enable.	0x1	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
12	INTSEL12		Custom IRQ 3 enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
11	INTSEL11		Custom IRQ 2 enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
10	INTSEL10		Custom IRQ 1 enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
9	INTSEL9		Custom IRQ 0 enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
8	INTSEL8		Variance IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
7	INTSEL7		Mean IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
6	INTSEL6		ADC delta fail IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
5	INTSEL5		ADC maximum fail IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
4	INTSEL4		ADC minimum fail IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
3	INTSEL3		Temperature result IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
2	INTSEL2		Supply rejection filter result ready IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
1	INTSEL1		DFT result IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		
0	INTSEL0		ADC result IRQ enable.	0x0	R/W
		0	Interrupt disabled.		
		1	Interrupt enabled.		

INTx Flag Registers—INTCFLAGx

Address: 0x00003010, Reset: 0x00000000, Name: INTCFLAG0

Address: 0x00003014, Reset: 0x00000000, Name: INTCFLAG1

Table 140. Bit Descriptions for INTCFLAGx

Bits	Bit Name	Settings	Description	Reset	Access
31	FLAG31		Attempt to break IRQ status. This bit is set if a Sequence B request arrives while Sequence A is running, indicating that Sequence B is ignored.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
30	Reserved		Reserved.	0x0	R
29	FLAG29		Outlier IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
28	Reserved		Reserved.	0x0	R
27	FLAG27		Data FIFO underflow IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
26	FLAG26		Data FIFO overflow IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
25	FLAG25		Data FIFO threshold IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
24	FLAG24		Data FIFO empty IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
23	FLAG23		Data FIFO full IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
[22:18]	Reserved		Reserved.	0x0	R
17	FLAG17		Sequencer timeout error IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
16	FLAG16		Sequencer timeout finished IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
15	FLAG15		End of sequence IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
14	Reserved		Reserved.	0x0	R
13	FLAG13		Boot load done IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		

Bits	Bit Name	Settings	Description	Reset	Access
12	FLAG12		Custom IRQ 3 status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
11	FLAG11		Custom IRQ 2 status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
10	FLAG10		Custom IRQ 1 status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
9	FLAG9		Custom IRQ 0 status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
8	FLAG8		Variance IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
7	FLAG7		Mean IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
6	FLAG6		ADC delta fail IRQ status. When this bit is set, it is indicated that the difference between two consecutive ADC results is greater than the value specified by ADCDELTA. If this bit is clear, it is indicated that no difference between two consecutive ADC values greater than the limit is detected since the last time this bit was cleared.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
5	FLAG5		ADC maximum fail IRQ status. When this bit is set, it is indicated that an ADC result is above the maximum value specified by ADCMAX. If this bit is clear, it is indicated that no ADC value above the maximum is detected.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
4	FLAG4		ADC minimum fail IRQ status. When this bit is set, it is indicated that an ADC result is below the minimum value as specified by ADCMIN. If this bit is clear, it is indicated that no ADC value below the limit is detected since the last time this bit was cleared.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
3	FLAG3		Temperature result IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
2	FLAG2		Supply rejection filter result ready IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
1	FLAG1		DFT result IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		
0	FLAG0		ADC result IRQ status.	0x0	R
		0	Interrupt not asserted.		
		1	Interrupt asserted.		

Analog Generation Interrupt Register—AFEGENINTSTA

Address: 0x0000209C, Reset: 0x00000000, Name: AFEGENINTSTA

The AFEGENINTSTA register provides custom interrupt generation. Writing to this register is only possible using the sequencer. Writing to this register using the SPI has no effect. Reading this register using the SPI does not return meaningful data.

Table 141. Bit Descriptions for AFEGENINTSTA

Bits	Bit Name	Settings	Description	Reset	Access
[31:4]	Reserved		Reserved.	0x0	R
3	CUSTOMINT3		General-Purpose Custom Interrupt 3. Set this bit manually using the sequencer program. Write 1 to this bit to trigger an interrupt.	0x0	R/W1C
2	CUSTOMINT2		General-Purpose Custom Interrupt 2. Set this bit manually using the sequencer program. Write 1 to this bit to trigger an interrupt.	0x0	R/W1C
1	CUSTOMINT1		General-Purpose Custom Interrupt 1. Set this bit manually using the sequencer program. Write 1 to this bit to trigger an interrupt.	0x0	R/W1C
0	CUSTOMINT0		General-Purpose Custom Interrupt 0. Set this bit manually using the sequencer program. Write 1 to this bit to trigger an interrupt.	0x0	R/W1C

External Interrupt Configuration 0 Register—EI0CON

Address: 0x00000A20, Reset: 0x0000, Name: EI0CON

Table 142. Bit Descriptions for EI0CON

Bits	Bit Name	Settings	Description	Reset	Access
15	IRQ3EN		External Interrupt 3 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO3 to wake up the device.	0x0	R/W
		0	External Interrupt 3 disabled.		
		1	External Interrupt 3 enabled.		
[14:12]	IRQ3MDE		External Interrupt 3 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		
11	IRQ2EN		External Interrupt 2 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO2 to wake up the device.	0x0	R/W
		0	External Interrupt 2 disabled.		
		1	External Interrupt 2 enabled.		
[10:8]	IRQ2MDE		External Interrupt 2 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		
7	IRQ1EN		External Interrupt 1 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO1 to wake up the device.	0x0	R/W
		0	External Interrupt 1 disabled.		
		1	External Interrupt 1 enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
[6:4]	IRQ1MDE		External Interrupt 1 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		
3	IRQOEN		External Interrupt 0 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO0 to wake up the device.	0x0	R/W
		0	External Interrupt 0 disabled.		
		1	External Interrupt 0 enabled.		
[2:0]	IRQ0MDE		External Interrupt 0 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		

External Interrupt Configuration 1 Register—EI1CON

Address: 0x00000A24, Reset: 0x0000, Name: EI1CON

Table 143. Bit Descriptions for EI1CON

Bits	Bit Name	Settings	Description	Reset	Access
15	IRQ7EN		External Interrupt 7 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO7 to wake up the device.	0x0	R/W
		0	External Interrupt 7 disabled.		
		1	External Interrupt 7 enabled.		
[14:12]	IRQ7MDE		External Interrupt 7 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		
11	IRQ6EN		External Interrupt 6 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO6 to wake up the device.	0x0	R/W
		0	External Interrupt 6 disabled.		
		1	External Interrupt 6 enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
[10:8]	IRQ6MDE		External Interrupt 6 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		
7	IRQ5EN		External Interrupt 5 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO5 to wake up the device.	0x0	R/W
		0	External Interrupt 5 disabled.		
		1	External Interrupt 5 enabled.		
[6:4]	IRQ5MDE		External Interrupt 5 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		
3	IRQ4EN		External Interrupt 4 enable bit. Set this bit before placing the device in hibernate mode to enable the ability of GPIO4 to wake up the device.	0x0	R/W
		0	External Interrupt 4 disabled.		
		1	External Interrupt 4 enabled.		
[2:0]	IRQ4MDE		External Interrupt 4 mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		

External Interrupt Configuration 2 Register—EI2CON

Address: 0x00000A28, Reset: 0x0000, Name: EI2CON

Table 144. Bit Descriptions for EI2CON

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Reserved		Reserved.	0x0	R
3	BUSINTEN		Bus interrupt detection enable bit. Set this bit before placing the device in hibernate mode to enable the ability of the SPI to wake up the device.	0x0	R/W
		0	Bus interrupt wakeup disabled.		
		1	Bus interrupt wakeup enabled.		
[2:0]	BUSINTMDE		Bus interrupt detection mode bits.	0x0	R/W
		000	Rising edge.		
		001	Falling edge.		
		010	Rising or falling edge.		
		011	High level.		
		100	Low level.		
		101	Falling edge (same as 001).		
		110	Rising or falling edge (same as 010).		
		111	High level (same as 011).		

External Interrupt Clear Register—EICLR

Address: 0x00000A30, Reset: 0xC000, Name: EICLR

Table 145. Bit Descriptions for EICLR

Bits	Bit Name	Settings	Description	Reset	Access
15	AUTCLRBUSEN		Enable autoclear of bus interrupt. Set this bit to 1 to enable autoclear.	0x1	R/W
14	AUTCLRIRQEN		Enable autoclear of External Interrupt 0 to External Interrupt 7. Set this bit to 1 to enable autoclear.	0x1	R/W
[13:9]	Reserved		Reserved.	0x0	R
8	BUSINT		Bus interrupt. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
7	IRQ7		External Interrupt 7. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
6	IRQ6		External Interrupt 6. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
5	IRQ5		External Interrupt 5. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
4	IRQ4		External Interrupt 4. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
3	IRQ3		External Interrupt 3. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
2	IRQ2		External Interrupt 2. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
1	IRQ1		External Interrupt 1. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W
0	IRQ0		External Interrupt 0. Set this bit to 1 to clear an internal interrupt flag. This bit is cleared automatically by the hardware.	0x0	R/W

DIGITAL INPUTS/OUTPUTS

DIGITAL INPUTS/OUTPUTS FEATURES

The AD5940 features eight GPIO pins. The GPIOs are grouped in one port, GP0, which is 8-bits wide. Each GPIO contains multiple functions that are configurable by user code.

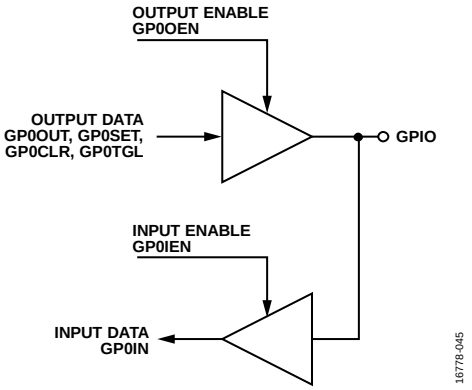

Figure 48. Digital Input/Output Diagram

DIGITAL INPUTS/OUTPUTS OPERATION

Input/Output Pull-Up Enable

GPIO pull-up resistors are enabled or disabled using the GP0PE register. Writing 1 to bits 0-7 enables the pull-up on corresponding GPIO. Clearing bits disables the pull-up on corresponding GPIO.

Input/Output Data Input

When the GPIOs are configured as inputs using the GP0IEN register, the GPIO input levels are available in the GP0IN register

Input/Output Data Output

When the GPIOs are configured as outputs, the values in the GP0OUT register are reflected on the GPIOs.

Bit Set

The GPIO port has a corresponding bit set register, GP0SET. Using the bit set register, it is possible to set one or more GPIO data outputs without affecting other outputs within the port. Only the GPIO corresponding to the write data bit equal to 1 is set. The remaining GPIOs are unaffected.

Bit Clear

GP0 has a corresponding bit clear register, GP0CLR. Use the bit clear register to clear one or more GPIO data outputs without affecting other outputs within the port. Only the GPIO corresponding to the write data bit equal to 1 is cleared. The remaining GPIOs are unaffected.

Bit Toggle

GP0 has a corresponding bit toggle register, GP0TGL. Using the bit toggle register, it is possible to invert one or more GPIO data outputs without affecting other outputs within the port. Only the GPIO corresponding to the write data bit equal to 1 are toggled. The remaining GPIOs are unaffected.

Input/Output Data Output Enable

GP0 has a data output enable register, GP0OEN, by which the data output path is enabled. When the data output enable register bits are set, the values in GP0OUT are reflected on the corresponding GPIOx pins.

Interrupt Inputs

Each GPIOx pin can be configured to react to external events. These events can be detected and used to wake up the device or to trigger specific sequences. These events are configured in the EIxCON register. Writing to the corresponding bit in the EICLR register clears the interrupt flag. For further information, see the Interrupts section.

Interrupt Outputs

The AD5940 has two external interrupts that can be mapped to certain GPIOx pins (see the GPOCON register). When an interrupt occurs, the AD5940 sets the GPIOx pin high. When the interrupt is cleared, the AD5940 brings the GPIO pin low. These interrupts are configured in the interrupt controller register (see the Interrupts section).

GPIOx Control with the Sequencer

Each GPIOx on the AD5940 can be controlled via the sequencer. This control allows syncing of external devices during timing critical applications using a dedicated register, SYNCEXTDEVICE. To control the GPIOs via this register, the GPIOx must first be configured as an output in GP0OEN and sync must be selected in the GP0CON register.

Digital Port Multiplex

The digital port multiplex block provides control over the GPIO functionality of the specified pins. These options are configured in the GP0CON register.

Table 146. GPIOx Multiplex Options

	Configuration Modes			
GPIOx	**0**	**1**	**10**	**11**
GP0	INT0	TRIG0	SYNC0	GPIO
GP1	GPIO	TRIG1	SYNC1	SLEEPDEEP
GP2	PORB	TRIG2	SYNC2	EXTCLK
GP3	GPIO	TRIG3	SYNC3	INT0
GP4	GPIO	TRIG0	SYNC4	INT1
GP5	GPIO	TRIG1	SYNC5	EXTCLK
GP6	GPIO	TRIG2	SYNC6	INT0

GP7	GPIO	TRIG3	SYNC7	INT1

GPIO REGISTERS

Table 147. GPIO Register Summary

Address	Name	Description	Reset	Access
0x00000000	GP0CON	GPIO Port 0 configuration	0x0000	R/W
0x00000004	GP0OEN	GPIO Port 0 output enable	0x0000	R/W
0x00000008	GP0PE	GPIO Port 0 pull-up/pull-down enable	0x0000	R/W
0x0000000C	GP0IEN	GPIO Port 0 input path enable	0x0000	R/W
0x00000010	GP0IN	GPIO Port 0 registered data input	0x0000	R
0x00000014	GP0OUT	GPIO Port 0 data output	0x0000	R/W
0x00000018	GP0SET	GPIO Port 0 data output set	0x0000	W
0x0000001C	GP0CLR	GPIO Port 0 data out clear	0x0000	W
0x00000020	GP0TGL	GPIO Port 0 pin toggle	0x0000	W

GPIO Port 0 Configuration Register—GP0CON

Address: 0x00000000, Reset: 0x0000, Name: GP0CON

The GP0CON register configures GPIO Port 0 (GPIO0).

Table 148. Bit Descriptions for GP0CON

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	PIN7CFG		GPIO7configuration bits.	0x0	R/W
		00	General-purpose input/output.		
		01	Sequence 3 trigger signal input from the MCU side.		
		10	Synchronizes External Device 7 output signal.		
		11	Interrupt 1 output.		
[13:12]	PIN6CFG		GPIO6 configuration bits.	0x0	R/W
		00	General-purpose input/output.		
		01	Sequence 2 trigger signal input from the MCU side.		
		10	Synchronizes External Device 6 output signal.		
		11	Interrupt 0 output.		
[11:10]	PIN5CFG		GPIO5 configuration bits.	0x0	R/W
		00	General-purpose input/output.		
		01	Sequence 1 trigger signal input from the MCU side.		
		10	Synchronizes External Device 5 output signal.		
		11	External clock input (EXTCLK).		
[9:8]	PIN4CFG		GPIO4 configuration bits.	0x0	R/W
		00	General-purpose input/output.		
		01	Sequence 0 trigger signal input from the MCU side.		
		10	Synchronizes External Device 4 output signal.		
		11	Interrupt 1 output.		
[7:6]	PIN3CFG		GPIO3 configuration bits.	0x0	R/W
		00	General-purpose input/output.		
		01	Sequence 3 trigger signal input from the MCU side.		
		10	Synchronizes External Device 3 output signal.		
		11	Interrupt 0 output.		
[5:4]	PIN2CFG		GPIO2 configuration bits.	0x0	R/W
		00	Power on reset signal output (PORB).		
		01	Sequence 2 trigger signal input from the MCU side.		
		10	Synchronizes External Device 2 output signal.		
		11	External clock input (EXTCLK).		

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	PIN1CFG		GPIO1 configuration bits.	0x0	R/W
		00	General-purpose input/output.		
		01	Sequence 1 trigger signal input from the MCU side.		
		10	Synchronizes External Device 1 output signal.		
		11	Deep sleep. Sleep flag that indicating that the AD5940 is in hibernate mode. Used when reading data FIFO. When the MCU receives the FIFO full/almost full interrupt, it waits for this pin to go high. Then, the MCU wakes the AD5940 and reads data FIFO. After data FIFO is read, the MCU sends a command to put the AD5940 back in sleep mode.		
[1:0]	PIN0CFG		GPIO0 configuration bits.	0x0	R/W
		00	Interrupt 0 output.		
		01	Sequence 0 trigger signal input from the MCU side.		
		10	Synchronizes External Device 0 output signal.		
		11	General-purpose input/output.		

GPIO Port 0 Output Enable Register—GP0OEN

Address: 0x00000004, Reset: 0x0000, Name: GP0OEN

The GP0OEN register enables GPIO Port 0 output.

Table 149. Bit Descriptions for GP0OEN

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:0]	OEN		Pin output drive enable. Each bit in this range is set to enable the output for that particular pin. Each bit is cleared to disable the output for each pin.	0x0	R/W

GPIO Port 0 Pull-Up and Pull-Down Enable Register—GP0PE

Address: 0x00000008, Reset: 0x0000, Name: GP0PE

Table 150. Bit Descriptions for GP0PE

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:0]	PE		Pin pull enable. Each bit in this range is set to enable the pull-up and/or pull-down for that particular pin. Each bit is cleared to disable the pull-up/pull-down for each pin.	0x0	R/W

GPIO Port 0 Input Path Enable Register

Address: 0x0000000C, Reset: 0x0000, Name: GP0IEN

GPIO Port 0 Input Enable

Table 151. Bit Descriptions for GP0IEN

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	RESERVED		Reserved.	0x0	R
[7:0]	IEN		Input Path Enable. Each bit is set to enable the input path and cleared to disable the input path for the GPIO pin.	0x0	R/W

GPIO Port 0 Registered Data Input

Address: 0x00000010, Reset: 0x0000, Name: GP0IN

GPIO Port 0 Registered Data Input

Table 152. Bit Descriptions for GP0IN

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:0]	In		Registered data input. Each bit reflects the state of the GPIO pin if the corresponding input buffer is enabled. If the pin input buffer is disabled the value seen is zero.	0x0	R

GPIO Port 0 Data Output Register

Address: 0x00000014, Reset: 0x0000, Name: GP0OUT

GPIO Port 0 Data Output

Table 153. Bit Descriptions for GP0OUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:0]	Out		Data out. Set by user code to drive the corresponding GPIO high. Cleared by user to drive the corresponding GPIO low.	0x0	R/W

GPIO Port 0 Data Out Set Register

Address: 0x00000018, Reset: 0x0000, Name: GP0SET

GPIO Port 0 Data Out Set

Table 154. Bit Descriptions for GP0SET

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:0]	Set		Set the Output HIGH. Set by user code to drive the corresponding GPIO high. Clearing this bit has no effect.	0x0	W

GPIO Port 0 Data Out Clear Register

Address: 0x0000001C, Reset: 0x0000, Name: GP0CLR

GPIO Port 0 Data Out Clear

Table 155. Bit Descriptions for GP0CLR

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:0]	CLR		Set the Output LOW. Each bit is set to drive the corresponding GPIO pin low. Clearing this bit has no effect.	0x0	W

GPIO Port 0 Pin Toggle Register

Address: 0x00000020, Reset: 0x0000, Name: GP0TGL

GPIO Port 0 Pin Toggle

Table 156. Bit Descriptions for GP0TGL

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved	0x0	R
[7:0]	TGL		Toggle the Output. Each bit is set to invert the corresponding GPIO pin. Clearing this bit has not effect.	0x0	W

SYSTEM RESETS

The AD5940 provides the following reset sources:

- External reset.
- Power-on reset (POR).
- Software reset of the digital part of the device. The low power potentiostat and LPTIA circuitry is not reset.

The AD5940 is reset during an external hardware reset or power cycle (POR).

The external reset or hardware reset is connected to the external $\overline{\text{RESET}}$ pin. When this pin is pulled low, a reset occurs. All circuits and control registers return to their default state.

The host microcontroller can trigger a software reset to the AD5940 by clearing SWRSTCON, Bit 0.

The AD5940 reset status register is RSTSTA. This register can be read to identify the source of the reset to the chip.

Software resets can be bypassed to ensure the circuits used to bias an external sensor are not disturbed. These circuits include the ultra low power DACs, potentiostat, and TIA amplifiers. The programmable switches circuits can also be configured to maintain their states in the event of a reset.

ANALOG DIE RESET REGISTERS

Key Register for SWRSTCON—MKEY

Address: 0x00000434, Reset: 0x0000, Name: MKEY

Table 157. Bit Descriptions for MKEY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	Key		Write 0xA51F to this register to unlock the SWRSTCON register. Write 0x000 to lock the SWRSTCON register..	0x0	W

Key Protection for the RSTCON Register—RSTCONKEY

Address: 0x00000A5C, Reset: 0x0000, Name: RSTCONKEY

Table 158. Bit Descriptions for RSTCONKEY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	KEY		Reset control key register. RSTCON is key protected with value 0x12EA. Write to the RSTCON register after the key is entered. A write to any other register before writing to RSTCON returns the protection to the lock state.	0x0	W

Software Reset Register—SWRSTCON

Address: 0x00000424, Reset: 0x0001, Name: SWRSTCON

Table 159. Bit Descriptions for SWRSTCON

Bits	Bit Name	Settings	Description	Reset	Access
[15:1]	Reserved		Reserved.	0x0	R
0	SWRSTL		Software reset. Write to the MKEY register to unlock this register.	0x1	R/W
		0	Not reset.		
		0xA158	Trigger reset.		

Reset Status Register—RSTSTA

Address: 0x00000A40, Reset: 0x0000, Name: RSTSTA

Table 160. Bit Descriptions for RSTSTA

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Reserved		Reserved.	0x0	R
3	MMRSWRST		MMR software reset. This bit is automatically set to 1 when writing the SWRSTCON register. Clear this bit by writing 1.	0x0	R/W1C
2	Reserved		Reserved.	0x0	R/W1C
1	EXTRST		External reset. This bit is automatically set to 1 when an external reset occurs. Clear this bit by writing 1.	0x0	R/W1C
0	POR		AFE power-on reset. This bit is automatically set when a power-on reset occurs. Clear this bit by writing 1.	0x0	R/W1C

POWER MODES

There are four main power modes for the AD5940:

- Active high power mode (>80 kHz).
- Active normal mode (<80 kHz).
- Hibernate.
- Shutdown.

ACTIVE HIGH POWER MODE (>80 kHz)

Active high power mode (>80 kHz) is recommended when generating or measuring high bandwidth signals greater than 80 kHz. The 32 MHz oscillator is selected to drive the high speed DAC and ADC circuits to handle the high bandwidth signal. To enable high power, mode use the following sequence:

1. Write PMBW = 0x000D.
2. Set the system clock divider to 2 and the ADC clock divider to 1.
3. Switch the oscillator to 32 MHz.
4. Set ADCFILTERCON, Bit 0 = 1 to enable a 1.6 MHz ADC sample rate.

ACTIVE LOW POWER MODE (<80 kHz)

Active low power mode (<80 kHz) is the default active state. The system clock is the 16 MHz internal oscillator (PWRMOD, Bits[1:0] = 0x1).

HIBERNATE MODE

When the AD5940 is in hibernate mode, the high speed clock circuits are powered down, resulting in all blocks being clocked when entering a low power, clock gated state. The 32 kHz oscillator remains active. The watchdog timer is also active. To place the AD5940 in hibernate mode, write PWRMOD, Bits[1:0] = 0x2. It is recommended that PWRMOD, Bit 14 = 0. Bit 14 controls a power switch to the ADC block. When this switch is turned off, the leakage from the ADC is reduced, which sub-sequently reduces the current consumption in hibernate mode.

Optionally the low power DAC, reference and amplifiers can remain active to maintain the bias of an external sensor. However, current consumption increases.

SHUTDOWN

Shutdown mode is similar to hibernate, except the user is expected to power down the low power analog blocks which includes, the low power DAC, low power TIA, low power reference and low power potentiostat.

LOW POWER MODE

The AD5940 provides a useful feature for ultra low power applications, such as EDA measurements. Various blocks can be powered down simultaneously by writing to the LPMODECON register. Within LPMODECON, there are a number of bits corresponding to certain analog blocks. By setting these bits to 1, the corresponding piece of circuitry is powered down to save power. For example, writing 1 to LPMODECON, Bit 1, powers down the high power reference.

The LPMODECON register features key protection. Before accessing the register, the user must write 0xC59D6 to LPMODEKEY.

Another feature that is useful in ultra low power applications is the ability to switch system clocks to the 32 kHz oscillator using the sequencer. To enable this feature, write 1 to LFSYSCLKEN, Bit 0. The sequencer then has the ability to switch system clocks to the 32 kHz oscillator. The LFSYSCLKEN register is key protected by LPMODKEY.

POWER MODES REGISTERS

Power Modes Register—PWRMOD

Address: 0x00000A00, Reset: 0x0001, Name: PWRMOD

Table 161. Bit Descriptions for PWRMOD

Bits	Bit Name	Settings	Description	Reset	Access
15	RAMRETEN		Retention for RAM.	0x0	R/W
		0	RAM is not retained during hibernate mode.		
		1	RAM is retained during hibernate mode.		
14	ADCRETEN		This bit keeps the ADC power switch on in hibernate mode.	0x0	R/W
		0	ADC power switch turned off during hibernate mode.		
		1	ADC power switch turned on during hibernate mode.		
[13:4]	Reserved		Reserved.	0x0	R
3	SEQSLPEN		Autosleep function by sequencer command.	0x0	R/W
		0	Disables the sequencer autosleep function.		
		1	Enables the sequencer autosleep function.		
2	TMRSLPEN		Autosleep function by sleep and wake-up timer.	0x0	R/W
		0	Disables the sleep and wake-up timer autosleep function.		
		1	Enables the sleep and wake-up timer autosleep function.		

Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	PWRMOD		Power mode control bits. When read, these bits contain the last power mode value entered by user code.	0x1	R/W
		01	Active mode. Normal working mode. All digital circuits powered up. The user can optionally power down blocks by disabling their input clock.		
		10	Hibernate mode. Digital core powered down. Most AFE die blocks powered down (low power DACs and references may remain active to bias an external sensor(s)). SRAM is powered down, with or without retention. The high speed clock is powered down. Only the low speed clock is powered up.		
		11	Reserved.		

Key Protection for the PWRMOD Register—PWRKEY

Address: 0x00000A04, Reset: 0x0000, Name: PWRKEY

Table 162. Bit Descriptions for PWRKEY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PWRKEY		PWRMOD key register. The PWRMOD register is key protected. Two writes to the key are necessary to change the value in the PWRMOD register: first 0x4859, then 0xF27B. Then, write to the PWRMOD register. A write to any other register before writing to PWRMOD returns the protection to the lock state.	0x0	R/W

Low Power Mode AFE Control Lock Register—LPMODEKEY

Address: 0x0000210C, Reset: 0x00000000, Name: LPMODEKEY

The LPMODEKEY register protects the LFSYSCLKEN and LPMODECON registers.

Table 163. Bit Descriptions for LPMODEKEY

Bits	Bit Name	Settings	Description	Reset	Access
[31:20]	Reserved		Reserved.	0x0	R
[19:0]	Key		These bits are the key for low power mode control by the sequencer related registers. The key prevents accidental writing to the registers.	0x0	R/W
		0xC59D6	Clocks related registers via a sequencer write.		
		0x00000	Locks the clock related registers via a sequencer write. Write any value other than 0xC59D6 to lock the sequencer read/write clock related registers.		

Low Power Mode Clock Select Register—LPMODECLKSEL

Address: 0x00002110, Reset: 0x00000000, Name: LPMODECLKSEL

The LPMODECLKSEL register is protected by LPMODKEY.

Table 164. Bit Descriptions for LPMODECLKSEL

Bits	Bit Name	Settings	Description	Reset	Access
[31:1]	Reserved		Reserved.	0x0	R
0	LFSYSCLKEN		Enable for switching the system clock to 32 kHz via the sequencer. Write 1 to this bit to switch to the 32 kHz oscillator. Clear this bit to switch to the 16 MHz oscillator.	0x0	R/W

Low Power Mode Configuration Register—LPMODECON

Address: 0x00002114, Reset: 0x00000102, Name: LPMODECON

The LPMODECON register is protected by LPMODEKEY.

Table 165. Bit Descriptions for LPMODECON

Bits	Bit Name	Settings	Description	Reset	Access
[31:9]	Reserved		Reserved	0x0	R
8	ALDOEN		Set this bit high to power down the analog LDO	0x1	R/W
7	V1P1HSADCEN		Set this bit high to enable the 1.11 V high speed common-mode buffer	0x0	R/W
6	V1P8HSADCEN		Set this bit high to enable the high speed 1.82 V reference buffer	0x0	R/W
5	PTATEN		Set this bit high to generate PTAT current bias	0x0	R/W
4	ZTATEN		Set this bit high to generate ZTAT current bias	0x0	R/W
3	REPEATADCCNVEN_P		Set this bit high to enable the repetition of ADC conversions	0x0	R/W
2	ADCCONVEN		Set this bit high to enable ADC conversions	0x0	R/W
1	HSREFDIS		Set this bit high to power down the high speed reference	0x1	R/W
0	HFOSCPD		Set this bit high to power down the high speed power oscillator	0x0	R/W

Power Mode Configuration Register—PMBW

Address: 0x000022F0, Reset: 0x00088800, Name: PMBW

The power mode configuration register, PMBW, configures the high and low power system modes for the high speed DAC and ADC circuits.

Table 166. Bit Descriptions for PMBW

Bits	Bit Name	Settings	Description	Reset	Access
[31:4]	Reserved		Reserved	0x8880	R
[3:2]	SYSBW		System bandwidth configure. The RCF of the high speed DAC and the AAF bandwidth configuration of the ADC are configured by a single register.	0x0	R/W
		00	No action for system configuration. The RCF and AAF are automatically configured according to the waveform generator frequency.		
		01	50 kHz, −3 dB bandwidth.		
		10	100 kHz, −3 dB bandwidth.		
		11	250 kHz ,−3 dB bandwidth.		
1	Reserved		Reserved.	0x0	R
0	SYSHS		Sets the high speed DAC and ADC in high power mode.	0x0	R/W
		0	Low power mode. Clear this bit for impedance measurements of <80 kHz.		
		1	High speed mode. Set this bit for impedance measurements of >80 kHz.		

CLOCKING ARCHITECTURE

CLOCK FEATURES

The AD5940 features the following clock options:

- A low frequency, 32 kHz internal oscillator (LFOSC).
- A high frequency, 16 MHz or 32 MHz internal oscillator (HFOSC). The 32 MHz setting is only intended to clock the high speed DAC to output signals >80 kHz, especially for high frequency impedance measurements.
- An external 16 MHz/32 MHz crystal option. If the 32 MHz crystal is used, ensure that CLKCON0, Bits[9:6] = 2 to limit the ADC and digital die clock sources to 16 MHz.
- An external clock input option on GPIO2. If the 32 MHz clock is used, ensure that CLKCON0, Bits[9:6] = 2 to limit the ADC and digital die clock sources to 16 MHz.

At power-up, the internal high frequency oscillator is selected as the AFE system clock with a 16 MHz setting. User code can divide the clock by a factor of 1 to 32 to reduce power consumption.

Note that the system performance is only validated with AFE system clock rates of 32 MHz and 16 MHz.

The clock architecture diagram is shown in Figure 49.

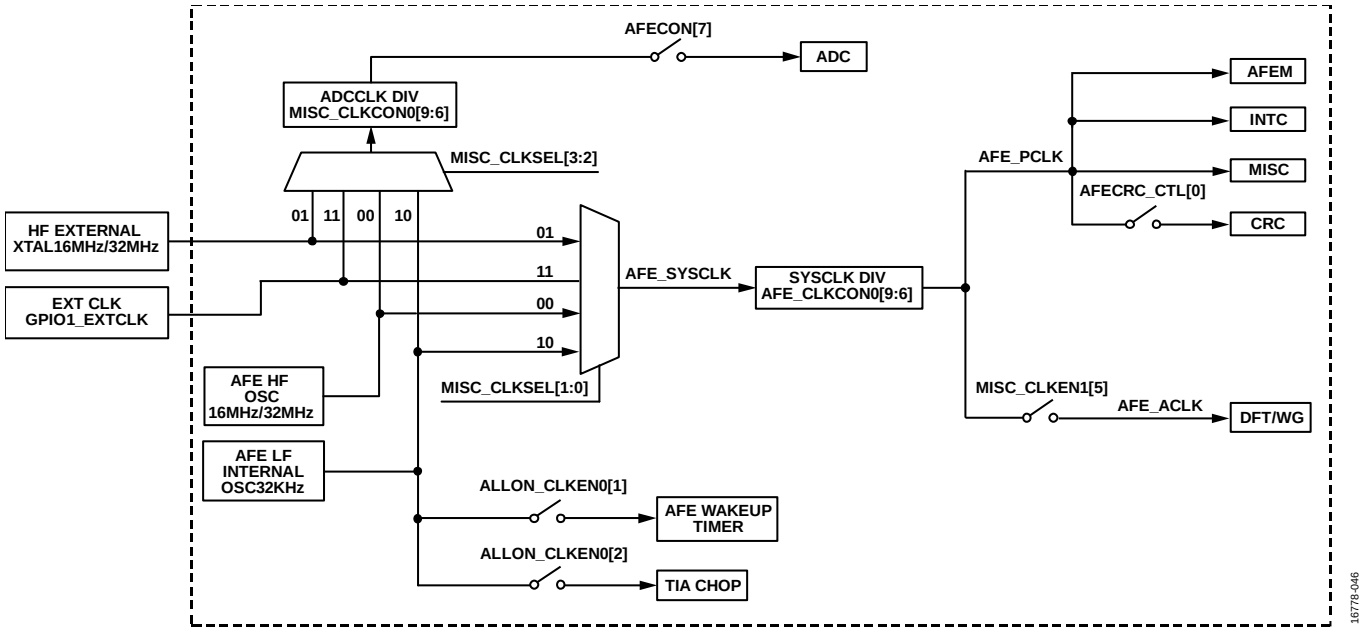

Figure 49. AD5940 System Clock Architecture

CLOCK ARCHITECTURE REGISTERS

Table 167. Clock Register Summary

Address	Name	Description	Reset	Access
0x00000420	CLKCON0KEY	Key protection register for CLKCON0	0x0000	W
0x00000408	CLKCON0	Clock divider configuration	0x0441	R/W
0x00000414	CLKSEL	Clock select	0x0000	R/W
0x00000A70	CLKEN0	Clock control of the low power TIA chop and wake-up timers	0x0000	R/W
0x00000410	CLKEN1	Clock gate enable	0x010A	R/W
0x00000A0C	OSCKEY	Key protection for OSCCON	0x0000	R/W
0x00000A10	OSCCON	Oscillator control	0x0003	R/W
0x000C20BC	HSOSCCON	High power oscillator configuration	0x0024	R/W
0x0000005C	RSTCONKEY	Key protection for the RSTCON register	0x0000	W
0x0000006C	LOSCTST	Internal low frequency oscillator test	0x008F	R/W

Key Protection Register for the CLKCON0 Register—CLKCON0KEY

Address: 0x00000420, Reset: 0x0000, Name: CLKCON0KEY

Table 168. Bit Descriptions for CLKCON0KEY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]			Write 0xA815 to this register before accessing CLKCON0	0x0	W

Clock Divider Configuration Register—CLKCON0

Address: 0x00000408, Reset: 0x0441, Name: CLKCON0

Table 169. Bit Descriptions for CLKCON0

Bits	Bit Name	Settings	Description	Reset	Access
[15:10]	Reserved		Reserved. Do not write to these bits.	0x1	R/W
[9:6]	ADCCLKDIV		ADC clock divider configuration. The ADC clock divider provides a divided clock from a 16 MHz root clock that drives the ADC clock. The ADC clock frequency (f_{ADC}) = root clock/ADCCLKDIVCNT. The value range is from 1 to 15. Values of 0 and 1 have the same results as divide by 1. f_{ADC} must be ≤ 32 MHz. The ADC is only evaluated with a 16 MHz and 32 MHz ADC clock.	0x1	R/W
[5:0]	SYSCLKDIV		System clock divider configuration. The system clock divider provides a divided clock from a 16 MHz root clock that drives most digital peripherals. The system clock frequency (f_{SYS}) = root clock/SYSCLKDIVCNT. The value range is from 1 to 32. Values larger than 32 are saturated to 32. Values of 0 and 1 have the same results as divide by 1. f_{SYS} must be ≤ 16 MHz.	0x1	R/W

Clock Select Register—CLKSEL

Address: 0x00000414, Reset: 0x0000, Name: CLKSEL

Table 170. Bit Descriptions for CLKSEL

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Reserved		Reserved.	0x0	R
[3:2]	ADCCLKSEL		Selects the ADC clock source.	0x0	R/W
		0	Internal high frequency oscillator clock.		
		1	External high frequency crystal clock.		
		10	Internal low frequency oscillator clock (not recommended).		
		11	External clock.		
[1:0]	SYSCLKSEL		Selects system clock source.	0x0	R/W
		0	Internal high frequency oscillator clock.		
		1	External high frequency crystal clock.		
		10	Internal low frequency oscillator clock (not recommended).		
		11	External clock.		

Clock Enable for Low Power TIA Chop and Wake-Up Timer—CLKEN0

Address: 0x00000070, Reset: 0x0004, Name: CLKEN0

Table 171. Bit Descriptions for CLKEN0

Bits	Bit Name	Settings	Description	Reset	Access
[15:3]	Reserved		Reserved.	0x0	R
2	TIACHSDIS		TIA chop clock disable.	0x1	R/W
		0	Turn on TIA chop clock.		
		1	Turn off TIA chop clock.		
1	SLPWUTDIS		Sleep/wake-up timer clock disable.	0x0	R/W
		0	Turn on sleep wake up timer clock.		
		1	Turn off sleep wake up timer clock.		
0	Reserved		Reserved.	0x0	R/W

Clock Gate Enable Register—CLKEN1

Address: 0x00000410, Reset: 0x010A, Name: CLKEN1

Table 172. Bit Descriptions for CLKEN1

Bits	Bit Name	Settings	Description	Reset	Access
[15:10]	Reserved		Reserved.	0x0	R
9	Reserved		Reserved. Never write to this bit. Leave this bit cleared to 0.	0x0	R/W
8	Reserved		Reserved. Never write to this bit.	0x1	R/W
[7:6]	Reserved		Reserved. Always leave at 1. Never write to these bits.	0x0	R/W
5	ACLKDIS		ACLK clock enable. This bit controls the AFEM control clock, including the analog interface and digital signal processing.	0x0	R/W
		1	Turn on ACLK clock.		
		0	Turn off ACLK clock.		
4	Reserved		Reserved. Always leave at 0. Never write to this bit.	0x0	R/W
3	Reserved		Reserved. Always leave at 1. Never write to this bit.	0x1	R/W
2	Reserved		Reserved. Always leave at 0. Never write to this bit.	0x0	R/W
1	Reserved		Reserved. Always leave at 0. Never write to this bit.	0x1	R/W
0	Reserved		Reserved. Always leave at 1. Never write to this bit.	0x0	R/W

Key Protection for the OSCCON Register—OSCKEY

Address: 0x00000A0C, Reset: 0x0000, Name: OSCKEY

Table 173. Bit Descriptions for OSCKEY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	OSCKEY		Oscillator control key register. The OSCCON register is key protected. OSCKEY must be written to with a value of 0xCB14 before accessing the OSCCON register. A write to any other register before writing to OSCCON returns the protection to the lock state.	0x0	R/W

Oscillator Control Register—OSCCON

Address: 0x00000A10, Reset: 0x0003, Name: OSCCON

The OSCCON register is key protected. To unlock this protection, write 0xCB14 to OSCKEY before writing to OSCCON. A write to any other register before writing to OSCCON returns the protection to the lock state.

Table 174. Bit Descriptions for OSCCON

Bits	Bit Name	Settings	Description	Reset	Access
[15:11]	Reserved		Reserved.	0x0	R
10	HFXTALOK		Status of the high frequency crystal oscillator. This bit indicates when the oscillator is stable after it is enabled. This bit is not a monitor and does not indicate a subsequent loss of stability.	0x0	R
		0	Oscillator is not yet stable or is disabled.		
		1	Oscillator is enabled and is stable and ready for use.		
9	HFOSCOK		Status of the high frequency oscillator. This bit indicates when the oscillator is stable after it is enabled. This bit is not a monitor and does not indicate a subsequent loss of stability.	0x0	R
		0	Oscillator is not yet stable or is disabled.		
		1	Oscillator is enabled and is stable and ready for use.		
8	LFOSCOK		Status of the low frequency oscillator. This bit indicates when the oscillator is stable after it is enabled. This bit is not a monitor and does not indicate a subsequent loss of stability.	0x0	R
		0	Oscillator is not yet stable or is disabled.		
		1	Oscillator is enabled and is stable and ready for use.		
[7:3]	Reserved		Reserved.	0x0	R
2	HFXTALEN		High frequency crystal oscillator enable. This bit is used to enable and disable the oscillator. The oscillator must be stable before use. This bit must be set before the SYSRESETREQ system reset can be initiated.	0x0	R/W
		0	The HFXTAL oscillator is disabled and placed in a low power state.		
		1	The HFXTAL oscillator is enabled.		
1	HFOSCEN		High frequency internal oscillator enable. This bit is used to enable and disable the oscillator. The oscillator must be stable before use. This bit must be set before the SYSRESETREQ system reset can be initiated.	0x1	R/W
		0	The high frequency oscillator is disabled and placed in a low power state.		
		1	The high frequency oscillator is enabled.		
0	LFOSCEN		Low frequency internal oscillator enable. This bit is used to enable and disable the oscillator. The oscillator must be stable before use.	0x1	R/W
		0	The low frequency oscillator is disabled and placed in a low power state.		
		1	The low frequency oscillator is enabled.		

High Power Oscillator Configuration Register—HSOSCCON

Address: 0x000020BC, Reset: 0x00000024, Name: HSOSCCON

Table 175. Bit Descriptions for HSOSCCON

Bits	Bit Name	Settings	Description	Reset	Access
[31:3]	Reserved		Reserved.	0x2	R
2	CLK32MHZEN		16 MHz/32 MHz output selector signal. This bit determines if the output is 32 MHz or 16 MHz. The ADC can run at 32 MHz, but system clock cannot run at 32 MHz. It is required to divide the system clock by 2 first before switching the oscillator to 32 MHz. Refer to the SYSCLKDIVCNT bit in the CLKCON0 register.	0x1	R/W
		0	Select 32MHz output.		
		1	Select 16MHz output.		
[1:0]	Reserved		Reserved.	0x0	R

Key Protection for RSTCON Register—RSTCONKEY

Address: 0x00000A5C, Reset: 0x0000, Name: RSTCONKEY

Table 176. Bit Descriptions for RSTCONKEY

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	Key		Reset control key register. RSTCON is key protected with value 0x12EA. Write to the RSTCON register after the key is entered. A write to any other register before writing to RSTCON returns the protection to the lock state.	0x0	W

Internal Low Frequency Oscillator Register—LOSCTST

Address: 0x00000A6C, Reset: 0x008F, Name: LOSCTST

Table 177. Bit Descriptions for LOSCTST

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	Reserved		Reserved.	0x0	R/W
[3:0]	Trim		Trim capacitors to adjust frequency. The output frequency can be trimmed by adjusting the charging capacitors.	0xF	R/W

APPLICATIONS INFORMATION

ELECTRODERMAL ACTIVITY (EDA) BIOIMPEDANCE MEASUREMENT USING A LOW BANDWIDTH LOOP

The AD5940 can be used for Electrodermal activity (EDA) measurements. This use case requires an always on measurement with a typical sampling rate of 4Hz and excitation signal of 100Hz. The AD5940 uses the low power DAC to generate the low frequency signal. The low power TIA is used to convert current to voltages and the DFT hardware accelerators are used to calculate the real and imaginary values of the data. A high-level block diagram is shown in Figure 52. An accurate ac impedance value is then calculated. By using the LPMODE features of the AD5940 an average current consumption as low as 70uA can be achieved. More details on this measurement can be found in the application AN-1557.

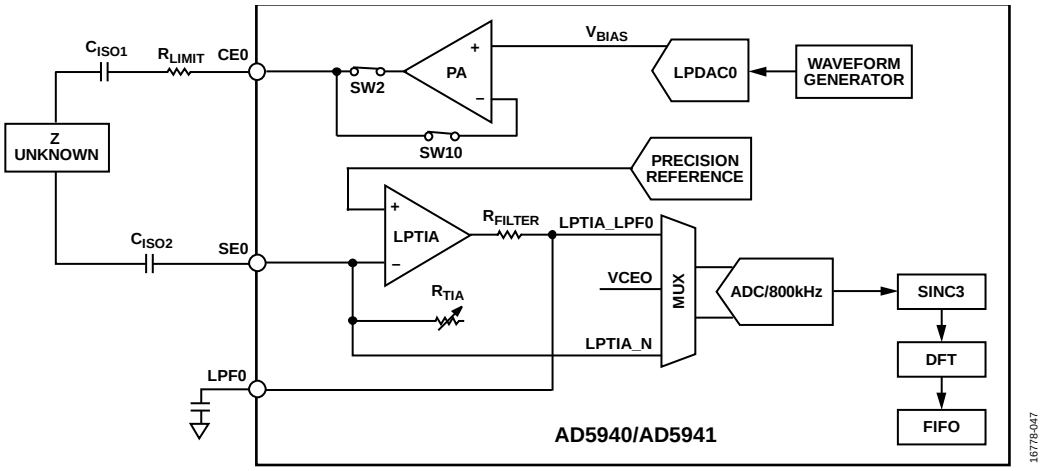

Figure 50. Low Frequency, 2-Wire Bioimpedance Loop (Maximum Bandwidth = 300 Hz)

BODY IMPEDANCE ANALYSIS (BIA) MEASUREMENT USING A HIGH BANDWIDTH LOOP

The AD5940 uses its high bandwidth impedance loop to perform an absolute 4-wire impedance measurements on the body. The high performance, 16-bit ADC, along with on-chip DFT hardware accelerator, target 100 dB of SNR at 50 kHz with impedance measurements up to 200 kHz. For further information, refer to application note AN-1557.

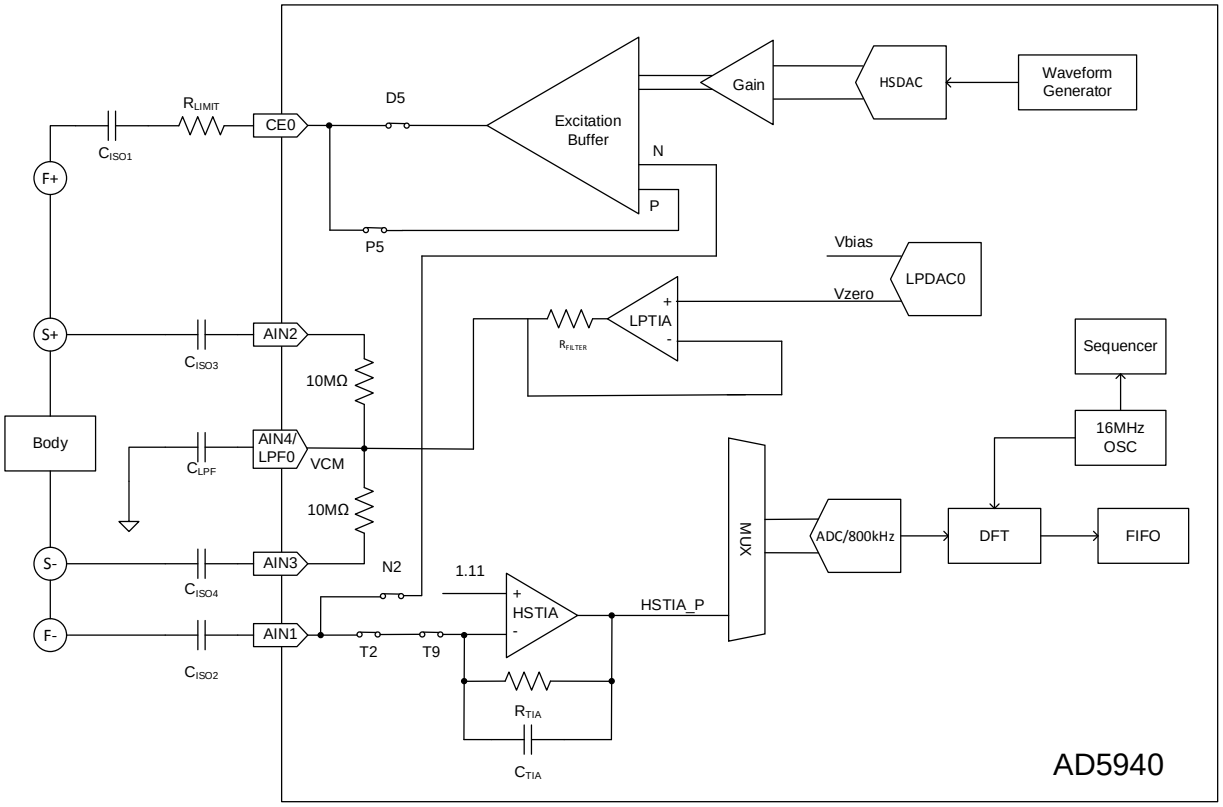

Figure 51. High Frequency, 4-Wire Bioimpedance Loop (Maximum Bandwidth = 200 kHz)

HIGH PRECISION POTENTIOSAT CONFIGURATION

The low bandwidth loop or the high bandwidth loop can be used for potentiostat applications. The switch matrix allows 2-, 3-, or 4-wire electrode connections. Single-reference electrode configuration is available in the low bandwidth loop. Single- or dual-reference electrode measurements configurations are available on the higher bandwidth loop. For further information, refer to application note AN-1563

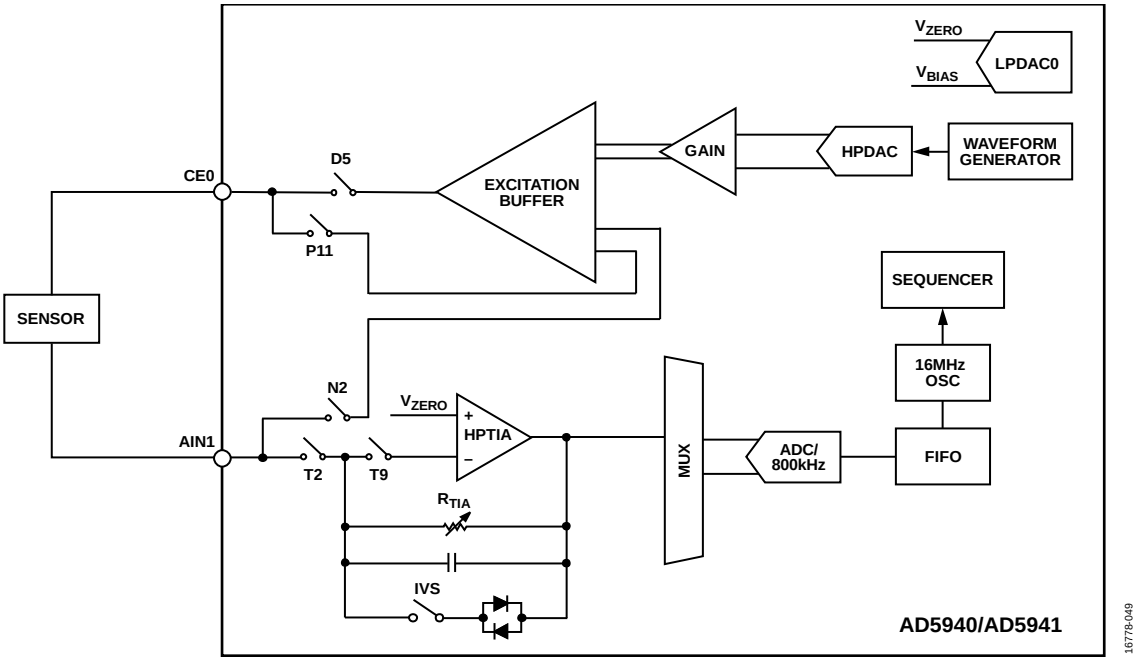

Figure 52. Using a High Bandwidth AFE Loop in Potentiostat Mode

USING AD5940, AD8232, AND AD8233 FOR BIOIMPEDANCE AND ELECTROCARDIOGRAM (ECG) MEASUREMENTS

The AD5940 can be used in conjunction with the AD8232 and AD8233 to perform bioimpedance and ECG measurements. The same electrodes can be used to facilitate both measurements.

When a bioimpedance measurement (for example, body composition, hydration, EDA, and so on) is required, the AD8232 and AD8233 are put into shutdown (the SDN pin on the AD8232 and AD8233 is controlled by the AD5940 GPIOx pin) and the AD5940 switch matrix disconnects the AD8232 and AD8233 from the electrodes.

When an ECG measurement is required, the AD5940 switch matrix disconnects the AD5940 AFE from the electrodes and connects to the AD8233 front end. The AD8233 analog output is connected to the high performance, 16-bit ADC on the AD5940 through an AINx pin. The measurement data is stored in the AD5940 data FIFO to be read by the host controller.

For more information, refer to AN-1557.

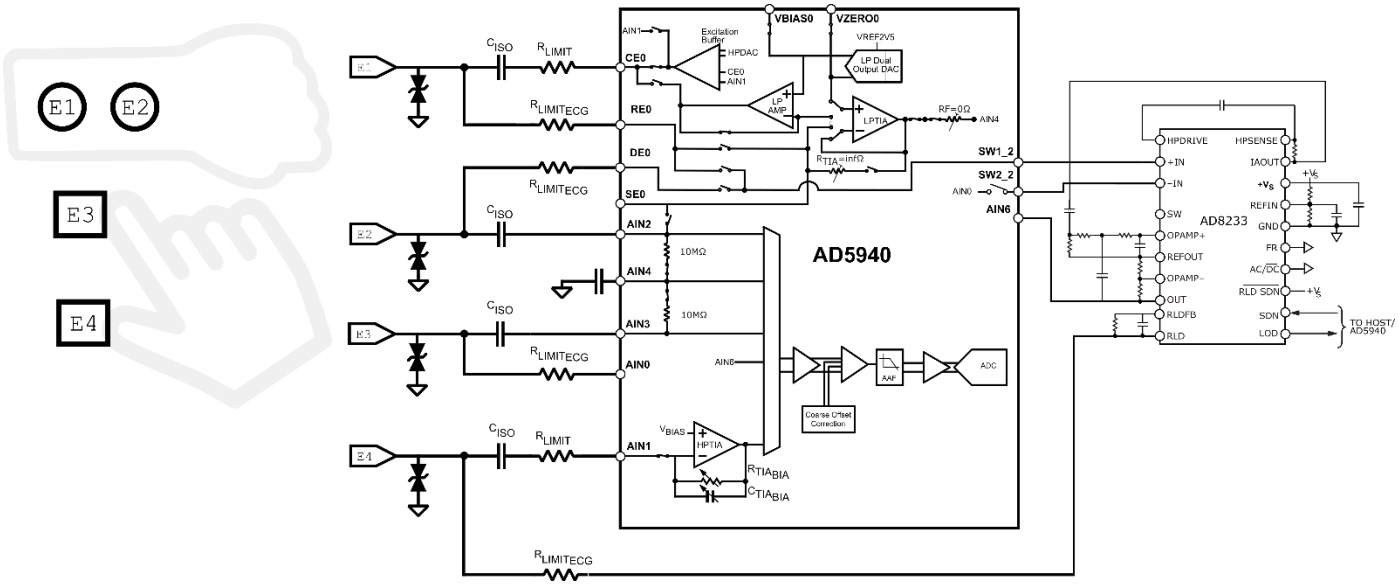

Figure 53. Body Composition and ECG System Solution Using the AD5940 with the AD8232 and AD8233

SMART WATER/LIQUID QUALITY AFE

The features and flexibility of the AD5940 make the device ideal for water analysis applications. Such applications typically have measurements such as pH, conductivity, oxidation/reduction, and temperature measurement. Figure 54 shows a simplified version of the AD5940 configured to satisfy these measurement needs. The high power potentiostat loop can be used for the conductivity measurement. Figure 54 shows a 2-wire conductivity sensor. The pH measurement indicates the acidity or alkalinity of the solution and uses an external amplifier for buffering purposes before conversion by the ADC.

In this application, the data FIFO and AFE sequence lend themselves to autonomous, preprogrammed, smart water measurements

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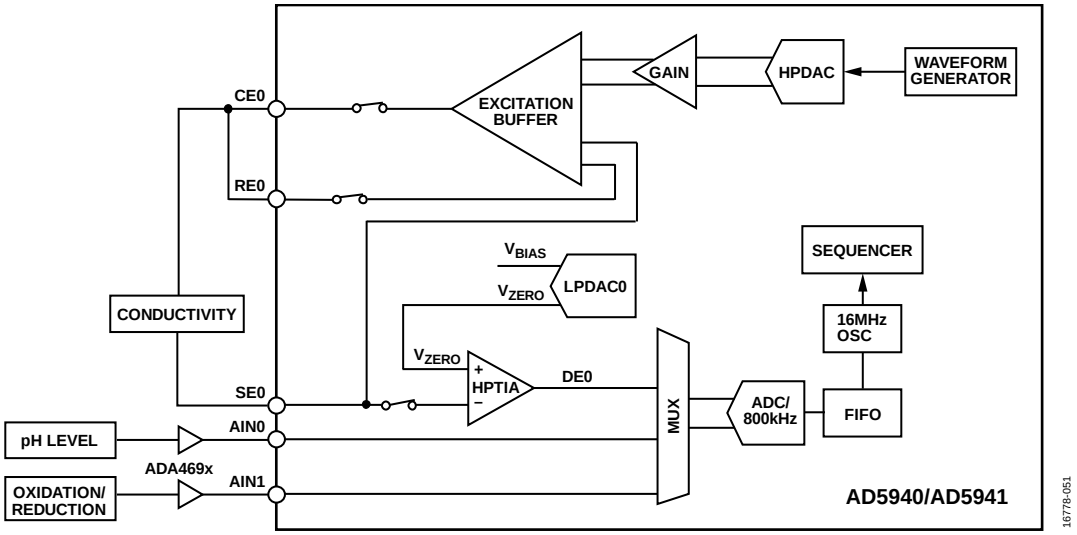

Figure 54. Typical Water Analysis Application Using the AD5940

OUTLINE DIMENSIONS

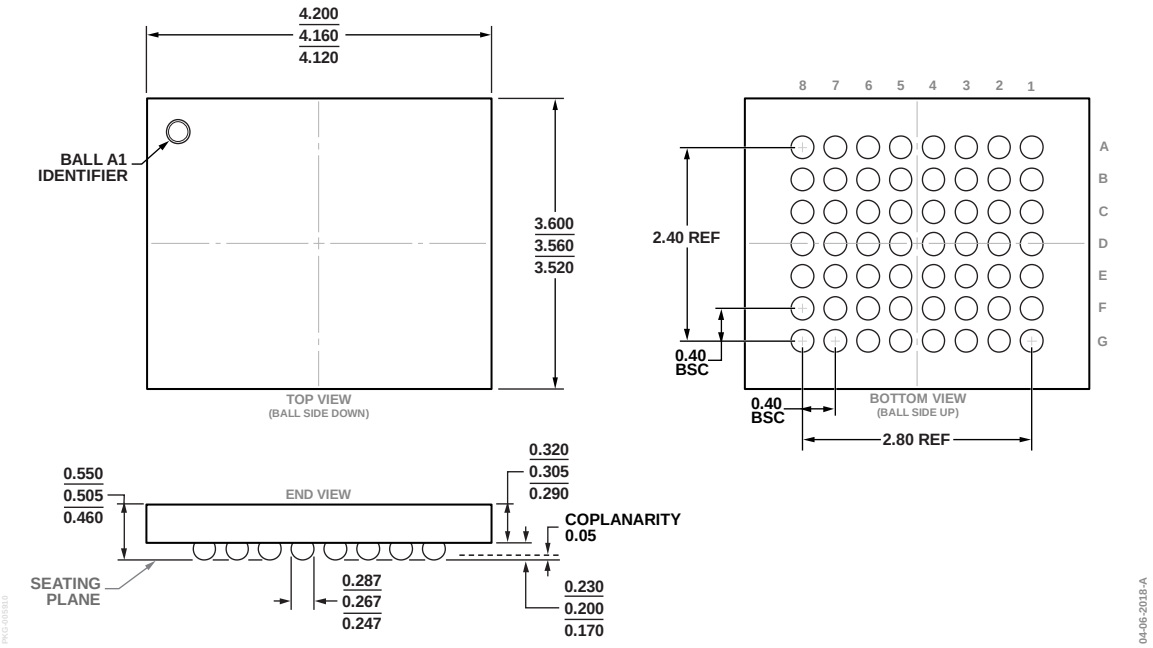

Figure 55. 56-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-56-3)
Dimensions shown in millimeters

PR16778-0-10/18(PrN)