



Advanced Battery Management PMIC With Ultralow I_q Buck and Buck-Boost

Preliminary Technical Data

ADP5360

FEATURES

Linear Battery Charger

High accuracy and programmable charge terminal voltage and charge current

Tolerant input voltage from -0.5V to 20V (USB VBUS)

Power Path Control allows system to operate with dead or missing battery

Compliant with JEITA charge temperature specification

Li-ion/poly Battery Monitor and Protection

Voltage based fuel gauge with adaptive filter limit

Independent battery protection of overcharge and over discharge

No need for external sense resistor

Ultra low quiescent current buck converter

Input start-up voltage range: 2.3 V to 5.5 V

Up to 100 mA output current in hysteresis mode

Up to 500mA output current in FPWM mode

1 MHz switching frequency in FPWM mode

Quick output discharge (QOD) option

Ultra low quiescent current buck-boost converter

Input start-up voltage range: 2.3 V to 5.5 V

Up to 150 mA output current in hysteresis mode

Quick output discharge (QOD) option

Supervisory with nMR and Watchdog timer

Full I₂C Programmability with dedicated Interrupt Pin

APPLICATIONS

Rechargeable Li-ion/Li-Poly Battery Powered Devices

Portable Consumer Devices

Portable Medical Devices

Wearable Devices

GENERAL DESCRIPTION

The ADP5360 combines one high performance linear charger for single Li-ion/Li-ion battery with highly programmable,

ultralow quiescent current fuel gauge and battery protection circuit, one ultralow quiescent buck and one buck-boost switching regulator, and a supervisory.

The ADP5360 charger operates from a 4.0V to 6.5 V input VBUS voltage range but is tolerant of VBUS voltages of up to 20 V that alleviates the concerns about the USB bus spiking during disconnect or connects scenarios.

The ADP5360 features an internal isolation FET between the linear charger output and the battery node. This permits battery isolation and system powering under a dead or missing battery scenario, which allows for immediate system function on connection to a USB power supply.

The integrated isolation FET allows fully battery protection features for over charge and over discharge.

The ADP5360 fuel gauge is a voltage base algorithm with adaptive filter limit and very low current consuming solution. It is optimize battery SoC(State of Charge) for rechargeable Li-Ion battery, which accurate indicate real time remain battery capacity.

The ADP5360 buck regulator operates at 1MHz switching frequency in force PWM mode. The regulator in hysteresis mode achieves excellent efficiency at a power of less than 1mW and provides up to 100 mA of output current.

The ADP5360 buck-boost regulator operates in hysteresis mode. The regulator output a voltage less or higher than battery voltage, and provides up to 150 mA of output current.

The ADP5360 supervisory circuits monitor the regulator output voltage and provides power-on reset signal, a watchdog timer can reset the microprocessor if it fails to kick within a preset timeout period. A reset signal can also be asserted by an external push-button through a manual reset input.

The I₂C-compatible interface enables the programmability of all battery charging parameters, protection threshold, buck output voltage, and status bit read back for operation monitor and safety control.

The ADP5360 operates over the -40°C to +125°C junction temperature range and is available in 32-ball 2.38mm x 2.38mm WLCSP package.

Rev. PRE

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TYPICAL APPLICATION CIRCUIT

ADP5360

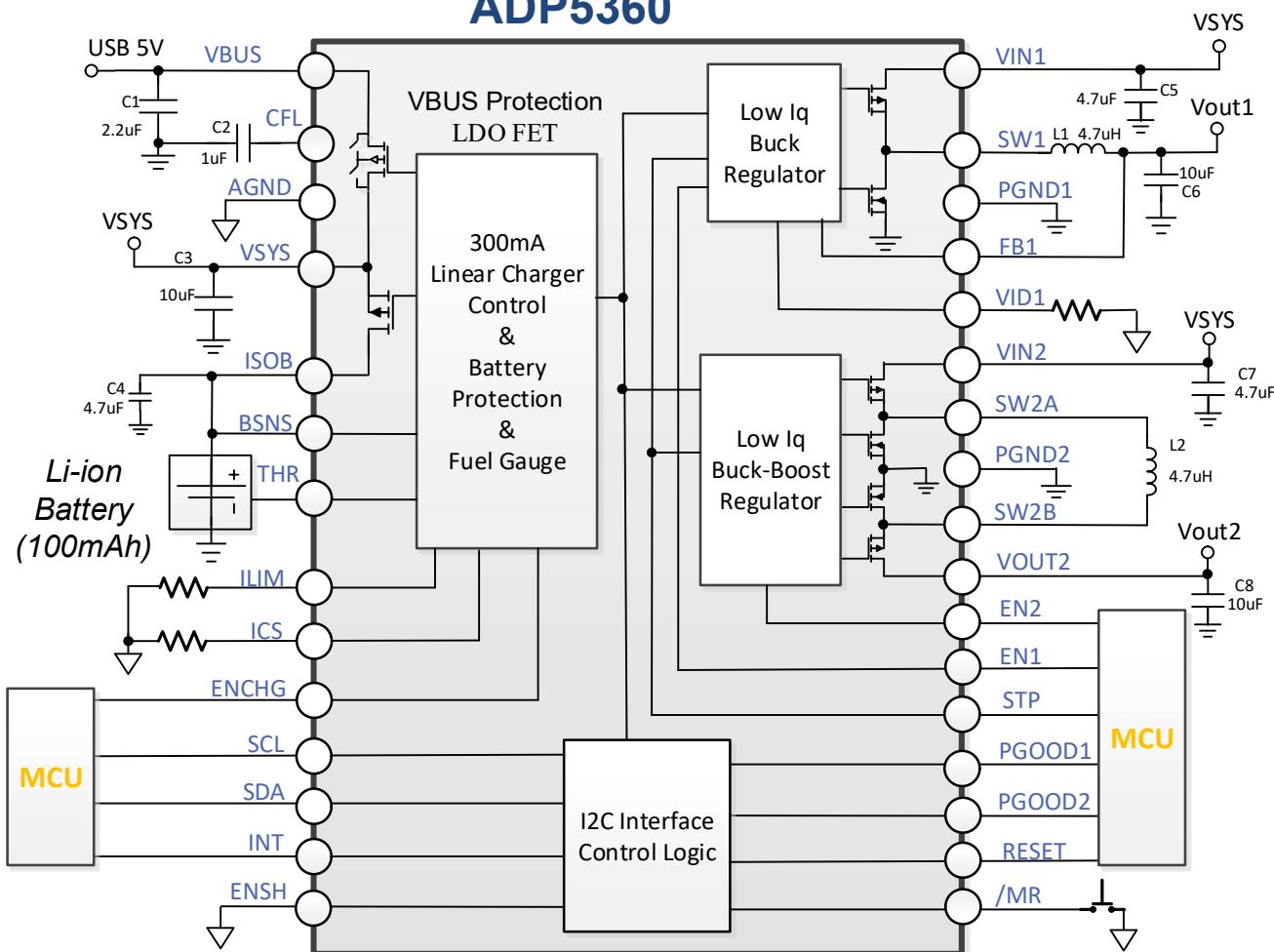


Figure 1. ADP5360 Application Diagram

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REVISION HISTORY

Jul/2015 - PRA0 : Initial Version

Nov/2015-PRA2: Update pin definition

- Add register map and table
- Change charge current to 300mA

Dec/2015 - PRB0 : Add buck-boost

Aug/2016 – PRC1: Regular update

Sep/2016 – PRC2: Register update, Watchdog update, THR update.

Nov/2017 – PRD0: General update

Aug/2018 – PRE: General update

- Remove LFCSP package,
- nMR Press shipment update
- IEND spec change

SPECIFICATIONS

BATTERY CHARGER SPECIFICATIONS

$-40^{\circ}\text{C} < T_j < 85^{\circ}\text{C}$, $V_{\text{BUS}} = 5.0 \text{ V}$, $V_{\text{HOT}} < V_{\text{THR}} < V_{\text{COLD}}$, $\text{VIN1} = \text{VIN2} = V_{\text{SYS}} = 3.8 \text{ V}$, $C_{\text{BUS}} = 2.2 \mu\text{F}$, $C_{\text{OUT1}} = C_{\text{OUT2}} = 10 \mu\text{F}$, $C_{\text{SYS}} = 10 \mu\text{F}$, $C_{\text{CFL}} = 4.7 \mu\text{F}$, $L_{\text{OUT1}} = L_{\text{OUT2}} = 4.7 \mu\text{H}$, all registers are at default values, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
GENERAL PARAMETERS						
Undervoltage Lockout	V_{UVLO}	Rising threshold, V_{ISOB} pin, $V_{\text{BUS}} = 0$ Falling threshold, V_{ISOB} pin, $V_{\text{BUS}} = 0$	1.8	2.1 1.9	2.15	V
Input Current Limit	I_{LIM}	Nominal USB initialized current level		90	100	mA
Operation Current						
VBUS Consumption	$I_{Q_{\text{BUS}}}$	All enabled, no charge current		2		mA
Battery Consumption	$I_{Q_{\text{PRO}}}$	Only enable battery protection, $V_{\text{BUS}} = 0$		0.2	TBD	uA
		Fuel gauge active mode, $V_{\text{BUS}} = 0$		5	TBD	uA
		Fuel gauge, sleep mode, $V_{\text{BUS}} = 0$		0.5	TBD	uA
Shutdown Current	I_{STDN}	Enable Buck and Buck-boost, $V_{\text{BUS}} = 0$		0.2	TBD	uA
		All disable		150	TBD	nA
		Shipment mode		20	TBD	nA
CHARGING PARAMETERS						
Fast Charge Current CC Mode	I_{CHG}	$V_{\text{ISOB}} = 3.8 \text{ V}$. $I_{\text{CHG}} = 10 \text{ mA}$ to 320 mA	95 TBD	100	105	mA
Fast Charge Current Accuracy						mA
Trickle Charge Current	$I_{\text{TRK_DEAD}}$	$I_{\text{TRK_DEAD}} = 5 \text{ mA}$,	2	5	8	mA
Weak Charge Current	$I_{\text{CHG_WEAK}}$				$I_{\text{TRK_DEAD}} + I_{\text{CHG}}$	mA
Trickle to Weak Charge Threshold	$V_{\text{TRK_DEAD}}$		2.4	2.5	2.6	V
Trickle to Weak Charge Threshold Hysteresis	$\Delta V_{\text{TRK_DEAD}}$			100		mV
Weak to Fast Charge Threshold	V_{WEAK}		2.89	3.0	3.11	V
	ΔV_{WEAK}			100		mV
Battery Termination Voltage	V_{TRM}			4.200		V
Termination Voltage Accuracy		On BAT_SNS, $T_j = 25^{\circ}\text{C}$, $I_{\text{END}} = 10 \text{ mA}^1$ $T_j = 0^{\circ}\text{C}$ to 85°C^1	-0.25 TBD		+0.25	%
Charge Complete Current	I_{END}	$I_{\text{END}} = 5 \text{ mA}$,	TBD	5	TBD	mA
Recharge Voltage Differential	V_{RCH}		TBD	120	TBD	mV
BATTERY ISOLATION FET						
Resistance Between ISOB and ISOS	$R_{\text{DSON_ISO}}$	$V_{\text{IN}} = 0 \text{ V}$, $V_{\text{ISOB}} = 3.8 \text{ V}$, $I_{\text{ISOB}} = 300 \text{ mA}$		200	TBD	$\text{m}\Omega$
Battery Supplementary Threshold	$V_{\text{TH_ISO}}$	$V_{\text{ISOS}} < V_{\text{ISOB}}$	0	5	10	mV
LDO and HIGH VOLTAGE BLOCKING FET						
Regulated System Voltage	$V_{\text{SYS_REG}}$	$V_{\text{TRM}} = 4.2 \text{ V}$, $V_{\text{SYSTEM}} = V_{\text{TRM}} + 100 \text{ mV}$		4.3		V
High Voltage Blocking FET On Resistance	$R_{\text{DSON_HV}}$	$I_{\text{VBUS}} = 300 \text{ mA}$		340	455	$\text{m}\Omega$
Input Voltage Good Threshold						
Rising	$V_{\text{VBUS_OK_RISE}}$		3.78	3.9	4.0	V
Falling	$V_{\text{VBUS_OK_FAL}}$			3.6	3.67	V
Overvoltage Threshold	$V_{\text{VBUS_OV}}$		6.2	6.5	6.8	V
Overvoltage Threshold Hysteresis				100		mV
THERMAL PROTECTION						
Thermal Warning Temperature	T_{warn}	T_{Wrising}		90		$^{\circ}\text{C}$

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Thermal Shutdown Temperature	T_{SD}	$T_{W\text{falling}}$ $T_{J\text{rising}}$ $T_{J\text{falling}}$	80 110 100			°C °C °C
THERMISTOR CONTROL						
Thermistor Current						
10,000 NTC	I_{NTC_10k}			60		µA
50,000 NTC	I_{NTC_50k}			12		µA
100,000 NTC	I_{NTC_100k}			6		µA
Thermistor Capacitance	C_{NTC}				100	pF
BATTERY DETECTION						
Sink Current	I_{SINK}		TBD	5	TBD	mA
Source Current	I_{SOURCE}	$I_{SOURCE} = I_{TRK_DEAD}$		2.5		mA
Battery Threshold						
Low	V_{BATL}		1.8	1.9	2.0	V
High	V_{BATH}			3.4		V
Battery Detection Timer	t_{BATOK}			333		ms
TIMERS						
Start Charging Delay Timer	t_{START}			0.3		sec
Trickle Charge Timer ¹	t_{TRK}			60		min
Fast Charge Timer ¹	t_{CHG}			600		min
Charge Complete Timer	t_{END}	$V_{BSNS} = V_{TRM}, I_{CHG} < I_{END}$		7.5		min
Deglitch Timer	t_{DG}	Applies to $V_{TRM}, V_{RCH}, I_{END}, V_{WEAK}, V_{TRK_DEAD}, V_{VBUS_OK}$		31		ms
Safety Timer	t_{SAFE}		36	40	44	min
Reset timeout period	t_{RP}			200		ms
MR for shipment mode	t_{sh}			200		mS
Watchdog Timer ¹	t_{WD}			12.5		Sec
I2C (SCL and SDA)						
Maximum Voltage on Digital Inputs	V_{DIN_MAX}				5.5	V
Low Level Input Voltage	V_{IL}	Applies to SCL, SDA			0.4	V
High Level Input Voltage	V_{IH}	Applies to SCL, SDA	0.9		0.4	V
Low Level Output Voltage	V_{OL}	Applies to SDA, $I_{SDA_SINK}=2mA$			0.4	V
nINT, nRESET, PGOOD1, PGOOD2						
Leakage Current	I_{LOGO_Leak}	$V_{LOGO} = 5V$	TBD	10		nA
Output Low Voltage	V_{LOGO_LOW}	$I_{LOGO} = 1 mA$	50	100		mV
Deglitch time	T_{DGL}					
ENCHG, EN1, EN2, STP, nMR, ENSD						
Input Voltage Threshold						
High	V_{IH}					V
Low	V_{IL}				0.4	V
Input Leakage Current	$I_{EN_LEAKAGE}$				TBD	nA

¹These values are programmable via I2C. Values are given with default register values.

BATTERY MONITOR SPECIFICATIONS

$V_{SYS} = 3.6 V$, $T_J = -40^\circ C$ to $+85^\circ C$ for minimum/maximum specifications, and $T_J = 25^\circ C$ for typical specifications, unless otherwise noted

Table 2.

Parameter	Symbol	Test Conditions / Comments	Min	Typ	Max	Unit
BATTERY VOLTAGE SENSING						
ADC Reading Voltage Range			0		4.8	V
ADC Reading Voltage Resolution		Based on 12-bit ADC		1.09		mV
ADC Reading Voltage accuracy		$T_J = +25^\circ C$	-12.5 TBD		+12.5 TBD	mV

BATTERY OVER DISCHARGE MORNITORING							
Under Voltage Rising Threshold	V _{OD_RISING}	UV_DISCH = 2.5 V	TBD	2.5	TBD	V	
Under Voltage Falling Threshold Hysteresis	V _{OD_FALLING_Hys}	HYS_UV_DISCH = 2%		2		%	
UV Deglitch Timer	T _{UV_DIS}	DGT_UV_DISCH = 30 mS	TBD	30	TBD	mS	
Over Discharge Current Threshold	I _{OC_DIS}	OC_DISCH = 600 mA		600		mA	
Over Discharge Current Accuracy			-10		+10	%	
Over Discharge Current Deglitch Timer	T _{OC_DIS}	DGT_OC_DISCH = 0.5 mS		0.5		mS	
Hiccup Off Time	T _{DIS_HCP}			3×T _{OC_DIS}			
BATTERY OVER CHARGE MORNITORING							
Over Voltage Rising Threshold	V _{OVC_RISING}	OV_CHG = 4.3 V	TBD	4.3	TBD	V	
Over Voltage Falling Threshold Hysteresis	V _{OVC_RISING_Hys}	HYS_OV_CHG = 2%		2		%	
Over Voltage Deglitch Timer	T _{OVC_CHG}	DGT_OV_CHG = 0.5 s		0.5		s	
Over Current Threshold	I _{OC}	OC_CHG = 150 mA	TBD	150	TBD	mA	
Over Current Accuracy			-10		+10	%	
Over Current Deglitch Time	T _{OC_CHG}	DGT_OC_CHG = 10 mS		10		mS	
Hiccup Off Time	T _{CHG_HCP}			7× T _{OC_CHG}			

BUCK REGULATOR SPECIFICATIONS

V_{IN1} = 3.6 V, V_{OUT1} = 2.5 V, T_J = -40°C to +85°C for minimum and maximum specifications, and T_J = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE	V _{IN1}	2.3		5.5	V	
UNDERVOLTAGE LOCKOUT	UVLO					
UVLO Threshold						
Rising	V _{UVLO_RISING}		2.3	2.35	V	
Falling	V _{UVLO_FALLING}	2.15	2.2		V	
OSCILLATOR CIRCUIT						
Switching Frequency in PWM Mode	f _{SW1}		1.0		MHz	
Feedback (FB) Threshold of Frequency Fold	V _{OSC_FOLD}		0.3		V	
FB1 PIN						
Output Options Range	V _{OUT1}	0.6		3.75	V	0.6 V to 3.75 V in various factory options
PWM Mode						
Fixed VID Code Voltage Accuracy	V _{FB1_PWM_FIX}	-0.6	+0.6		%	T _J = 25°C, output voltage setting via factory fuse
		-1.2	+1.2		%	-40°C ≤ T _J ≤ +85°C
Hysteresis Mode						
Fixed VID Code Threshold Accuracy from Active Mode to Standby Mode	V _{FB1_HYS_FIX}	-0.7 5	+0.75		%	T _J = 25°C
		-2.5	+2.5		%	-40°C ≤ T _J ≤ +85°C
Hysteresis of Threshold Accuracy from Active Mode to Standby Mode	V _{FB1_HYS (HYS)}		1		%	
Feedback Bias Current	I _{FB}		50		nA	Output Option 0, V _{OUT} = 2.5 V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW1 PIN						
High-Side Power FET On Resistance	R _{DS(ON) H}		324	470	mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	R _{DS(ON) L}		196	320	mΩ	Pin to pin measurement
Current-Limit in PWM Mode	I _{LIM_PWM}	800	1000	1200	mA	PWM mode
Peak Current in Hysteresis Mode	I _{LIM_HYS}		400		mA	Hysteresis mode
Minimum On Time	t _{MIN_ON}		40	70	ns	
SOFT START						
Default Soft Start Time	t _{SS1}		1		ms	
C _{OUT1} DISCHARGE SWITCH ON RESISTANCE	R _{DIS1}		260		Ω	

BUCK-BOOST REGULATOR SPECIFICATIONS

V_{IN2} = 3.6 V, V_{OUT2} = 1.8 V, T_J = -40°C to +85°C for minimum and maximum specifications, and T_J = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Input Supply Voltage Range	V _{IN2}	2.3		5.5	V	
UNDERVOLTAGE LOCKOUT	UVLO					
UVLO Threshold						
Rising	V _{UVLO_RISING}		2.3	2.35	V	
Falling	V _{UVLO_FALLING}	2.15	2.2		V	
Output Voltage Range	V _{OUT2}	1.8		5.5	V	Factory trim or I ² C, 6 bits
Output Voltage Accuracy	V _{OUT2}	-1.5		+1.5	%	
SW2A and SW2B pins						
High-Side FET Resistance – A	R _{DS(on)1_2A-H}		400	TBD	mΩ	
Low-Side FET Resistance – A	R _{DS(on)1_2A-L}		350	TBD	mΩ	
High-Side FET Resistance – B	R _{DS(on)1_2B-H}		400	TBD	mΩ	
Low-Side FET Resistance – B	R _{DS(on)1_2B-L}		350	TBD	mΩ	
Peak Current-Limit Threshold	I _{TH(LIM1_2)}	TBD	400	TBD	mA	I _{LIMx} = 400mA
Soft Start Time						
Soft Start Time	t _{SS2}		1		ms	
Programmable Soft Start Range		1		512	ms	
C _{OUT} Discharge Switch On Resistance	R _{DIS2}		260		Ω	

I²C-COMPATIBLE INTERFACE TIMING SPECIFICATIONS

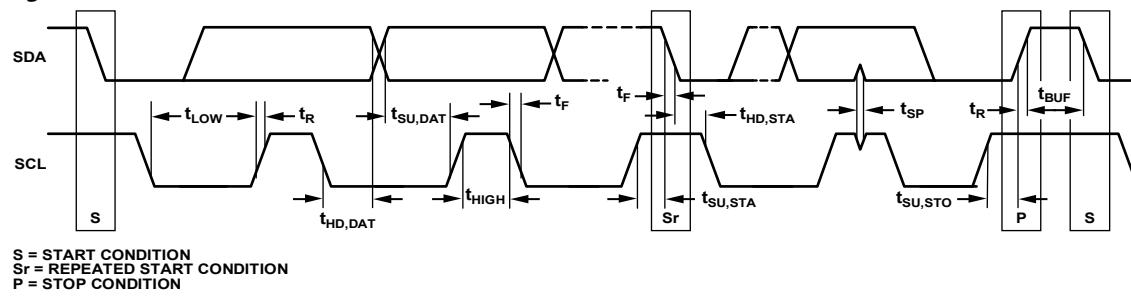
Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
I ² C-COMPATIBLE INTERFACE					
Capacitive Load, Each Bus Line	C _S			400	pF
SCL Clock Frequency	f _{SCL}			400	kHz
SCL High Time	t _{HIGH}	0.6			μs
SCL Low Time	t _{LOW}	1.3			μs
Data Setup Time	t _{SUDAT}	100			ns
Data Hold Time ¹	t _{HDDAT}	0		0.9	μs
Setup Time for Repeated Start	t _{SUSTA}	0.6			μs
Hold Time for Start/Repeated Start	t _{HDSTA}	0.6			μs
Bus Free Time Between a Stop and a Start Condition	t _{BUF}	1.3			μs
Setup Time for Stop Condition	t _{SUSTO}	0.6			μs

Rise Time of SCL/SDA	t_R	20	300	ns
Fall Time of SCL/SDA	t_F	20	300	ns
Pulse Width of Suppressed Spike	t_{SP}	0	50	ns

¹ A master device must provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL. See Figure 2, the I²C timing diagram.

Timing Diagram



09370-002

Figure 2. I²C Timing Diagram

RECOMMENDED INPUT AND OUTPUT CAPACITANCE AND INDUCTANCE

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CAPACITANCE					
VBUS Capacitance	Effective capacitance	1.0	2.2		μF
CFL Pin Capacitance	Effective capacitance	0.47	1.0	10	μF
VSYS Pin Total Capacitance	Effective capacitance	4.7	10		μF
ISOB Pin Total Capacitance	Effective capacitance	4.7	10		μF
VIN1 Pin Total Capacitance	Effective capacitance	0.7	1		μF
VIN2 Pin Total Capacitance	Effective capacitance	0.7	1		μF
VOUT1 Total Capacitance	Effective capacitance	1	10		μF
VOUT2 Total Capacitance	Effective capacitance	1	10		μF
INDUCTANCE					
Buck Inductance		2.2	4.7	6.8	μH
Buck-boost Inductance		2.2	4.7	6.8	μH

ABSOLUTE MAXIMUM RATINGS**Table 6.**

Parameter	Rating
VBUS to PGND1	-0.5 V to +20 V
PGND1, PGND4 to AGND	-0.3 V to +0.3 V
All Other Pins to AGND	-0.3 V to +6 V
Continuous Drain Current, Battery Supplementary Mode, from ISOB to ISOS, $T_J = 125^\circ\text{C}$	1.1 A
Storage Temperature Range	-65°C to +150°C
Operating Junction Temperature Range	-40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Unit
32-ball WLCSP	TBD	TBD	TBD	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADP5360 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADP5360. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices that potentially cause failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

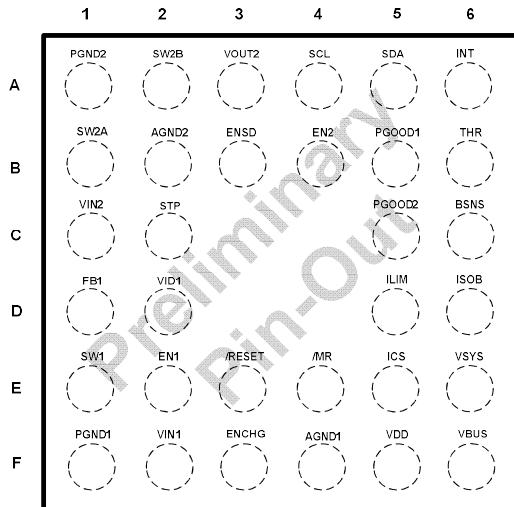


Figure 3. Pin Configuration, 32-Ball 2.4mm x 2.4mm WLCSP Package (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	PGND2	Power ground for the buck-boost regulator.
A2	SW2B	Switching mode for buck-boost regulator.
A3	VOUT2	Buck-Boost regulator output pin.
A4	SCL	I ² C Serial Clock. Requires an external pull-up resistor.
A5	SDA	I ² C Serial Data. Requires an external pull-up resistor.
A6	nINT	Processor Interrupt (Active Low). Requires an external pull-up resistor. If this pin is not used, it can be left floating.
B1	SW2A	Switching mode for buck-boost regulator.
B2, F4	AGND2, AGND1	Analog ground.
B3	ENSD	Shut down mode select pin, when it low to disable shut down mode. When it high to enable shut down mode.
B4	EN2	Enable pin for buck boost regulators.
B5	PGOOD1	Power-good signal output. This open-drain output is the power-good signal for the selected VBUSOK, BATOK, CHGOK, VOUT2OK or VOUT1OK.
B6	THR	Battery pack thermistor connection.
C1	VIN2	Input power for buck regulator.
C2	STP	Stop switching for selected channel.
C5	PGOOD2	Power-good signal output. This open-drain output is the power-good signal for the selected VBUSOK, BATOK, CHGOK, VOUT2OK or VOUT1OK.
C6	BSNS	Battery voltage sense pin.
D1	FB1	Feedback sensing input for the buck regulator.

D2	VID1	Buck regulator output voltage configure pin. Connect a resistor from VID1 to AGND to program buck regulator default output voltage, float the pin to disable pin select feature and use register default set.
D5	ILIM	Input current limit select pin. Connect a resistor to GND to set default input current limit level, float the pin to disable pin select feature and use register default set.
D6	ISOB	Battery supply side input to internal isolation FET/Battery current regulation FET.
E1	SW1	Switching mode for buck regulator.
E2	EN1	Enable pin for buck regulators.
E3	/RESET	Reset output.
E4	/MR	Manual reset input pin.
E5	ICS	Charge current set pin. Connect one resistor to ground to set default charge current, float the pin to disable pin select feature and use register default set.
E6	VSYS	Linear charger supply side input to the internal isolation FET.
F1	PGND1	Power ground for the buck regulator.
F2	VIN1	Input power for buck regulator.
F3	ENCHG	Logic input for enable charger function.
F5	VDD	Internal circuit power supply.
F6	VBUS	Power Connection to USB VBUS.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{VBBUS}=5.0\text{ V}$, $V_{ISOB}=3.6\text{ V}$, all registers are at default values, unless otherwise noted.

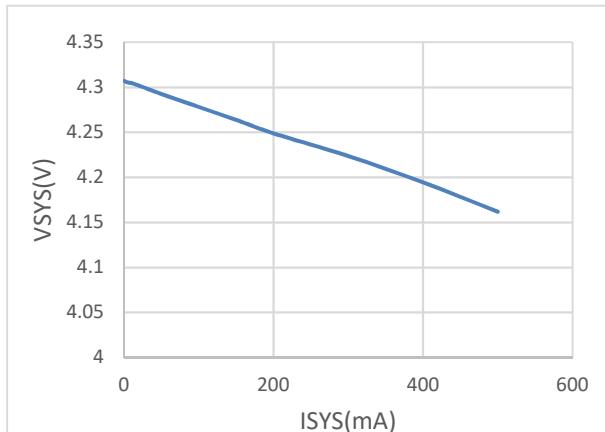


Figure 4. VSYS vs. ISYS, VSYS = 4.3V, ISYS from 0.2mA to 500mA

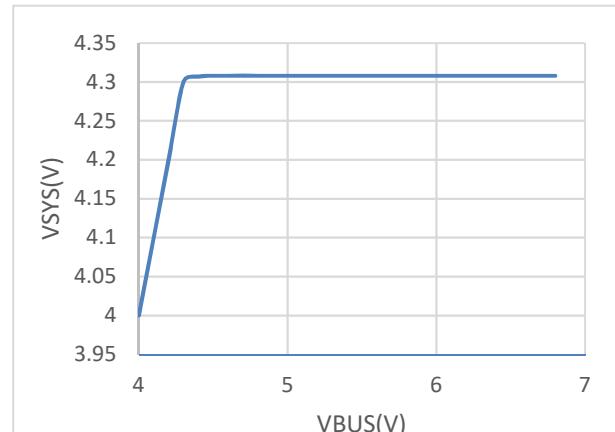


Figure 7 VSYS vs. VBUS, VSYS = 4.3V, VBUS from 4V to 6.8V

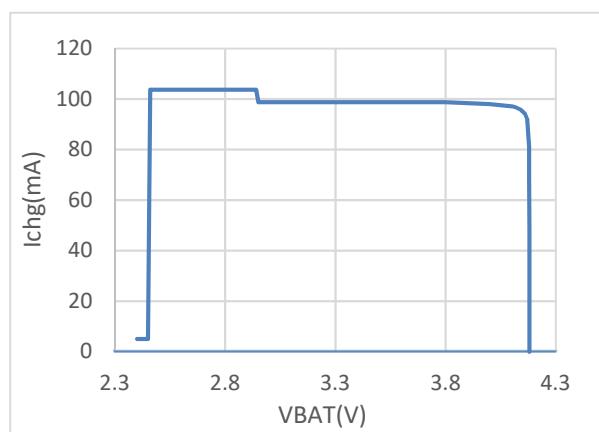


Figure 5. Battery charge current vs. Battery Voltage $ICHG = 100\text{mA}$

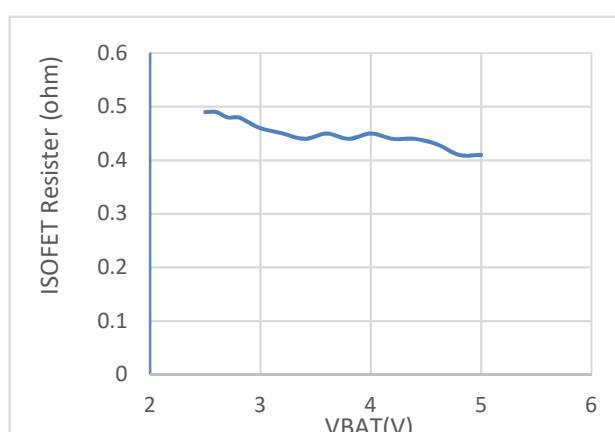


Figure 8. ISOFET Resister vs. Battery Voltage

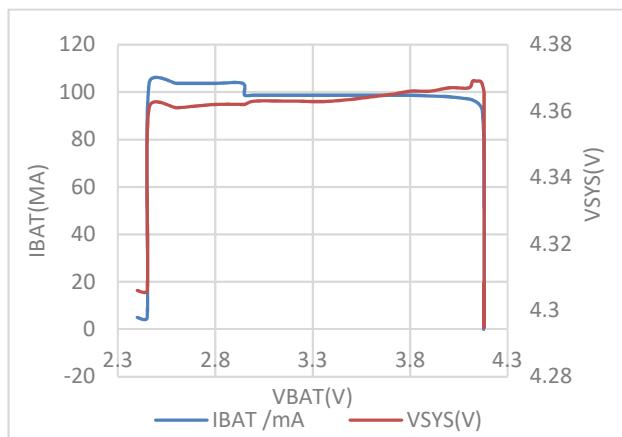


Figure 6. VBAT vs. IBAT&VSYS, Charge Profile

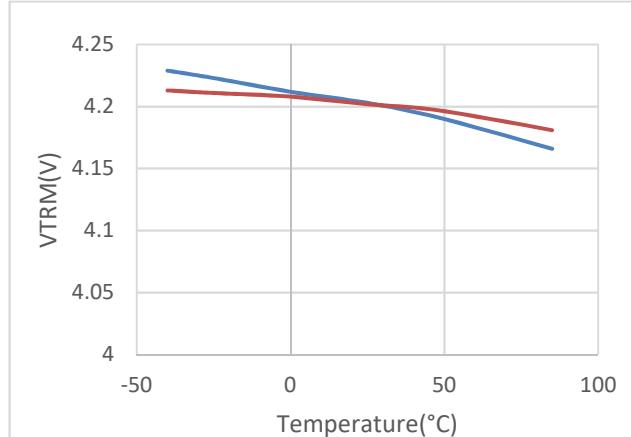


Figure 9. VTRM vs. Temperature

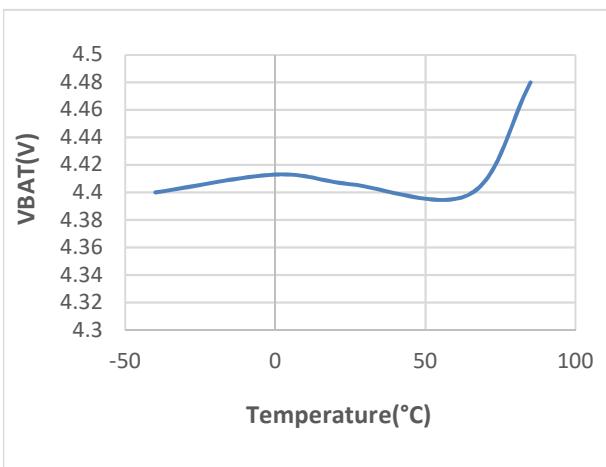


Figure 10. Battery OV Threshold vs Temp

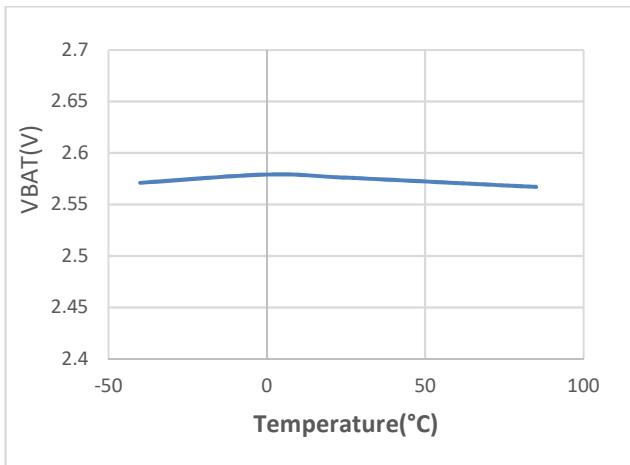


Figure 13. Battery UV Threshold vs Temp

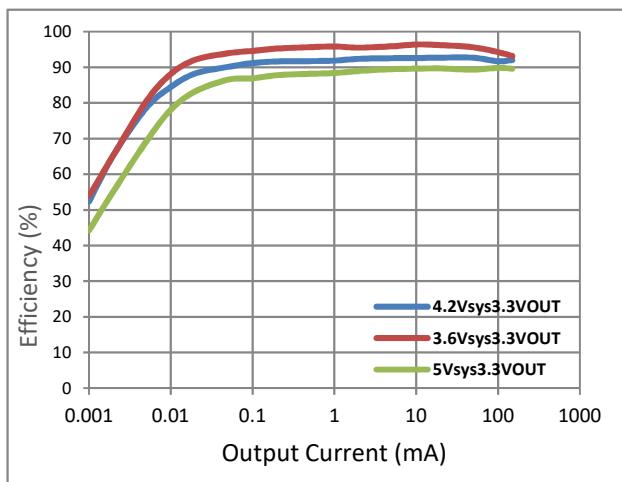


Figure 11. Buck Efficiency vs. Output Current

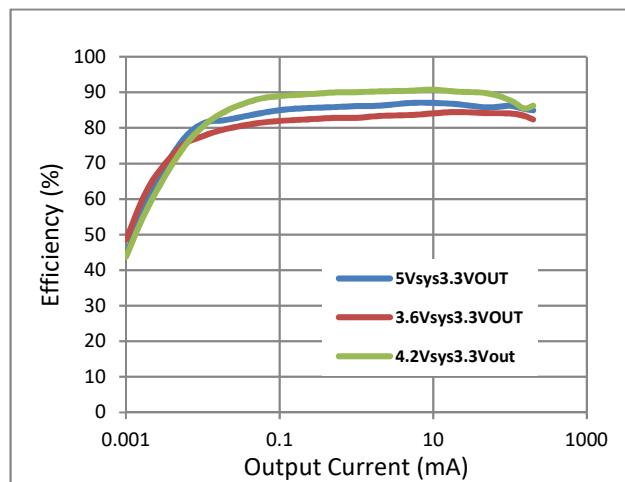


Figure 14. Buckboost Efficiency vs. Output Current

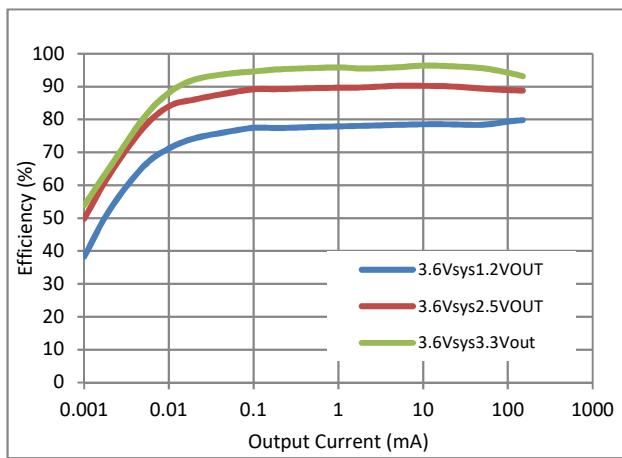


Figure 12. Buck Efficiency vs. Output Current

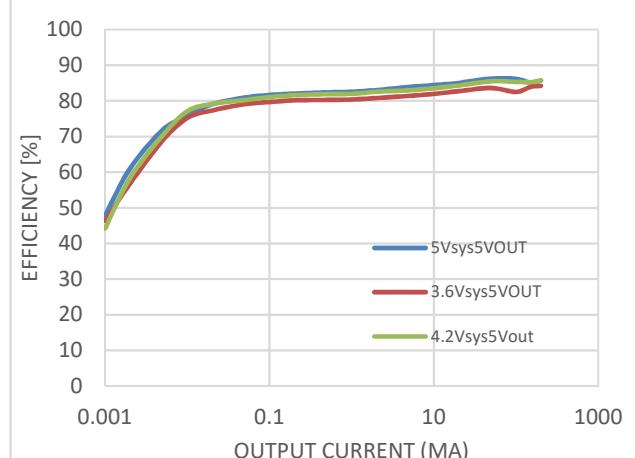


Figure 15. Buckboost Efficiency vs. Output Current

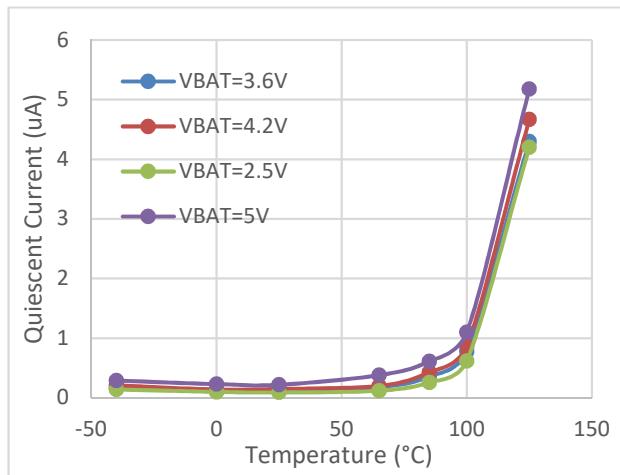


Figure 16. Quiescent Current vs. Temperature

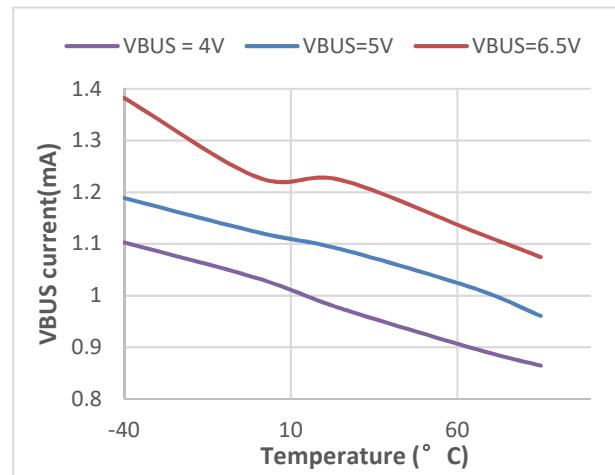


Figure 19. VBUS current vs. Temperature

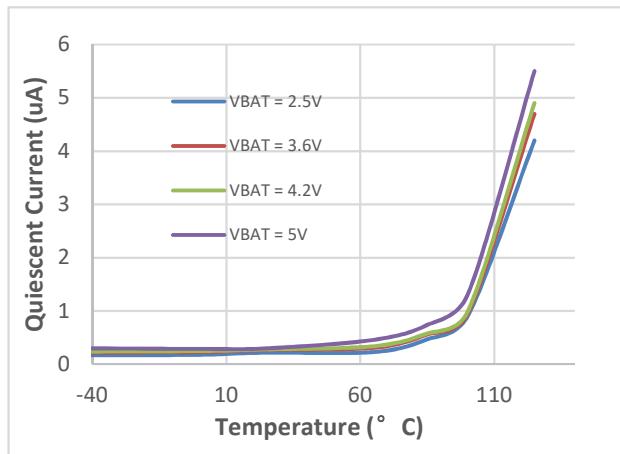


Figure 17. Buckboost Quiescent Current vs. Temperature

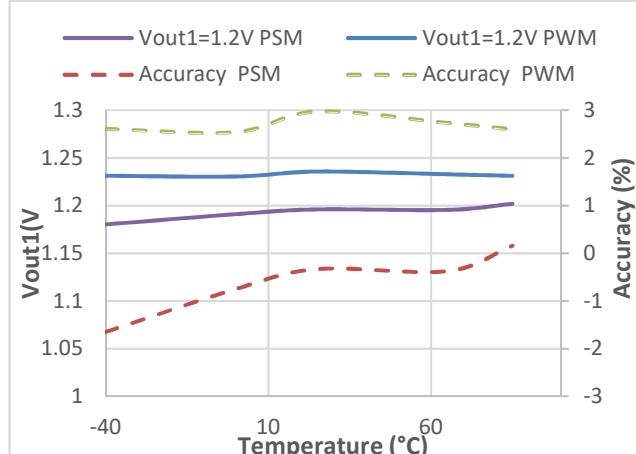


Figure 20. Buck Output vs. Temperature

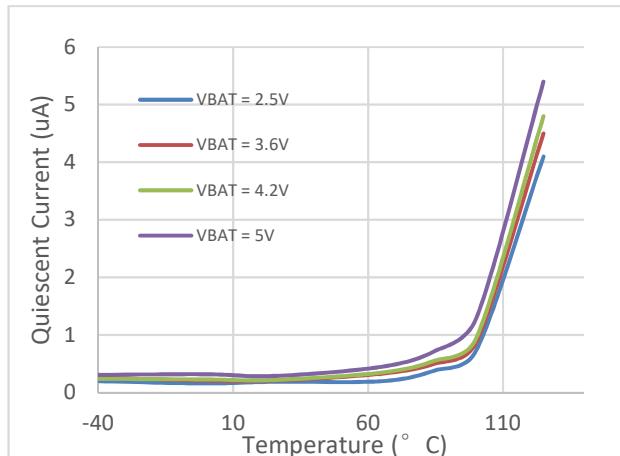


Figure 18. Buck PSM Quiescent Current vs. Temperature

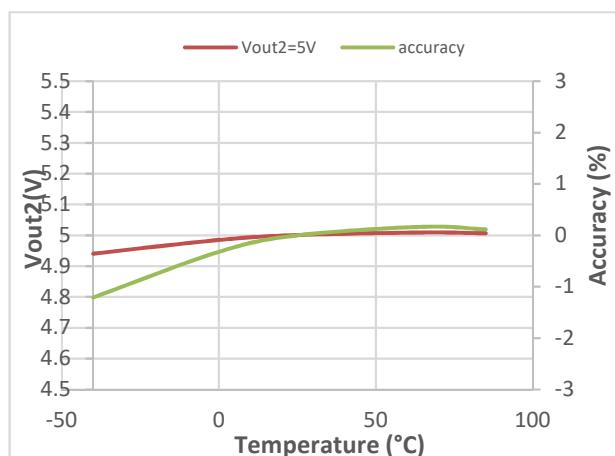


Figure 21. Buckboost Output vs. Temperature

TYPICAL WAVEFORMS

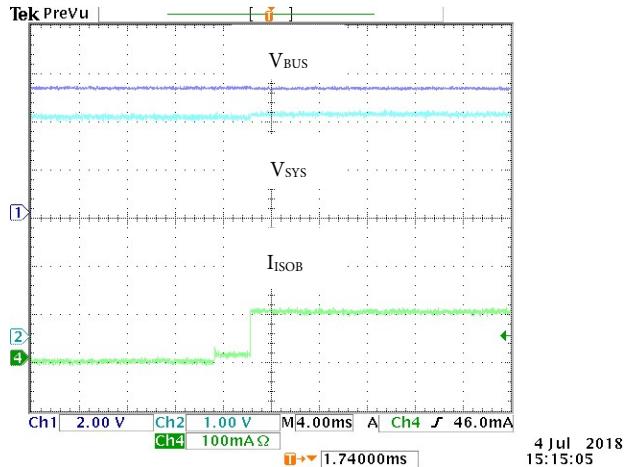


Figure 22. Charge Start up, V_{BUS}=5V, V_{SYS}=3.6V,
ILIM=200mA, ICHG=50mA

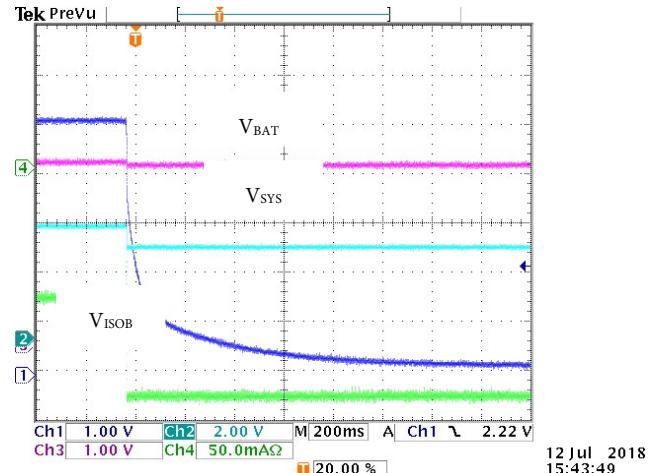


Figure 25. USB Disconnect, V_{BUS}=5V, V_{BAT}=3.6V, ICHG=100mA

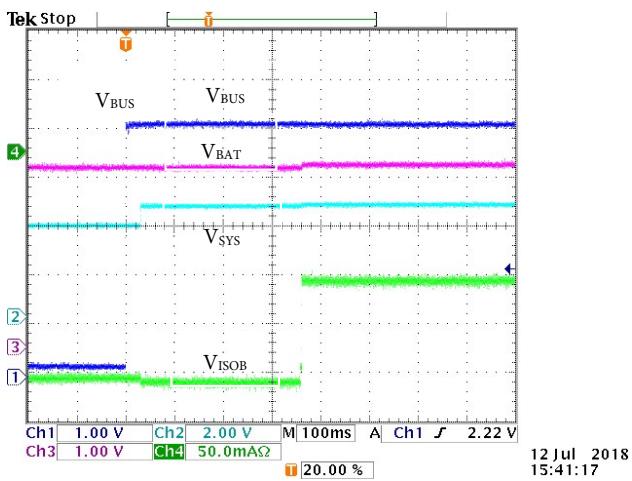


Figure 23. USB Connect, V_{BUS}=5V, V_{BAT}=3.6V

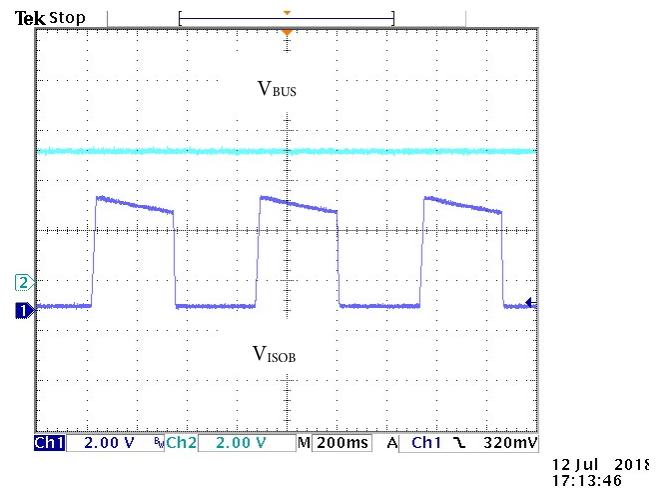


Figure 26. Battery Detection Waveform

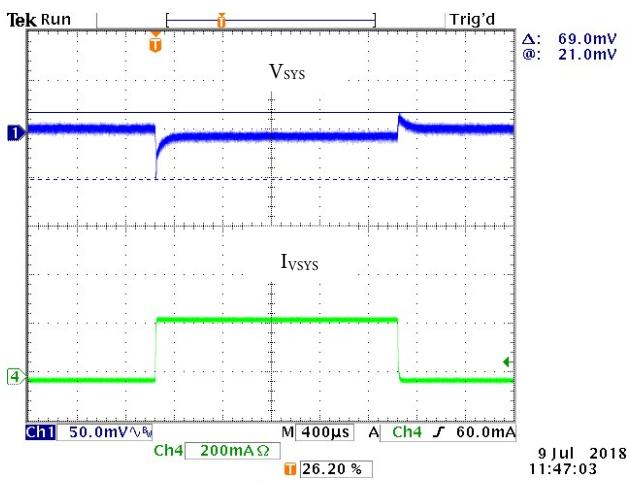


Figure 24. VSYS Load Transient, I_{ISOB} = 50mA to 300mA

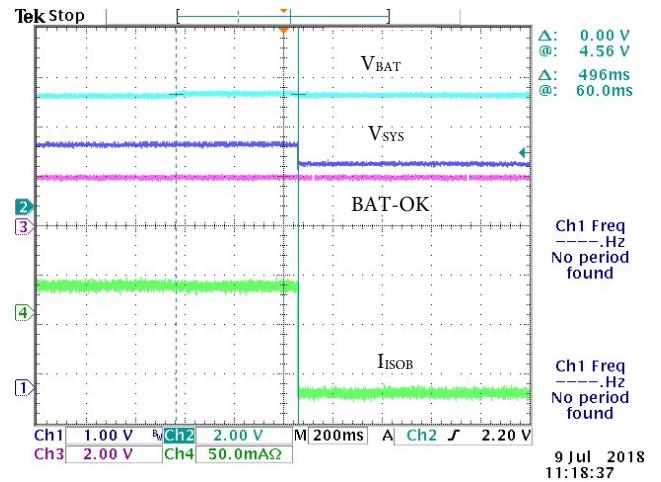
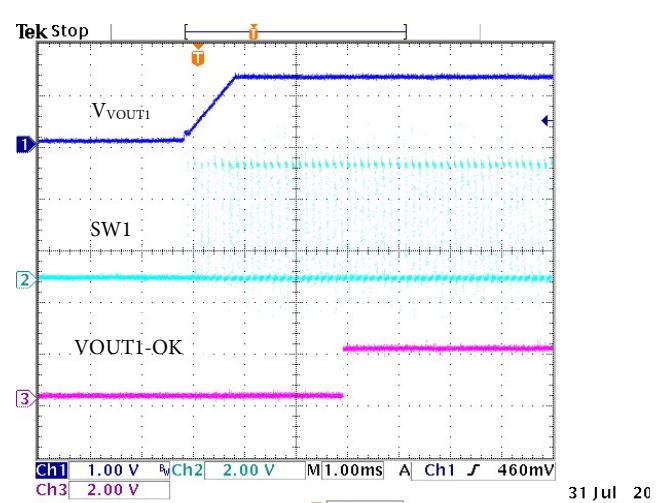
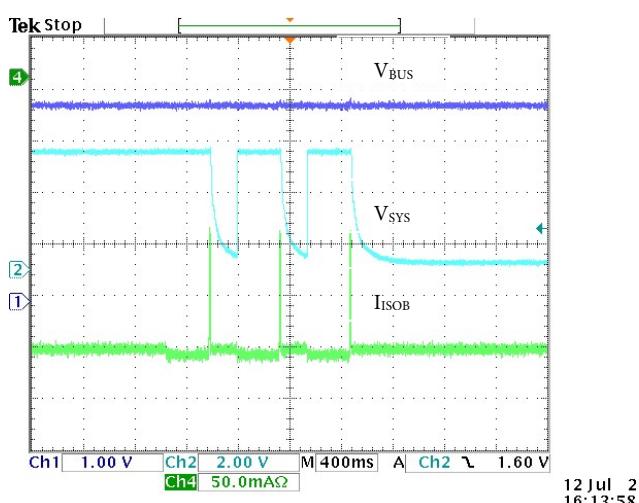
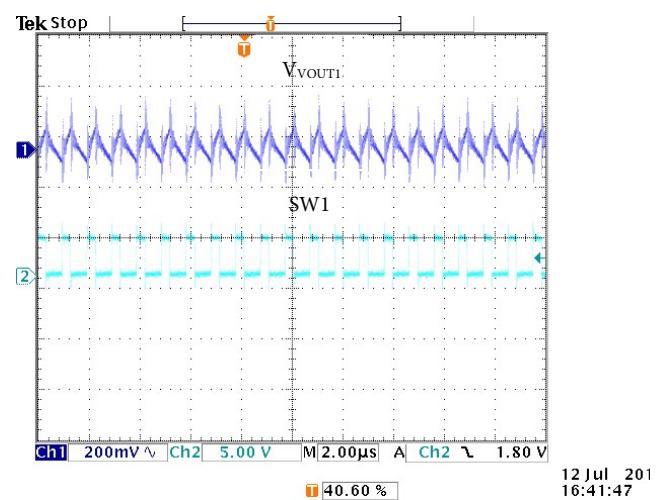
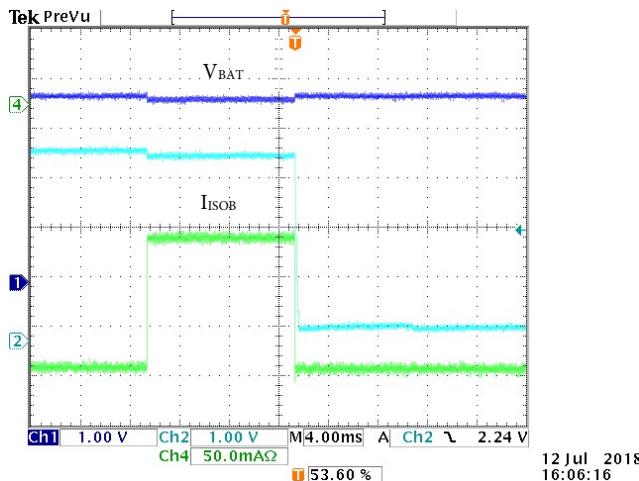
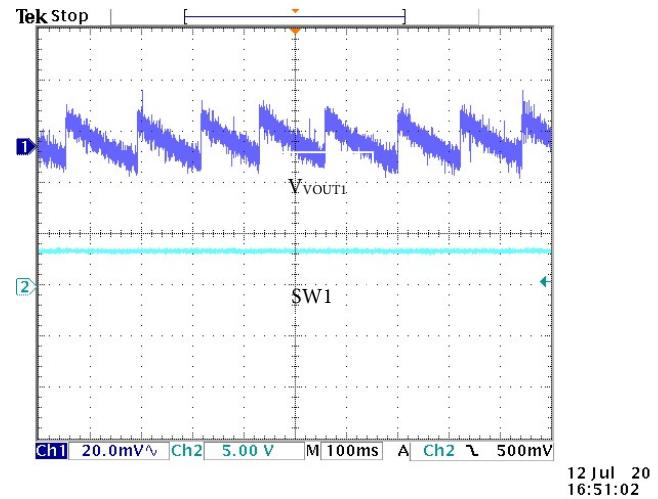
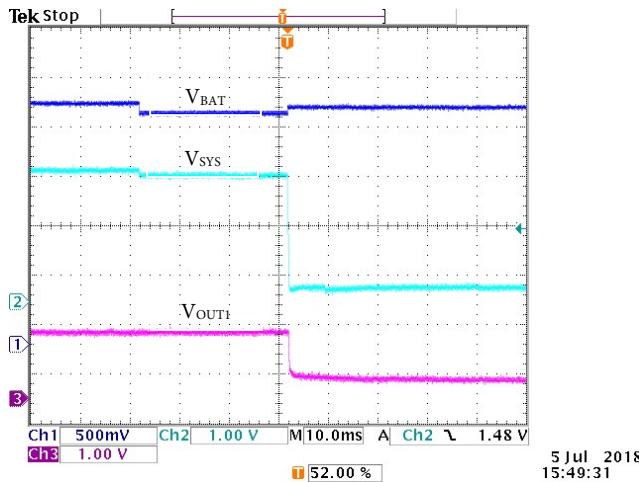


Figure 27. Battery UV Protection Waveform, Battery supply, no V_{BUS},
I_{SYS} = 100mA, Delightch time = 30ms



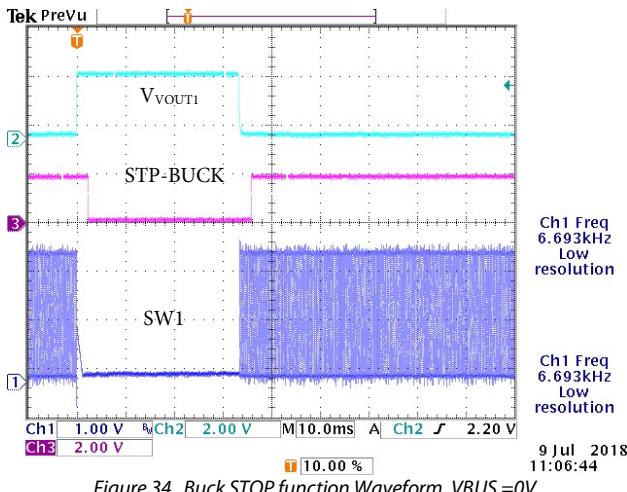


Figure 34. Buck STOP function Waveform, $V_{BUS} = 0V$,

$V_{ISOB} = 3.6V, V_{OUT1} = 1.2V$

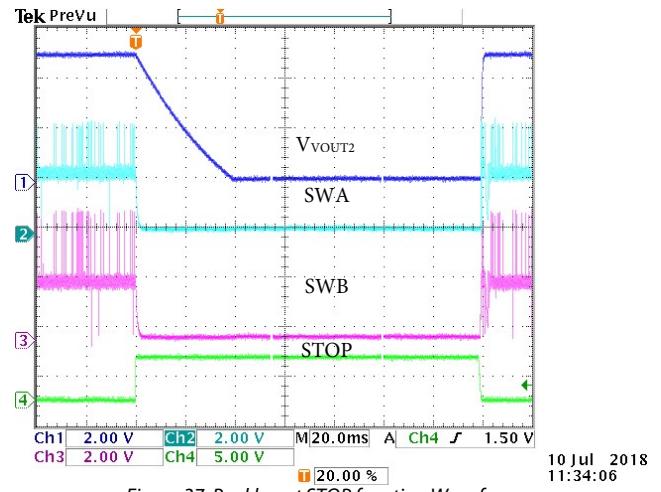


Figure 37. Buckboost STOP function Waveform,

$V_{BUS} = 5V, V_{ISOB} = 3.6V, V_{OUT2} = 5V$

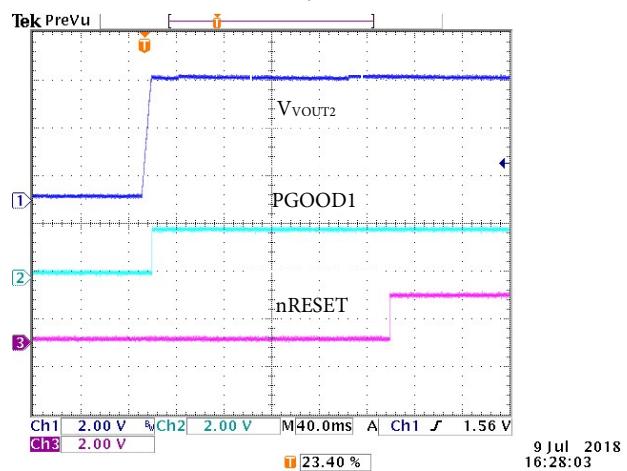


Figure 35. Buckboost Output Soft start Waveform,

$V_{BUS} = 0V, V_{ISOB} = 3.6V, V_{OUT2} = 5V, SS = 8ms$

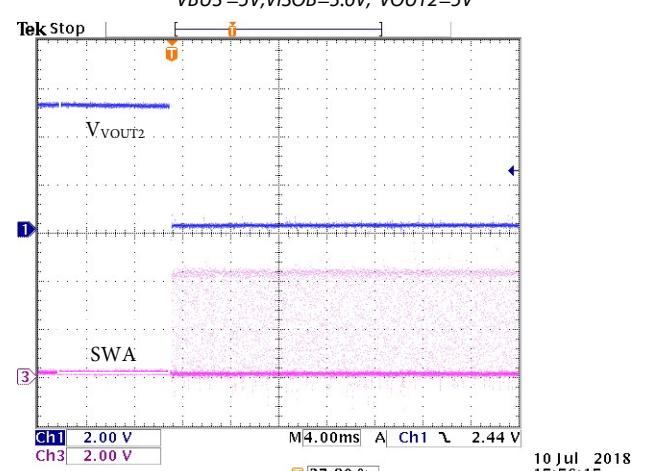


Figure 38. Buckboost Output Short Waveform,

$V_{BUS} = 5V, V_{ISOB} = 3.6V, V_{OUT2} = 5V$

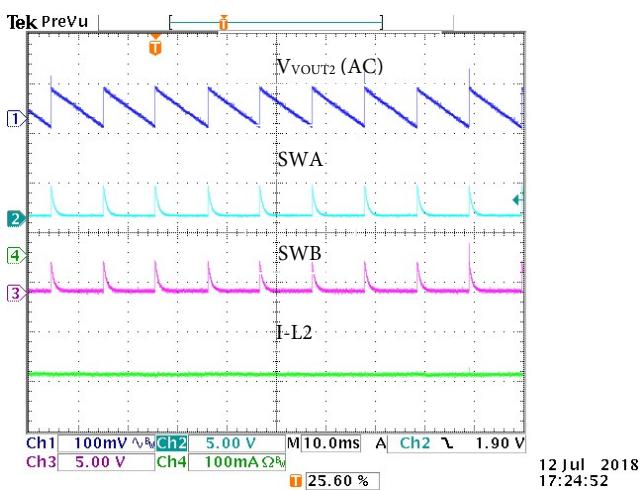


Figure 36. Buckboost Steady Waveform,

$V_{BUS} = 5V, V_{ISOB} = 3.6V, V_{OUT2} = 5V$

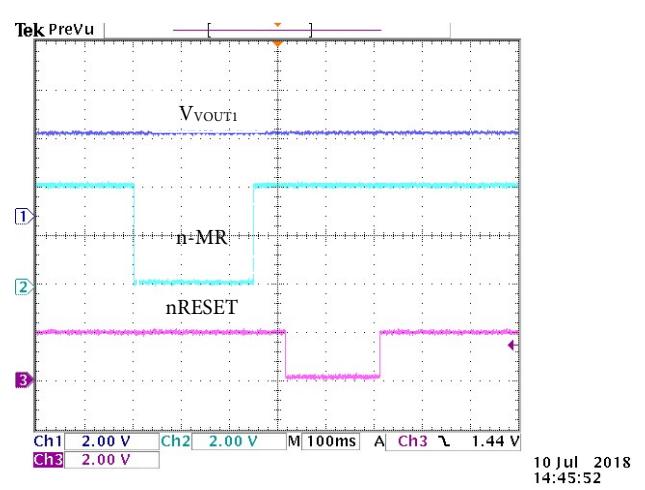


Figure 39. nRESET output and V_{OUT1} , $V_{BUS} = 0V, V_{ISOB} = 3.6V$,

$V_{OUT1} = 1.2V, T_{reset} = 200ms$

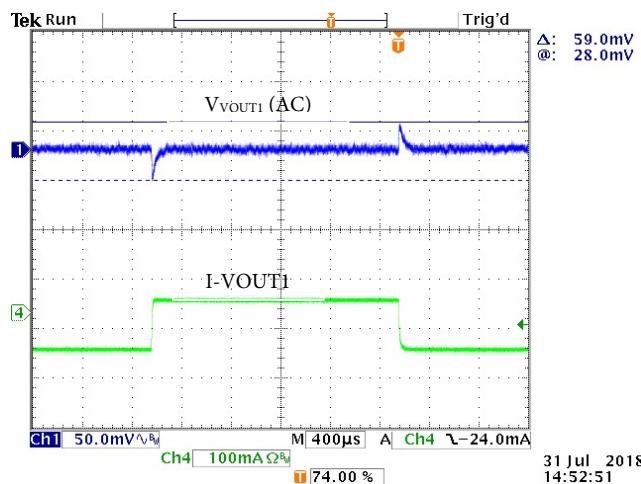


Figure 40. Buck Output Transient Waveform, Vin=4.3V, V OUT1=3.3V,Iout = 1mA to 100mA(PWM Mode)

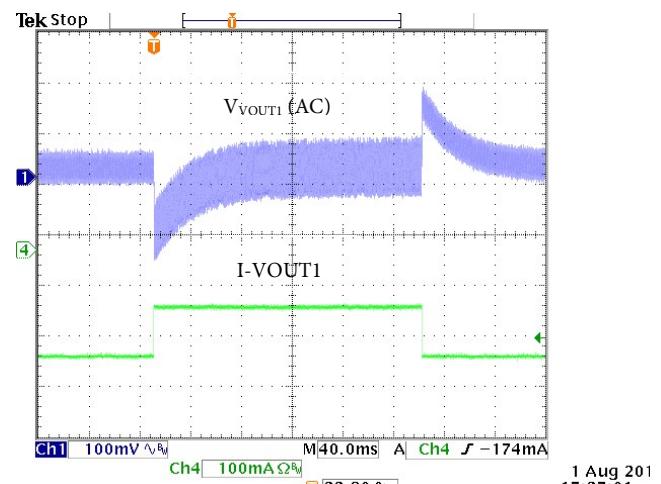


Figure 42. Buck Output Transient Waveform, Vin=4.3V, V OUT1=3.3V
(PWM mode)

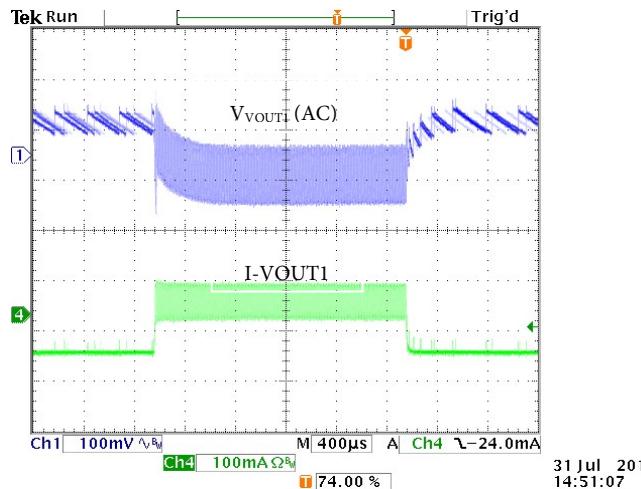


Figure 41. Buck Output Transient Waveform, Vin=4.3V, V OUT1=3.3V,Iout = 1mA to 100mA(PSM Mode)

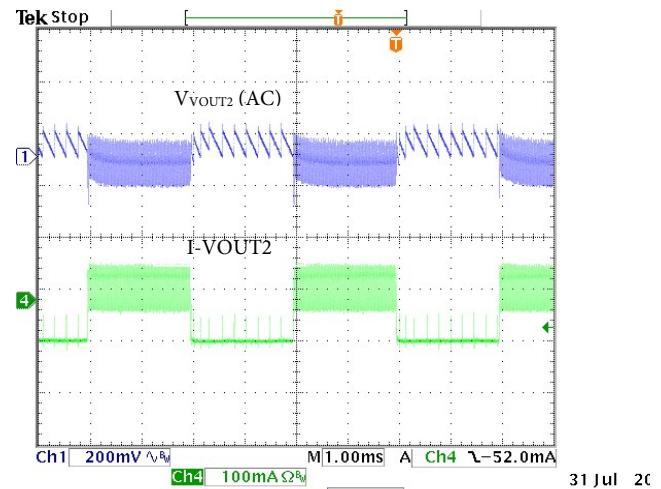


Figure 43. Buckboost Output Transient Waveform,
Vin=4.3V, V OUT2=3.3V,Iout = 1mA to 100mA

FUNCTION BLOCK DIAGRAM

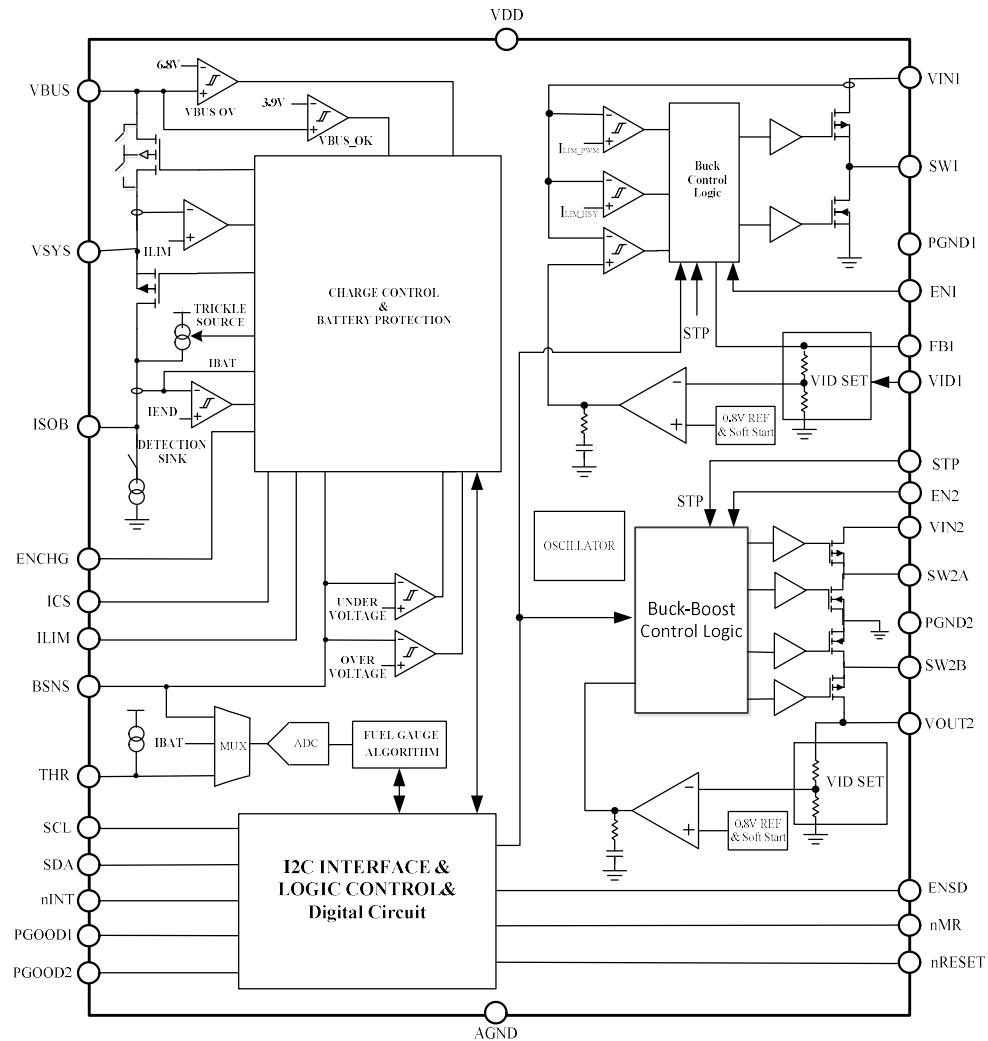


Figure 44. Function Block Diagram

THEORY OF OPERATION

BATTERY CHARGER

Charger Introduction

The ADP5360 integrates a fully I²C-programmable charger for single-cell lithium-ion or lithium-polymer batteries suitable for a wide range of portable applications.

The linear charger architecture enables up to 500 mA totally output current on the system power supply, and up to 320 mA charge current into the battery from a dedicated charger.

The charger of ADP5360 operates from an input voltage from 4 V to 6.5 V but is tolerant of voltages of up to 20 V. This alleviates the concern about USB bus spiking during disconnection or connection scenarios.

The ADP5360 features an internal FET between the linear charger output and the battery. This permits battery isolation and, hence, system powering in a dead battery or no battery scenario, which allows for immediate system function on connection to a USB power supply.

The charger of ADP5360 enables charging via the mini USB VBUS pin from a wall charger, car charger, or USB host port. Based on the type of USB source, which is detected by an external USB detection device, the ADP5360 can be set to apply the correct current limit for optimal charging and USB compliance. The USB charger permits correct operation under all USB compliant sources such as, wall chargers, host chargers, hub chargers, and standard hosts and hubs.

A processor is able to control the USB charger using the I²C to program the charging current and numerous other parameters including

- Trickle charge current level and voltage threshold.
- Fast charge (constant current) current level
- Fast charge (constant voltage) charge voltage level.
- Fast charge safety timer period.
- Weak battery threshold detection.
- End of charge current level for charge complete.
- Recharge threshold.
- VBUS input current limit.

Input Current Limit and USB Compatibility

The VBUS input current limit can be programmed via an internal I²C ILIM register from 50mA to 500mA, ensure compatibility with different requirements. Otherwise, the input current limit can use an external resister from ILIM pin to ground to set the input current limit as default. Float the ILIM pin will use register default value.

Table 9. VBUS input current limit default set Using the ILIM Pin

Register	ILIM (mA)
R _{ILIM} = 100 kΩ	50
R _{ILIM} = 68 kΩ	100

Register	ILIM (mA)
R _{ILIM} = 47 kΩ	150
R _{ILIM} = 36 kΩ	200
R _{ILIM} = 27 kΩ	250
R _{ILIM} = 20 kΩ	300
R _{ILIM} = 15 kΩ	400
R _{ILIM} = 10 kΩ	500

The current limit defaults to 100 mA to allow compatibility with a USB host or hub that is not configured. This input current limit will reset to 100mA default value during every cycle power on VBUS to protect USB port. When the input current limit feature is used, the available input current may be too low for the charger to meet the programmed charging current, I_{CHG}, and the rate of charge is reduced. In this case, the VBUS_ILIM flag is set.

When connecting voltage to VBUS without having the proper voltage level on the battery side, the HV blocking part is in a state wherein it draws only 1 mA (typical) of current until the V_{VBUS} has reached the V_{VBUS_OK} level.

Trickle Charge Mode

A deeply discharged Li-Ion cell may exhibit a very low cell voltage making it unsafe to charge the cell at high current rates. The ADP5360 charger uses a trickle charge mode to lift the cell voltage to a safe level for fast charging. A cell with a voltage below V_{TRK_DEAD} is charged with the trickle mode current, I_{TRK_DEAD}. During trickle charge mode, the CHARGER_STATUS register is set.

During trickle charging, the ISOS node is regulated to V_{SYS_REG} by the linear regulator and the battery isolation FET is off, which means the battery is isolated from the system power supply. The V_{SYS_REG} output voltage reference as table 10.

Table 10. V_{SYS_REG} output voltage

VTRM setting	V _{SYS_REG} (V)	
	V _{SYSTEM} = V _{TRM} +100mV	V _{SYSTEM} = 5V
VTRM ≤ 4.2 V	4.3 V	5V
4.2 V < VTRM ≤ 4.3 V	4.4 V	
4.3 V < VTRM ≤ 4.4 V	4.5 V	
4.4 V < VTRM ≤ 4.5 V	4.6 V	
4.5 V < VTRM ≤ 4.6 V	4.7V	

Trickle Charge Mode Timer

The duration of trickle charge mode is monitored to ensure the battery is revived from its deeply discharged state. If trickle charge mode runs for longer than 60 minutes without the cell voltage reaching V_{TRK_DEAD}, a fault condition is assumed and the

charging stops. The battery isolation FET will turn on and VSYS node through to ISOB node. The fault condition is asserted on the CHARGER_STATUS register, allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

Weak Charge Mode (Constant Current)

When the battery voltage exceeds V_{TRK_DEAD} but is less than V_{WEAK} , the charger switches to the weak charge mode and the VSYS node is regulated to V_{SYS_REG} by the battery isolation FET, and $V_{SYSTEM} = 5V$ is no active on V_{SYS_REG} output.

During weak charge mode, the battery will be charged with programmed I_{CHG} from VSYS node through isolation FET and trickle current I_{TRK_DEAD} . Due to the VBUS input current limit, the real charge current I_{CHG} from VSYS node may less than programmed value. And system load also can share the current from ISOS node. However, the trickle current I_{TRK_DEAD} keep to charge to battery always during weak charge mode.

Fast Charge Mode (Constant Current)

When the battery voltage exceeds V_{WEAK} , the charger switches to fast charge mode, charging the battery with the constant current, I_{CHG} . During fast charge mode (constant current), the CHARGER_STATUS register is set. The default I_{CHG} value can be set by external resister from ICS pin to ground, and changed by register set via I2C. Float the ICS pin will use register default value.

Table 11. Charge current default set Using the ICS Pin

Register	I_{CHG} (mA)
$R_{ICS} = 100\text{ k}\Omega$	10
$R_{ICS} = 68\text{ k}\Omega$	50
$R_{ICS} = 47\text{ k}\Omega$	80
$R_{ICS} = 36\text{ k}\Omega$	100
$R_{ICS} = 27\text{ k}\Omega$	150
$R_{ICS} = 20\text{ k}\Omega$	200
$R_{ICS} = 15\text{ k}\Omega$	250
$R_{ICS} = 10\text{ k}\Omega$	300

During constant current mode, other features may prevent the current, I_{CHG} , from reaching its full programmed value. Input current limiting for USB compatibility may affect the value of I_{CHG} under certain operating conditions. The voltage on VSYS is regulated to stay at V_{SYS_REG} by the battery isolation FET, and $V_{SYSTEM} = 5V$ is no active on V_{SYS_REG} output.

The ADP5360 features dynamic charge current adaptive in terms of input VBUS voltage drop during charging state. It monitor VBUS voltage and reduce charge current level once the VBUS voltage lower than the threshold, which can be program by I2C. When charge current adaptive due to VBUS voltage level, the ADPICHG status bit is set high. This feature is default disable and can be enable by I2C set.

Fast Charge Mode (Constant Voltage)

As the battery charges, its voltage rises and approaches the termination voltage, V_{TRM} . The ADP5360 charger monitors the voltage on the BSNS pin to determine when charging should end. However, the internal impedance of the battery pack combined with PCB and other parasitic series resistances creates a voltage drop between the sense point at the BSNS pin and the cell terminal itself. To compensate for this and ensure a fully charged cell, the ADP5360 enters a constant voltage charge mode when the BSNS voltage reach to termination voltage. The ADP5360 reduces charge current gradually as the cell continues to charge, maintaining a voltage of V_{TRM} on the BSNS pin. During fast charge mode (constant voltage), the CHARGER_STATUS register is set.

Fast Charge Mode Timer

The duration of fast charge mode is monitored to ensure that the battery is charging correctly. If the fast charge mode runs for longer than t_{CHG} without the voltage at the BSNS pin reaching V_{TRM} , a fault condition is assumed and charging stops and the battery isolation FET is turn on and in full conducting status. The fault condition is asserted on the CHARGER_STATUS register allowing the user to initiate the fault recovery procedure specified in the Fault Recovery section.

If the fast charge mode runs for longer than t_{CHG} , and V_{TRM} has been reached on the BSNS pin but the charge current has not yet fallen below I_{END} , charging stops by turn off the battery isolation FET while the linear regulator still works and the VSYS node is regulated to V_{SYS_REG} . No fault condition is asserted in this circumstance and ADP5360 will go to charge complete status.

Safety Timer

If the watchdog timer (see the **Watchdog Timer** section for more information) expires while in charger mode, the ADP5360 charger initiates the safety timer, t_{SAFE} . Charging continues for a period of t_{SAFE} , then stops by turn on the battery isolation FET, and sets the CHARGER_STATUS register.

Charge Complete

The ADP5360 charger monitors the charging current while in constant voltage fast charge mode. If the current falls below I_{END} and remains below I_{END} for t_{END} , the charger is stopped by turning the battery isolation FET off but the system voltage is maintained at V_{SYS_REG} by the linear regulator and set the CHG_CMPLT flag. If the charging current falls below I_{END} for less than t_{END} and then rises above I_{END} again, the t_{END} timer resets.

Recharge

After the detection of charge complete, and the isolate FET turns off, the ADP5360 charger still monitors the BSNS pin. If the BSNS pin voltage falls to V_{RCH} , the charger reactivates charging. Under most circumstances, triggering the recharge threshold results in the charger starting directly into fast charge constant current mode.

Battery Charging Enable/Disable

The ADP5360 charging function can be disabled by setting the I²C EN_CHG bit to low. If the I²C EN_CHG bit is low, the linear regulator is still on and regulate VSYS voltage to V_{SYS_REG}, the battery isolation FET is turn off and the linear regulator provides the power for the system.

BATTERY ISOLATION FET

The ADP5360 charger features an integrated battery isolation FET for power path control and battery protection. The battery isolation FET isolates a deeply discharged Li-Ion cell from the system power supply in both trickle and fast charge modes, thereby allowing the system to be powered at all times, the battery isolation FET maintains the V_{SYS_REG} voltage on the VSYS pin.

When VBUS is below V_{VBUS_OK}, the battery isolation FET is in full conducting status.

The battery isolation FET supplements the battery to support high current functions on the system power supply.

When voltage on VSYS drops below ISOB, the battery isolation FET enters into full conducting mode.

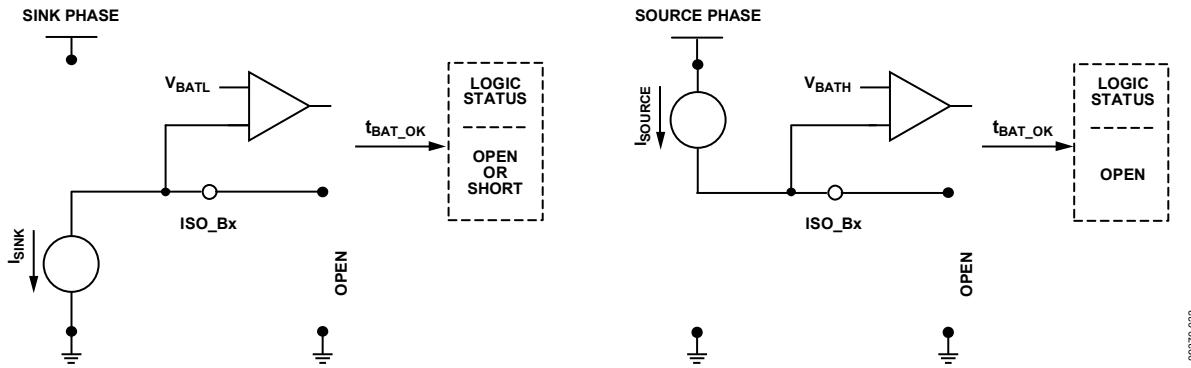


Figure 45. Battery Detection Sequence

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BATTERY TEMPERATURE

Battery Pack Thermistor Input

The ADP5360 charger features battery pack temperature sensing that precludes charging when the battery pack temperature is outside the specified range. The THR pin provides three programmable current source, 60uA, 12uA and 6uA accordingly support 10kΩ, 47kΩ and 100kΩ NTC at 25°C. The THR pin should be connected directly to the battery pack thermistor terminal.

When the THR function is enable, the THR node voltage sense by ADC and can be read in 12 bit register THR_V_HIGH and THR_V_LOW. Thus, the thermistor value and battery temperature also can be calculated below equation,

$$R_{NTC} = \frac{THR_V}{60\mu A}$$

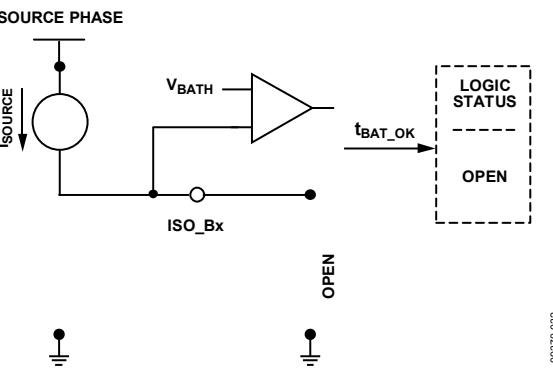
BATTERY DETECTION

Battery Level Detection

The ADP5360 charger features a battery detection mechanism to detect an absent battery. The charger actively sinks and sources current into the ISOB/BSNS node when the V_{BUS} has reached the V_{BUS_OK} level, and voltage vs. time is detected. The sink phase is used to detect a charged battery, whereas the source phase is used to detect a discharged battery.

The sink phase (see Figure 45) sinks I_{SINK} current from the ISOB/BSNS pin for a time, t_{BATOK}. If the BSNS pin is below V_{BATL} when the t_{BATOK} timer expires, the charger assumes no battery is present, and starts the source phase. If the BSNS exceeds the V_{BATL} voltage when the t_{BATOK} timer expires, the charger assumes the battery is present, and begins a new charge cycle.

The source phase sources I_{SOURCE} current to ISOB or the BSNS pin for a time, t_{BATOK}. If the BSNS pin exceeds V_{BATH} before the t_{BATOK} timer expires, the charger assumes that no battery is present. If the BSNS does not exceed the V_{BATH} voltage when the t_{BATOK} timer expires, the charger assumes that a battery is present, and begins a new charge cycle.



THR_V is ADC read back from THR_V_HIGH and THR_V_LOW register, 60uA is selected THR pin source current.

When VBUS voltage higher than V_{VBUS_OK_RISE}, the THR function is forced enable for charger control requirement. The update rate is 1 second. When the VBUS voltage low than V_{VBUS_OK_RISE}, set the EN_THR bit(Register 0x07) high to enable THR function. Then the THR node voltage update rate is 30 seconds to save quiescent current.

If the battery pack thermistor is not connected directly to the ADP5360 THR pin, a 100 kΩ (tolerance ±20%) dummy resistor must be connected between the THR and AGND. Leaving the THR pin open results in a false detection of the battery temperature being <0°C and charging is disabled.

The ADP5360 charger monitors the voltage on the THR pin and suspends charging if the voltage is outside the range of less than 0°C or larger than 60°C. For temperatures greater than 0°C, the THR_STATUS register is set accordingly, and for

temperatures lower than 60°C, the THR_STATUS register is, likewise, set accordingly.

JEITA Li-Ion Battery Temperature Charging Specification

The charge of ADP5360 is compliant with the JEITA Li-Ion battery charging temperature specifications as shown in Table 12.

The JEITA function can be enabled via the I²C interface. When the ADP5360 detects a JEITA cool condition, charging current is reduced according to Table 13.

When the ADP5360 identifies a hot or cold battery condition, the ADP5360 takes the following actions: the battery isolation FET turns off and linear regulated at V_{SYS_REG} and provide power for the system.

Table 12. JEITA Li-Ion Battery Charging Specification Defaults

Parameter	Symbol	Conditions	Min	Max	Unit
JEITA Cold Temperature Limits	I _{JEITA_COLD}	No battery charging occurs.		0	°C
JEITA Cool Temperature Limits	I _{JEITA_COOL}	Battery charging occurs at approximately 50% or 10% of programmed level. See Table 13 for specific charging current reduction levels.	0	10	°C
JEITA Typical Temperature Limits	I _{JEITA_TYP}	Normal battery charging occurs at default/programmed levels.	10	45	°C
JEITA Warm Temperature Limits	I _{JEITA_WARM}	Battery termination voltage (V _{TRM}) is reduced by 100 mV from programmed value.	45	60	°C
JEITA Hot Temperature Limits	I _{JEITA_HOT}	No battery charging occurs.	60		°C

Table 13. JEITA Reduced Charge Current Levels

JEITA Cool Temperature Limit—Reduced Charge Current Levels		
ICHG[4:0]	ICHG JEITA (mA)	
	ILIM_JEITA_COOL = 0	ILIM_JEITA_COOL = 1
00000 = 10 mA	10	10
00001 = 20 mA	10	10
00010 = 30 mA	10	10
00011 = 40 mA	20	10
00100 = 50 mA	20	10
00101 = 60 mA	30	10
00110 = 70 mA	30	10
00111 = 80 mA	40	10
01000 = 90 mA	40	10
01001 = 100 mA	50	10
01010 = 110 mA	50	10
01011 = 120 mA	60	10
01100 = 130 mA	60	10
01101 = 140 mA	70	10
01110 = 150 mA	70	20
01111 = 160 mA	80	20
10000 = 170 mA	80	20
10001 = 180 mA	90	20
10010 = 190 mA	90	20
10011 = 200 mA	100	20
10100 = 210 mA	100	20
10101 = 220 mA	110	20
10110 = 230 mA	110	20
10111 = 240 mA	120	20
11000 = 250 mA	120	30
11001 = 260 mA	130	30
11010 = 270 mA	130	30
11011 = 280 mA	140	30
11100 = 290 mA	140	30
11101 = 300 mA	150	30

11110 = 310 mA	150	30
11111 = 320 mA	160	30

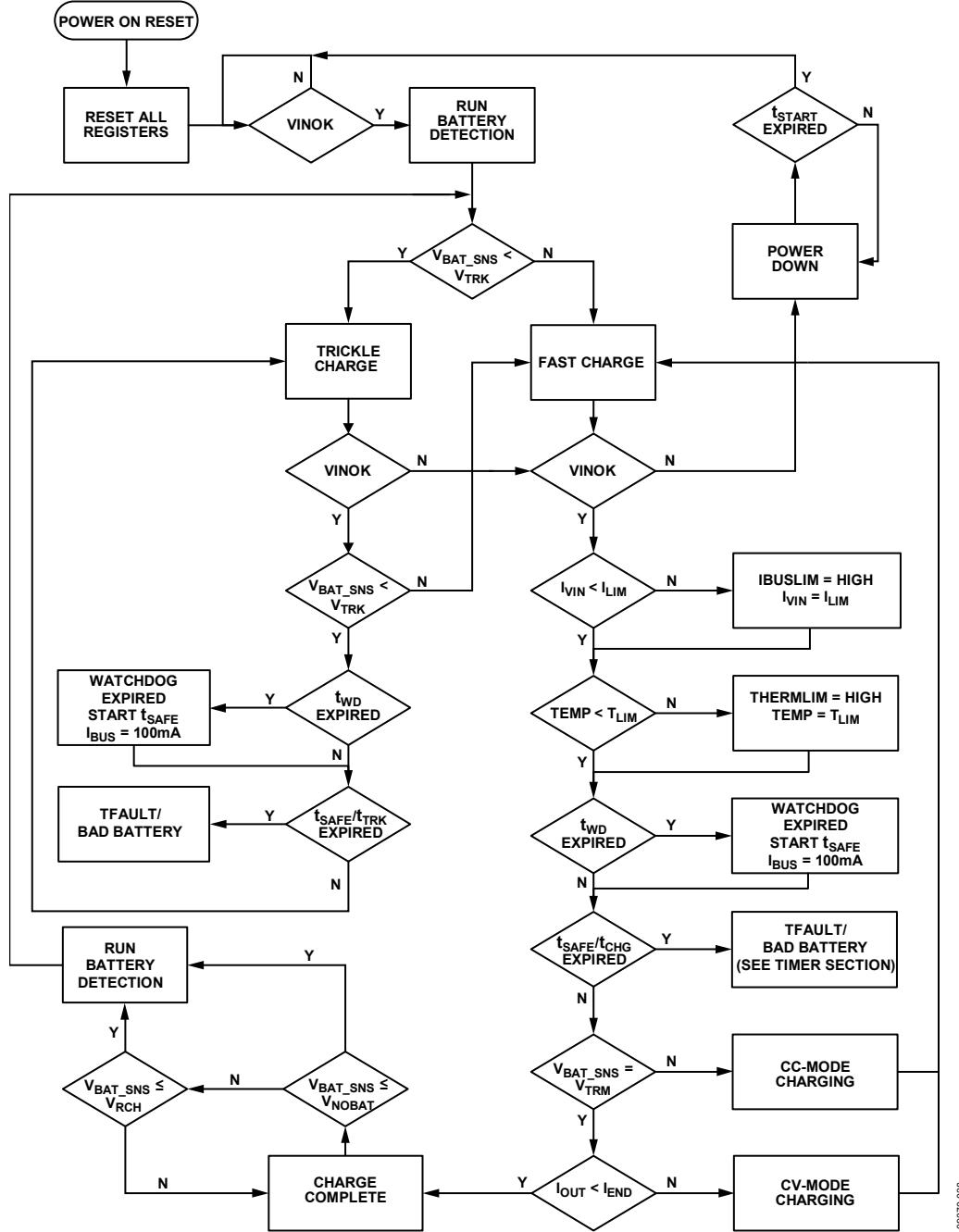
Battery Charger Operational Flow Chart

Figure 46. ADP5360 charger operational Flowchart

00370-038

BATTERY FUEL GAUGE

General Description

The ADP5360 Li-Ion battery fuel gauge is optimized hybrid algorithm to indicate battery remaining capacity, which is voltage based and coulomb counter together, between 0 to 100. Use a 12-bit ADC measure battery node voltage and battery current. State of Charge (SoC) is calculated with a model integrated in ADP5360. Ten battery open circuit voltage values and battery capacity based on battery characterization need to be written to the register of ADP5360 and used for SoC calculation. The sense current information and calculate battery capacity value determine the SoC change rate, with continuous load current and big voltage drop, the fuel gauge operate as coulomb counter with high accuracy calculation. When the battery voltage reach to terminal voltage and charger complete, the battery fuel gauge will indicate 100% for battery capacity.

When the SoC data lower than SOC_LOW_TH configuration, the interrupt will assert and SOCLOW_INT bit set high as long as low SoC interrupt feature is allow.

Operation Mode

ADP5360 fuel gauge default as shut down mode that provides extremely low standby current consumption from battery. After fuel gauge function was enabled, the SoC will be initialized and calculate first data only according to battery voltage. There are two operation modes can be selected: active mode and sleep mode. The fuel gauge operation modes selection are controlled by I²C.

During active mode, the battery SoC will be updated every 10 seconds and the battery voltage and instant current (I_{INS}) will be sampled every second. The new mapping SoC will compare to the last SoC value then update by the adaptive SoC limit.

According to the sense current and input battery capacity, the ADP5360 will calculate the SoC limit for SoC update each cycle.

During sleep mode, the SoC update cycle is 1 minutes, voltage and current will be sampled each 7.5 seconds. During this mode, the 12-bit-ADC works interval and shut down in most time to save much quiescent current. Table 14 show the fuel gauge quiescent current, ADC sample rate and SoC update rate. When the sense current higher than sleep current threshold setting, register SLP_CURR, the ADP5360 fuel gauge will exit sleep mode to active mode automatically.

Table 14. Fuel Gauge Operation Mode

Operation Mode	Current (typical)	ADC sample rate	SoC update rate
Sleep	0.2 uA	7.5/15/30/60 s	1/4/8/16 min

Flowchart of SoC Calculation

Active	5 uA	1 s	10 s
--------	------	-----	------

Battery Capacity Adjustment By Aging

ADP5360 features reporting total battery charge energy start from the moment of ADP5360 power up, which allow estimate the battery situation of aging.

The 12 bits register BAT_SOCACM accumulate increased SOC during every charge cycle, for example, the SOC increase from 20% to 80% by one time charging, the BAT_SOCACM will add 60 points, so 100 points means one full charge cycle.

When the BAT_SOCACM increase and reach to 4096 points, which means the battery has complied near to 41 times full charge. Then the BAT_SOCACM register will overflow and clear itself. The interrupt SOCACM_INT immediately assert and system can adjust battery capacity manually or select automatic adjustment by set EN_BATCAP_ADJ bit high. When select battery aging automatic adjustment function, the battery capacity reduction proportion can be programmable by register BATCAP_ADJ. And the BATCAP register can't be re-write due to it will be adjust automatic by ADP5360 itself.

Battery Capacity Adjustment By Temperature

The li-ion battery capacity is very depend on ambient operation temperature. The ADP5360 can automatically adjust battery capacity calculate value base on temperature variation when set EN_BATCAP_TEMP high. The temperature information comes from THR node voltage sense, so the battery THR function need to be active and EN_THR set high.

The battery capacity calculate value adjustment proportion can be program by register BATCAP_TEMP, and it decrease with the temperature rise. Note that this battery capacity adjustment only effective when the THR node voltage sense during the corresponding range of Temp_High_45 to Temp_low_0, see below figure.

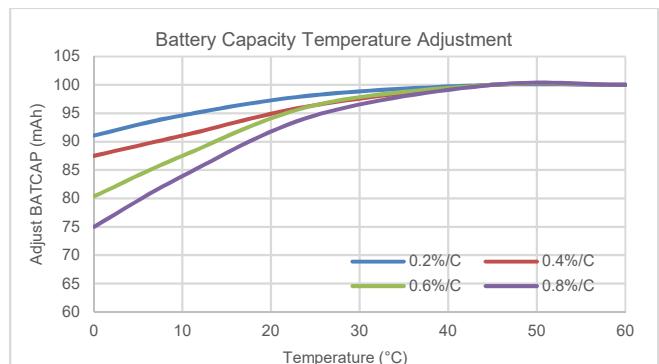


Figure 47. ADP5360 battery capacity adjustment by temperature in Fuel Gauge

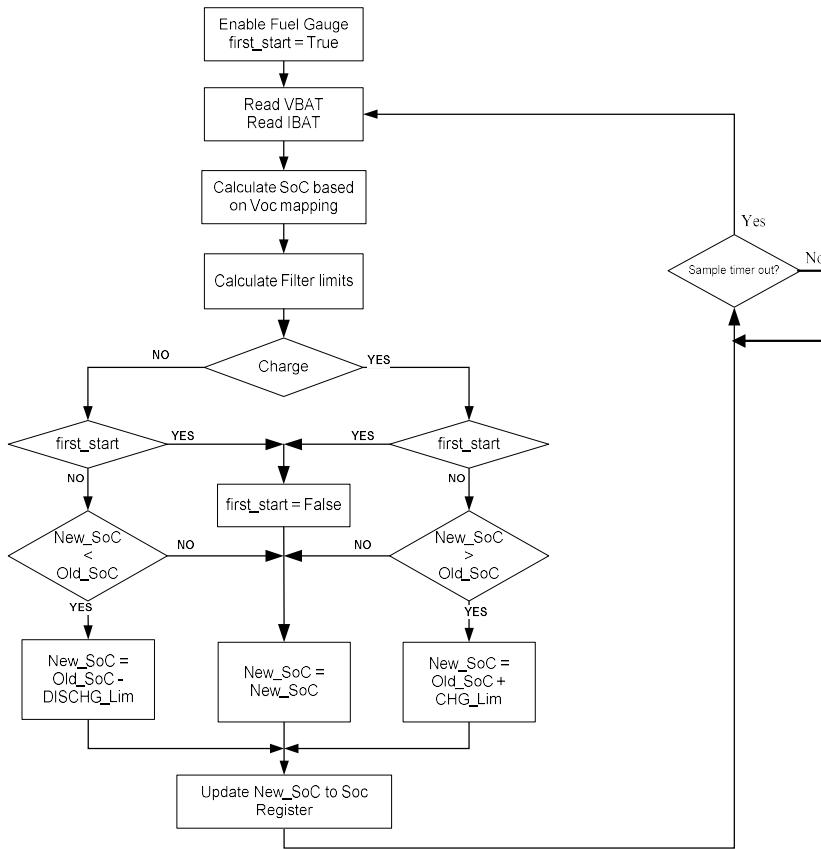


Figure 48. ADP5360 fuel gauge algorithm Flowchart

BATTERY PROTECTION

The ADP5360 features fully battery protection feature for Li-ion and Li-poly battery. The battery protection was default enabled after ISOB pin voltage higher than V_{UVLO} and exit from shipment mode. The ADP5360 support below faults protection:

- Under voltage protection when battery over discharge.
- Over discharge current protection.
- Over voltage protection when battery over charge.
- Over charge current protection.

When the BSNS pin voltage lower than battery under voltage threshold after deglitch time, under voltage protection will triggered, the isolation FET turns off and isolate all system load to ISOB node, the BAT_UV_STAT bit is set high to indicate the battery status and fault register assert meanwhile. During under voltage protection, the charger allow to start trickle charge to battery and exit under voltage protection once battery voltage higher than under voltage threshold. Or not allow any charge for some battery safety consideration if register 0x11 EN_CHGLB bit set low. The under voltage threshold and response time can be selected by I2C program.

When the battery discharge current through the isolation FET increase and higher than over current threshold after deglitch time, the over current protection will triggered, the isolation FET

turns off and isolate all system load to ISOB node. The protection behavior can be select to latch up or hiccup mode by setting OC_DIS_HICCUP bit. If select latch up protection mode, the isolation FET will keep in turn off and shut down Vsyst output after three times retry. Clear fault register or VBUS power reset can recover to normal operation once the fault removed. If select hiccup protection mode, the isolation FET will always try to turn on after some time shut down until the system load fault removed.

When it occurs battery over voltage protection in charging, the LDO FET is turn off, stop charge and stay in suspend status. The isolation FET can be select to turn off or keep turn on during the protection.

When the battery over charge current triggered, the LDO FET is turn off, stop charge and stay in suspend status. The isolation FET is also turn off and shut down Vsyst output. If select latch up over charge protection mode, the charger will keep in suspend status and battery not allow for charging after three times retry. To trig manual reset or power reset can recover to normal operation when the fault removed. If select hiccup protection mode, the charger will always try to restart charge until the charger fault removed. Clear fault register or VBUS power reset can recover to normal operation after the fault removed.

All battery protection function selection need to be done once the ADP5360 power up, please do not change the battery protection function during battery fault occur.

BUCK REGULATOR OPERATION

Operation mode

The [ADP5360](#) has two operate mode, forced PWM mode and hysteresis mode, which can be controlled by I2C program.

PWM Mode

In PWM mode, the buck regulator in the [ADP5360](#) operates at a fixed 1MHz frequency that is set by an internal oscillator. At the start of each oscillator cycle, the high-side MOSFET switch turns on and sends a positive voltage across the inductor. The inductor current increases until the current sense signal exceeds the peak inductor current threshold, which turns off the high-side MOSFET switch. This threshold is set by the error amplifier output. During the high-side MOSFET off time, the inductor current decreases through the low-side MOSFET until the next oscillator clock pulse starts a new cycle.

In PWM mode, the regulator can supply up to 500 mA of output current. The regulator can provide lower voltage ripple in PWM mode, which is useful for noise sensitive applications.

Hysteresis Mode

In hysteresis mode, the buck regulator in the [ADP5360](#) charges the output voltage slightly higher than its nominal output voltage with PWM pulses by regulating the constant peak inductor current, which can be program by I2C. When the output voltage increases until the output sense signal exceeds the hysteresis upper threshold, the regulator enters standby mode. In standby mode, the high-side and low-side MOSFETs and a majority of the circuitry are disabled to allow a low quiescent current as well as high efficiency performance.

During standby mode, the output capacitor supplies energy into the load and the output voltage decreases until it falls below the hysteresis comparator lower threshold. The buck regulator wakes up and generates the PWM pulses to charge the output again.

Because the output voltage occasionally enters standby mode and then recovers, the output voltage ripple in hysteresis mode is larger than the ripple in PWM mode.

In hysteresis mode, the regulator supplies up to 100 mA of output current with a relatively large output ripple compared to PWM mode.

Program Output Voltages

The [ADP5360](#) provides adjustable output voltage settings by connecting one resistor through the VID1 pin to AGND. The VID detection circuitry works in the start-up period, and the voltage ID code is sampled and held into the internal register and does not change until the next power recycle. ADP5360 fuel gauge default as shut down mode that provides extremely low standby current consumption from battery. After fuel gauge

function was enabled, the SoC will be initialized and calculate first data only according to battery voltage. There are two operation modes can be selected: active mode and sleep mode. The fuel gauge operation modes selection are controlled by I2C.

Table 17 lists the output voltage options by the VID1 pin configurations. Furthermore, the [ADP5360](#) output voltage provide more output voltage options from 0.6V to 3.75V with 50mV step, which can be program by register set via I2C. It also provides a fixed output voltage programmed via the factory fuse. In this condition, connect the VID pin to the PVIN pin.

For the output voltage settings, the feedback resistor divider is built into the [ADP5360](#), and the feedback pin (FB1) must be tied directly to the output. An ultralow power voltage reference and an integrated high impedance feedback divider network contribute to the low quiescent current. Float the ILIM pin will use register default value.

Table 15. Output Voltage (V_{OUT}) default set Using VID1 Pin.

RVID1	V_{OUT} (V)
$R_{VID1} = 100\text{ k}\Omega$	3.3
$R_{VID1} = 68\text{ k}\Omega$	3.0
$R_{VID1} = 47\text{ k}\Omega$	2.8
$R_{VID1} = 36\text{ k}\Omega$	2.5
$R_{VID1} = 27\text{ k}\Omega$	1.8
$R_{VID1} = 20\text{ k}\Omega$	1.5
$R_{VID1} = 15\text{ k}\Omega$	1.2
$R_{VID1} = 10\text{ k}\Omega$	1.0

Enable/Disable

The [ADP5360](#) includes a hardware enable pin (EN1). A logic high in the EN1 pin starts the buck regulator. Due to the low quiescent current design, it is typical for the regulator to start switching after a delay of a few milliseconds from the EN1 pin being pulled high.

The I2C register bit EN_BUCK also can control buck enable and disable, which is logically “AND” with EN1 pin. For example, set high to EN_BUCK bit then use hardware EN1 pin control buck enable and disable, or pull high EN1 pin then set EN_BUCK bit by I2C control.

PGOOD indication

The [ADP5360](#) register bit VOUT1OK indicates the buck regulator work appropriate or not. A logic high indicates that the output voltage of buck regulator is above 90% (typical) of its nominal output. When the regulated output voltage falls below 87% (typical) of its nominal output, the bit VOUT1OK goes low.

The bit VOUT1OK status indication can be mask to hardware pin output PGOOD1pin or PGOOD2 pin by I2C set register PGOODx_MASK.

Soft Start

The [ADP5360](#) buck regulator has an internal soft start function that ramps up the output voltage in a controlled manner upon

startup, thereby limiting the inrush current. This feature prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the device. The default typical soft start time is 1 ms for the regulator. Other soft start time 8 ms, 64 ms and 512 ms can be programmed for ADP5360 by I2C.

100% Duty Cycle Operation

When the input voltage approaches the output voltage, the ADP5360 stops switching and enters 100% duty cycle operation. It connects the output via the inductor and the internal high-side power switch to the input. When the input voltage is charged again and the required duty cycle falls to 95% typical, the buck immediately restarts switching and regulation without allowing overshoot on the output voltage.

Active Discharge

The ADP5360 integrates an optional discharge switch from the switching node to ground. This switch turns on when its associated regulator is disabled, which helps discharge the output capacitor quickly. The typical value of the discharge switch is $290\ \Omega$ for the regulator.

The active discharge feature can be enabled by set DISCHG_BUCKBST bit high for buck-boost regulator.

Current Limit

The buck regulator in the ADP5360 has protection circuitry that limits the direction and the amount of current to a certain level that flows through the high-side MOSFET and the low-side MOSFET in cycle-by-cycle mode. The positive current limit on the high-side MOSFET limits the amount of current that can flow from the input to the output. The negative current limit on the low-side MOSFET prevents the inductor current from reversing direction and flowing out of the load.

Short-Circuit Protection

The buck regulator in ADP5360 includes frequency foldback to prevent current runaway on a hard short in PWM mode. When the output voltage at the feedback pin (FB1) falls below 0.3 V typical, indicating the possibility of a hard short at the output, the switching frequency is reduced to half of the internal oscillator frequency. The reduction in the switching frequency allows more time for the inductor to discharge, preventing a runaway of output current.

STOP switching

The ADP5360 includes one STP pins, which can be configured as STOP pins to allow the user temporarily stop the buck regulator switching.

When a logic high level is applied to the STP pin, the corresponding regulator is forced to stop the switching immediately. When a logic low level is applied to the pin, the regulator resumes the switching. Noted tens of nS delay time exists from STP signal goes high to PWM switching fully stops.

The stop signal control is valid only when the regulator is enabled, or else the stop signal is ignored.

Usually the stop signal is used for hysteresis mode with its fast transient response, the DCM mode could possibility generate a PGOOD failure due to its slow transient response.

Set STP_BUCK bit set low to disable buck regulator STOP switching feature.

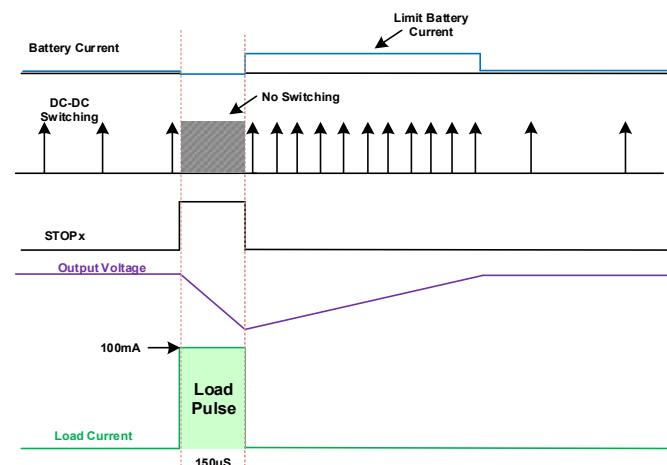


Figure 49. STOPx Signal Diagram

BUCK-BOOST REGULATOR OPERATION

Operation Mode

The buck-Boost Regulators in ADP5360 is synchronous current-mode switching regulator designed to maintain a fixed output voltage V_{OUT2} from an input supply V_{IN2} that can be greater than, equal to, or less than V_{OUT2} .

The buck-boost regulator works in hysteresis mode and regulate the output voltage slightly higher than its target output voltage with PWM pulses by the regulation of constant peak inductor current. When the output voltage increases until the output sense signal exceeds the hysteresis upper threshold, the regulator enters the sleep mode. In sleep mode, the high-side and low-side MOSFET and a majority of the circuitry are disabled to allow for a low quiescent current as well as high efficiency performance. During sleep mode, the output capacitor supplies the energy into the load and the output voltage decreases until it falls below the hysteresis comparator lower threshold, the regulator wakes up and generate the PWM pulses to charge the output again.

Program Output Voltages

The ADP5360 buck-boost regulator provide output voltage options from 1.8V to 2.9V with 100mV step, and 2.95V to 5.5V with 50mV step, which can be program by register set via I2C. It also provides a fixed output voltage programmed via the factory fuse.

For the output voltage settings, the feedback resistor divider is built into the ADP5360. An ultralow power voltage reference and an integrated high impedance (50 M Ω typical) feedback divider network contribute to the low quiescent current.

Enable/Disable

The ADP5360 includes a hardware enable pin (EN2). A logic high in the EN2 pin starts the buck-boost regulator. Due to the low quiescent current design, it is typical for the regulator to start switching after a delay of a few milliseconds from the EN2 pin being pulled high.

The I2C register bit EN_BUCKBST also can control buck-boost enable and disable, which is logically “OR” with EN2 pin. For example, set low to EN_BUCKBST bit then use hardware EN2 pin control buck-boost enable and disable, or pull low EN2 pin then set EN_BUCKBST bit by I2C control.

PGOOD indication

The ADP5360 register bit VOUT2OK indicates the buck-boost regulator work appropriate or not. A logic high indicates that the output voltage of buck-boost regulator is above 90% (typical) of its nominal output. When the regulated output voltage falls below 87% (typical) of its nominal output, the bit VOUT2OK goes low.

The bit VOUT2OK status indication can be mask to hardware pin output PGOOD1pin or PGOOD2 pin by I2C set register PGOODx_MASK.

Soft Start

The ADP5360 buck-boost regulator has an internal soft start function that ramps up the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This feature prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the device. The default typical soft start time is 1 ms for the regulator. Other soft start time 8 ms, 64 ms and 512 ms can be programmed for ADP5360 by I2C.

Active Discharge

The ADP5360 integrates an optional discharge switch from the output node to ground. This switch turns on when its associated regulator is disabled, which helps discharge the output capacitor quickly. The typical value of the discharge switch is $290\ \Omega$ for the regulator.

The active discharge feature can be enabled by set DISCHG_BUCKBST bit high for buck-boost regulator.

Current-Limit Protection

The buck-boost regulators in the ADP5360 include peak current-limit protection circuitry to limit the amount of positive current flowing through the high-side MOSFET switch. The peak current limit on the power switch limits the amount of current that can flow from the input to the output. The programmable current-limit threshold feature allows for the use of small size inductors for low current applications.

The peak current limit threshold on buck-boost regulator can be programmable by the register ILIM1, ILIM2 and via I2C or factory fuse. 2-bits programmable options provides 100mA to 800mA with 100mA step peak-current threshold range.

Notes the peak current limit is different to the average current limit in battery input side. The average battery current is a factor of different elements including VIN/VOUT relationship, the inductance, switching frequency, peak current limit threshold and others. The average battery current limit on each buck or buck-boost regulator can be roughly calculated and predicted by above factors, however the average current limit accuracy is difficult to guarantee due to all kinds of variations, therefore, a careful design must be taken if input source is coming from weak battery, which usually has high output impedance.

STOP switching

The STOP feature also can configure to buck-boost regulator with STP pin input which allow the user temporarily stop the buck-boost regulator switching.

When a logic high level is applied to the STP pin, the corresponding regulator is forced to stop the switching immediately. When a logic low level is applied to the pin, the regulator resumes the switching. Noted tens of nS delay time exists from STP signal goes high to PWM switching fully stops.

The stop signal control is valid only when the regulator is enabled, or else the stop signal is ignored.

Set STP_BUCKBST bit low to disable buck-boost regulator STOP switching feature.

SUPERVISORY

Reset Output

The ADP5360 provides microprocessor supply voltage supervision by controlling the reset input of the microprocessor. When the monitored voltage falls below its associated threshold, the nRESET is asserted correspondingly. Asserting nRESET this quickly ensures that the entire system can be reset at once before any part of the system voltage falls below its recommended operating voltage. The default monitor voltage is buck output Vout1 and can be select as Vout2 by I2C register program. The nRESET will monitor both Vout1 and Vout2 when set VOUT1_RST and VOUT2_RST bit both high.

Manual Reset Input

The ADP5360 features a manual reset input. When drive MR low from high with deglitch time t_{DG} , the nINT pin assert an interrupt if set bit EN_MR_INT high. When MR transitions from low to high, the nRESET output assert and remains for the duration of the reset timeout period before deasserting. The MR input has an internal $600\ k\Omega$ pull-up resistor so that the input remains high when unconnected. To generate a reset, connect an external push-button switch between MR and ground. Noise immunity is provided on the MR input, and fast, negative going transients of up to 400 ns (typical) are ignored. A $0.1\ \mu F$ capacitor between MR and ground provides additional noise immunity if required.

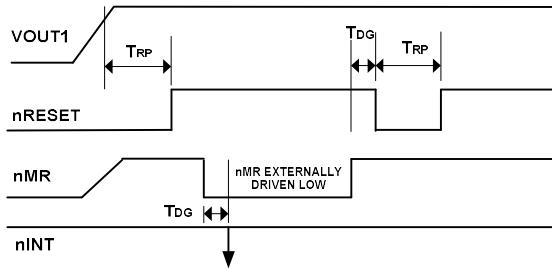


Figure 50. Manual Reset Timing Diagram

When drive \overline{MR} low for longer than t_{sh} time out then release MR , the ADP5360 will shut down all function blocks and enter to shipment mode if this function was enable by set register 0x2D bit 1, and the next time drive MR low for t_{sh} to exit shipment mode and restart the ADP5360 with default all register factory setting.

Watchdog Timer

The ADP5360 features a watchdog timer which monitor microprocessor activity. A timer circuit is cleared with every write RESET_WD bit. If the timer counts through the preset watchdog timeout period (t_{WD}), a nRESET output is asserted. The microprocessor must toggle the WDI register to avoid being reset.

When nRESET is asserted, the watchdog timer is cleared and does not being counting again until the nRESET output is deasserted. The watchdog timer can be disable by setting register via I2C. The watchdog timer would be ignored when nRESET is not activated.

If the watchdog timer expires without being reset while in charger mode, the ADP5360 charger assumes there is a software problem and triggers the safety timer, t_{SAFE} . For more information see the Safety Timer section.

SHIPMENT MODE

The ADP5360 provides optional shipment mode as default status after ISOB power up. During shipment mode, most function block is shut down and the ADP5360 achieves ultra low shut down current. The ISOFET also turns off and no VSYS output voltage help all system under very low quiescent current. To connect ENSD pin to high to enable this shipment mode, the ADP5360 will enter to shipment mode when initial power up. Connect ENSD pin to low to disable shipment mode function.

To exit from shipment, VBUS voltage goes higher than UVLO or drive \overline{MR} low for t_{sh} . After exit from shipment, set register 0x36 bit 0 or drive MR low for 12s if this function was enable by set register 0x2D bit 1 to enter shipment mode again. Be noted that all register value will be refresh to default value when enter shipment mode.

FAULT RECOVERY

Before performing the following operation, it is important to ensure that the cause of the fault has been rectified.

To recover from a fault status, power off VBUS or write the corresponding I2C register bit high.

THERMAL MANAGEMENT

Thermal Warning and Thermal Shutdown

The ADP5360 features a thermal warning and shutdown threshold detector. If the die temperature exceeds T_{wn} , the temperature warning register TSD90 bit will set high and a temperature warning interrupt asserts if its corresponding nINT is enable. If the die temperature exceeds T_{sd} , the ADP5360 all function are disabled, and the TSD110 bit is set. The ADP5360 charger can be re-enabled when the die temperature drops below the T_{sd} falling limit and the TSD110 bit is reset. To reset the TSD110 bit, write to the I²C Fault Register 0x0D or cycle the power.

I²C INTERFACE

The ADP5360 includes an I²C-compatible serial interface to control the battery charging, fuel gauge, boost and LED driver and also to readback the system status.

I²C ADDRESSES

The I²C chip default address 7-bit is 0x46. Different I²C address can be factory programmable. Different I²C address option helps to avoid I²C address conflict to other I²C slave chipset in system. For different I²C chip address requirement, please contact your local Analog Devices sales or distribution representative.

SDA AND SCL PINS

The ADP5360 has two dedicated I²C interface pins, SDA and SCL. SDA is an open-drain line for receiving and transmitting data. SCL is an input line for receiving the clock signal. Pull up these pins to external I/O supply using external resistors.

Serial data is transferred on the rising edge of SCL. The read data is generated at the SDA pin in read mode.

The subaddress content selects which of the ADP5360 registers is written to first. The ADP5360 sends an acknowledgement to the master after the 8-bit data byte has been written (see Figure 51 for an example of the I²C write sequence to a single register). The ADP5360 increments the subaddress automatically and starts receiving a data byte at the next register until the master sends an I²C stop as shown in Figure 51.

Figure 51 shows the I²C read sequence of a single register. ADP5360 sends the data from the register denoted by the

subaddress and increments the subaddress automatically, sending data from the next register until the master sends an I²C stop condition as shown in Figure 51.

DEFAULT RESET

ADP5360 contains one write-only register DEFAULT_SET to reset all registers to the factory default values.

INTERRUPTS

ADP5360 provides an interrupt output (nINT pin) for fault conditions. During normal operation, the nINT pin is pulled high (an external pull-up resistor should be used). When a fault condition occurs, the ADP5360 pulls the nINT pin low to alert the I²C host that a fault condition has occurred.

Many different interrupt sources can trigger the nINT pin. By default, no interrupt sources are configured. To select one or more interrupt sources to trigger the nINT pin, set the appropriate bits to 1 in Register Charger Interrupt_Enable and Buck Interrupt_Enable.

When the nINT pin is triggered, one or more bits in Register Charger Interrupt_Flag and Buck Interrupt_Flag are set to 1. The fault condition that triggered the nINT pin can be read from Register Charger Interrupt_Flag and Buck Interrupt_Flag.

To clear an interrupt, write a 1 to the appropriate bit in Register Charger Interrupt_Flag and Buck Interrupt_Flag, or ADP5360 power recycle. Reading the interrupt or writing a 0 to the bit does not clear the interrupt.

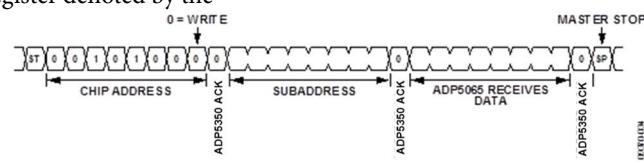


Figure 51. I²C Single Register Write Sequence

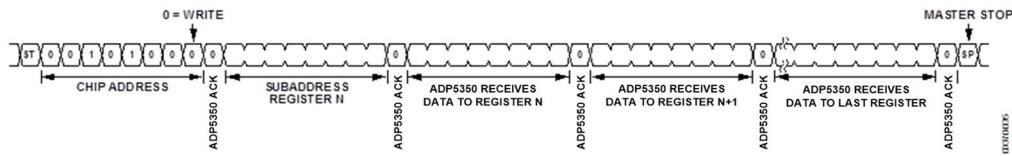


Figure 52. I²C Multiple Register Write Sequence

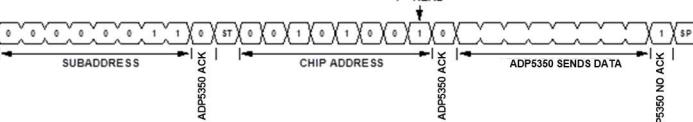


Figure 53. I²C Single Register Read Sequence

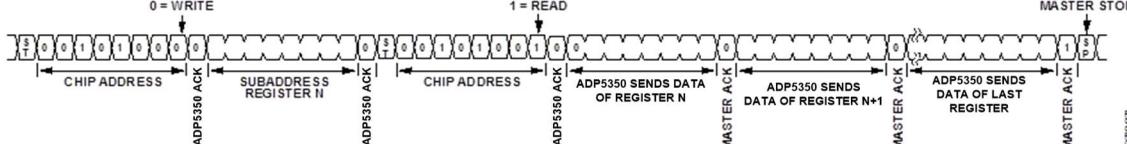


Figure 54. I²C Multiple Register Read Sequence

CONTROL REGISTER MAP

Table 16. Register Map

Table 17. Manufacturer and Model ID, Register Address 0x00 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:4]	MANUF[3:0]	R	0001	The 4-bit manufacturer identification bus.
[3:0]	MODEL[3:0]	R	0000	The 4-bit model identification bus.

Table 18. Silicon Revision, Register Address 0x01 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:4]	Not Used	R		
[3:0]	REV[3:0]	R	0000	The 4-bit silicon revision identification bus.

Table 19. Charger_VBUS_ILIM, Register Address 0x02 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:5]	VADPICHG	R/W	100 = 4.6 V	Adaptive current limit to VBUS voltage threshold programming. 010 = 4.4 V 011 = 4.5 V 100 = 4.6 V 101 = 4.7 V 110 = 4.8 V 111 = 4.9 V
4	Not used	R		
3	VSYSTEM	R/W	0 = $V_{TRM} + 100mV$	VSYS voltage programming. 0 = $V_{TRM} + 100mV$ 1 = 5 V
[2:0]	ILIM[2:0]	R/W	001 = 100 mA	VBUSx pin input current-limit programming bus. The current into VBUSx can be limited to the following programmed values: 000 = 50 mA. 001 = 100 mA. 010 = 150 mA. 011 = 200 mA. 100 = 250 mA. 101 = 300 mA. 110 = 400 mA. 111 = 500 mA.

Table 20. Charger_Termination_Settings, Register Address 0x03 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:2]	VTRM[5:0]	R/W	100011 = 4.20 V	<p>Termination voltage programming bus. The values of the float voltage can be programmed as per the following values:</p> <p>000000 = 3.50 V. 000001 = 3.52 V. 000010 = 3.54 V. 000011 = 3.56 V. 000100 = 3.58 V. 000101 = 3.60 V. 000110 = 3.62 V. 000111 = 3.64 V. 001000 = 3.66 V. 001001 = 3.68 V. 001010 = 3.70 V. 001011 = 3.72 V. 001100 = 3.74 V. 001101 = 3.76 V. 001110 = 3.78 V. 001111 = 3.80 V. 010000 = 3.82 V. 010001 = 3.84 V. 010010 = 3.86 V. 010011 = 3.88 V. 010100 = 3.90 V. 010101 = 3.92 V. 010110 = 3.94 V. 010111 = 3.96 V. 011000 = 3.98 V. 011001 = 4.00 V. 011010 = 4.02 V. 011011 = 4.04 V. 011100 = 4.06 V. 011101 = 4.08 V. 011110 = 4.10 V. 011111 = 4.12 V. 100000 = 4.14 V. 100001 = 4.16 V. 100010 = 4.18 V. 100011 = 4.20 V. 100100 = 4.22 V. 100101 = 4.24 V. 100110 = 4.26 V. 100111 = 4.28 V. 101000 = 4.30 V. 101001 = 4.32 V. 101010 = 4.34 V. 101011 = 4.36 V. 101100 = 4.38 V. 101101 = 4.40 V. 101110 = 4.42 V. 101111 = 4.44 V. 110000 = 4.46 V. 110001 = 4.48 V. 110010 = 4.50 V.</p>

Bit No.	Mnemonic	Access	Default	Description
				110011 = 4.52V. 110100 = 4.54V. 110101 = 4.56V. 110110 = 4.58V. 110111 to 111111 = 4.6 V.
[1:0]	ITRK_DEAD[1:0]	R/W	10 = 5 mA	Trickle and weak charge current programming bus. The values of the trickle and weak charge currents can be programmed as per the following values: 00 = 1mA. 01 = 2.5mA. 10 = 5 mA. 11 = 10 mA.

Table 21. Charger_Current_Setting, Register Address 0x04 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:5]	IEND[2:0]	R/W	001 = 2.5 mA	Termination current programming bus. The values of the termination current can be programmed as per the following values: 001 = 2.5 mA 010 = 5 mA 011 = 10 mA 100 = 15 mA 101 = 20 mA 110 = 25 mA 111 = 30 mA
[4:0]	ICHG[4:0]	R/W	01001 = 100mA	Fast charge current programming bus. The values of the constant current charge can be programmed as per the following values: 00000 = 10 mA. 00001 = 20 mA. 00010 = 30 mA. 00011 = 40 mA. 00100 = 50 mA. 00101 = 60 mA. 00110 = 70 mA. 00111 = 80 mA. 01000 = 90 mA. 01001 = 100 mA. 01010 = 110 mA. 01011 = 120 mA. 01100 = 130 mA. 01101 = 140 mA. 01110 = 150 mA. 01111 = 160 mA. 10000 = 170 mA. 10001 = 180 mA. 10010 = 190 mA. 10011 = 200 mA. 10100 = 210 mA. 10101 = 220 mA. 10110 = 230 mA. 10111 = 240 mA. 11000 = 250 mA. 11001 = 260 mA. 11010 = 270 mA. 11011 = 280 mA.

Bit No.	Mnemonic	Access	Default	Description
				11100 = 290 mA. 11101 = 300 mA. 11110 = 310 mA. 11111 = 320 mA.

Table 22. Charger_Voltage_Threshold, Register Address 0x05 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	DIS_RCH	R/W	0 = Enable recharge 1 = recharge disable.	0 = recharge enable. 1 = recharge disable.
[6:5]	VRCH[1:0]	R/W	01 = 100 mV	Recharge voltage programming bus. The values of the recharge threshold can be programmed as per the following values: 00 = 60 mV. 01 = 120 mV. 10 = 180 mV. 11 = 240 mV.
[4:3]	VTRK_DEAD[1:0]	R/W	01 = 2.5 V	Trickle to fast charge dead battery voltage programming bus. The values of the trickle to fast charge threshold can be programmed as per the following values: 00 = 2.0 V. 01 = 2.5 V. 10 = 2.6 V. 11 = 2.9 V.
[2:0]	VWEAK[2:0]	R/W	011 = 3.0 V	Weak battery voltage rising threshold. 000 = 2.7 V. 001 = 2.8 V. 010 = 2.9 V. 011 = 3.0 V. 100 = 3.1 V. 101 = 3.2 V. 110 = 3.3 V. 111 = 3.4 V.

Table 23. Charger_Timer_Setting, Register Address 0x06 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:4]	Not used	R		
3	EN_TEND	R/W	0	When low, this bit disables the charge complete timer (t_{END}), and a 4 ms deglitch timer remains on this function.
2	EN_CHG_TIMER	R/W	1	When high, the trickle/fast charge timer is enabled. When low, the trickle/fast charge timer is disabled.
[1:0]	CHG_TMR_PERIOD	R/W	11	Trickle/fast charge timer period. 00 = 15 minutes/150 minutes. 01 = 30 minutes/300 minutes. 10 = 45 minutes/450 minutes. 11 = 60 minutes/600 minutes.

Table 24. Charger_Functional Setting, Register Address 0x07 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	EN_JEITA	R/W	0	When low, this bit disables the JEITA Li-Ion temperature battery charging specification.
6	ILIM_JEITA_COOL	R/W	0	Select battery charging current when in temperature cool. 0: Approximately 50% of programmed charge current. 1: Approximately 10% of programmed charge current.
5	Not used(EN_TRK)	R/W		
4	OFF_ISOFET	R/W	0	When high, the ISOFET is forced turn off and VSYS shut down even when only battery present.

Bit No.	Mnemonic	Access	Default	Description
3	EN_LDO	R/W	1	When low the charge LDO is disabled. When high the charge LDO is enabled.
2	EN_EOC	R/W	1	When high, end of charge is allowed.
1	EN_ADPICHG	R/W	0	When high, VBUS adaptive current limit function is enabled during charge. When low, VBUS adaptive current limit function is disabled during charge.
0	EN_CHG	R/W	0	When low, the charging is disabled. When high and EN_LDO = high, the charging is enabled.

Table 25. Charger_Status1, Register Address 0x08 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	VBUS_OV	R	Not applicable	When high, this bit indicate that the VBUS voltage over than threshold.
6	ADPICHG	R	Not applicable	When high, this bit indicates that the adaptive input current limit active and VBUS voltage regulator to V_ADPICHG.
5	VBUS_ILIM	R	Not applicable	When high, this bit indicates that the current into a VBUSx pin is limited by the high voltage blocking FET and the charger is not running at the full programmed I_{CHG} .
[4:3]	Not used.	R		
[2:0]	CHAGER_STATUS[2:0]	R	Not applicable	Charger status bus. 000 = off. 001 = trickle charge. 010 = fast charge (CC mode). 011 = fast charge (CV mode). 100 = charge complete. 101 = LDO mode. 110 = trickle or fast charge timer expired. 111 = battery detection.

Table 26. Charger_Status2 , Register Address 0x09 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:5]	THR_STATUS[2:0]	R	Not applicable	THR pin status. 000 = off. 001 = battery cold. 010 = battery cool. 011 = battery warm. 100 = battery hot. 111 = thermistor OK.
4	BAT_OV_STAT	R	Not applicable	Battery over voltage status 0 = Battery not over voltage protection 1 = Battery over voltage protection
3	BAT_UV_STAT	R	Not applicable	Battery under voltage status 0 = Battery not under voltage protection 1 = battery under voltage protection
[2:0]	BAT_CHG_STATUS2:0]	R	Not applicable	Battery status bus. 000 = Normal. 001 = no battery. 010 = $BAT_{SNS} < V_{TRK}$ when in charge. 011 = $V_{TRK} \leq BAT_{SNS} < V_{WEAK}$ when in charge. 100 = $BAT_{SNS} \geq V_{WEAK}$ when in charge. 101 = $BAT_{SNS} > V_{OVCHG}$ when in charge.

Table 27. Battery_Thermistor_Control, Register Address 0x0A Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:6]	ITHR	R/W	00 = ITHR is 60uA	Select battery thermistor NTC resistance. 00 = ITHR is 60uA 01 = ITHR is 12 uA 10,11 = ITHR is 6uA
[5:1]	Not used	R		
0	EN_THR	R/W	0	When high, the THR current source is enabled even when the voltage at the VBUS pins is below V_{VBU5_OK} .

Table 28. Thermistor_60C Threshold, Register Address 0x0B Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	Temp_High_60	R/W	0x56	Thermistor voltage threshold for 60°C. Thermistor_60 voltage threshold [V] = (Temp_High_60 × 0.002) [V]

Table 29. Thermistor_45C Threshold, Register Address 0x0C Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	Temp_High_45	R/W	0x8F	Thermistor voltage threshold for 45°C. Thermistor_45 voltage threshold [V] = (Temp_High_45 × 0.002) [V]

Table 30. Thermistor_10C Threshold, Register Address 0x0D Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	Temp_Low_10	R/W	0x71	Thermistor voltage threshold for 10°C. Thermistor_10 voltage threshold [V] = (Temp_Low_10 × 0.01) [V]

Table 31. Thermistor_0C Threshold, Register Address 0x0E Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	Temp_Low_0	R/W	0xB4	Thermistor voltage threshold for 0°C. Thermistor_0 voltage threshold [V] = (Temp_Low_0 × 0.01) [V]

Table 32. THR_Voltage Low, Register Address 0x0F Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	THR_V_Low [7:0]	R	Not applicable	Thermistor node voltage low 8 bit, unit is mV. NTC = THR_V[11:0]/ITHR [kΩ]

Table 33. THR_Voltage High, Register Address 0x10 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:4]	Not used	R		
[3:0]	THR_V_High[11:8]	R	Not applicable	Thermistor node voltage high 4 bit, unit is mV NTC = THR_V[11:0]/ITHR [kΩ]

Table 34. Battery Protection Control Register, Register Address 0x11 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:5]	Not used	R		
4	ISOFET_OVCHG	R/W	0	When low, ISOFET turn on when battery charge over voltage protection. When high, ISOFET turn off when battery charge over voltage protection.

Bit No.	Mnemonic	Access	Default	Description
3	OC_DIS_HICCUP	R/W	0	Battery discharge over current protection . 0 = Latch up 1 = Hiccup
2	OC_CHG_HICCUP	R/W	0	Battery over charge current protection . 0 = Latch up 1 = Hiccup
1	EN_CHGLB	R/W	1	When low, the battery charge is not allowed when battery UV protection. When high, the battery charge is allowed when battery UV protection.
0	EN_BATPRO	R/W	Factory set	When low, the battery protection function is disabled. When high, the battery protection function is enabled.

Table 35. Battery Discharge Under Voltage Setting Register, Address 0x12 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:4]	UV_DISCH	R/W	1001 = 2.50 V	Battery undervoltage protection threshold. 0000 = 2.05 V 0001 = 2.10 V 0010 = 2.15 V 0011 = 2.20 V 0100 = 2.25 V 0101 = 2.30 V 0110 = 2.35 V 0111 = 2.40 V 1000 = 2.45 V 1001 = 2.50 V 1010 = 2.55 V 1011 = 2.60 V 1100 = 2.65 V 1101 = 2.70 V 1110 = 2.75 V 1111 = 2.80 V
[3:2]	HYS_UV_DISCH	R/W	00	Battery undervoltage protection for over discharge hysteresis. 00 = 2% UV_DISCH voltage threshold. 01 = 4% UV_DISCH voltage threshold. 10 = 6% UV_DISCH voltage threshold. 11 = 8% UV_DISCH voltage threshold.
[1:0]	DGT_UV_DISCH	R/W	00 = 30 mS	Battery undervoltage protection deglitch time. 00 = 30 mS. 01 = 60 mS. 10 = 120 mS. 11 = 240 mS.

Table 36. Battery Discharge Over Current Setting Register, Address 0x13 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:5]	OC_DISCH	R/W	111 = 600 mA	Battery over current protection for over discharger threshold. 000 = 50 mA 001 = 100 mA 010 = 150 mA 011 = 200 mA 100 = 300 mA 101 = 400 mA 110 = 500 mA

Bit No.	Mnemonic	Access	Default	Description
				111 = 600 mA
4	Not use	R		
[3:1]	DGT_OC_DISCH	R/W	001 = 0.5 mS	Battery discharge over current protection deglitch time setting. 001 = 0.5 mS. 010 = 1 mS. 011 = 5 mS. 100 = 10 mS. 101 = 20 mS. 110 = 50 mS 111 = 100 mS.
0	Not use	R		

Table 37. Battery Charge Over Voltage Setting Register, Address 0x14 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:3]	OV_CHG	R/W	01111 = 4.30 V	Battery over voltage protection threshold. 00000 = 3.55 V 00001 = 3.60 V 00010 = 3.65 V 00011 = 3.70 V 00100 = 3.75 V 00101 = 3.80 V 00110 = 3.85 V 00111 = 3.90 V 01000 = 3.95 V 01001 = 4.00 V 01010 = 4.05 V 01011 = 4.10 V 01100 = 4.15 V 01101 = 4.20 V 01110 = 4.25 V 01111 = 4.30 V 10000 = 4.35 V 10001 = 4.40 V 10010 = 4.45 V 10011 = 4.50 V 10100 = 4.55 V 10101 = 4.60 V 10110 = 4.65 V 10111 = 4.70 V 11000 = 4.75 V 11001 – 11111 = 4.80 V
[2:1]	HYS_OV_CHG	R/W	00	Battery over voltage protection for charge hysteresis. 00 = 2% voltage OV_CHG threshold. 01 = 4% voltage OV_CHG threshold. 10 = 6% voltage OV_CHG threshold. 11 = 8% voltage OV_CHG threshold.
0	DGT_OV_CHG	R/W	0 = 0.5 s	Battery over voltage protection deglitch time. 0 = 0.5 s. 1 = 1 s.

Table 38. Battery Charge Over Current Setting Register, Address 0x15 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:5]	OC_CHG	R/W	011 = 150 mA	Battery over current protection for over discharger threshold.

Bit No.	Mnemonic	Access	Default	Description
				000 = 25 mA 001 = 50 mA 010 = 100 mA 011 = 150mA 100 = 200 mA 101 = 250 mA 110 = 300 mA 111 = 400 mA
[4:3]	DGT_OC_CHG	R/W	01 = 10mS	Battery charge over current protection deglitch time setting. 00 = 5 mS. 01 = 10 mS. 10 = 20 mS. 11 = 40 mS.
[2:0]	Not used	R		

FUEL GAUGE: REGISTER BIT DESCRIPTIONS

Table 39. V_SOC_0, Register Address 0x16 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_0	R/W	0x7D	The battery voltage when SoC is 0%. The default voltage is 3.5V. Battery voltage [V] = (2.5 + V_SOC_0 × 0.008) [V]

Table 40. V_SOC_5, Register Address 0x17 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_5	R/W	0x91	The battery voltage when SoC is 5%. The default voltage is 3.66V. Battery voltage [V] = (2.5 + V_SOC_5 × 0.008) [V]

Table 41. V_SOC_11, Register Address 0x18 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_11	R/W	0x94	The battery voltage when SoC is 11%. The default voltage is 3.684V. Battery voltage [V] = (2.5 + V_SOC_11 × 0.008) [V]

Table 42. V_SOC_19, Register Address 0x19 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_19	R/W	0x99	The battery voltage when SoC is 19%. The default voltage is 3.724V. Battery voltage [V] = (2.5 + V_SOC_19 × 0.008) [V]

Table 43. V_SOC_28, Register Address 0x1A Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_28	R/W	0x9E	The battery voltage when SoC is 28%. The default voltage is 3.764V. Battery voltage [V] = (2.5 + V_SOC_28 × 0.008) [V]

Table 44. V_SOC_41, Register Address 0x1B Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_41	R/W	0xA3	The battery voltage when SoC is 41%. The default voltage is 3.804V. Battery voltage [V] = $(2.5 + V_SOC_41 \times 0.008) [V]$

Table 45. V_SOC_55, Register Address 0x1C Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_55	R/W	0xAB	The battery voltage when SoC is 55%. The default voltage is 3.868V. Battery voltage [V] = $(2.5 + V_SOC_55 \times 0.008) [V]$

Table 46. V_SOC_69, Register Address 0x1D Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_69	R/W	0xB5	The battery voltage when SoC is 69%. The default voltage is 3.948V. Battery voltage [V] = $(2.5 + V_SOC_69 \times 0.008) [V]$

Table 47. V_SOC_84, Register Address 0x1E Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_84	R/W	0xC4	The battery voltage when SoC is 84%. The default voltage is 4.068V. Battery voltage [V] = $(2.5 + V_SOC_84 \times 0.008) [V]$

Table 48. V_SOC_100, Register Address 0x1F Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	V_SOC_100	R/W	0xD5	The battery voltage when SoC is 100%. The default voltage is 4.204V. Battery voltage [V] = $(2.5 + V_SOC_100 \times 0.008) [V]$

Table 49. BAT_CAP , Register Address 0x20 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	BAT_CAP	R/W	0x32	The battery capacity input. Battery capacity = [BAT_CAP × 2] mAh

Table 50. BAT_SOC, Register Address 0x21 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	Not used	R		Not used
[6:0]	BAT_SOC	R	Not applicable	Battery state of charge output. SoC = BAT_SOC %, only valued between 0 to 100%

Table 51. BAT_SOCACM_CTL, Register Address 0x22 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:6]	BATCAP_AGE	R/W	01 = 1.5%	Battery capacity reduce percentage once BAT_SOCACM overflow. 00 = 0.8 % 01 = 1.5 %

Bit No.	Mnemonic	Access	Default	Description
				10 = 3.1 % 11 = 6.3 %
[5:4]	BATCAP_TEMP	R/W	00 = 0.2%/ $^{\circ}$ C	Battery capacity compensation with temperature coefficient. 00 = 0.2%/ $^{\circ}$ C 01 = 0.4%/ $^{\circ}$ C 10 = 0.6%/ $^{\circ}$ C 11 = 0.8%/ $^{\circ}$ C
[3:2]	Not used			
1	EN_BATCAP_TEMP	R/W	0	Battery capacity temperature compensation function selection. 0 = Disable battery capacity temperature compensation. 1 = Enable battery capacity temperature compensation.
0	EN_BATCAP_AGE	R/W	0	Battery capacity aging compensation function selection. 0 = Disable battery capacity adjust automatically. 1 = Enable battery capacity adjust automatically.

Table 52. BAT_SOCACM_H, Register Address 0x23 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	BAT_SOCACM[11:4]	R	Not applicable	Accumulation of charge SOC high 8 bits Number of times for charging = BAT_SOCACM[11:0]/100

Table 53.. BAT_SOCACM_L, Register Address 0x24 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:4]	BAT_SOCACM[3:0]	R	Not applicable	Accumulation of charge SOC low 4 bits Number of times for charging = BAT_SOCACM[11:0]/100

Table 54. VBAT_READ_H, Register Address 0x25 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	VBAT_READ[12:5]	R	Not applicable	The battery voltage reading, highest 8 bits, unit is mV

Table 55. VBAT_READ_L, Register Address 0x26 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:3]	VBAT_READ[4:0]	R	Not applicable	The Battery voltage reading, lowest 5 bits, unit is mV
[2:0]	Not used	R		

Table 56. FUEL_GAUGE_MODE , Register Address 0x27 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:6]	SOC_LOW_TH	R/W	01 = 11%	Indication of low SoC threshold. 00 = 6% 01 = 11% 10 = 21% 11 = 31%
[5:4]	SLP_CURR	R/W	01 = 10mA	Fuel gauge sleep mode current threshold 00 = 5 mA 01 = 10mA 10 = 20 mA 11 = 40 mA

Bit No.	Mnemonic	Access	Default	Description
[3:2]	SLP_TIME	R/W	00 = 1 min	Fuel gauge sleep mode SOC update rate 00 = 1 min 01 = 4 min 10 = 8 min 11 = 16 min
1	FG_Mode	R/W	0	Fuel Gauge Operation Mode selection 1: Enable Sleep mode 0: Disable Sleep mode
0	EN_FG	R/W	0	Fuel Gauge function selection 0: Disable Fuel gauge 1: Enable Fuel gauge

Table 57. SOC_RESET , Register Address 0x28 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	SOC Reset	W	0	Write "1" then write "0" to reset the BAT_SOC, VBAT_ADC_H and VBAT_ADC_L register.
[6:0]	Not used	R		

SWITCHING REGULATOR: REGISTER BIT DESCRIPTIONS**Table 58.. Buck Configure Register, Address 0x29 Bit Descriptions**

Bit No.	Mnemonic	Access	Default	Description
[7:6]	BUCK_SS	R/W	00 = 1 mS	Buck regulator output soft start time 00 = 1 mS. 01 = 8 mS. 10 = 64 mS. 11 = 512 mS.
[5:4]	BUCK_IMIN	R/W	11 = 400mA	Buck regulator peak current limit 00 = 100mA. 01 = 200mA. 10 = 300mA. 11 = 400mA.
3	BUCK_MODE	R/W	0 = Hystersis Mode	Buck operate mode selection. 0 = Hystersis Mode 1 = Force PWM Mode
2	STP_BUCK	R/W	0 = Disable	Enable stop feature to buck regulator. 0 = Disable pulse stop feature 1 = Enable pulse stop feature
1	DISCHG_BUCK	R/W	0 = Disable	Configure the output discharge functionality for buck. 0 = Disable output discharge function. 1 = Enable output discharge function.
0	EN_BUCK	R/W	1 = Enable buck output	Buck ouptut control. 0 = Disable buck output. 1 = Enabel buck output.

Table 59. Buck Output Voltage Setting Register, Address 0x2A Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:6]	BUCK_DLY	R/W	00 = 0 uS	Buck switch delay time in hystersys. 00 = 0 uS 01 = 5 uS

Bit No.	Mnemonic	Access	Default	Description
				10 = 10 μ s 11 = 20 μ s
[5:0]	VOUT_BUCK	R/W	Factory set	Buck output voltage setting. 000000 = 0.6 V. 000001 = 0.65V. 111111 = 3.75 V

Table 60. Buck-boost Configure Register, Address 0x2B Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:6]	BUCKBST_SS	R/W	00 = 1 mS	Buck-boost regulator output soft start time 00 = 1 mS. 01 = 8 mS. 10 = 64 mS. 11 = 512 mS.
[5:3]	BUCKBST_IMIN	R/W	011 = 400mA	Buck-boost regulator peak current limit 000 = 100mA. 001 = 200mA. 010 = 300mA. 011 = 400mA. 100 = 500 mA. 101 = 600 mA. 110 = 700 mA. 111 = 800 mA.
2	STP_BUCKBST	R/W	0 = Disable	Enable stop feature to buck-boost regulator. 0 = Disable pulse stop feature 1 = Enable pulse stop feature
1	DISCHG_BUCKBST	R/W	0 = Disable	Configure the output discharge functionality for buck-boost. 0 = Disable output discharge function. 1 = Enable output discharge function.
0	EN_BUCKBST	R/W	0 = Disable buck-boost output	Buck-boost output control. 0 = Disable buck-boost output. 1 = Enable buck-boost output.

Table 61. Buck-Boost Output Voltage Setting Register, Address 0x2C Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:6]	BUCKBST_DYL	R/W	00 = 0uS	Buck boost switch delay time in hysteresis. 00 = 0 μ s 01 = 5 μ s 10 = 10 μ s 11 = 20 μ s
[5:0]	VOUT_BUCKBST	R/W	Factory set	Buck boost output voltage setting. 000000 = 1.8 V. 000001 = 1.9 V. 001011 = 2.9 V. 001100 = 2.95. 111111 = 5.5 V

SUPERVISORY: REGISTER BIT DESCRIPTIONS

Table 62. Supervisory Setting Register, Address 0x2D Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	VOUT1_RST	R/W	1	Buck output voltage monitor to RESET selection. 0 = disable buck voltage monitor to RESET 1 = Enable buck voltage monitor to RESET
6	VOUT2_RST	R/W	0	Buck-boost output voltage monitor to RESET selection. 0 = disable buck-boost voltage monitor to RESET 1 = Enable buck-boost voltage monitor to RESET
5	RESET_TIME	R/W	0 = 200 mS	RESET timeout period selection. 0 = 200 ms 1 = 1.6 sec
[4:3]	WD_TIME	R/W	00 = 12.5 s	Watchdog timeout period selection. 00 = 12.5 s 01 = 25.6 s 10 = 50 s 11 = 100 s
2	EN_WD	R/W	0 = Disable	When high, watchdog timer function is enable. When low, watchdog timer function is disable.
1	EN_MR_SD	R/W	0 = Disable	When high, enter to shipment mode after nMR press low for 12s. When low, disable nMR press enter shipment mode function.
0	RESET_WD	W	0	High resets the watchdog safety timer. Bit is reset automatically.

STATUS AND FAULT: REGISTER BIT DESCRIPTIONSTable 63. Faults Register Address 0x2E Bit Descriptions¹

Bit No.	Mnemonic	Access	Default	Description
7	BAT_UV ¹	R/W	0	When high, this bit indicate the battery under voltage during over discharge.
6	BAT_OC ¹	R/W	0	When high, this bit indicate the battery over current during over discharge.
5	BAT_CHGOC ¹	R/W	0	When high, this bit indicate the battery over current during over charge.
4	BAT_CHGOV ¹	R/W	0	When high, this bit indicate the battery over voltage during over charge.
3	Not used	R		
2	WD_TIMEOUT ¹	R/W	0	When high, watchdog timeout has occurred.
1	TSD90 ¹	R/W	0	When high, the over temperature warning fault has occurred.
0	TSD 110 ¹	R/W	0	When high, the temperature shut down fault has occurred.

To reset the fault bits in the fault register, cycle power on VBUSx or write high to the corresponding I²C bit.

Table 64. PGOOD_STATUS register, Register Address 0x2F Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:6]	Not used	R		
5	MR_PRESS	R	Not applicable	When high, this bit indicate nMR pin pull to low after t _{DG} .
4	CHG_CMPLT	R	Not applicable	This bit shows charge complete 0 = The charger is not in charge complete status; 1 = The charger is in charge complete status;
3	VBUSOK	R	Not applicable	This bit shows real-time status of VBUSx voltage. 0 = the voltage at the VBUSx is below V _{VBUS_OK} or above V _{VBUS_OV} ; 1 = the voltage at the VBUSx is above V _{VBUS_OK} and below V _{VBUS_OV} ;

Bit No.	Mnemonic	Access	Default	Description
2	BATOK	R	Not applicable	This bit shows real-time status of battery voltage. 0 = Battery voltage less than V_{WEAK} . 1 = Battery voltage more than V_{WEAK} ;
1	VOUT2OK	R	Not applicable	This bit shows real-time power good status for buck-boost regulator. Only effective in Buck-boost standalone fixed output mode: 0 = Buck-boost Regulator power-good status is low; 1 = Buck-boost Regulator power-good status is high;
0	VOUT1OK	R	Not applicable	This bit shows real-time power good status for buck. Not effective if Buck is configured as load-switch mode: 0 = Buck power-good status is low; 1 = Buck power-good status is high;

Table 65. PGOOD1_MASK register, Register Address 0x30 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	PG1_REV	R/W	Factory set	This bit configures PGOOD1 pin output active low output. 0 = Disable active low. 1 = Enable active low.
[6:5]	Not use			
4	CHGCMPLT_MASK1	R/W	0	This bit configures external PGOOD1 pin: 0 = Not output charger complete signal to external PGOOD1 pin; 1 = Output charger complete signal to external PGOOD1 pin;
3	VBUSOK_MASK1	R/W	Factory set	This bit configures external PGOOD1 pin: 0: Not output Vbus voltage status signal to external PGOOD1 pin; 1: Output Vbus voltage status signal to external PGOOD1 pin;
2	BATOK_MASK1	R/W	0	This bit configures external PGOOD1 pin: 0: Not output battery voltage okay signal to external PGOOD1 pin; 1: Output battery voltage okay signal to external PGOOD1 pin;
1	VOUT2OK_MASK1	R/W	0	This bit configures external PGOOD1 pin for buck-boost output. 0 = Not output Buck-boost PGOOD signal to external PGOOD1 pin; 1 = Output Buck-boost PGOOD signal to external PGOOD1 pin;
0	VOUT1OK_MASK1	R/W	Factory set	This bit configures external PGOOD1 pin. Not effective if buck is configured as load-switch mode: 0 = Not output Buck PGOOD signal to external PGOOD1 pin; 1 = Output Buck PGOOD signal to external PGOOD1 pin;

Table 66. PGOOD2_MASK register, Register Address 0x31 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	PG2_REV	R/W	0	This bit configures PGOOD2 pin output active low output. 0 = Disable active low. 1 = Enable active low.
[6:5]	Not use			
4	CHGCMPLT_MASK2	R/W	0	This bit configures external PGOOD2 pin: 0 = Not output charger complete signal to external PGOOD2 pin; 1 = Output charger complete signal to external PGOOD2 pin;
3	VBUSOK_MASK2	R/W	0	This bit configures external PGOOD2 pin: 0: Not output Vbus voltage status signal to external PGOOD2 pin; 1: Output Vbus voltage status signal to external PGOOD2 pin;
2	BATOK_MASK2	R/W	0	This bit configures external PGOOD2 pin: 0: Not output battery voltage okay signal to external PGOOD2 pin; 1: Output battery voltage okay signal to external PGOOD2 pin;
1	VOUT2OK_MASK2	R/W	0	This bit configures external PGOOD2 pin for buck-boost output.

Bit No.	Mnemonic	Access	Default	Description
				0 = Not output Buck-boost PGOOD signal to external PGOOD2 pin; 1 = Output Buck-boost PGOOD signal to external PGOOD2 pin;
0	VOUT1OK_MASK2	R/W	0	This bit configures external PGOOD2 pin. Not effective if buck is configured as load-switch mode: 0 = Not output Buck PGOOD signal to external PGOOD2 pin; 1 = Output Buck PGOOD signal to external PGOOD2 pin;

Table 67. Interrupt_Enable_1, Register Address 0x32 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	EN_SOCLOW_INT	R/W	0	When high, the battery low SoC interrupt is allow.
6	EN_SOCACM_INT	R/W	0	When high, the SoC accumulation interrupt is allow.
5	EN_ADPICHG_INT	R/W	0	When high, the VBUS adaptive input current limit adaptive regulation interrupt is allow.
4	EN_BATPRO_INT	R/W	0	When high, the battery protection interrupt is allow.
3	EN_THR_INT	R/W	0	When high, the THR temperature thresholds interrupt is allow.
2	EN_BAT_INT	R/W	0	When high, the battery voltage thresholds interrupt is allow.
1	EN_CHG_INT	R/W	0	When high, the charger mode change interrupt is allow.
0	EN_VBUS_INT	R/W	0	When high, the VBUS pin voltage thresholds interrupt is allow.

Table 68. Interrupt_Enable_2, Register Address 0x33 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	EN_MR_INT	R/W	0	When high, the MR press interrupt is allow.
6	EN_WD_INT	R/W	0	When high, the watchdog alarm interrupt is allow.
5	EN_BUCKPG_INT	R/W	0	When high, the VOUT1OK change interrupt is allow.
4	EN_BCKBSTPG_INT	R/W	0	When high, the VOUT2OK change interrupt is allow.
3	EN_THRWRN_INT	R/W	0	When high, the thermal warning interrupt is allow.
[2:0]	Not used	R/W		

Table 69. Interrupt_Flag_1, Register Address 0x34 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	SOCLOW_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by low battery voltage.
6	SOCACM_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by SOC accumulation to 4096 and over flow.
5	ADPICHG_INT	R	Not applicable	When high, this bit indicates an interrupt caused by VBUS input current limit adaptive regulation.
4	BATPRO_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by battery protection trig with battery fault events.
3	THR_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by THR temperature thresholds.
2	BAT_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by battery voltage thresholds.
1	CHG_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by a charger mode change.
0	VBUS_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by VBUS voltage thresholds.

Table 70. Interrupt_Flag_2, Register Address 0x35 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
7	MR_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by MR press.

Bit No.	Mnemonic	Access	Default	Description
6	WD_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by the watchdog alarm. The watchdog timer expires within 2 sec or 4 sec depending on the WDPERIOD setting of 32 sec or 64 sec, respectively.
5	BUCKPG_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by VOUT1OK trig.
4	BUCKBSTPG_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by VOUT2OK trig.
3	THRWRN_INT ²	R	Not applicable	When high, this bit indicates an interrupt caused by thermal warning occur.
[2:0]	Not used	R		

² When read the register, interrupt bit will reset automatically.

Table 71. SHIPMODE register, Register Address 0x36 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:1]	Not use	R		
0	EN_SHIPMODE	R/W	0	When high, ADP5360 enter to shipment mode. When low, ship mode is disable.

Table 72. DEFAULT_SET register, Register Address 0x37 Bit Descriptions

Bit No.	Mnemonic	Access	Default	Description
[7:0]	DEFAULT_SET	W	0	Write “0x7F” to this bit will reset all register to default values.

Read and reset

APPLICATIONS INFORMATION

EXTERNAL COMPONENTS

VBUS Capacitor Selection

According to the USB 2.0 specification, USB peripherals have a detectable change in capacitance on VBUS when VBUS are attached. The peripheral device VBUS bypass capacitance must be at least 1 μF but not larger than 10 μF . The combined capacitance for the VBUS and CFL pins must not exceed 10 μF at any temperature or dc bias condition. Suggested VBUS capacitors are shown in Table 73.

Table 73. Suggested VBUS Capacitors

Vendor	Part Number	Value (μF)	Voltage (V)	Size
Murata	GRM188R61E225K	2.2	25	0603
TDK	C1608X5R1E225	2.2	25	0603

CFL Capacitor Selection

The internal supply voltage of the ADP5360 is equipped with a noise suppressing capacitor at the CFL terminal. Use typical CFL capacitance 1uF but not exceed 2.2uF during operation. Do not connect any external voltage source, any resistive load, or any other current load to the CFL terminal. Suggested CFL capacitor are show in Table 74.

Table 74. Suggested CFL, VIN1 and VIN2 Capacitors

Vendor	Part Number	Value (μF)	Voltage (V)	Size
Murata	GRM155R60J105KE19D	1	6.3	0402
TDK	CGB2A3X5R0J105M033BB	1	6.3	0402

VSYS Capacitor Selection

To guarantee the performance of the charger in various operation modes, including trickle charge, CC charge, and CV charge, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application. The total VSYS capacitance consists of a number of capacitors when the VSYS node tied together with input node of Buck and Buck boost regulator.

The VSYS capacitance should be not less than 10 μF . Suggested VSYS capacity are show in Table 75.

Table 75. Suggested VSYS, ISOB, Vout1 and Vout2 Capacitors

Vendor	Part Number	Value (μF)	Voltage (V)	Size
Murata	GRM188R60J106K	10	6.3	0603
TDK	C1608X5R0J106M080AB	10	6.3	0603

ISOB Capacitor Selection

The ISOB effective capacitance must not be less than 4.7 μF at any point during operation. Typically, a nominal capacitance of 10 μF is required to fulfill the condition at all points of operation.

Suggestions for an ISOB capacitor are show in Table 75.

Buck Input Capacitor Selection

An input capacitor is required to reduce the input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the VIN1 pin. Use the following equation to determine the rms input current:

$$I_{RMS} \geq I_{LOAD(MAX)} \sqrt{\frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}}$$

For most applications, the VIN1 pin will tie together with VSYS pin and VSYS capacitance will be effective, so a 1 μF capacitor is sufficient for VIN1 pin. The input capacitor can be increased without any limit for better input voltage filtering. Suggested VIN1 capacitor are show in Table 74.

Buck Inductor Selection

The high switching frequency of the ADP5360 buck converter allows the selection of small chip inductors when the buck operate at FPWM mode.

The peak-to-peak inductor current ripple, $I_{RIPPLE1}$, is calculated using the following equation:

$$I_{RIPPLE1} = V_{OUT1} \times ((V_{IN1} - V_{OUT1}) / (V_{IN1} \times f_{SW} \times L_1))$$

where:

V_{OUT1} is the buck output voltage.

V_{IN1} is the buck input voltage at the VIN1 node.

f_{SW} is the buck switching frequency.

L_1 is the buck output inductor value.

The minimum dc current rating of the inductor must be greater than the inductor peak current, I_{PEAK1} which is calculated using the following equation:

$$I_{PEAK1} = I_{LOAD1(MAX)} + I_{RIPPLE1}/2$$

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger inductors have smaller DCR values, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material. Because the buck regulators are high switching frequency dc-to-dc converters, shielded ferrite core material is recommended for its low core losses and low electromagnetic interference (EMI).

Suggested buck inductors are shown in Table 76.

Table 76. Recommended Inductors

Vendor	Model	Inductance (μ H)	Dimensions (mm)	DCR (m Ω)	I _r (A)
TDK	MLP2016H4R7	4.7	2.0 × 1.6 × 0.85	160	1.1
Wurth	74479776247A	4.7	2.0 × 1.6 × 1.0	140	1.2

Buck Output Capacitor Selection

Output capacitance is required to minimize the output voltage overshoot and undershoot, also minimize the output ripple significantly both in hysteresis mode and FPWM mode. Capacitors with low equivalent series resistance (ESR) values produce the lowest output ripple in FPWM mode.

Suggested buck output capacitor are shown in **Error! Reference source not found.**

Buck Boost Input Capacitor Selection

An input capacitor is required to reduce the input voltage ripple, input ripple current, and source impedance. Place the input capacitor as close as possible to the VIN2 pin.

For most applications, the VIN2 pin will tie together with VSYS pin and VSYS capacitance will be effective, so a 1 μ F capacitor is sufficient for VIN2 pin. The input capacitor can be increased without any limit for better input voltage filtering. Suggested VIN2 capacitor are show in Table 74.

Buck Boost Inductor Selection

Inductor conduction losses are caused by the flow of current through the inductor, which has an associated internal dc resistance (DCR). Larger inductors have smaller DCR values, which may decrease inductor conduction losses. Inductor core losses are related to the magnetic permeability of the core material.

Suggested buck boost inductors are shown in Table 76.

Buck Boost Output Capacitor Selection

Output capacitance is required to minimize the output voltage overshoot and undershoot, also minimize the output ripple significantly in hysteresis mode.

Suggested buck boost output capacitor are shown in Table 75

PCB LAYOUT GUIDELINES

Poor layout can affect ADP5360 performance, causing EMI and electromagnetic compatibility (EMC) problems, ground bounce, and voltage losses. Poor layout can also affect regulation and stability. A good layout is implemented using the following guidelines:

Place the decoupling capacitor, inductor, input capacitor, and output capacitor close to the IC.

- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Use a dedicated trace to connect the BSNS pin to the battery pack output node for accurate sensing of the battery voltage.
- Use Size 0603 or Size 0402 resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

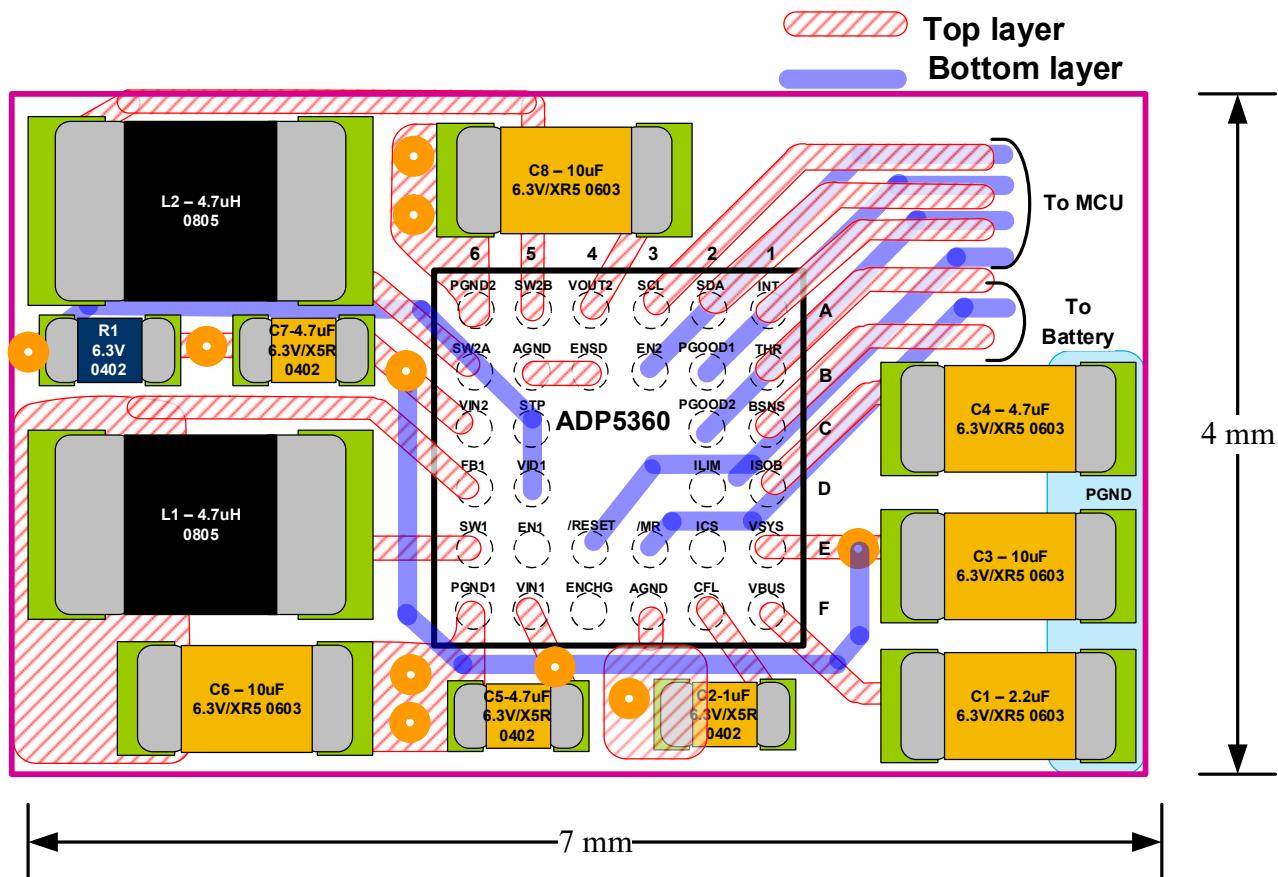


Figure 55. Recommend Layout

FACTORY-PROGRAMMABLE OPTIONS

Table 77. Fuse-Programmable Trim Options for the ADP5360

Parameter	Value	Default Setting
I ² C Address	0x46 0x56 0x66 0x76	0x46
EN_CHG	Charger is enabled Charger is disabled	Charger is disabled
ITHR	60 uA 12 uA 6 uA	60 uA
VTRM	3.90 V 4.00 V 4.10 V 4.20 V 4.26 V 4.30 V 4.36 V 4.40 V	4.20 V
EN_BATPRO	The battery protection function is disabled. The battery protection function is enabled.	The battery protection function is enabled.
UV_DISCH	2.2 V 2.5 V 2.6 V 2.8 V	2.5 V
OC_DISCH	100 mA 200 mA 400 mA 600 mA	600 mA
OV_CHG	4.25 V 4.30 V 4.40 V 4.50 V	4.30V
OC_CHG	100 mA 150 mA 200 mA 400 mA	150 mA
EN_BUCK	Disable buck output. Enabel buck output.	Enabel buck output.
BUCK_SS	1 mS. 8 mS. 64 mS. 512 mS.	1 mS
BUCK_MODE	Hystersis Mode Force PWM Mode	Hystersis Mode
DISCHG_BUCK	Disable output discharge function. Enable output discharge function.	Disable output discharge function.
VOUT_BUCK	1.0 V 1.2 V 1.5 V 1.8 V 2.5 V 2.8 V	1.2 V

	3.0 V 3.3 V	
EN_BUCKBST	Disable buck-boost output. Enabel buck-boost output.	Disable buck-boost output.
BUCKBST_SS	1 mS. 8 mS. 64 mS. 512 mS.	1 mS
DISCHG_BUCKBST	Disable output discharge function. Enable output discharge function.	Disable output discharge function.
VOUT_BUCKBST	2.5 V 3.3 V 3.6 V 4.0 V 4.2 V 4.6 V 5.0 V 5.5 V	5.0 V
PG1_REV	Disable PGOOD1 pin output active low. Enable PGOOD1 pin output active low.	Disable PGOOD1 pin output active low.
VBUSOK_MASK1	Do not output the V_{VBUS} voltage status signal to the external PGOOD1 pin Output the V_{VBUS} voltage status signal to external PGOOD1 pin	Do not output the V_{VBUS} voltage status signal to the external PGOOD1 pin
VOUT1OK_MASK1	Do not output Buck PGOOD signal to external PGOOD1 pin; Output Buck PGOOD signal to external PGOOD1 pin;	Do not output Buck PGOOD signal to external PGOOD1 pin;

PACKAGE OUTLINE DIMENSIONS

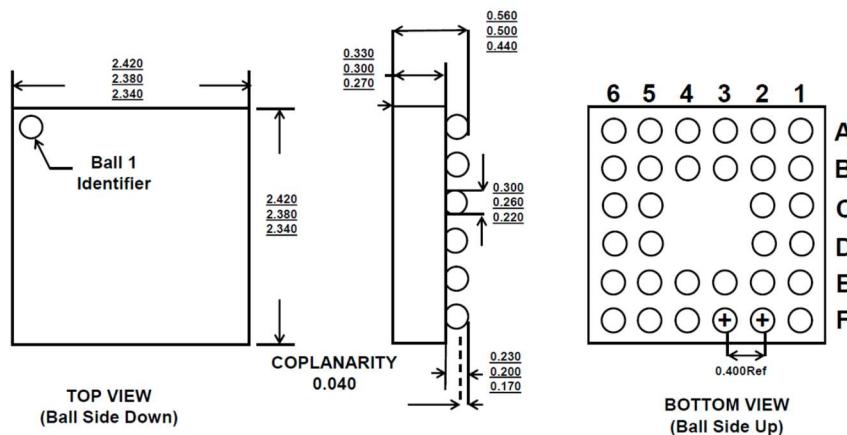


Figure 56. 32-Ball Wafer Level Chip Scale Package [WLCSP]
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADP5360ACBZ-1-R7	-40°C to +85°C	32-Ball Wafer Level Chip Scale Package [WLCSP]	TBD
ADP5360CB-EVALZ		Evaluation Board	

¹ Z = RoHS Compliant Part.