Updates from ADPD4000-4001 to ADPD4100-4101

ADPD4000-4001 and ADPD4100-4101 are pin-to-pin compatible. In addition to improved performance, new features, including subsampling and TIA ceiling detection, have been added to ADPD4100-4101. To accommodate the new features as well as other optimizations, there are changes to the register map.

We have two revisions of Watch available - one with ADPD4000(which we refer as DVT1) and other with ADPD4100(which we refer as DVT2).

Watch Revision	ADPD	Chip ID Reg: 0x0008
DVT1	ADPD4000	0x00C0
DVT2	ADPD4100	0x01C2

There is no difference in functionality between the two, only minor change in ADPD device.

This document lists the changes to register map and the TIA ceiling detection and subsampling features.

1. Integrator time offset

Related registers: 0x010B, 0x012B, 0x014B, 0x016B, 0x018B, 0x01AB, 0x01CB, 0x01EB, 0x020B, 0x022B, 0x024B, 0x026B

Description: this group of registers sets the integrator time offset for individual timeslots with 8 bits for coarse (1 µs) increments and 5 bits for fine (31.25ns) increments per LSB, providing the maximal integrator time offset 255.96875 µs.

Update: **the register bit assignment has been changed** - ADPD4000-4001, bits [12:8] for fine offset (0 – 968.75 ns) and bits [7:0] for coarse time offset (0 – 255 µs); ADPD4100-4101, bits [4:0] for fine offset (0 – 968.75 ns) and bits [12:5] for coarse time offset (0 – 255 µs). Bits [15:13] remain reserved. **MUST CHANGE FOR GOING FROM ADPD4000-4001 TO ADPD4100-4101.**
(Refer to ADPD4000-4001 DS, p.80 and ADPD4100-4101 DS, p.94)

2. TIA ceiling detection and CH2 setup

Related registers: 0x0104, 0x0124, 0x0144, 0x0164, 0x0184, 0x01A4, 0x01C4, 0x01E4, 0x0204, 0x0224, 0x0244, 0x0264

Description: ADPD4000-4001 and ADPD4100-4101 have two independent analog signal paths, CH1 and CH2. Each path consists of TIA (transimpedance amplifier), BPF (band-pass filter), and INT (integrator). The TIA gain and integrator resistor can be configured. The TIA ceiling detection has been added to ADPD4100-4101 for TIA saturation detection.

Update: Bits [15:13] are reserved with default 0x7 for ADPD4000-4001. Bits [15:13] are for TIA ceiling detection and CH2 setup in ADPD4100-4101. CH1 and CH2 have the same integrator resistor setting in ADPD4000-4001 while the integrator resistor can be independently set for CH1 and CH2 in ADPD4100-4101. **It is very important to check the setting of this register for simultaneous two-channel measurement**. Using the ADPD4000-4001 setting for ADPD4100-4101 enables the TIA ceiling detection and sets CH2 integrator resistor at 100 kΩ.
(Refer to ADPD4000-4001 DS, p.74 and ADPD4100-4101 DS, p.91)

3. Subsampling

Related registers: 0x0100, 0x0120, 0x0140, 0x0160, 0x0180, 0x01A0, 0x01C0, 0x01E0, 0x0200, 0x0220, 0x0240, 0x0260

Description: this group of registers sets the controls for individual timeslots. With the subsampling being added to ADPD4100-4101, bit [15] of this register enables subsampling when it is set.
Update: bit [15] is reserved for ADPD4000-4001, while **setting bit [15] enables subsampling in ADPD4100-4101**. (Refer to ADPD4000-4001 DS, p.72 and ADPD4100-4101 DS, p.89)

4. AFE Path Configuration

Related registers: 0x0101, 0x0121, 0x0141, 0x0161, 0x0181, 0x01A1, 0x01C1, 0x01E1, 0x0201, 0x0221, 0x0241, 0x0261
Description: this group of registers sets the controls for individual timeslots for preconditioning duration, AFE Path configuration, etc. With the AFE path configuration being
added to both ADPD4000-4001 and ADPD4100-4101, in bit [8:0] of this register.
For signal path selection:
Value: 0x1DA: TIA, BPF, integrator, and ADC in ADPD4000-4001
Value: 0x0DA: TIA, BPF, integrator, and ADC in ADPD4100-4101
 (Refer to ADPD4000-4001 DS, p.75 and ADPD4100-4101 DS, p.89)

5. FIFO Threshold

Related registers: 0x0006
Description: FIFO interrupt generation threshold. Generate FIFO interrupt during a FIFO write when the number of bytes in the FIFO exceeds this value.
The FIFO is 256 bytes. Therefore, the maximum value for FIFO_TH is 0xFF in ADPD4000-4001
The FIFO is 512 bytes. Therefore, the maximum value for FIFO_TH is 0x1FF in ADPD4100-4101
(Refer to ADPD4000-4001 DS, p.69 and ADPD4100-4101 DS, p.82)