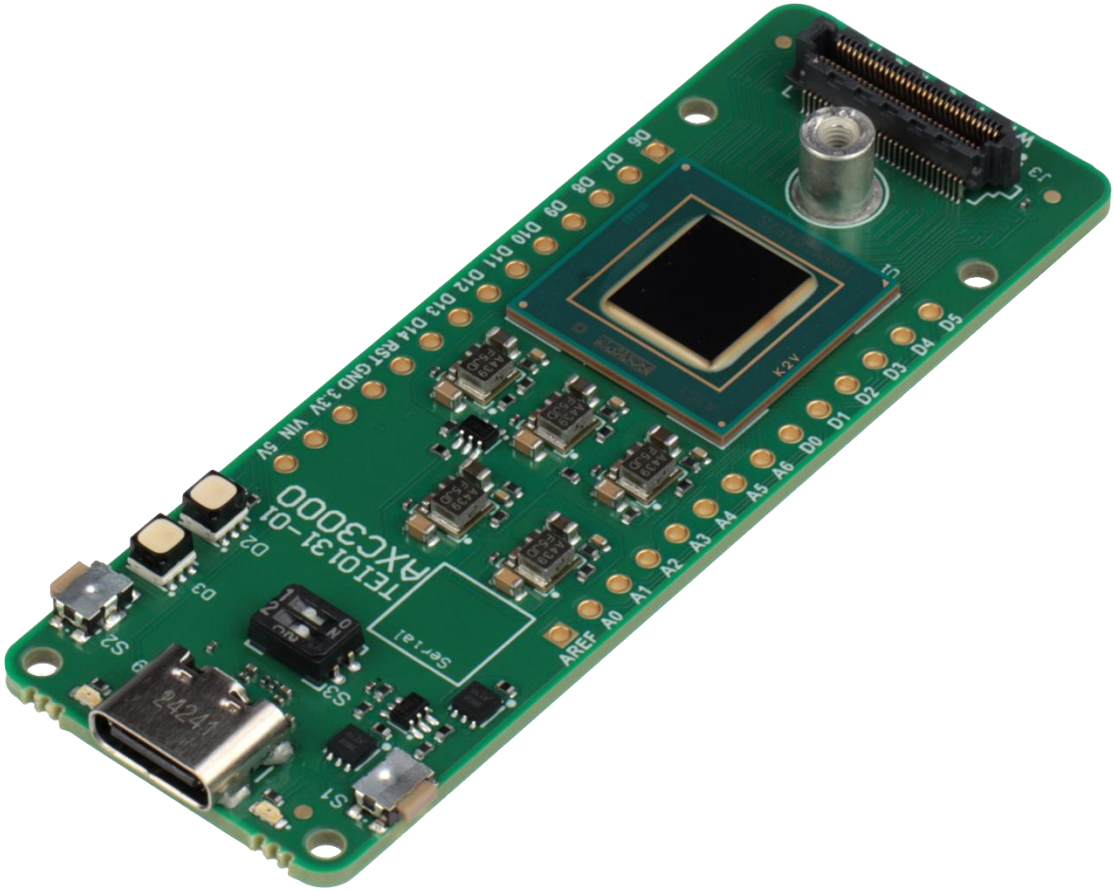
Power Thermal Calculator Workshop



Software and hardware requirements to complete all exercises.

Software Requirements: Altera Power Thermal Calculator v25.1.1

Hardware Requirements: Not needed

Document Control

Document Version:	Version 1.0
Document Date:	09/07/2025
Document Author(s):	Steven Kravatsky, Erika Peter, Naji Naufel, ESC Team.
Document Classification:	Released
Document Distribution:	This document is still under development. All specifications, procedures, and processes described in this document are subject to change without prior notice
Prior Version History:	Version: 0.1

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Table of Contents

1. Introduction

This workshop provides why and how (in a step-by-step approach) to

- use the stand-alone power thermal calculator (PTC) for an Agilex-3 device.

Knowing the FPGA power is crucial because it influences the board design such as the power rails, power envelope (i.e. is a heat sink/ fan needed) and more.

The stand-alone Power thermal calculator (PTC) is used for:

- power estimation before the design is started and/or if the design is in progress and to do the preliminary thermal analysis for the design.

Once a design is near completion, the PTC within Quartus can be used to provide more accurate power numbers. The PTC within Quartus would use the actual FPGA design information including routing and exact resource usage to have a more accurate power estimation.

2. Getting Started

The first objective is to ensure that you have all the necessary software installed so that the lab can be completed successfully. Below is a list of items required to complete this lab. A number of options are provided.

Option 1: Completing the lab using CloudLabs.

- Personal computer or laptop running 64-bit Linux / Windows 10 or later with at least an Intel i5 core (or equivalent), 8GB RAM.

Option 2: Completing the lab using a laptop

- Power Thermal Calculator (PTC) 25.1.1
- Personal computer or laptop running 64-bit Linux / Windows 10 or later with at least an Intel i5 core (or equivalent), 16/24 GB of free hard disk space and considerable memory.
- Hardware is not needed for this workshop

A desire to learn!

3. What is FPGA power and why is it important?

Power is the amount of energy needed to operate a device.

Power calculation is important for several reasons, including:

- power rails can be determined correctly (i.e. how to power up the device) which in turn affects the board layout,
- power for the FPGA (which is one device of a design) could be calculated.

Knowing the total power, helps ensure that the power envelope of the FPGA/ design is not exceeded. If more power is required than the FPGA can dissipate, heat sinks and/or air flow (i.e. fans) will be needed to dissipate increase the power flow from the device. When there is too much power and the FPGA is unable to dissipate the heat even with heat sinks or fans, this can lead to thermal runaway. This is when the heat keeps building up uncontrollably which causes the temperature to rise even more which in turn creates even more heat. The FPGA can overheat and stop working completely when this happens.

Total FPGA power consists of static (standby) power and dynamic power.

Static power is the amount of power that a device consumes with no resources is being used in the device. Static power depends on factors such as die size (i.e. a larger device in the same family results in more static power being consumed as compared to a smaller device from the same family), temperature, process variations, and process node technology.

Static power for each Altera device is known and this number is shown in the power and thermal calculator (PTC).

Dynamic Power includes routing and resource power. Resources that use dynamic power include memories, clocking, and other blocks. For example, when faster clock rates are used, more dynamic power is consumed, thus there is a trade of performance vs power. I/O power, which is part of the total dynamic power, is the power used by the capacitors connected to the I/Os. Using more I/Os results in more I/O power. I/O standards can also affect the power. For example, differential I/O standards use less power than non-differential I/O standards.

There are ways to reduce power which will be discussed in this workshop.

Agilex-3 devices, which are mid-range FPGAs, support many applications that need high performance yet lower power.

There are other items to consider for power such as inrush current and configuration power, which will not be covered in this lab.

4. What is Power Thermal Calculator (PTC) and why use it?

Power Thermal Calculator (PTC) provides the approximate FPGA power usage. It shows the power per resource used (i.e. logic, memory, DSP blocks, clocking), static power, I/O power and the total power used.

The accuracy of the PTC results vs silicon measurements depends on various details such as input parameters with toggle rates and temperature. Per the PTC User guide, when final power models are used, the accuracy of the PTC as compared to silicon is within 10% provided there are accurate inputs and toggle rates.

There are two versions of the PTC that can be used depending on the stage of the design.

The first PTC is the stand-alone version, which is used when the FPGA design is not started/only partially started, but the power numbers are needed ahead of time. An example would be where the board hardware design needs to be worked on in parallel with the FPGA design. The stand-alone PTC is the focus of this workshop.

The second version is the embedded one (within Quartus) which can be used when the design is complete/nearly complete. The embedded version will use results from actual design, and thus, it will produce more accurate results than the stand-alone version. The more complete the Quartus design is, the more accurate the PTC results will be as compared to silicon.

5. PTC

The following step by step describes how to use the Power Thermal Calculator (PTC) when the design is not started/very early. It also shows the differences in the power when resources are changed and even errors if the number of resources of the device are exceeded.

5.1.1 Opening the PTC

5.1.1.1 Select in the Windows Search menu → Quartus 25.1.1.125 Pro Edition → Power Thermal Calculator 25.1. 1

An important item to note is that different versions of Quartus and PTC can be installed on a computer, thus this workshop deals with PTC v25.1. 1

The PTC version should match the Quartus version to reduce possible issues.

Note: If you not see the PTC in the Windows search menu, go to the install path of Quartus 25.1.1, which by default is at C:\altera_pro\25.1.1\quartus\bin64 and select the quartus.ptc file directly.

Selecting the FPGA family

When the PTC opens, there are two Altera families (Agilex and Stratix 10) that can be selected. A snippet of the window is shown below:

As an aside, other Altera families i.e. Cyclone, etc use the Early Power Estimator (EPE). The EPE, unlike the PTC, is an Excel spreadsheet that has embedded macros. The embedded macros, depending on the security on the computer, may not run. However, the PTC does not have the embedded macros thus this issue will not be seen.

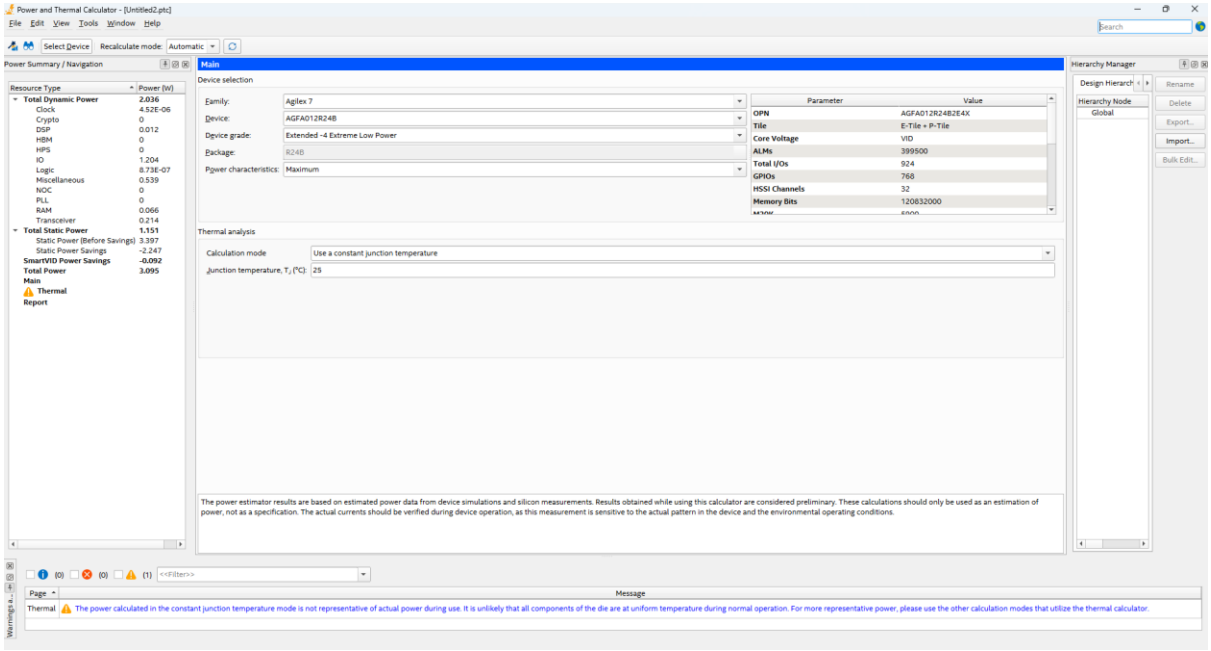
5.1.1.2 Select Agilex

As seen below.

Family	Status
Agilex	Available
Stratix 10	Available

5.1.1.3 Select OK

The Agilex family includes various sub-families as Agilex-7 and Agilex-3 families. The Agilex 3 family will be used in this case. The window will open with default settings as below. The default settings might be different on your computer, but they will be changed in the following sections to the correct Agilex 3 device.



5.1.2 Selecting the device in the PTC

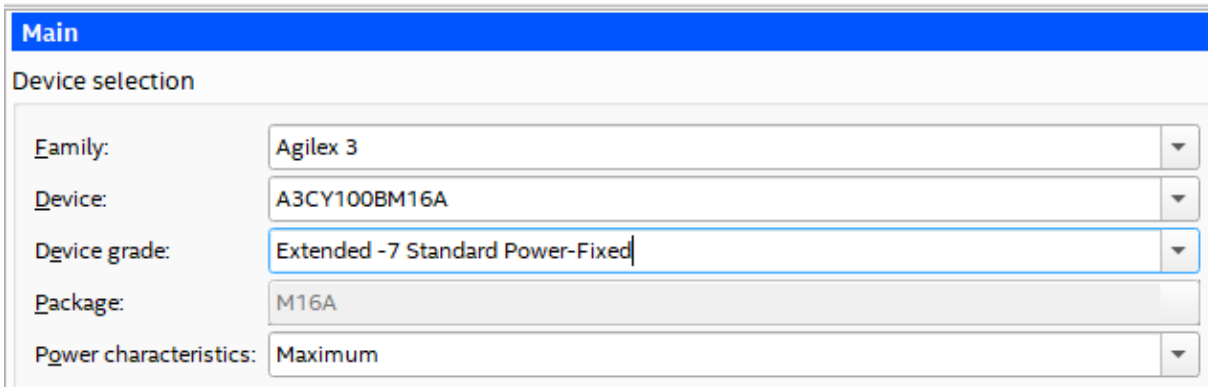
The next step is to change the device selection to the one we have on the AXC3000 board.

5.1.3.1. Change the settings for the family, device and power characteristics.

Change the device family to Agilex 3 and change the part number to A3CY100BM16A. There may be a delay when selecting the device family.

Change the Device grade to **Extended-7 Standard Power-Fixed.**

The part number will be entered using the pull-down menu. The power characteristics are set to Maximum, which is the worst-case condition for power.



The details of these settings are:

Family

This is the Altera family that is targeted. The PTC supports Stratix 10 and Agilex device families. The Agilex 3 family is part of the Agilex family.

Device

This is the specific device in question. The devices are listed in alphabetical order in the pull-down menu. The AXC3000 uses a **A3CY100BM16AE7S** Agilex 3 device.

The device selected affects the static power, because the larger the device, the larger the static power. The device selected will also affect the dynamic power. The larger the device, the more resources can be implemented and thus the power consumption can increase.

Device grade

Different variations for device grade include extended (0° to +100° C), industrial (-40° to +100° C) and power variations i.e. standard vs low power. The device grade for temperature and power depends on where the FPGA will be used i.e. will it be used in colder conditions. There is also the FPGA core speed of 6 (faster) and 7.

There are power vs frequency trade-offs.

Power Characteristics

It is recommended to use worst case (i.e. maximum), so the maximum (worst case) power can be designed for and reported. With the worst-case power numbers, the power rails and total power will be reported as the worst case results.

5.1.3 Thermal Analysis-Change

There is a warning on the bottom of this main page that states

Since the screenshot image is small, the text states

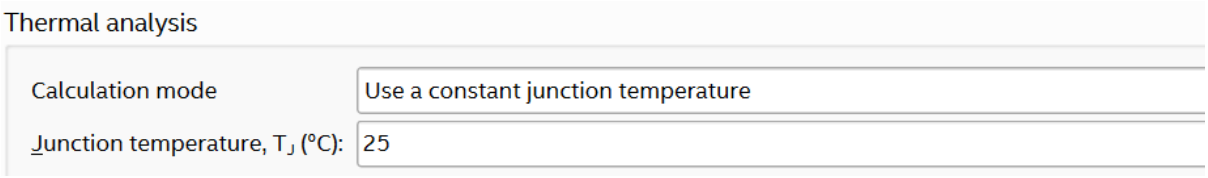
"*The power calculated in the constant junction temperature mode is not representative of actual power during use. It is unlikely that all components of the die are at uniform temperature during normal operation. For more representative power, please use the other calculation modes that utilize the thermal calculator.*"

Now, the reason for this warning is that although the Agilex-3 device has a monolithic die, the power in different portions of the die will be different. For example, there can be

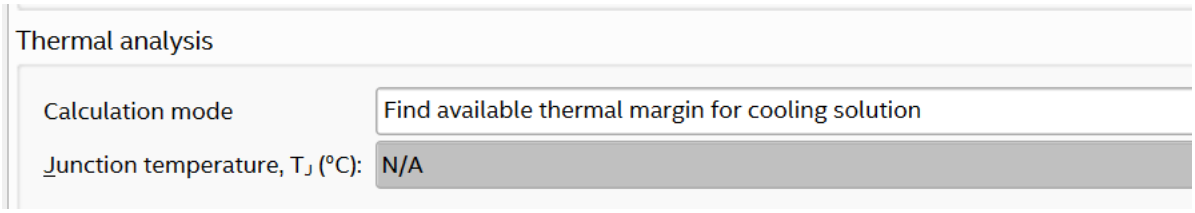
more resources in one section of the die or even different fmax for different portions of the die which make certain sections run faster and thus the power will be different.

5.1.3.1 Select and change the default Thermal Analysis setting to Find Available thermal margin for cooling solution

This change is as:



To



There are different 4 options for the calculation modes that can be selected. They are

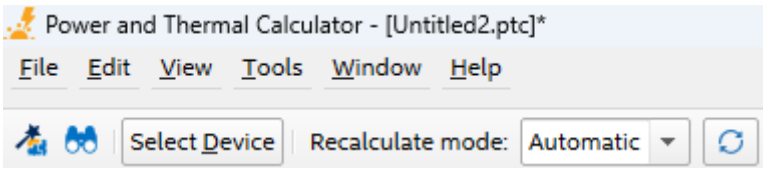
a) A constant junction temperature (default setting. There will be a warning in the PTC. This mode is not a representation of power used)
b) Find cooling solution for maximum junction temperature limit. This option will look if a heat sink/fan is needed.
c) Find an available thermal margin for cooling solution. Quartus will do the calculation for the thermal margin.
d) Find ambient temperature for specified cooling solution.

The static values will change depending on the power options.

5.1.4 Automatic Recalculate Mode.

5.1.4.1 Check that the Recalculate Mode is set to Automatic.

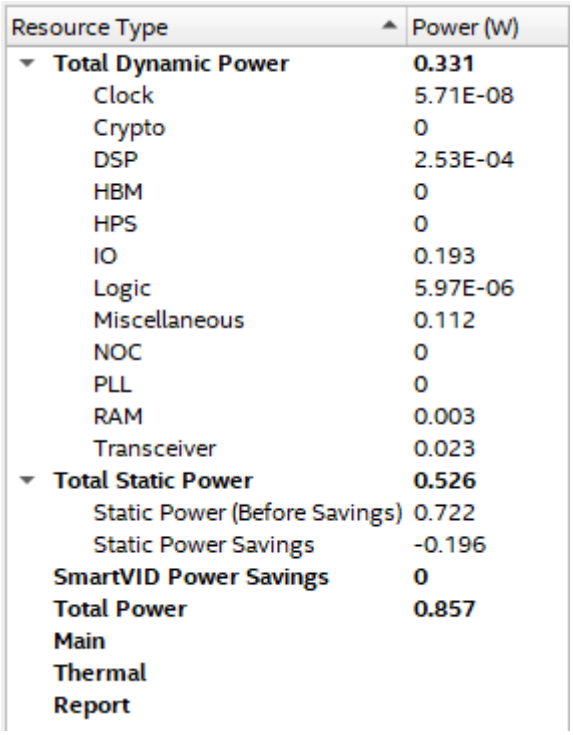
Automatic is the default setting for the PTC, but it is worthwhile to check.



If it is set to Manual, it is possible to forget to select it to recalculate. This will cause the power numbers to be incorrect. Automatic means as items changed in the PTC, the power numbers will automatically update.

5.2 Static Power with no FPGA resources entered.

Within the Power Summary/ Navigation Window of the PTC, it shows static and dynamic power values. The numbers will change in the next steps as resources are added.



Resource Type	Power (W)
Total Dynamic Power	**0.331**
Clock	5.71E-08
Crypto	0
DSP	2.53E-04
HBM	0
HPS	0
IO	0.193
Logic	5.97E-06
Miscellaneous	0.112
NOC	0
PLL	0
RAM	0.003
Transceiver	0.023
Total Static Power	**0.526**
Static Power (Before Savings)	0.722
Static Power Savings	-0.196
SmartVID Power Savings	**0**
Total Power	**0.857**
Main	
Thermal	
Report	

SmartVid means that these devices can operate at lower voltage, but they will have the same performance level, which in turn reduces the power consumption.

5.3 FPGA Resources

Within a FPGA design, many FPGA resources can be utilized. The FPGA resources include logic, memory, DSP blocks, clocks, PLLs, I/Os, transceivers, HPS, and Crypto. The number of resources depend on the application. This particular device does not have a HPS nor transceivers.

For this workshop, let's assume that the following resources are used so that the device is mostly full. Having a device over 75% full would be a reasonable FPGA utilization. The FPGA can be filled more, but the issue is that if any changes in the future are needed for the design, there could be no available resources to do so. These numbers are not from an actual design but rather it illustrates the steps needed in the PTC to see the results.

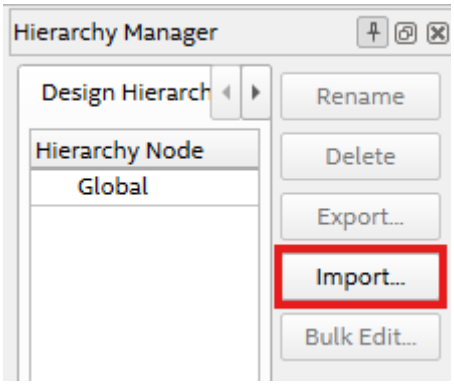
(Appendix A describes more details on how to determine resources if the design is not started.)

Logic at fmax	Memory	DSP	Clock	PLL	I/O
68,000 Half ALMS running at 400 MHz. The ALMs are about 91% of device, while the FF are about 67%	262 M20K running at 400 MHz (about 87%)	138 instances at 400 MHz (about 93% used)	400 MHz clocks	4 PLLs running at 600 MHz	Using about 41% of the I/Os

5.3.1 Entering resources in the PTC

To simplify the manual entry for this workshop for the various FPGA resources, a ptc (Power Thermal Calculator) file was created. Even if the details are entered manually, the PTC will save the output as a ptc file.

5.3.1.1 Select the Import Feature as seen below.



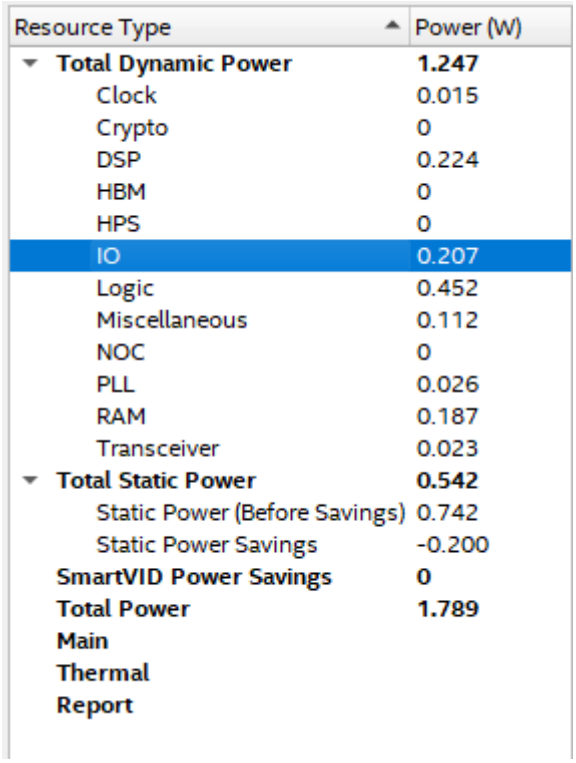
5.3.1.2 Select the workshop.ptc file.

From the workshop provided files, **select the workshop.ptc** file.

The provided .ptc file populates many fields of resources, which will be explained later, along with changes that will be made to experiment with the differences in power.

5.3.1.3 View the power numbers in the Power Summary/Navigation

Note the static power is increased (as there are more features), as well as the total power is increased. The results are expected. The dynamic power is a significant amount of the total power, which is expected because the resources and associated fmax that are used.



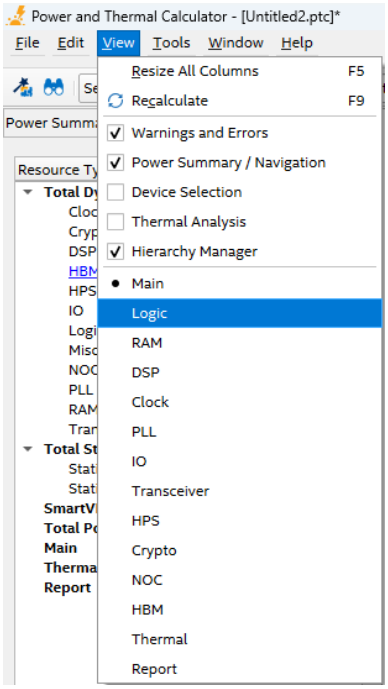
Resource Type	Power (W)
Total Dynamic Power	**1.247**
Clock	0.015
Crypto	0
DSP	0.224
HBM	0
HPS	0
IO	0.207
Logic	0.452
Miscellaneous	0.112
NOC	0
PLL	0.026
RAM	0.187
Transceiver	0.023
Total Static Power	**0.542**
Static Power (Before Savings)	0.742
Static Power Savings	-0.200
SmartVID Power Savings	**0**
Total Power	**1.789**
Main	
Thermal	
Report	

The following section will review the different resources and make changes to see the differences in the power.

5.3.2 Logic Resources

The logic resources can be reviewed first.

5.3.2.1 From the menu View at the top of the PTC Window, select Logic



After the logic option is selected, the view looks like the following.

	Entity Name	Full Hierarchy Name	# Half ALMs	# FFs	Clock Freq. (MHz)	Toggle %	Routing Factor	Power (W)			User Comment
								Routing	Block	Total	
1		|works...rkshop	58000	76000	400	12.5%	3	0.152	0.272	0.423	
2		|works...rkshop	3880	2000	400	12.5%	3	0.004	0.010	0.014	
3			0	0	0	12.5%	3	0	0	0	

Entity Name

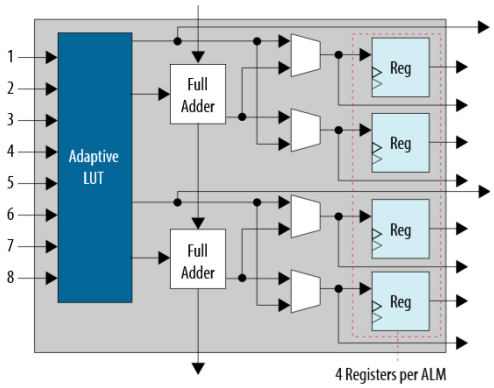
By entering entity names, this means that the power of the sub-blocks can be entered and reviewed. If the power is too high for a certain block, this module can be focused on.

Half ALM

Within Agilex, the basic building of logic is called ALM (adaptive logic module). ALMs have eight inputs, fracturable look up table (LUT), two dedicated adders and four registers. These modules can be configured to implement different logic functionalities such as logic and register.

A block diagram of the ALM is:

Figure 8. ALM Block Diagram



Half ALM means that it would use half of the ALM, as logic functionality does not need to completely fill the ALM. Two half ALMs can perform two separate functions, which doubles the efficiency. ALMs can support "certain combinations of completely independent functions and various combinations of functions that have common inputs."

FFs

FF stands for flip flops (registers). There are registers that are part of the ALM block.

Clock Frequency (MHz)

The faster the clock frequency the more power that will be used. Dynamic Power can be calculated as C(capacitive)*V (Voltage squared) *f (frequency).

Toggle %

Toggle is the "percentage of clock cycles when the block output signal change value. This value is multiplied by clock frequency to determine number of transitions per second.

100% means that with every clock cycle the signal changes value. 50% corresponds to a randomly changing signal, since half the time the signal will hold the same values and thus not transition. Most logic toggles infrequently and hence toggle below 50% are most realistic."

The toggle rate by default is set to 12.5%, which is left as default here.

The next step is to see what happens if the number of logic usage is exceeded i.e. to see if warnings/errors are seen.

5.3.2.2 Change the Half ALMs from 58,000 to 68,000

Change the number of Half ALMs 58,000

	Entity Name	Full Hierarchy Name	# Half ALMs	# FFs	Clock Freq. (MHz)	Toggle %	Routing Factor	Power (W)			User Comment
								Routing	Block	Total	
1		|works...rkshop	58000	76000	400	12.5%	3	0.152	0.272	0.423	
2		|works...rkshop	3880	2000	400	12.5%	3	0.004	0.010	0.014	
3			0	0	0	12.5%	3	0	0	0	

to 68,000

	Entity Name	Full Hierarchy Name	# Half ALMs	# FFs	Clock Freq. (MHz)	Toggle %	Routing Factor	Power (W)			User Comment
								Routing	Block	Total	
1		|works...rkshop	68000	76000	400	12.5%	3	0.153	0.284	0.436	
2		|works...rkshop	3880	2000	400	12.5%	3	0.004	0.010	0.014	
3			0	0	0	12.5%	3	0	0	0	

There will be an error at the bottom of the page that states:

Page	
Logic	Total number of ALMs is 35940, which exceeds the maximum allowed value of 34000.

The PTC knows the number of maximum resources for each device, and thus it can report if the number of resources is exceeded. Having the error checker is useful, because it will verify that not more resources are used than are available. It will also report the % of the device that is used.

5.3.2.3 Change the number of Half ALMs back to 58,000

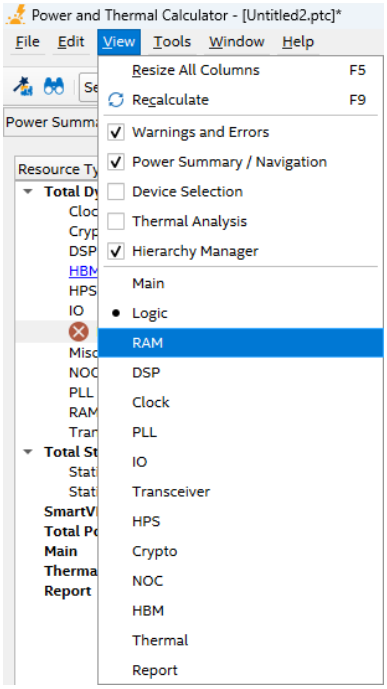
Remove the error by changing the half ALMs back to **58,000**

	Entity Name	Full Hierarchy Name	# Half ALMs	# FFs	Clock Freq. (MHz)	Toggle %	Routing Factor	Power (W)			User Comment
								Routing	Block	Total	
1		|works...rkshop	58000	76000	400	12.5%	3	0.152	0.272	0.423	
2		|works...rkshop	3880	2000	400	12.5%	3	0.004	0.010	0.014	
3			0	0	0	12.5%	3	0	0	0	

5.3.3 Memory

FPGAs contain considerable on-board memory (storage). On-board memory means the memory will be fast because it is within the device.

5.3.3.1 From the menu View in the PTC window, select RAM



The RAM window will open as

	Entity Name	Full Hierarchy Name	RAM Type	# of Instances	Vertical Network	Starting eSRAM ID / Vertical Network Column	Data Width	RAM Depth	RAM Mode	Port	
										Clock Freq. (MHz)	Clock
1	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	True Dual Port	400	50%
2	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	True Dual Port	400	50%
3			M20K	0	N/A	N/A	1	1	Simple Dual Port	0	0%

Details on the entries

Entity Name

By entering entity names, this means that the power of the sub-blocks can be entered and reviewed. If the power is too high for a certain block, this section can be focused on.

Full Hierarchy Name

This could be used if the design was implemented in Quartus.

Ram Type

There are two choices for memory in the PTC which are M20K (which are 20K memory blocks) and MLAB (memory LABs).

M20K memory (20 K bits) blocks, which are configurable, are used for larger memory configurations.

MLABs are used for the wide and shallow memories, where each MLAB is 640 bits. MLAB is where logic resources are used as memory.

The default memory is M20K, but there is a pull down for the MLABs.

# of instances

This is the number of instances for that memory configuration.

Data Width

Memory consists of width (of the data input bus) and depth (number of words).

The memory width for MLAB is 1 to 20, and for M20K is 1 to 40 except when configured as true dual port, where it will be 1 to 20.

Ram Depth

A memory consists of width (width of the data input bus) and depth (number of words). The default depth is 1, but it can be changed to larger depths.

Ram Mode

Memories can be configured in many different modes such as single dual port, true dual port, ROM (read only) and simple quad port. With simple dual port, there is one read and one write port, while with true dual port there are two ports and simple quad port has 4 ports.

With true dual port memories, two operations on two unique addresses can be done at the same time. True dual port usually has 2 clocks, while simple dual port has one clock.

True dual port memories and quad port memories run slower than simple true port RAM memories.

Clock Frequency

Clock Frequency refers to the fmax of the memories.

Ports (i.e. Port A, Port B)

The percentage of the clock, read and write can be adjusted. The clock % will need to be more than 0% so that it can clock. However, the amount of time for read and write can vary, i.e. 50/50, this will mean that the read/write will be half of the time. It can be other combinations for read and write such as 30/70%

5.3.3.2 How does the RAM mode change the power?

From the top of the RAM page, it shows the total thermal power (W)

RAM summary

Total thermal power (W):	**0.187**
MLAB utilization:	0%
M20K utilization:	86.260%
eSRAM utilization:	0%

5.3.3.3 Change the RAM mode to Simple Dual Port

Change the True Dual Port

	Entity Name	Full Hierarchy Name	RAM Type	# of Instances	Vertical Network	Starting eSRAM ID / Vertical Network Column	Data Width	RAM Depth	RAM Mode
1	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	True Dual Port
2	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	True Dual Port
3			M20K	0	N/A	N/A	1	1	Simple Dual Port

to **Simple Dual Port** as

	Entity Name	Full Hierarchy Name	RAM Type	# of Instances	Vertical Network	Starting eSRAM ID / Vertical Network Column	Data Width	RAM Depth	RAM Mode
1	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	Simple Dual Port
2	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	True Dual Port
3			M20K	0	N/A	N/A	1	1	Simple Dual Port

Note that with this change, the amount of thermal power changes significantly. The reason for this difference is the architecture. A simple dual port has one clock on one side with one read and write port. True dual port has 2 read and 2 write ports, and it will use more power.

The amount of thermal power changes

5.3.3.4 Change the memory back again to True dual port

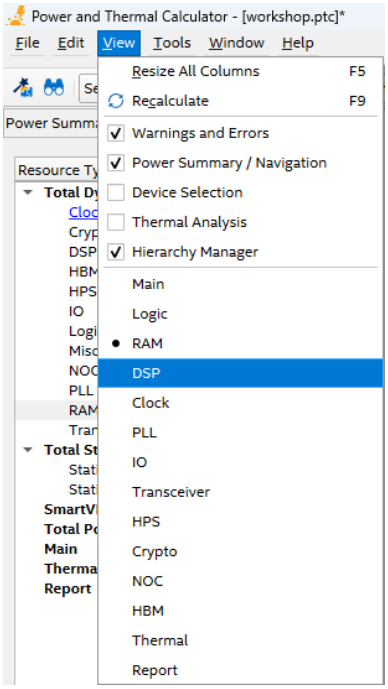
Change the Simple Dual Port → back to True Dual Port as

	Entity Name	Full Hierarchy Name	RAM Type	# of Instances	Vertical Network	Starting eSRAM ID / Vertical Network Column	Data Width	RAM Depth	RAM Mode
1	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	True Dual Port
2	topcore...	|works...plevel	M20K	113	N/A	N/A	1	1	True Dual Port
3			M20K	0	N/A	N/A	1	1	Simple Dual Port

5.3.4 DSP

Within the device, there are hardened yet configurable, variable precision DSP blocks. DSP blocks are useful for implementing DSP applications such as multipliers, multiplier and adders, AI functionality and other application.

5.3.4.1 From the menu View in the PTC Window, select DSP

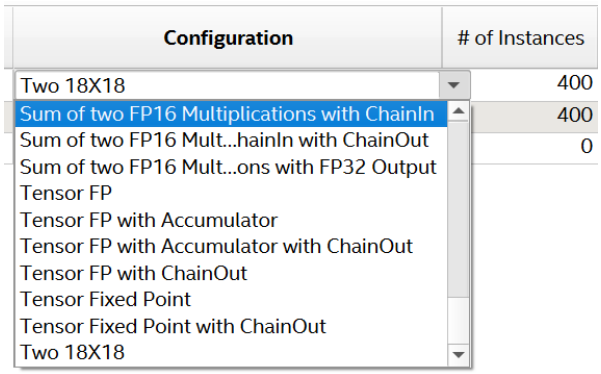


The DSP window will appear.

	Entity Name	Full Hierarchy Name	Configuration	# of Instances	Clock Freq. (MHz)	Clock Enable %	Toggle %	PreAdder?	Coefficient?	Registered Stages
1	topcore...	|works...plevel	Two 18X18	64	400	100%	12.5%	No	No	4
2	topcore...	|works...plevel	Two 18X18	64	400	100%	12.5%	No	No	4
3			Two 18X18	0	0	100%	12.5%	No	No	4

5.3.4.2 Select the pull-down menu of the Configuration to see options

There are many Configuration options for DSP blocks. The Agilex 5 are “first midrange or edge-centric FPGAs with an AI tensor block” thus there are various options with Tensor configuration blocks as seen below:



The default configuration selection is two 18x18. However, Tensor configuration of the DSP blocks allows high-efficiency AI and DSP configurations.

Entity Name

By entering entity names, this means that the power of the sub-blocks can be entered and reviewed. If the power is too high for a certain block, this can be focused on.

Configuration

There are many different DSP combinations. There are options such as FP16 (floating point) and variations of the Tensor blocks. The options depend on the complexity of the implementation.

# of instances

This is the number of instances for that configuration.

Clock Frequency

Clock Frequency refers to the fmax of the DSP blocks. There is a trade-off of performance vs power i.e. the faster the fmax, the more the power.

Clock Enable

This is the % of the time that the clock will be enabled.

Toggle

Toggle is the "percentage of clock cycles when the block output signal change value. This value is multiplied by clock frequency to determine number of transitions per second". The default is 12.5%

Pre-adder and Coefficient

Depending on the configuration, this can be enabled or not.

Register Stages

There are stages of 0 to 5, where the higher number means the faster the throughput.

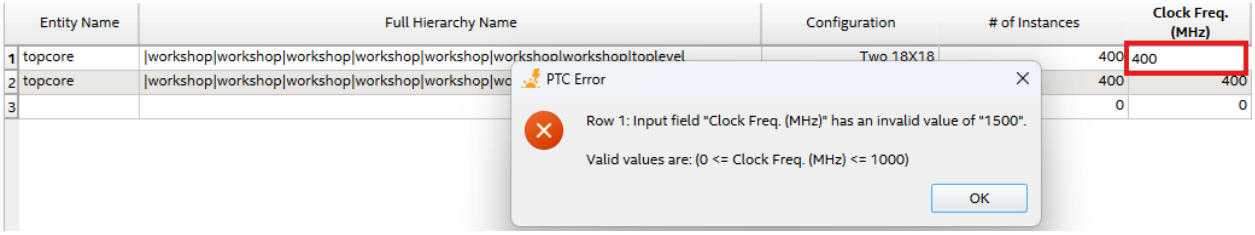
5.3.4.3 What happens if the DSP clock frequency is set to a very high fmax?

There are self-checks within PTC if the device parameters are exceeded. One error can be if the fmax of the DSP is exceeded. The highest fmax that the DSP can run at is 1 GHz.

However, what would happen if the fmax is exceeded is set to 1500 by mistake?

5.3.4.4 Change the clock frequency of the DSP to be 1500 MHz.

If the Clock Frequency is tried to change from 400 (in colour red) to 1500 MHz, an error will appear.



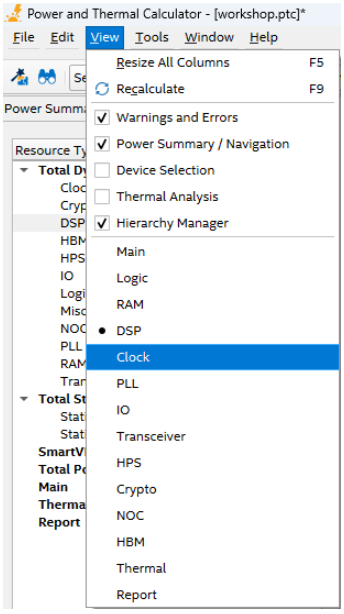
5.3.4.5 Select OK

This will remove the error.

5.3.5 Clock Resources

FPGAs need many clocks. The FPGA resources need to be synchronized. Synchronization allows the FPGA to behave "in a more reliable manner for all PVT conditions" (process, voltage, and temperature). Asynchronous designs, on the other hand, which rely on delays and skews "are prone to glitches and race conditions that can render the resulting implementation unreliable, increasing the complexity of constraints".

5.3.5.1 From the menu View in the PTC Window, select Clock



The clock window will open as

	Entity Name	Full Hierarchy Name	Clock Freq. (MHz)	Total Fanout	Global Enable %	Local Enable %	Utilization Factor	Power (W)
1		|works...rkshop	400	1000	100%	100%	6	0.007
2		|works...rkshop	400	1000	100%	100%	6	0.007
3			0	0	100%	100%	2	0

Entity Name

By entering entity names, this means that the power of the sub-blocks can be entered and reviewed. If the power is too high for a certain block, this can be focused on.

Clock Frequency

Clock Frequency refers to the fmax of the clock. The faster the fmax, the more power will be used.

Fanout

This refers to the number of other logics i.e. memory that the clocks are connected to.

Global Enable and Local Enable

This is the amount of time that the enables are on. The defaults are 100%

Utilization

The utilization factor is the impact on the clock network.

One thing to note is that the PTC will determine if the utilization factor needs to be higher than the default of 2. Should the utilization factor be set to 2, the PTC reported that there was a warning that Selected Utilization Factor is uncharacteristically low for specified Fanout value. (This could be tried, if wished).

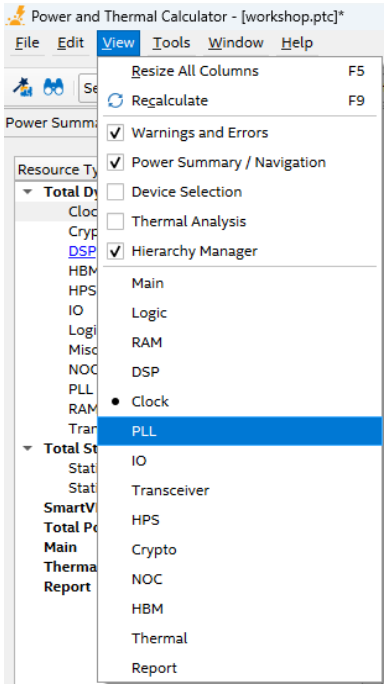
5.3.6 PLL

PLLs, which is an abbreviation for phase locked loop, provides clock management.

PLLs have many advantages such as

-it can reduce the number of clock pins (as there are many configurable output clock frequencies),
-assist with timing with the configurable settings (i.e. make changes to clock phase),
-has feedback.

5.3.6.1 From the menu View in the PTC Window, select PLL



The window will appear as:

	Entity Name	Full Hierarchy Name	PLL Type	Bank ID	# of Instances	# Counters	VCO Freq. (MHz)	Power (W)
1	topcore...	|works...plevel	I/O Bank IOPLL	2A_T/2A_B	1	1	600	0.007
2		|works...rkshop	I/O Bank IOPLL	2A_T/2A_B	1	1	600	0.007
3		|works...rkshop	I/O Bank IOPLL	3A_T/3A_B	1	1	600	0.007
4		|works...rkshop	I/O Bank IOPLL	3A_T/3A_B	1	1	600	0.007
5			I/O Bank IOPLL	2A_T/2A_B	0	1	600	0

Entity Name

By entering entity names, this means that the power of the sub-blocks can be entered and reviewed. If the power is too high for a certain block, this can be focused on.

PLL type

There are 2 PLL types of Agilex PLLs. There is I/O Bank IOPLL and fabric feeding IOPLL. The I/O PLLs are located adjacent to the hard memory controllers and LVDS serializer/deserializer (SERDES) blocks in the I/O banks. Each I/O bank contains two I/O bank I/O PLLs and one fabric-feeding I/O PLL. Both PLLs are configurable with dedicated clock input pins. However, the I/O bank IOPLL has more features such as dedicated output, zero buffer and external feedback modes.

Bank ID

The Bank ID is the location of the I/O bank on Agilex device.

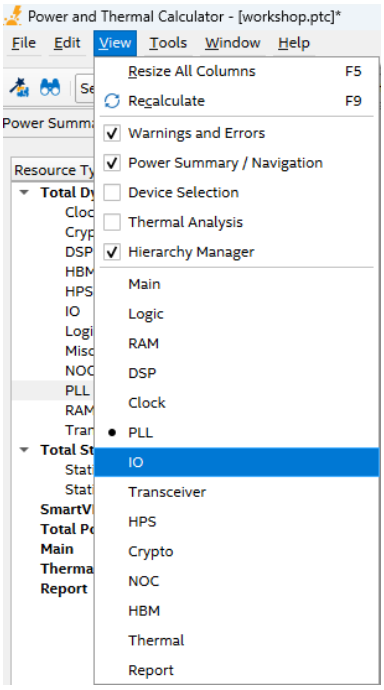
# of instances

This is the number of PLLs that will be used. Only 2 instances are allowed per Bank ID

5.3.7 IO

All FPGAs need I/O connections to connect to other external components on the board. The I/Os are used to connect to components such as clock sources (i.e. oscillators), external memory interfaces, and more.

5.3.7.1 From the menu View in the PTC Window, select IO



The I/O window will appear as

	Entity Name	Full Hierarchy Name	Application	Bank ID	# of Instances	Interface Parameters				
						Interface Direction	Frequency (MHz) / Data Rate (Mbps)	Interface Rate	Toggle %	Write Enable %
1	topcore...	|works...plevel	GPIO	2A_B	20	Bi-directional	400	SDR	12.5%	50%
2		|works...rkshop	GPIO	2A_T	20	Bi-directional	400	SDR	12.5%	50%
3		|works...rkshop	GPIO	3A_B	20	Bi-directional	400	SDR	12.5%	50%
4		|works...rkshop	GPIO	3A_T	20	Bi-directional	0	SDR	12.5%	50%
5			GPIO	2A_B	0	Bi-directional	0	SDR	12.5%	50%

Application

The application refers to either GPIO (general purpose I/O), external memory, HVIO (high voltage) and SERDES (serializer/deserializer) interfaces. FPGAs need to use serialization and deserialization when the incoming rates are faster than the max rate for the I/Os that the FPGA can accept.

Bank ID

The Bank ID refers to the I/O banks on the Agilex devices.

# of instance

Number of I/Os that are used. Different banks have different number of IOs

Interface Parameters that include direction, frequency, interface rate, toggle%, OE, registered

Interface Direction

The inputs could be bi-directional, inputs or outputs.

Clock frequency affects power. The faster the clock runs the higher the power.

Interface Rate

The Interface rate can be either SDR (single data rate) or DDR (double date rate). With SDR, the data is either on the rising or falling edge of the clock while in DDR, the data is on both the rising and falling edge of the clock. DDR Data can be transferred at 2x the rate of SDR, because both edges of the clock are used.

Toggle %

Toggle rate is the "percentage of clock cycles when the I/O change value". This number is multiplied by the clock frequency to determine the throughput. If the interface is DDR, the number is multiplied by 2x because there is data on the rising and falling edge of the clock. The default value is 12.5%.

OE% is the % that the output enable is enabled.

Registered which can be toggled as Yes/No would have registers in the I/O element if the toggle is set to Yes.

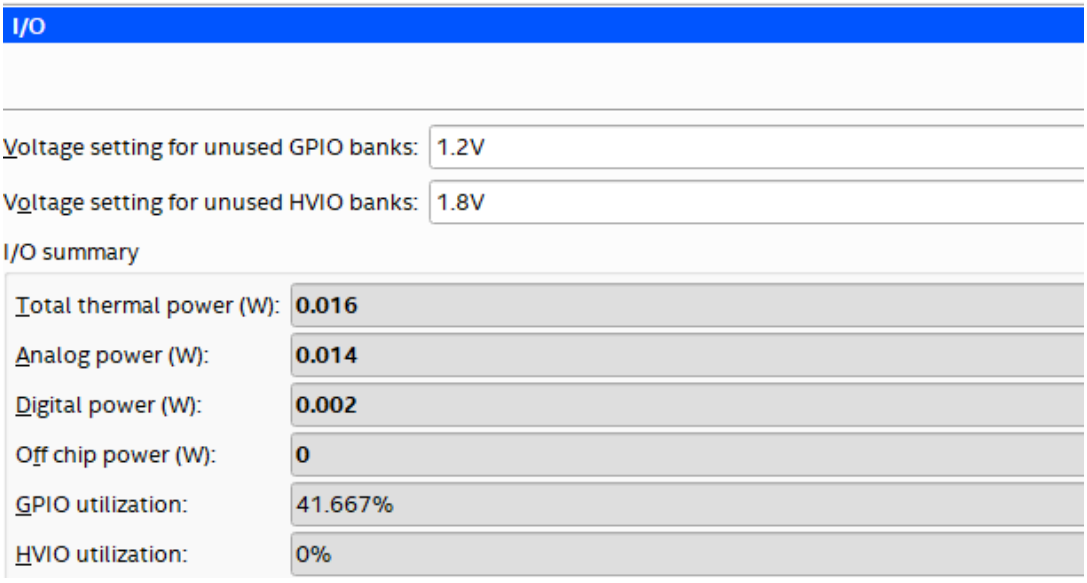
5.3.7.2 Scroll to the right-hand side of the I/O window.

	Memory IP Parameters			I/O Analog Settings				
	DQ Width	Data Lanes	A/C Lanes	I/O Standard	Input Termination	Current Strength / Output Termination	Slew Rate	VOI
O	0	0	0	1.2-V	Off	Series 34 Ohm	0	
O	0	0	0	1.2-V	Off	Series 34 Ohm	0	
O	0	0	0	1.2-V	Off	Series 34 Ohm	0	
O	0	0	0	1.2-V	Off	Series 34 Ohm	0	
O	0	0	0	0.7-V LVSTL	Off	Series... Ohm C	0	

I/O standard

There are many I/O standards that are available to be used. The I/O standard depends on what the FPGA connects to. POD is the acronym for pseudo-open drain interface. HSUL stands for high-speed unterminated logic, while SSTL stands for Stub Series Terminated logic. The 1.2V is the default settings. The I/O standards, which affect power, depend on the external components that the FPGAs connect to.

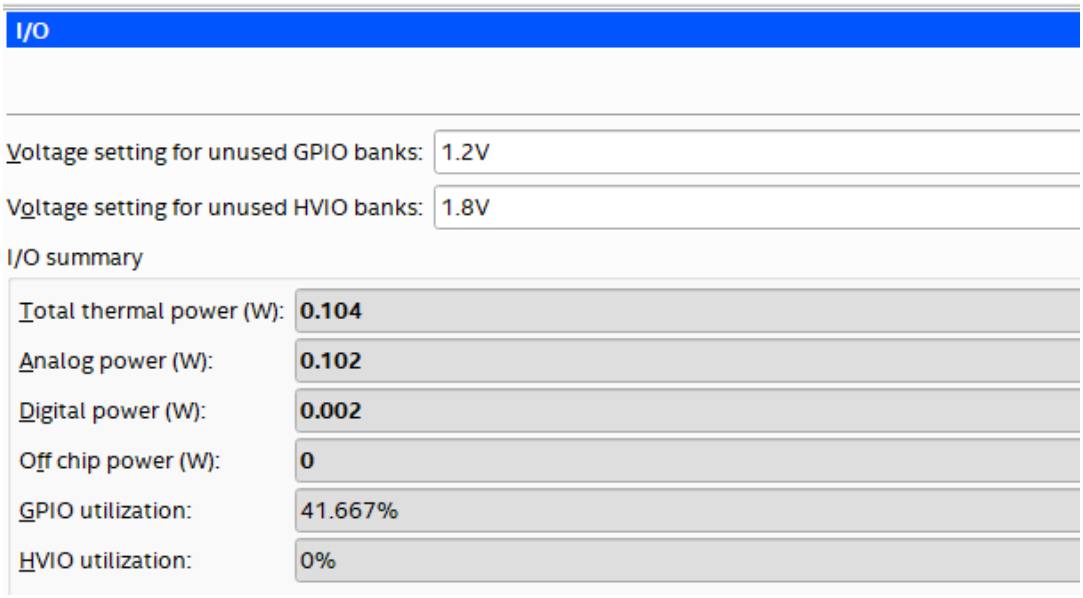
To see the effect of power via the I/O standards selection, the power is seen as



5.3.7.3 Scroll to the right-hand side of the I/O Window and change the power to SSTL-12.

	Memory IP Parameters		I/O Analog Settings						
	Data Lanes	A/C Lanes	I/O Standard	Input Termination	Current Strength / Output Termination	Slew Rate	VOD Setting	Programmable De-Emphasis	Load (pF)
1	0	0	1.2-V	Off	Series 34 Ohm	0	N/A	Off	0
2	0	0	1.2-V	Off	Series 34 Ohm	0	N/A	Off	0
3	0	0	SSTL-12	Off	Series 34 Ohm	0	N/A	Off	0
4	0	0	1.2-V	Off	Series 34 Ohm	0	N/A	Off	0
5	0	0	0.7-V LVSTL	Off	Series 40 Ohm C	0	N/A	High (Constant Impedance)	0

Note the I/O Power has increased considerably as



For reference, SSTL-12 is a single ended SSTL external termination that needs an input Vref (voltage reference) and a termination voltage (VTT).

5.3.7.4 Change the I/O standard back to 1.2 V.

The next step is to **change the I/O standard back to 1.2 V as:**

	Memory IP Parameters		I/O Analog Settings						
	Data Lanes	A/C Lanes	I/O Standard	Input Termination	Current Strength / Output Termination	Slew Rate	VOD Setting	Programmable De-Emphasis	Load (pF)
1	0	0	1.2-V	Off	Series 34 Ohm	0	N/A	Off	0
2	0	0	1.2-V	Off	Series 34 Ohm	0	N/A	Off	0
3	0	0	1.2-V	Off	Series 34 Ohm	0	N/A	Off	0
4	0	0	1.2-V	Off	Series 34 Ohm	0	N/A	Off	0
5	0	0	0.7-V LVSTL	Off	Series 40 Ohm C	0	N/A	High (Constant Impedance)	0

For reference, there are other tabs as well that can be used for a design. The information on the Thermal tab is useful for the Thermal engineer to help design cooling solutions. The information on the Report tab are useful for the engineer who work power design, because the tab provides current values that are needed for voltage regulators.

6. Techniques to reduce power

There are trade-offs of performance vs power. With more performance, there is an increase of power.

There are items to look at to reduce power that include:

1) Reduce the clock frequency, if possible. The faster clock fmax that resources run at, the more dynamic power will be used.

2) Use different I/O standards and/or lower power I/O standards, if possible. Using differential I/O standards can reduce power.

3) Reduce the number of resources. Using less resources will use less power.

4) Use the smallest size device that is possible for the design. The smaller the device, the less static power that it will use.

5) Device grade i.e. standard vs low power/extended low power can make a difference in the power results. Slower speed grade devices mean the max performance of the device is less which in turn results in lower power.

6) Using Quartus with a complete design will provide more accurate values because it will use the design to do power analysis. The toggle rate, etc will be more accurate.

7. Experiment with changing PTC settings

Experiment with changing settings in the PTC to see changes

Experiment in the PTC, by adding more resources, reducing resource, increasing/decreasing faster clock rates, adding transceivers, and more to see what effects that this makes on the power.

Question: Where do you see the most change in the power?

8. Close the PTC window

Select in the top left of the PTC window → File -Save

Save the file as workshop_modifed. This will give you two files for reference.

The file extension will be .ptc (Power Thermal Calculator File).

Select in the top left of the PTC Window → File →Exit to close the PTC window.

CONGRATULATIONS! YOU HAVE SUCCESSFULLY COMPLETED THE PTC Workshop!

In summary, this workshop provides why and how (in a step-by-step approach) to

- use the Altera Power Thermal Calculator (PTC) for an Agilex-3 device.

Knowing the power of a design affects the complete design as it influences the power rails, power envelope (i.e. is a heat sink/ fan needed) and more.

The stand-alone Power Thermal calculator (PTC) can be used for:

- power estimation before the design is started and/or if the design is in progress
- and to do the preliminary thermal analysis for the design.

9. Appendix A How to do resource estimation if the design is not done?

Sometimes, due to quick time schedules, PCBs might need to be created in parallel before the FPGA design is even started.

The question is then: How can the power be known if the design is not even started?

The first step is to document the requirements of the desired application (functionality). For example, would it be a video application, machine learning, communication, industrial, or many other applications?

The next step is to break down the functionality into its major building blocks. For example, if it is a video or machine learning application, there would be blocks such as a sensor interface, DisplayPort and/or HDMI (for inputs), data processing i.e. color space converter.

Once the major blocks are known, the resources of the major blocks would then need to be calculated/determined.

There are different approaches to calculating resources if the design is not completed. The different, following approaches could be combined. This would give a rough idea of

the magnitude of the power estimate of what power would be needed. The power number would need to be refined later, as the design gets implemented, however, it would be a start. More resources running at a faster fmax increases the power.

One approach is to see if there is a reference design/user guide/design example. Perhaps part of the reference design could be used. Having a reference design even if only part of the reference guide is used especially for a development board is a very good way to test part of the design rather than "re-inventing the wheel". A reference design would have many of the building blocks connected. As an example, Quartus generates reference examples such as for MIPI CSI-2, external memory, etc that can be compiled to see the number of resources.

Another way is to open Quartus and implement some of the functionality such as counters, memory, etc to see the number of resources that are needed.

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