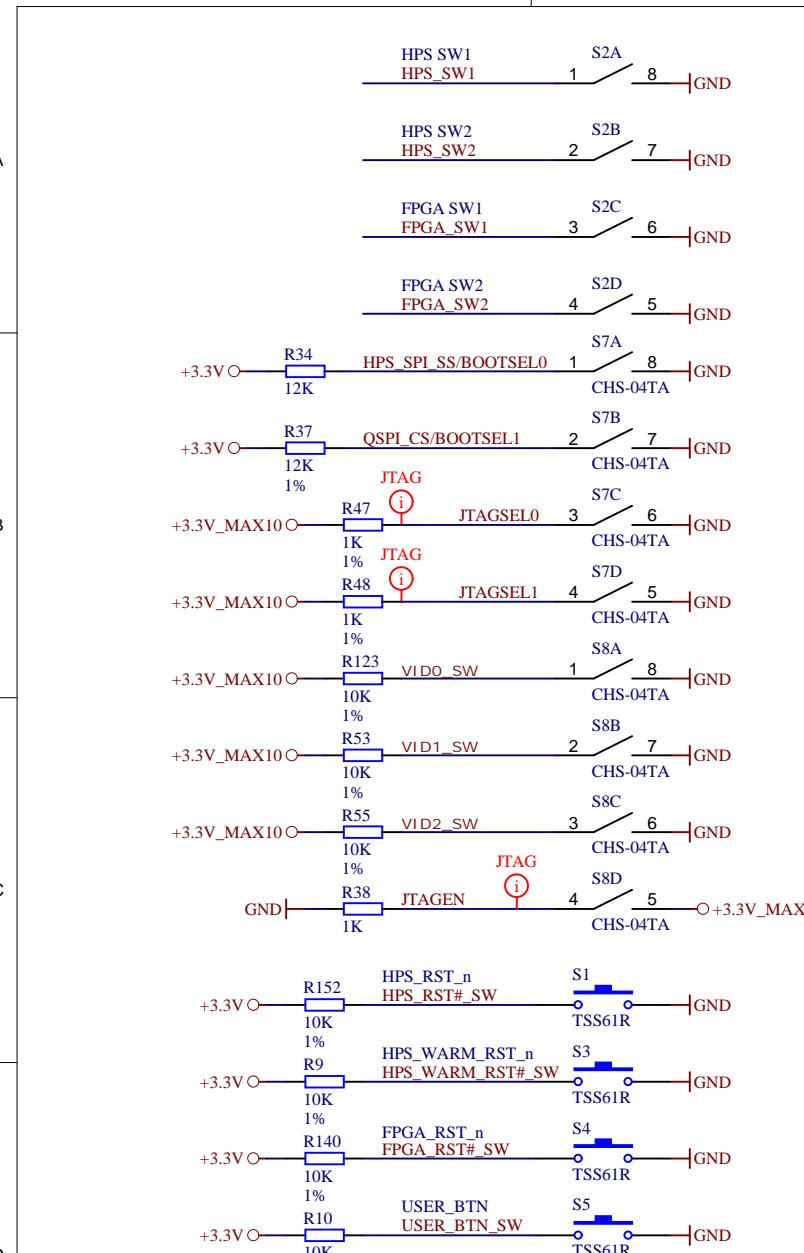


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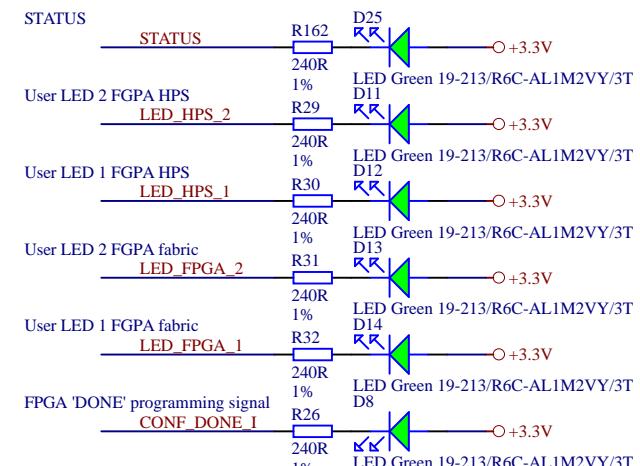
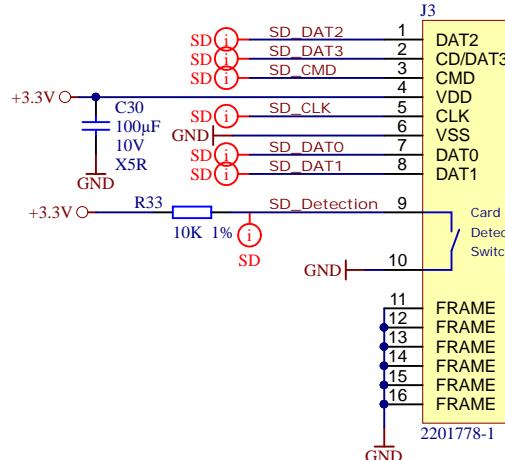


BOOTSEL0 | BOOTSEL1 | BOOTSEL2 | Boot Select

0		0		1		FPGA
1		0		1		SD/MMC (3.3V)
1		1		1		SPI(3.3V)

JTAGSEL0 | JTAGSEL1 | JTAGEN | JTAG Selection

X		X		1 - (ON) MAX10
0 - (ON)		0 - (ON)		0 - (OFF) CYCLONE V HPS
0 - (ON)		1 - (OFF)		0 - (OFF) CYCLONE V FPGA
1 - (OFF)		0 - (ON)		0 - (OFF) FMC



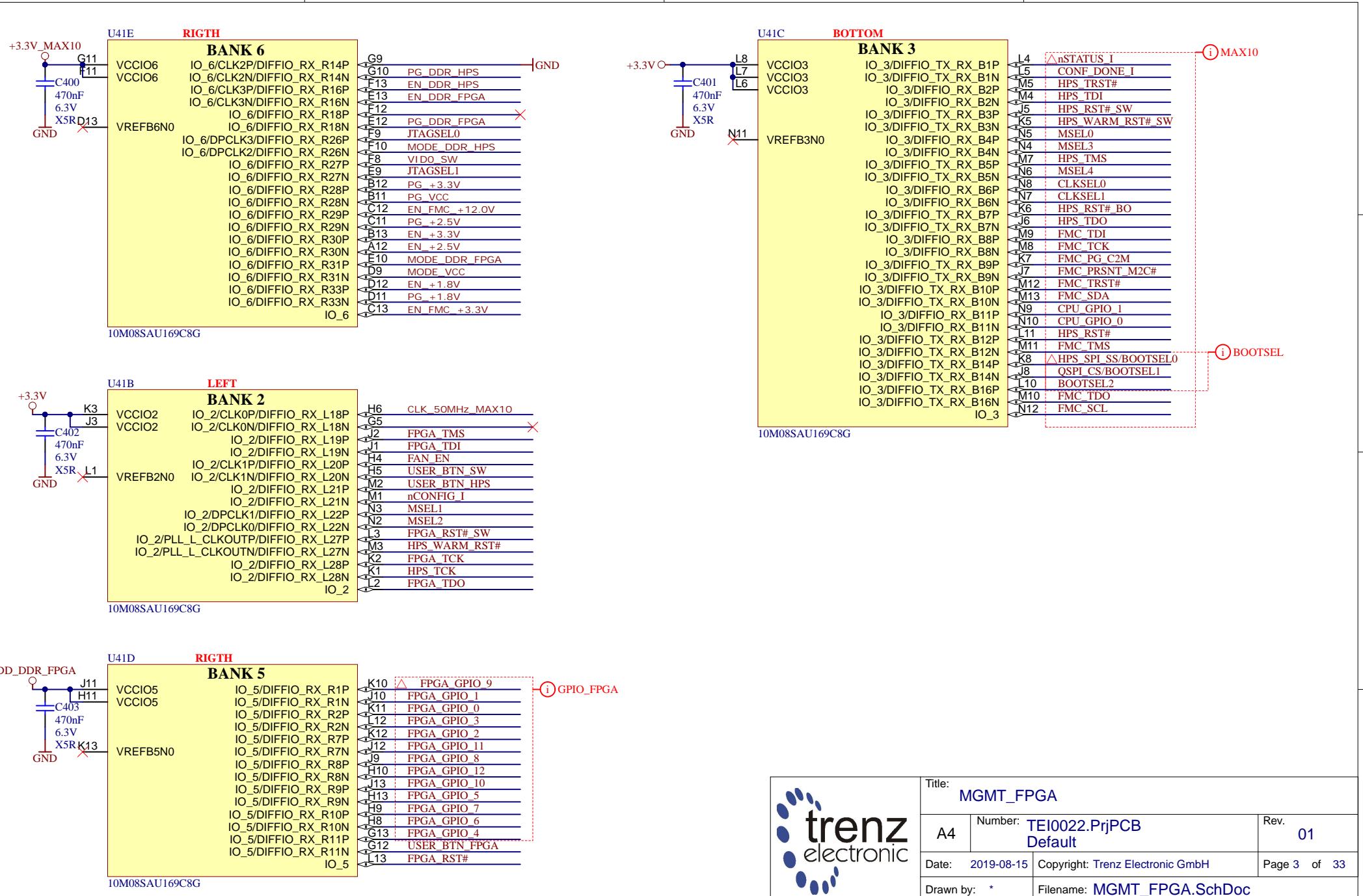
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A4 Number: TEI0022.PrjPCB Default

Rev. 01

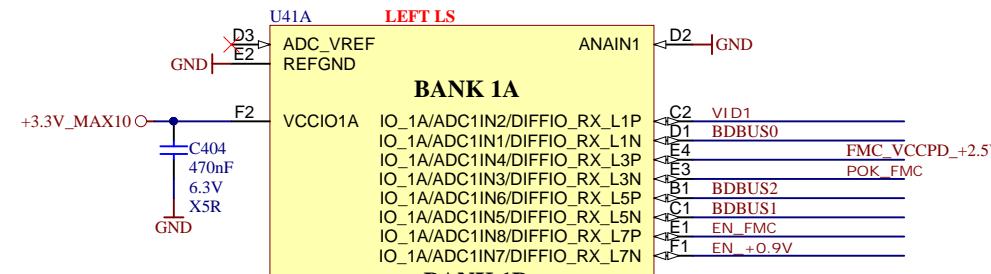
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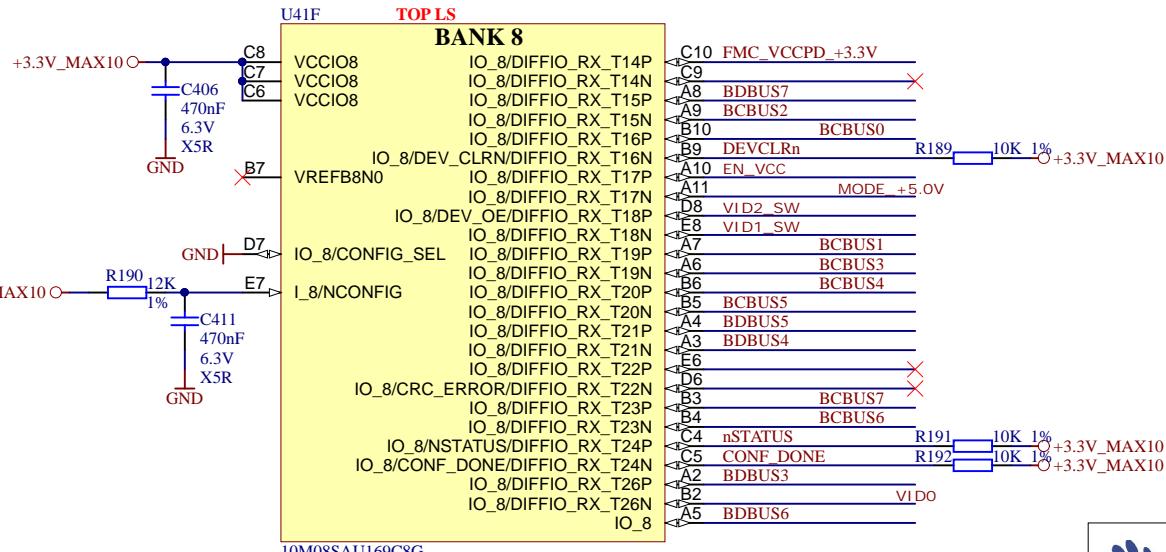


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A4	Number: TEI0022.PrjPCB Default	Rev. 01
Date: 2019-08-15	Copyright: Trenz Electronic GmbH	Page 3 of 33
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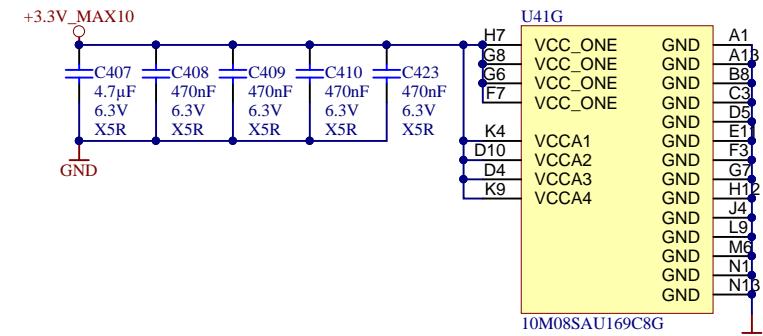
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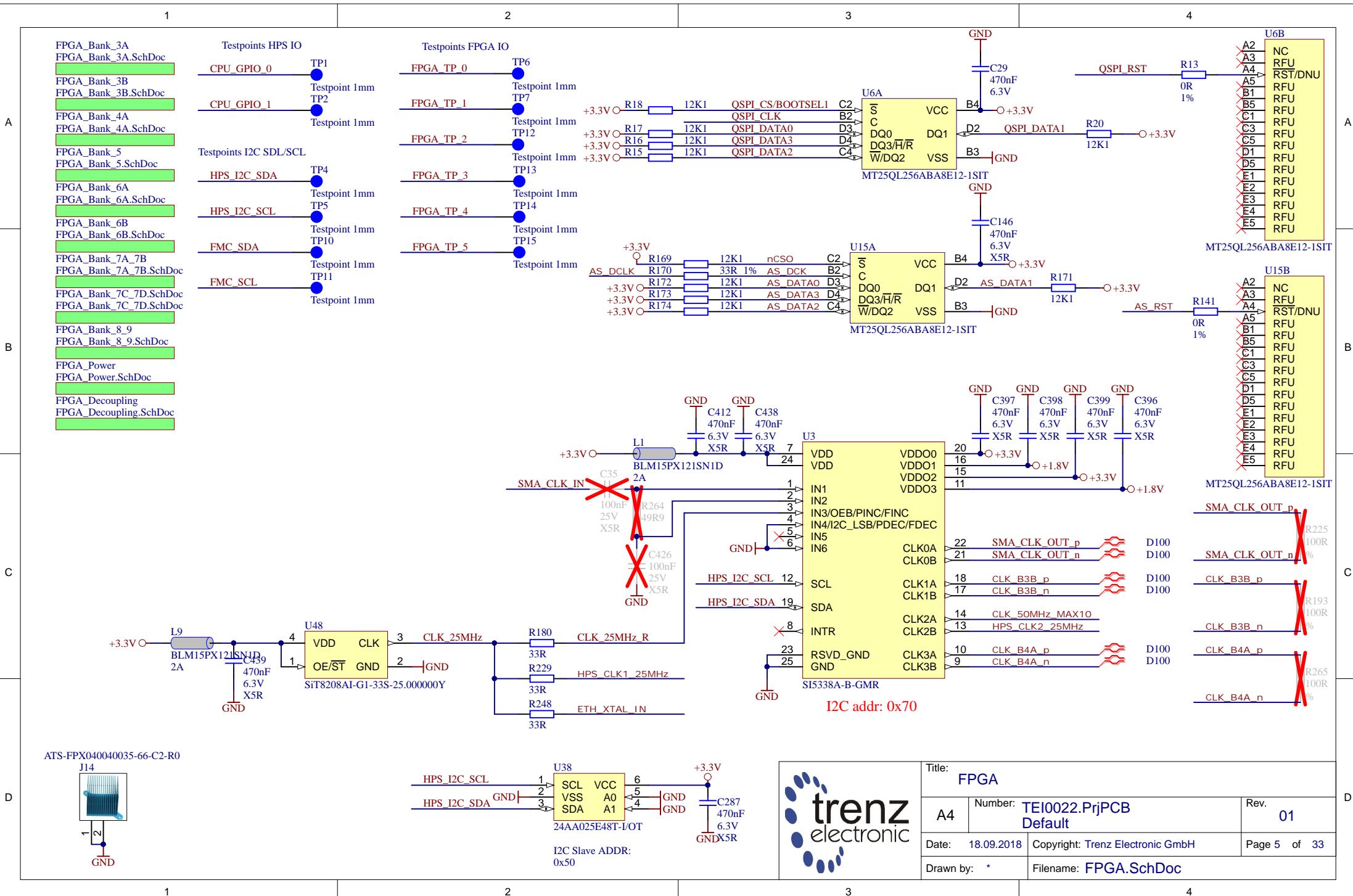


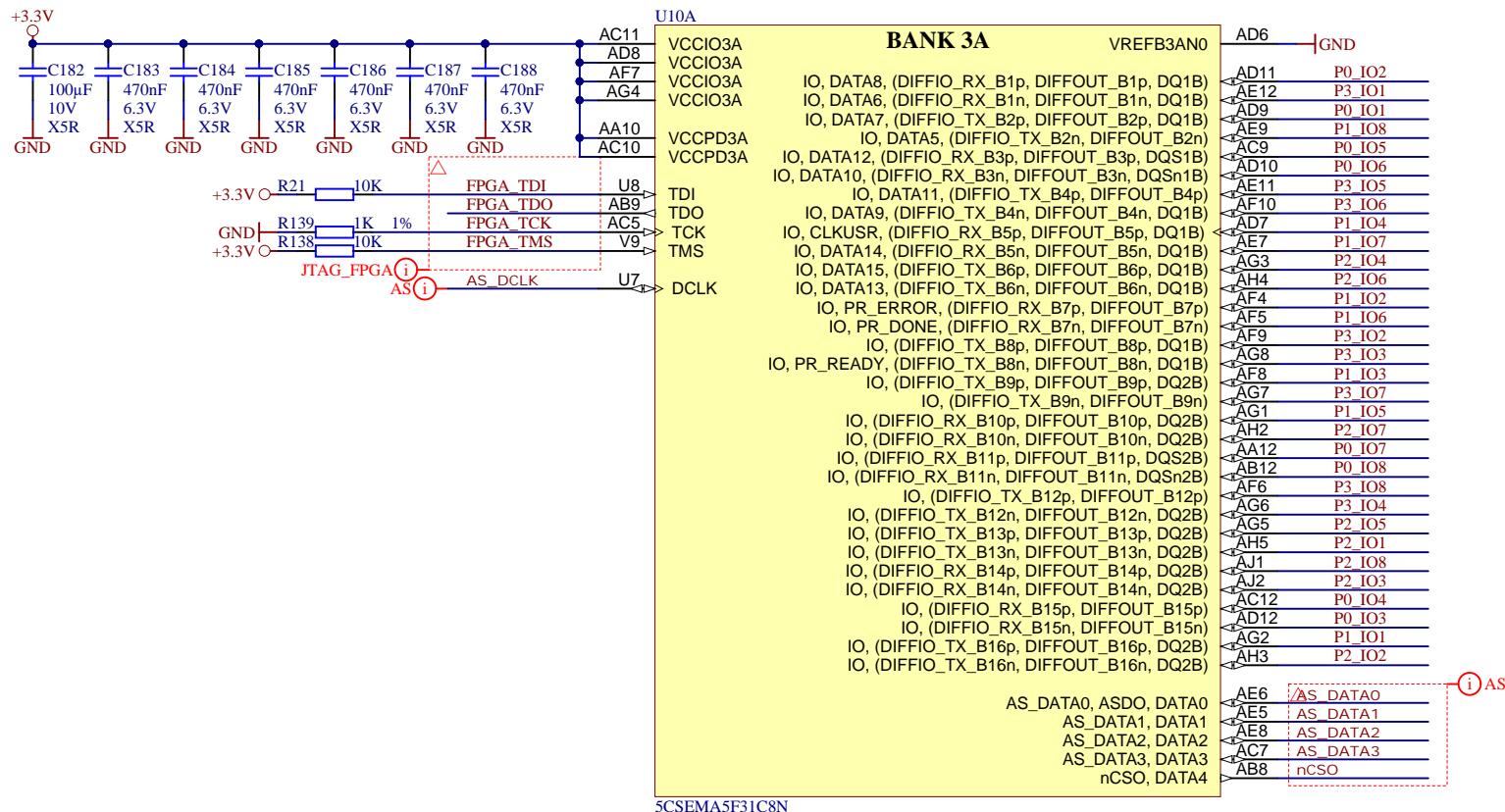
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A4 Number: TEI0022.PrjPCB Default Rev. 01

Date: 2019-08-15 Copyright: Trenz Electronic GmbH

Drawn by: * File: MGMT_FPGA_Misc.SchDoc Page 4 of 33



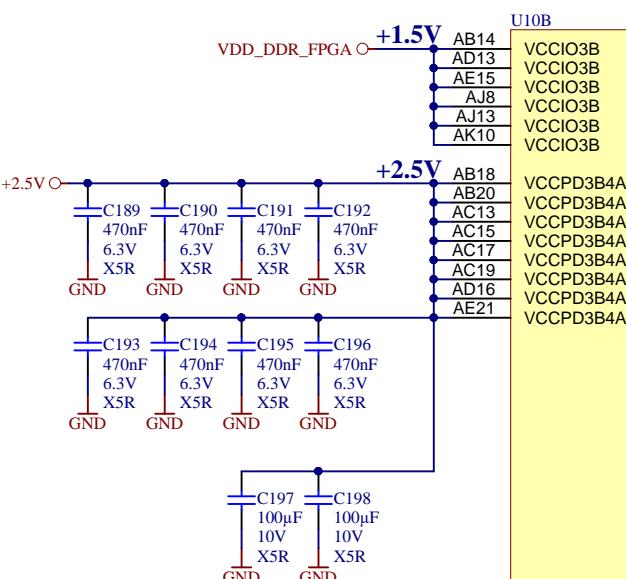
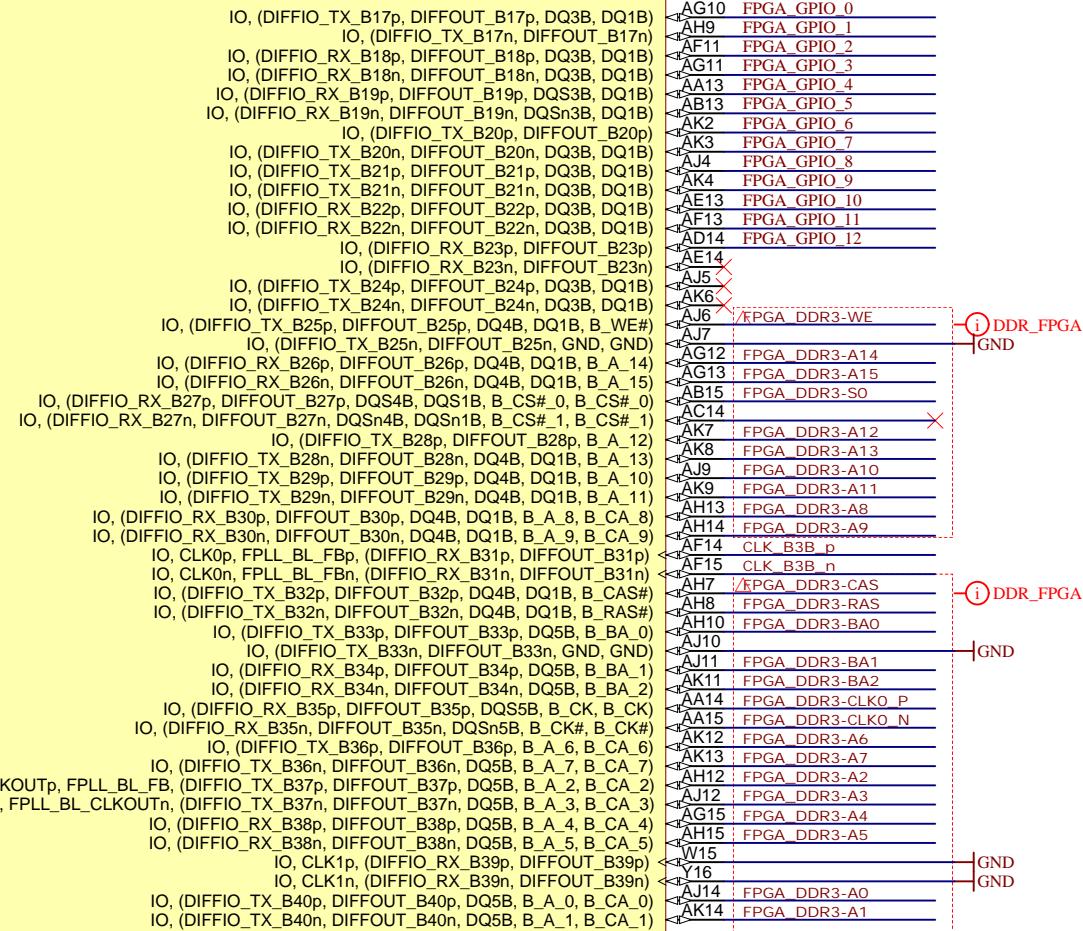
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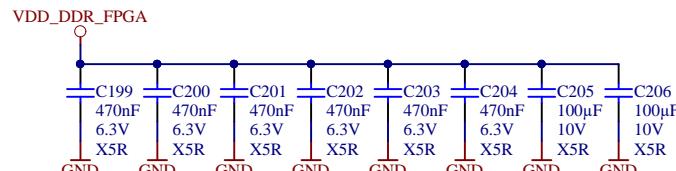
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**BANK 3B**

5CSEMA5F31C8N



Title: **FPGA_Bank_3B**

A4 Number: **TEI0022.PrjPCB Default**

Rev. **01**

Date: **18.09.2018** Copyright: **Trenz Electronic GmbH**

Page **7** of **33**

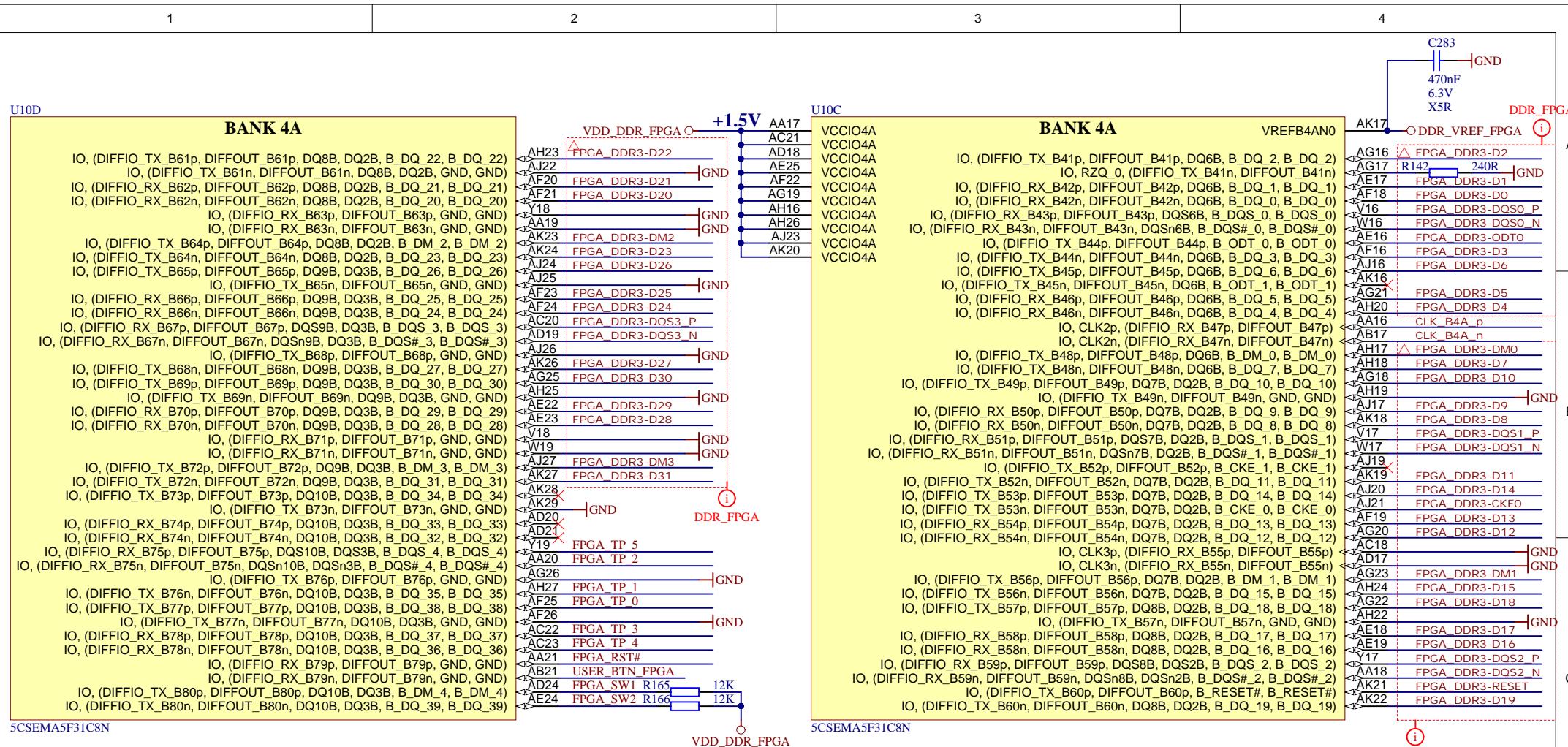
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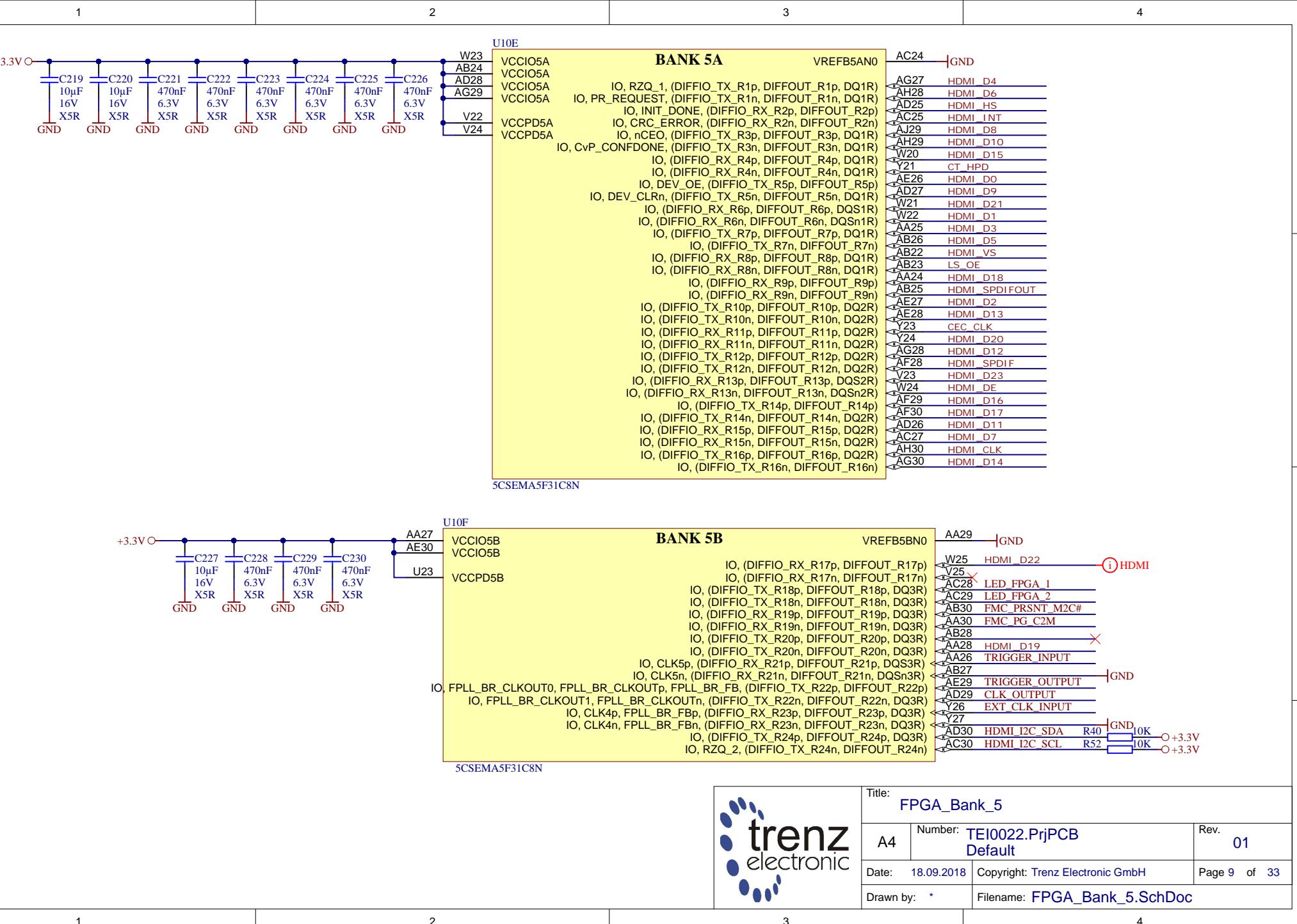


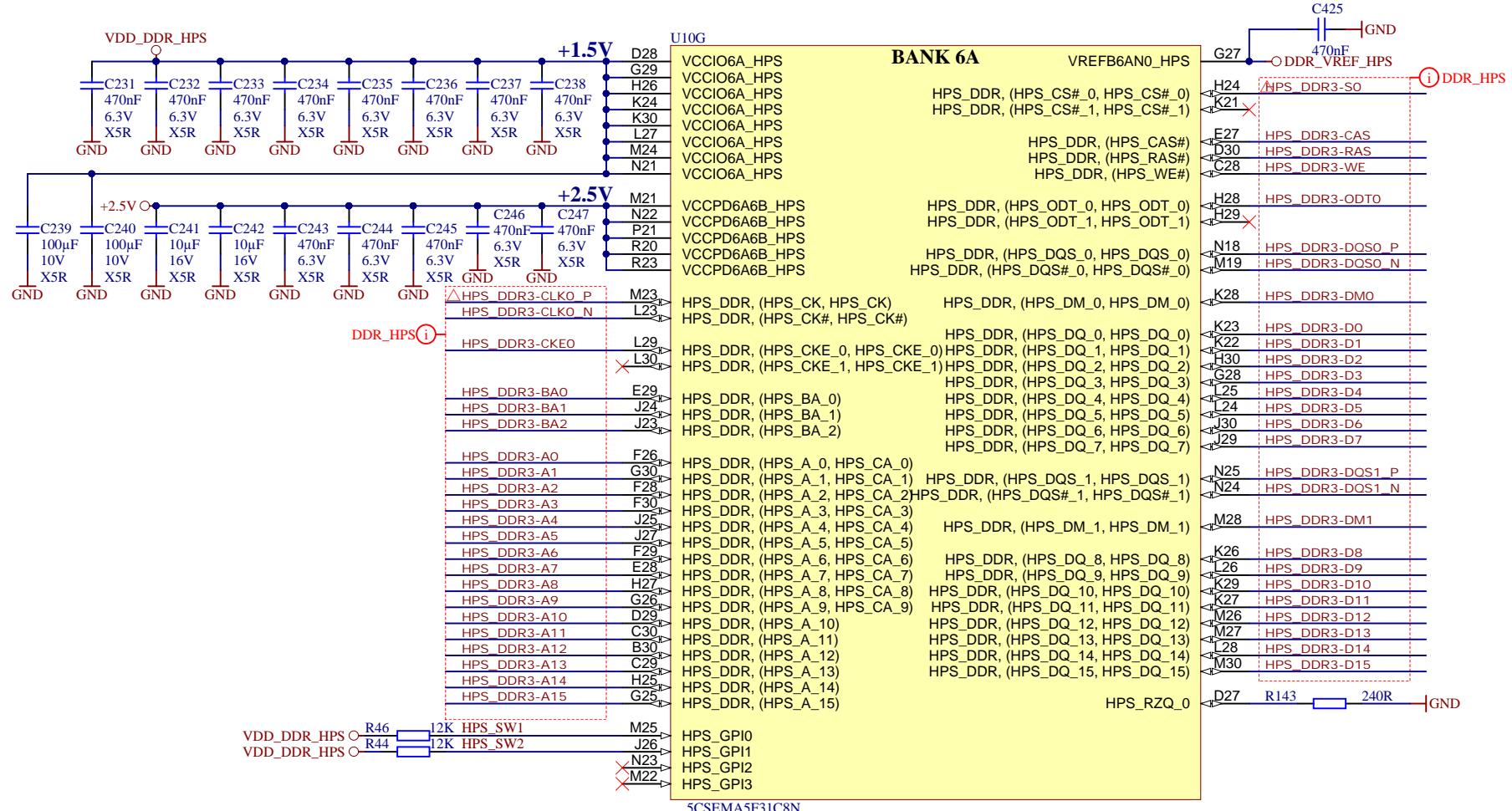
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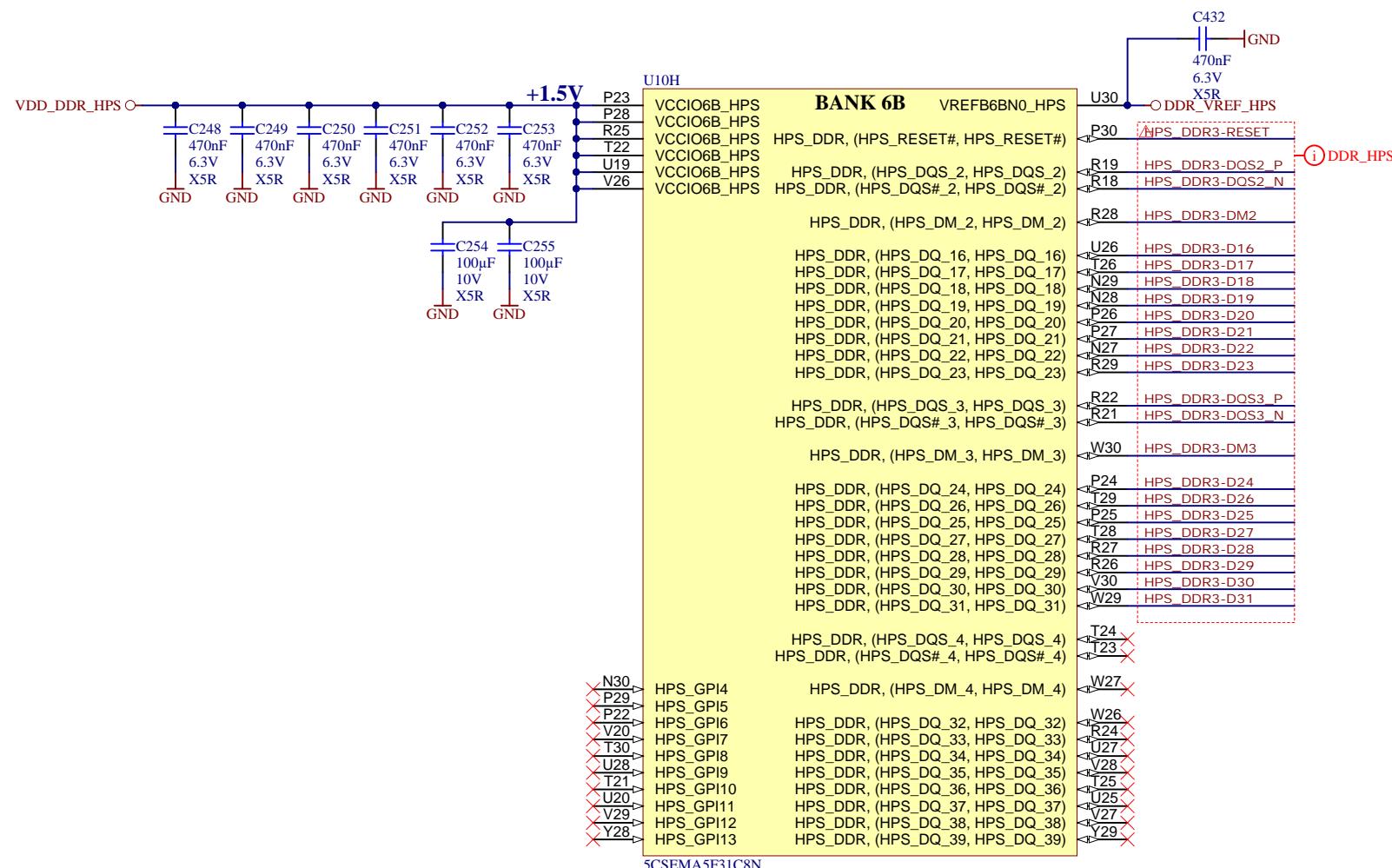
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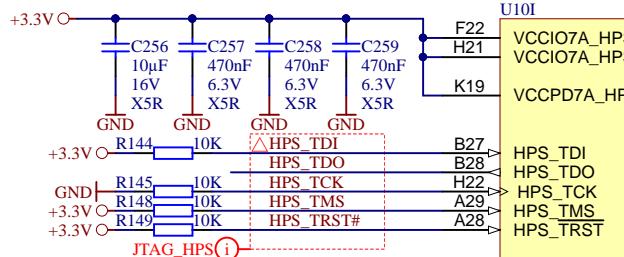


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Title: FPGA_Bank_6B		
A4	Number: TEI0022.PrjPCB Default	Rev. 01
Date: 18.09.2018	Copyright: Trenz Electronic GmbH	Page 11 of 33
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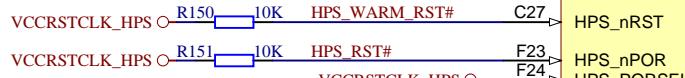
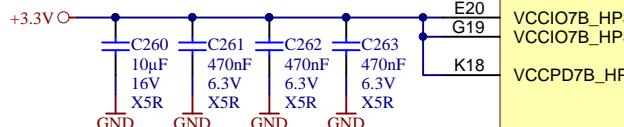
U10I
VCCIO7A_HPS
VCCIO7A_HPS
VCCPD7A_HPS

BANK 7A

TRACE_CLK, (TRACE_CLK, HPS_GPIO48)
TRACE_D0, (TRACE_D0, SPIS0_CLK, UART0_RX, HPS_GPIO49)
TRACE_D1, (TRACE_D1, SPIS0_MOSI, UART0_TX, HPS_GPIO50)
TRACE_D2, (TRACE_D2, SPIS0_MISO, I2C1_SDA, HPS_GPIO51)
TRACE_D3, (TRACE_D3, SPIS0_SS0, I2C1_SCL, HPS_GPIO52)
TRACE_D4, (TRACE_D4, SPIS1_CLK, CAN1_RX, HPS_GPIO53)
TRACE_D5, (TRACE_D5, SPIS1_MOSI, CAN1_TX, HPS_GPIO54)
TRACE_D6, (TRACE_D6, SPIS1_SS0, I2C0_SDA, HPS_GPIO55)
TRACE_D7, (TRACE_D7, SPIS1_MISO, I2C0_SCL, HPS_GPIO56)

HPS_CLK1, (HPS_CLK1, HPS_CLK1)
HPS_CLK2, (HPS_CLK2, HPS_CLK2)
HPS_CLK3, (HPS_CLK3, SPIM0_SS0, BOOTSEL0, (SPIM0_SS0, CAN1_TX, UART1_RTS, HPS_GPIO60))

UART0_RX, (UART0_RX, CAN0_RX, SPIM1_SS1, HPS_GPIO61)
UART0_TX, CLKSEL1, (UART0_TX, CAN0_TX, SPIM1_SS1, HPS_GPIO62)

**BANK 7B**

VCCIO7B_HPS
VCCIO7B_HPS
VCCPD7B_HPS

NAND_ALE, (NAND_ALE, RGMII1_TX_CLK, QSPI_SS3, HPS_GPIO14)
NAND_CE, (NAND_CE, RGMII1_TXD0, USB1_D0, HPS_GPIO15)
NAND_CLE, (NAND_CLE, RGMII1_RXD1, USB1_D1, HPS_GPIO16)
NAND_RE, (NAND_RE, RGMII1_RXD2, USB1_D2, HPS_GPIO17)
NAND_RB, (NAND_RB, RGMII1_RXD3, USB1_D3, HPS_GPIO18)
NAND_DQ0, (NAND_DQ0, RGMII1_RXD0, HPS_GPIO19)
NAND_DQ1, (NAND_DQ1, RGMII1_MDIO, I2C3_SDA, HPS_GPIO20)
NAND_DQ2, (NAND_DQ2, RGMII1_MDC, I2C3_SCL, HPS_GPIO21)
NAND_DQ3, (NAND_DQ3, RGMII1_RX_CTL, USB1_D4, HPS_GPIO22)
NAND_DQ4, (NAND_DQ4, RGMII1_TX_CTL, USB1_D5, HPS_GPIO23)
NAND_DQ5, (NAND_DQ5, RGMII1_RX_CLK, USB1_D6, HPS_GPIO24)
NAND_DQ6, (NAND_DQ6, RGMII1_RXD1, USB1_D7, HPS_GPIO25)
NAND_DQ7, (NAND_DQ7, RGMII1_RXD2, HPS_GPIO26)
NAND_WP, (NAND_WP, RGMII1_RXD3, QSPI_SS2, HPS_GPIO27)
NAND_WE, (NAND_WE, QSPI_SS1, HPS_GPIO28)

QSPI_I00, (QSPI_I00, USB1_CLK, HPS_GPIO29)
QSPI_I01, (QSPI_I01, USB1_STP, HPS_GPIO30)
QSPI_I02, (QSPI_I02, USB1_DIR, HPS_GPIO31)
QSPI_I03, (QSPI_I03, USB1_NXT, HPS_GPIO32)
QSPI_SS0, (QSPI_SS0, HPS_GPIO33)
QSPI_CLK, (QSPI_CLK, HPS_GPIO34)
QSPI_SS1, (QSPI_SS1, HPS_GPIO35)

E22 GND
B26 CPU_GPIO_0
C25 FTDL_RX
A25 HPS_I2C_SDA
H23 HPS_I2C_SCL
A24 LED_HPS_1
G21 LED_HPS_2
C24 THERM_N
E23 ALERT_N

A23 USER_BTN_HPS
C22 CPU_GPIO_1
B23 STATUS
H20 HPS_SPI_SS/BOOTSEL0

B22 AS_RST
G22 CLKSEL1 R272 1K GND
C23 FMC_SDA
D22 FMC_SCL
E24 QSPI_RST
D24 CLKSEL0 R273 1K GND

H19 ETH_TXCK
F20 ETH_TXDO
J19 ETH_TXD1
F21 ETH_TXD2
F19 ETH_TXD3
A21 ETH_RXDO
E21 ETH_MDIO
B21 ETH_MDC
K17 ETH_RXCTL
A20 ETH_TXCTL
G20 ETH_RXCK
B20 ETH_RXD1
B18 ETH_RXD2
D21 ETH_RXD3
D20 BOOTSEL2 R39 12K +3.3V

C20 QSPI_DATA0
H18 QSPI_DATA1
A19 QSPI_DATA2
E19 QSPI_DATA3
A18 QSPI_CS/BOOTSEL1
D19 R276 49R9 QSPI_CLK
C19 PHY_TINT
QSPI
QSPI

5CSEMA5F31C8N



Title: **FPGA_Bank_7A_7B**

A4 Number: **TEI0022.PrjPCB Default**

Rev. **01**

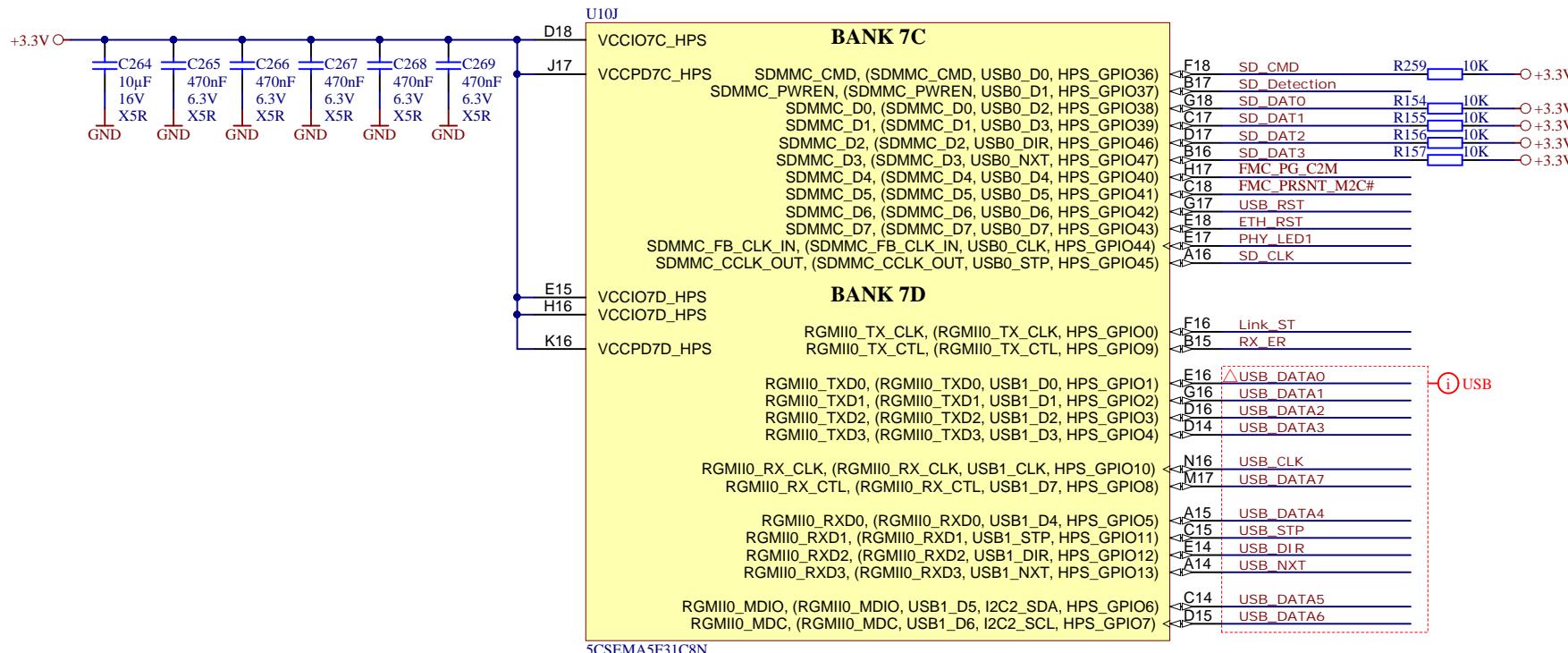
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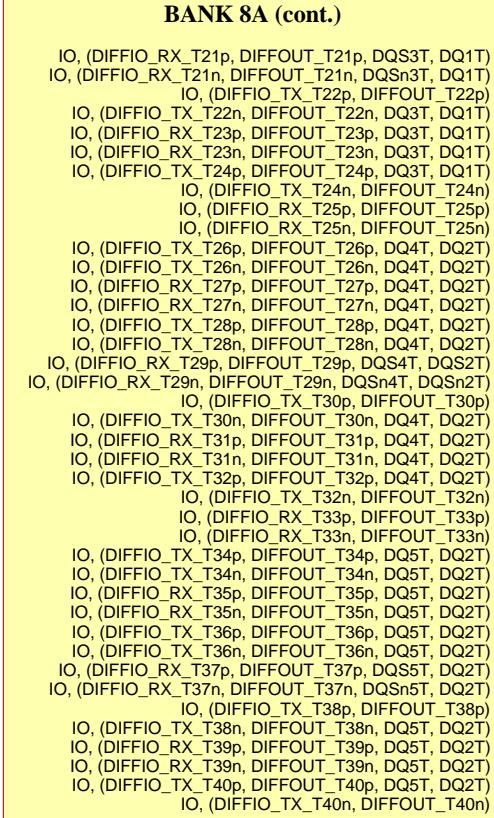
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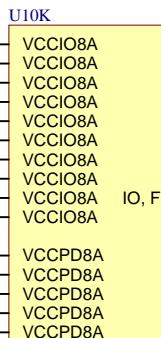
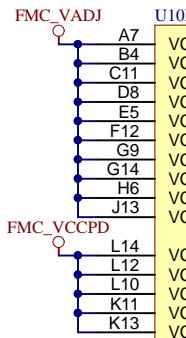


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A4	Number: TEI0022.PrjPCB Default	
Date: 18.09.2018	Copyright: Trenz Electronic GmbH	Page 13 of 33
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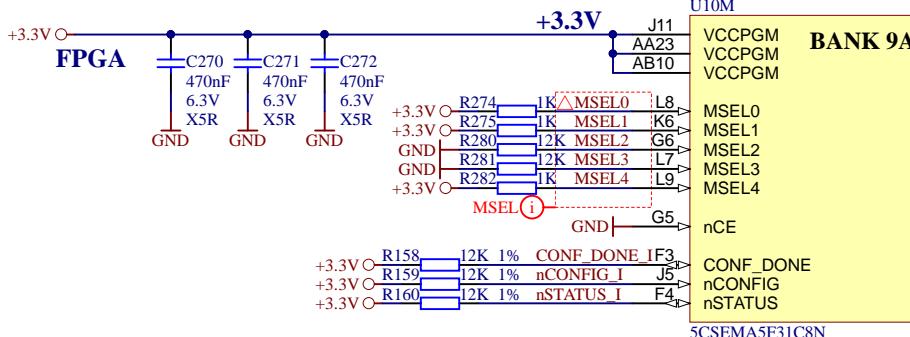
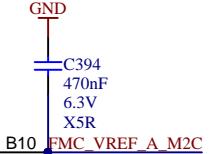
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5CSEMA5F31C8N

**BANK 8A**

IO, CLK7p, (DIFFIO_RX_T1p, DIFFOUT_T1p)	H15 CLK1_M2C_P	RX
IO, CLK7n, (DIFFIO_RX_T1n, DIFFOUT_T1n)	G15 CLK1_M2C_N	RX
IO, (DIFFIO_TX_T2p, DIFFOUT_T2p, DQ1T)	B13 LA04_P	TX
IO, (DIFFIO_RX_T2n, DIFFOUT_T2n, DQ4T, DQ2T)	A13 LA04_N	TX
IO, (DIFFIO_RX_T3p, DIFFOUT_T3p, DQ1T)	C13 LA00_CC_P	RX
IO, (DIFFIO_RX_T3n, DIFFOUT_T3n, DQ1T)	B12 LA00_CC_N	RX
IO, (DIFFIO_TX_T4p, DIFFOUT_T4p, DQ1T)	A11 LA02_P	TX
IO, (DIFFIO_RX_T4n, DIFFOUT_T4n, DQ1T)	A10 LA02_N	TX
IO, (DIFFIO_RX_T5p, DIFFOUT_T5p, DQS1T)	F15 LA01_CC_P	RX
IO, (DIFFIO_RX_T5n, DIFFOUT_T5n, DQSn1T)	F14 LA01_CC_N	RX
IO, (DIFFIO_TX_T6p, DIFFOUT_T6p)	C12 LA06_P	TX
IO, (DIFFIO_RX_T6n, DIFFOUT_T6n, DQ1T)	B11 LA06_N	TX
IO, (DIFFIO_RX_T7p, DIFFOUT_T7p, DQ1T)	D11 LA21_P	RX
IO, (DIFFIO_RX_T7n, DIFFOUT_T7n, DQ1T)	D10 LA21_N	RX
IO, (DIFFIO_TX_T8p, DIFFOUT_T8p, DQ1T)	A9 LA12_P	TX
IO, (DIFFIO_RX_T8n, DIFFOUT_T8n)	A8 LA12_N	TX
IO, (DIFFIO_RX_T8p, DIFFOUT_T8p)	K14 CLK0_M2C_P	RX
IO, (DIFFIO_RX_T9n, DIFFOUT_T9n)	J14 CLK0_M2C_N	RX
IO, (DIFFIO_TX_T10p, DIFFOUT_T10p, DQ2T, DQ1T)	C7 LA16_P	TX
IO, (DIFFIO_RX_T10n, DIFFOUT_T10n, DQ2T, DQ1T)	B7 LA16_N	TX
IO, (DIFFIO_RX_T11p, DIFFOUT_T11p, DQ2T, DQ1T)	E9 LA09_P	RX
IO, (DIFFIO_RX_T11n, DIFFOUT_T11n, DQ2T, DQ1T)	D9 LA09_N	RX
IO, (DIFFIO_RX_T12p, DIFFOUT_T12p, DQ2T, DQ1T)	C8 LA14_P	TX
IO, (DIFFIO_RX_T12n, DIFFOUT_T12n, DQ2T, DQ1T)	B8 LA14_N	TX
IO, (DIFFIO_RX_T13p, DIFFOUT_T13p, DQS2T, DQS1T)	H14 LA15_P	RX
IO, (DIFFIO_RX_T13n, DIFFOUT_T13n, DQSn2T, DQSn1T)	G13 LA15_N	RX
IO, (DIFFIO_RX_T14p, DIFFOUT_T14p)	C10 LA08_P	TX
IO, (DIFFIO_RX_T14n, DIFFOUT_T14n, DQ2T, DQ1T)	C9 LA08_N	TX
IO, (DIFFIO_RX_T15p, DIFFOUT_T15p, DQ2T, DQ1T)	F13 LA17_CC_P	RX
IO, (DIFFIO_RX_T15n, DIFFOUT_T15n, DQ2T, DQ1T)	E13 LA17_CC_N	RX
IO, (DIFFIO_RX_T16p, DIFFOUT_T16p, DQ2T, DQ1T)	A6 LA20_P	TX
IO, (DIFFIO_RX_T16n, DIFFOUT_T16n)	A5 LA20_N	TX
IO, (DIFFIO_RX_T17p, DIFFOUT_T17p)	H8 LA25_P	TX
IO, (DIFFIO_RX_T17n, DIFFOUT_T17n)	G8 LA25_N	TX
IO, (DIFFIO_RX_T18p, DIFFOUT_T18p, DQ3T, DQ1T)	A4 LA26_P	TX
IO, (DIFFIO_RX_T18n, DIFFOUT_T18n, DQ3T, DQ1T)	E12 LA19_P	TX
IO, (DIFFIO_RX_T19p, DIFFOUT_T19p, DQ3T, DQ1T)	D12 LA19_N	RX
IO, (DIFFIO_RX_T19n, DIFFOUT_T19n, DQ3T, DQ1T)	D6 LA18_CC_P	TX
IO, (DIFFIO_RX_T20p, DIFFOUT_T20p, DQ3T, DQ1T)	C5 LA18_CC_N	TX



MSEL4 | MSEL3 | MSEL2 | MSEL1 | MSEL0 | Configuration Scheme

1		0		0		1		0	AS (x1 and x4) Fast
1		0		0		1		1	AS (x1 and x4) Standard



Title: **FPGA_Bank_8_9**

Number: **TEI0022.PrjPCB Default**

Rev. **01**

Date: **18.09.2018** Copyright: **Trenz Electronic GmbH**

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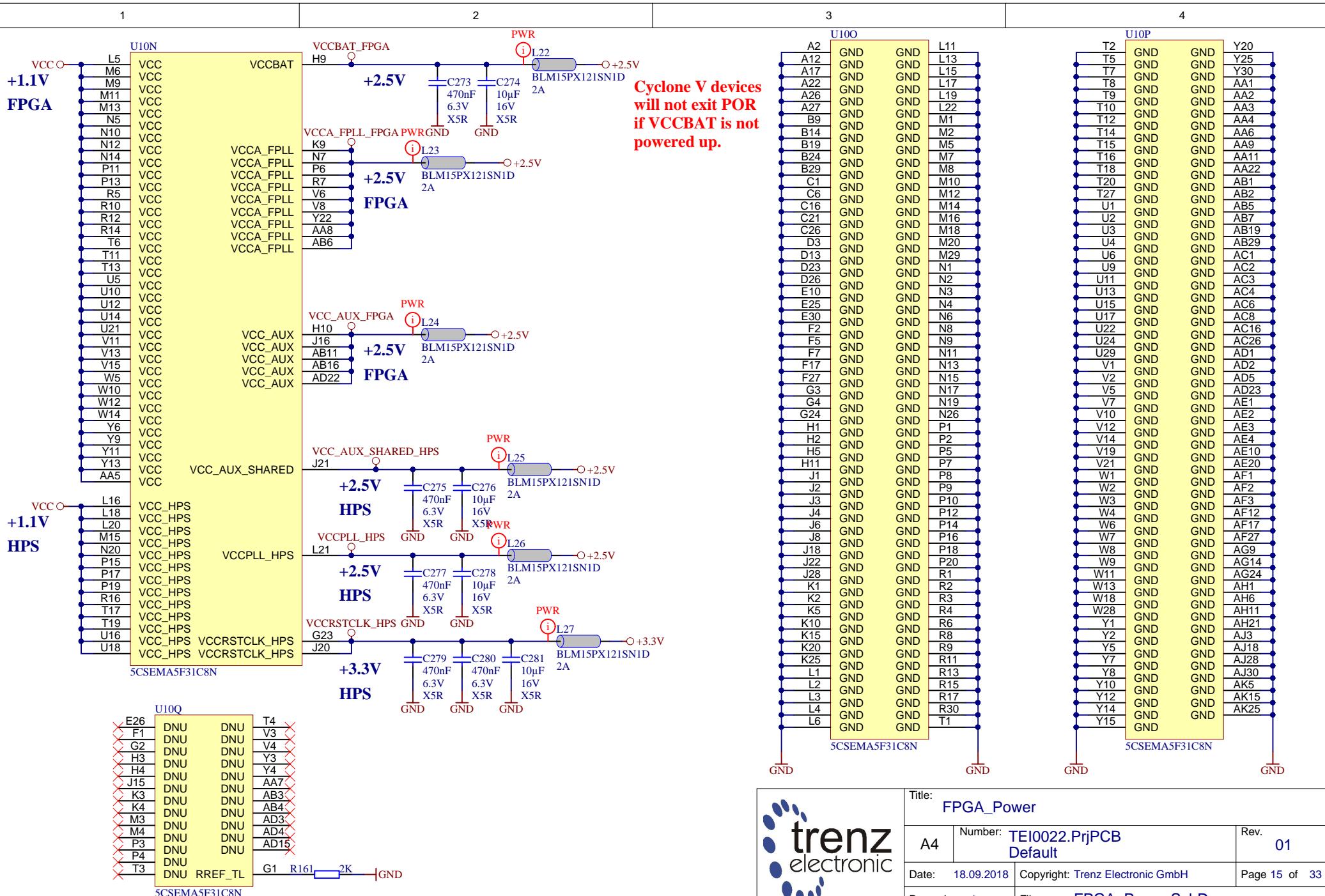
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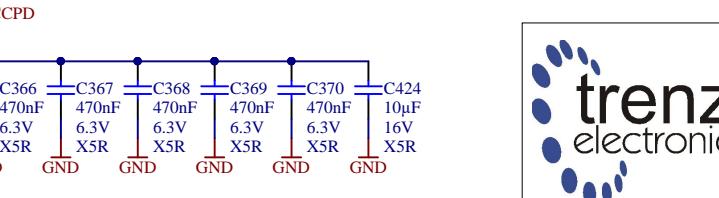
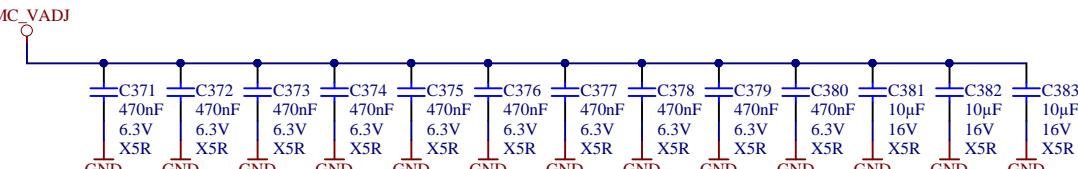
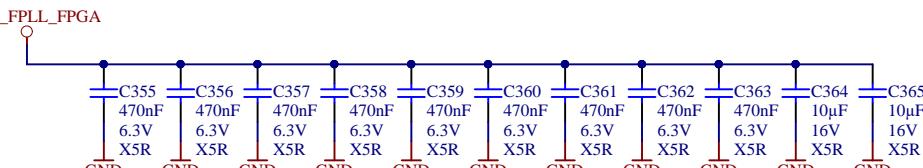
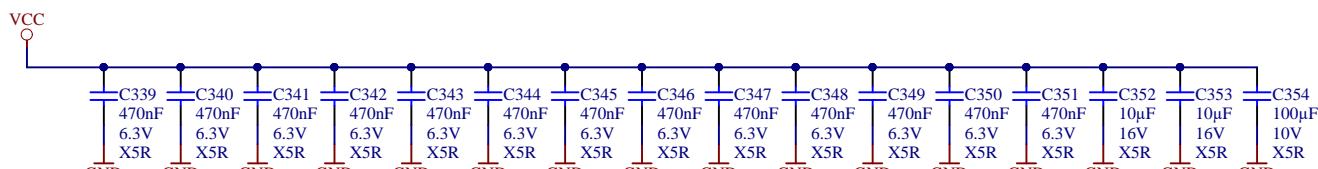
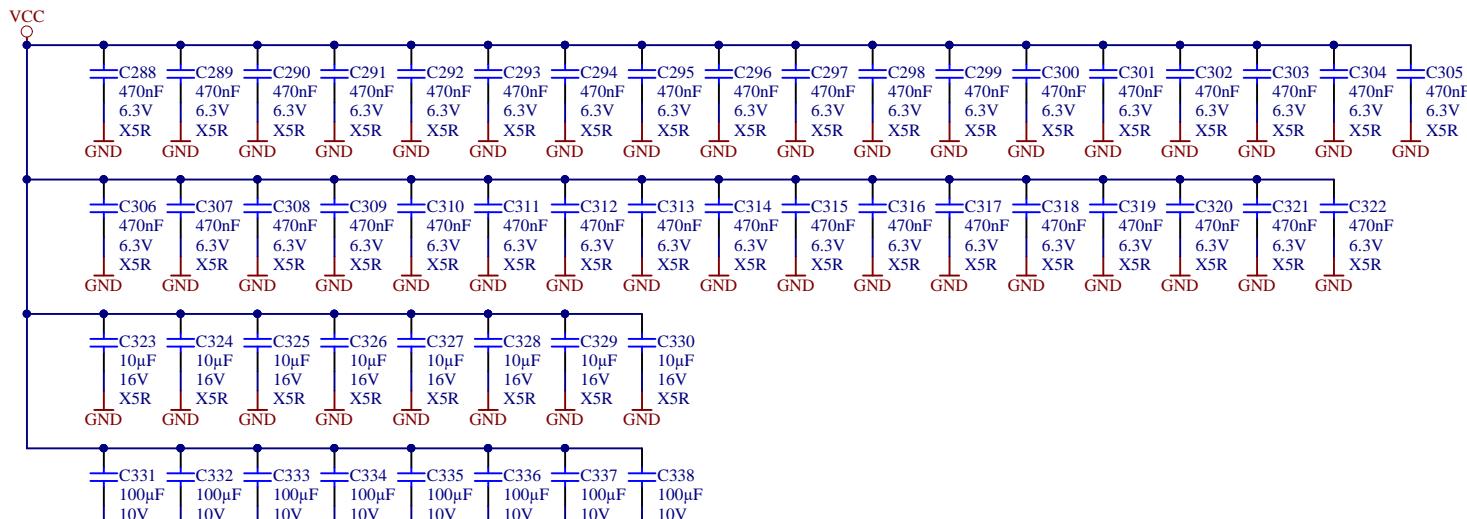
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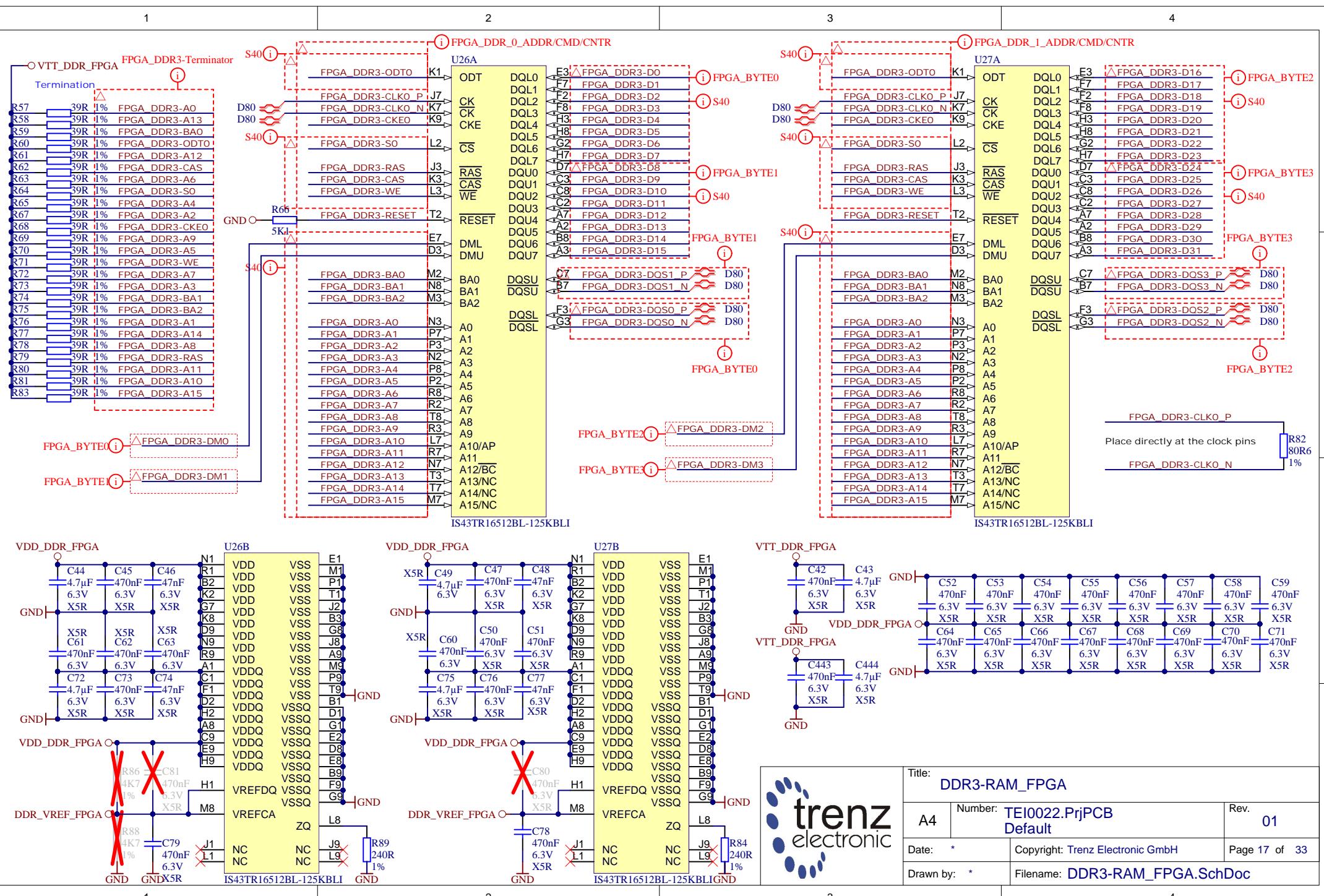
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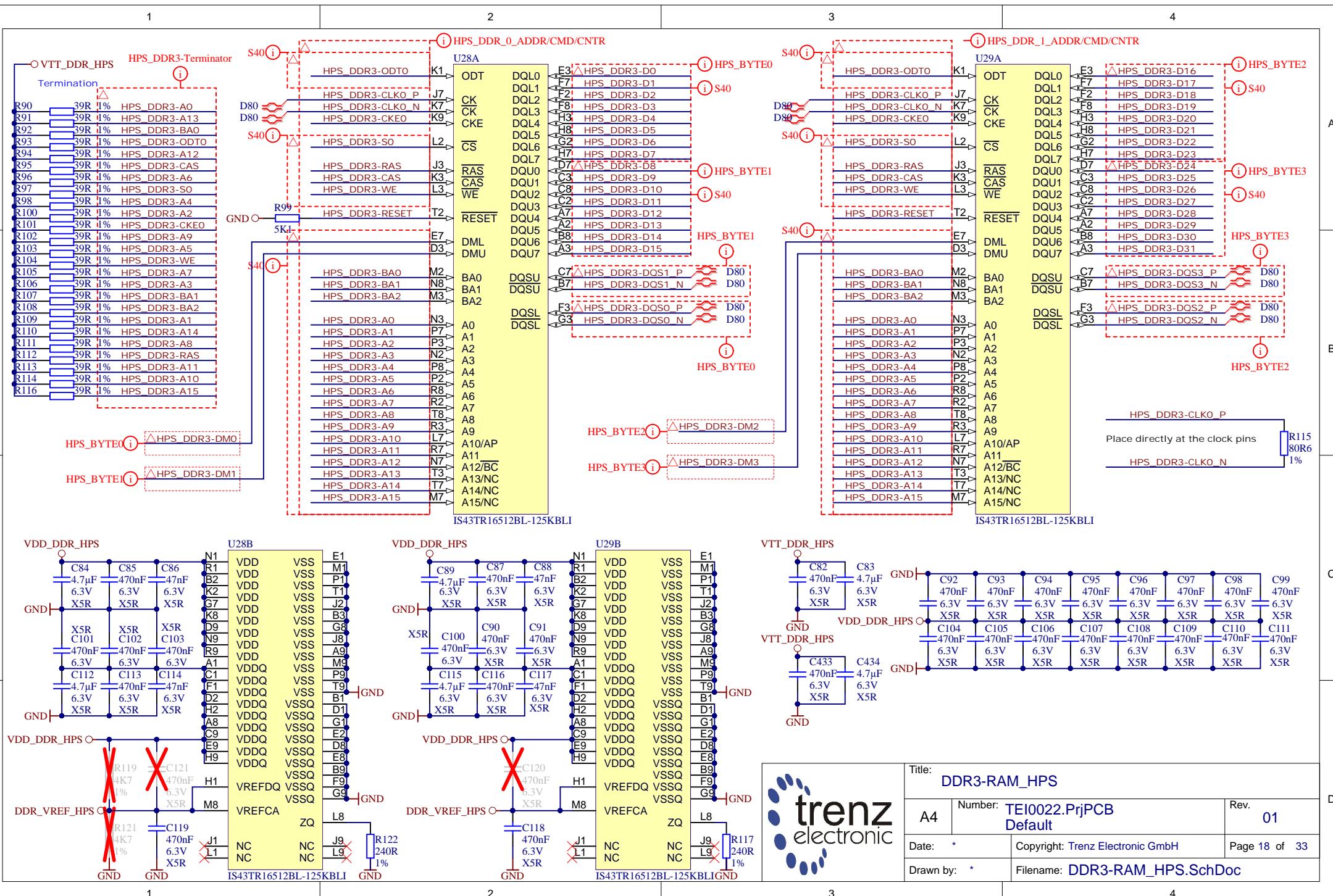
Rev. **01**

Date: **18.09.2018** Copyright: **Trenz Electronic GmbH**

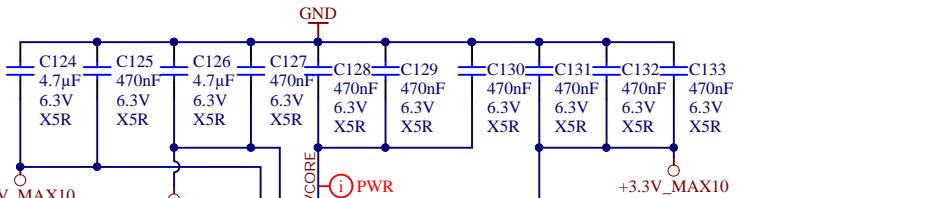
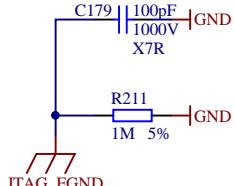
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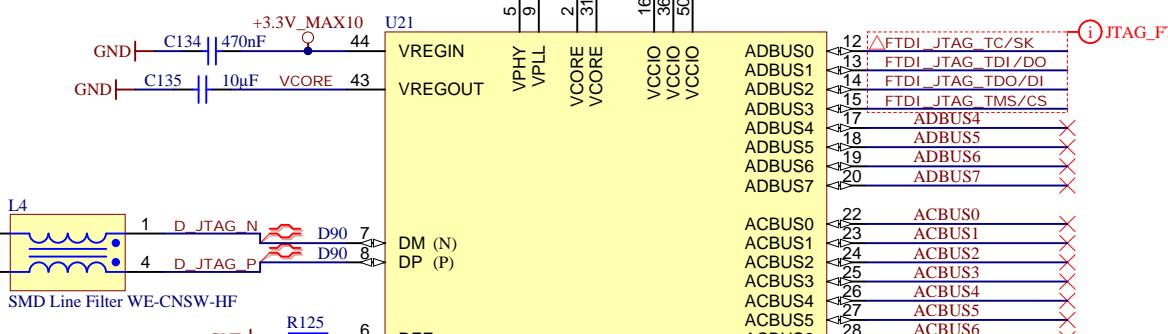
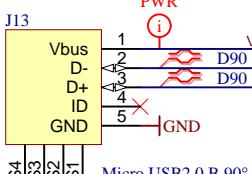




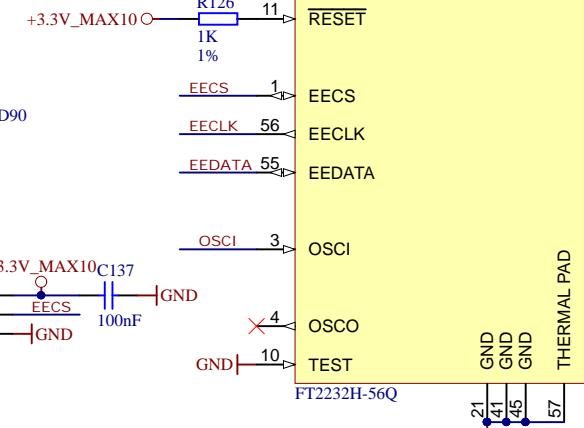
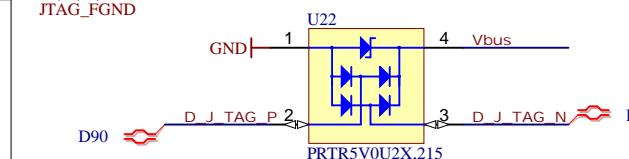
A



B



C



Title: FTDI_JTAG

A4 Number: TEI0022.PrjPCB Default

Rev. 01

Date: 2015-10-30 Copyright: Trenz Electronic GmbH

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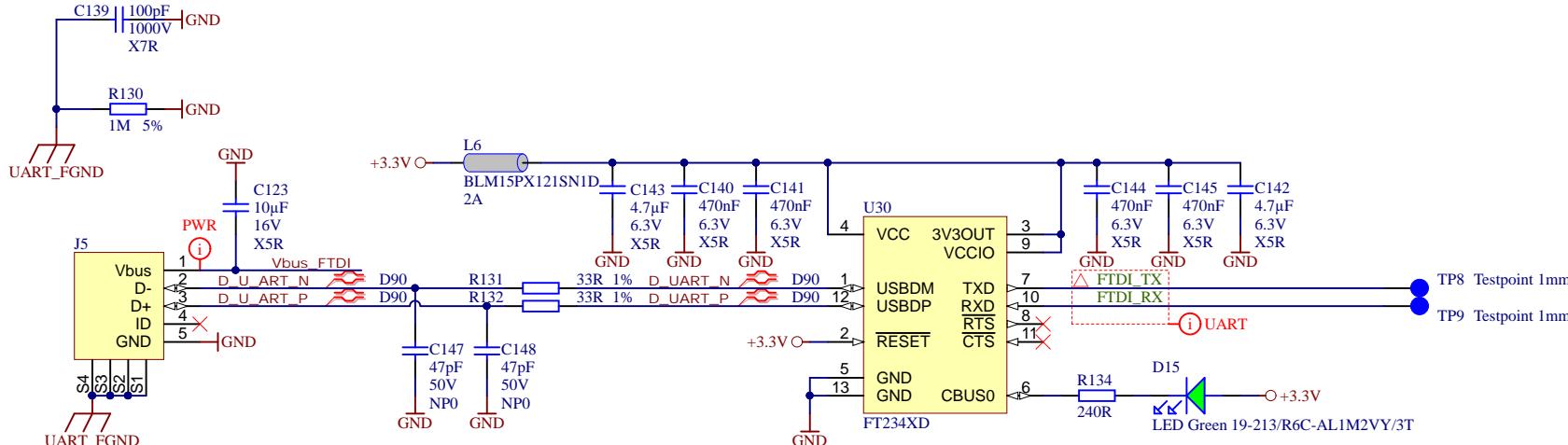
A

B

C

D

USB/UART Bridge



Title: FTDI_UART

A4 | Number: TEI0022.PrjPCB
Default

Rev.
01

Date: * Copyright: Trenz Electronic GmbH
Drawn by: * Filename: FTDI_UART.SchDoc

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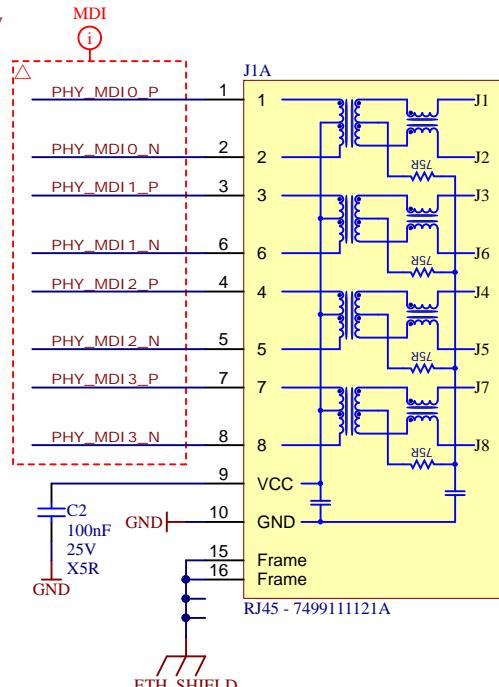
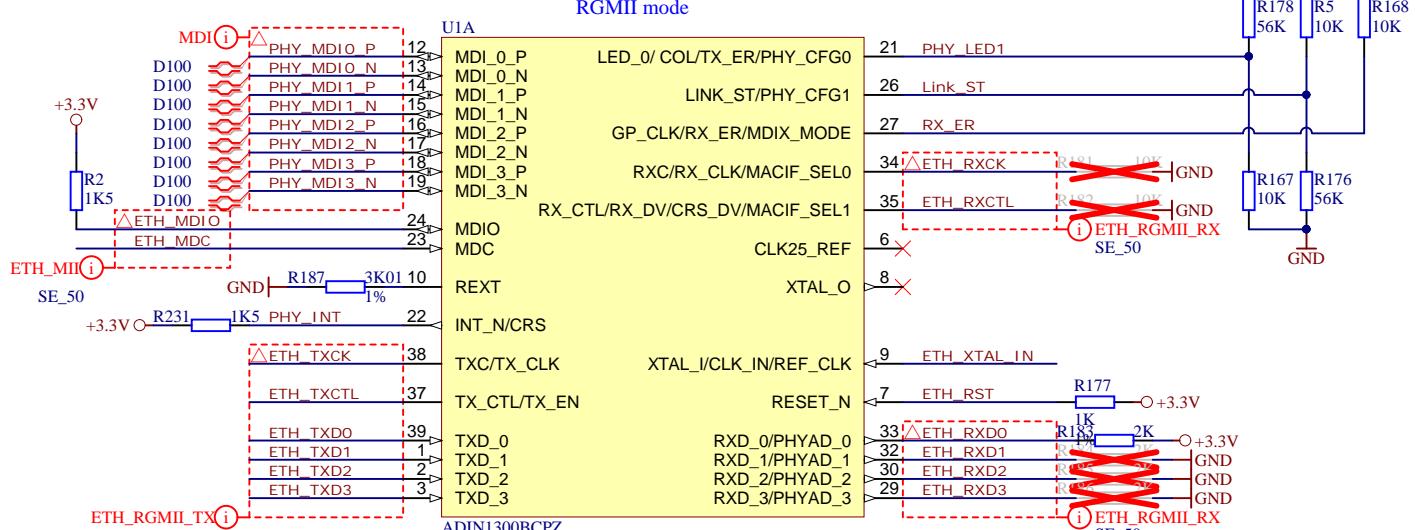
2

3

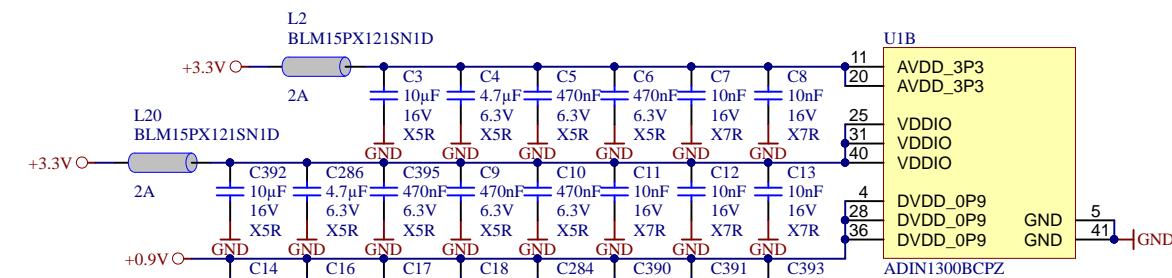
4

A

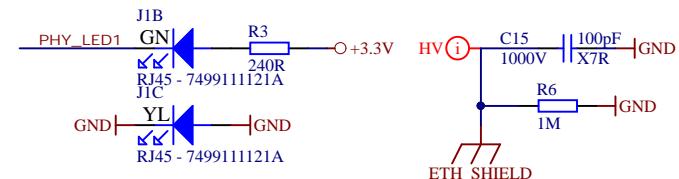
PHY Address: 0b0001
RGMII mode



C



D



Title: Ethernet

A4 Number: TEI0022.PrjPCB Default

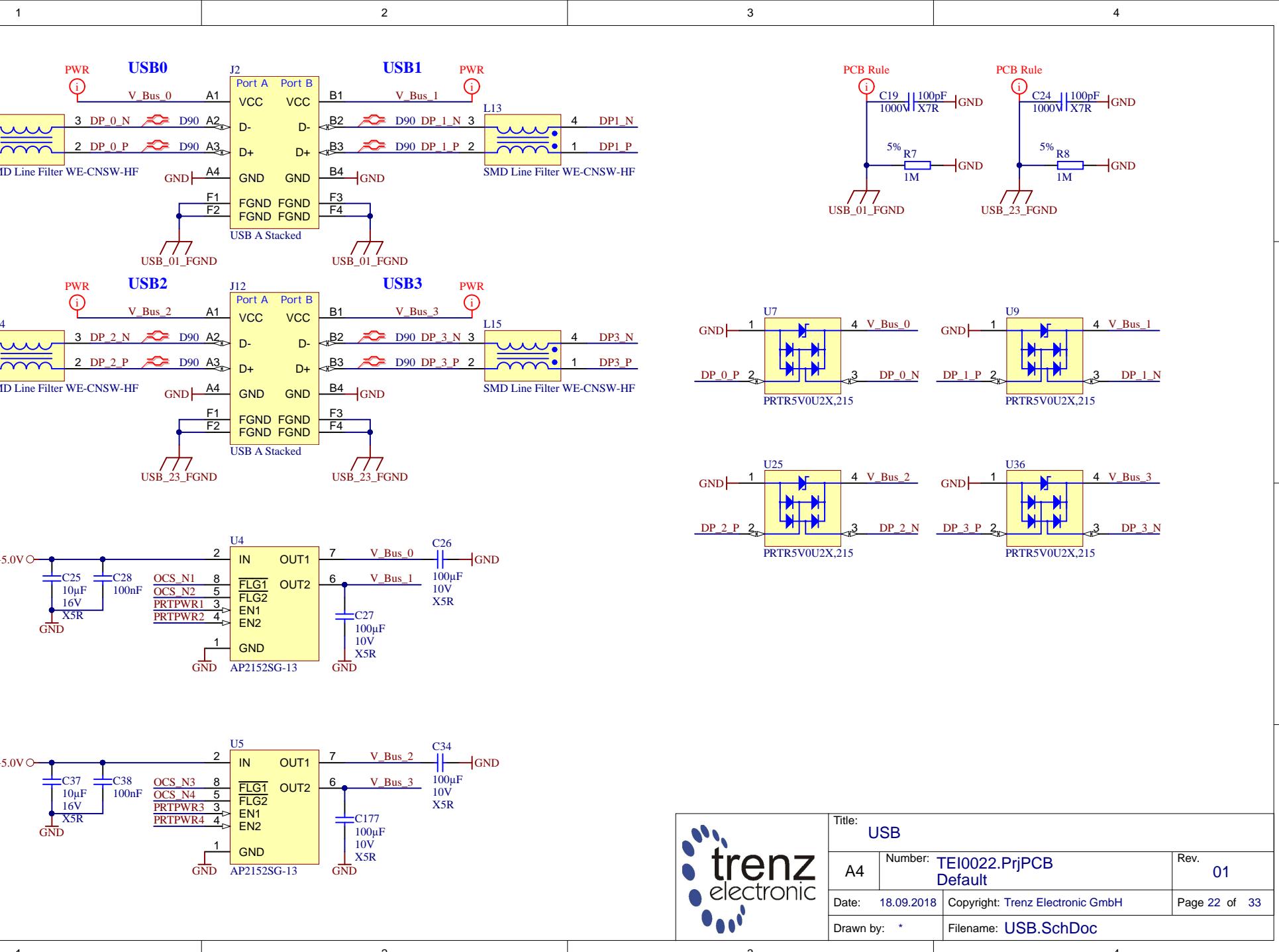
Rev. 01
Date: 18.09.2018 Copyright: Trenz Electronic GmbH
Drawn by: * File: Ethernet.SchDoc
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1

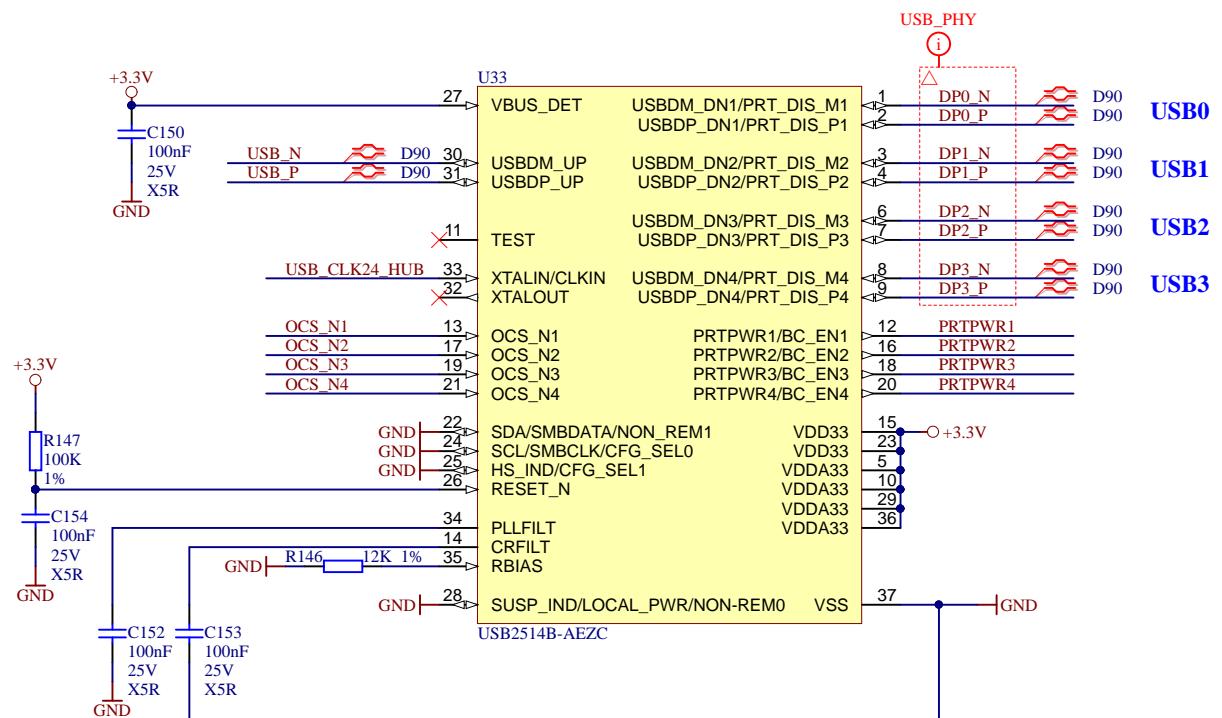
2

3

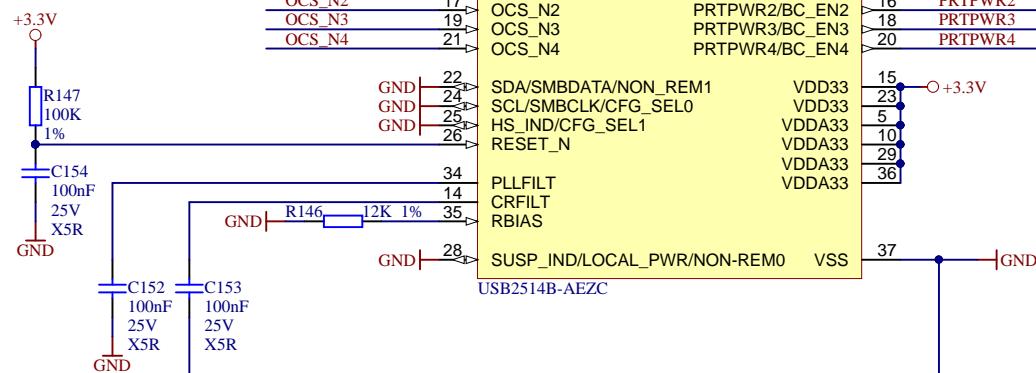
4



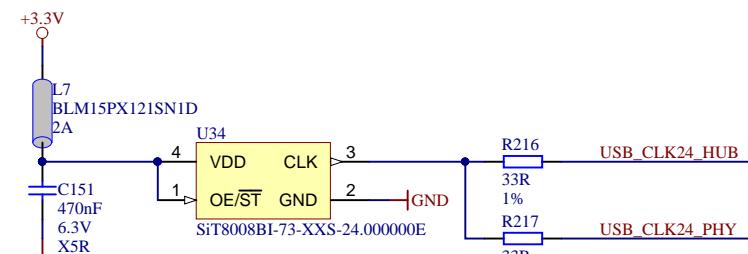
A



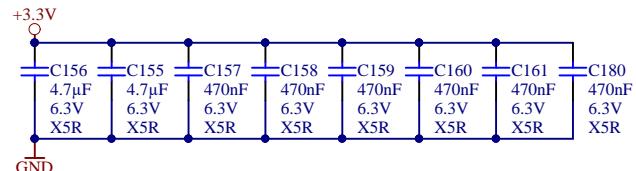
B



C



D



Title: USB-HUB

A4 | Number: TEI0022.PrjPCB
Default

Rev. 01

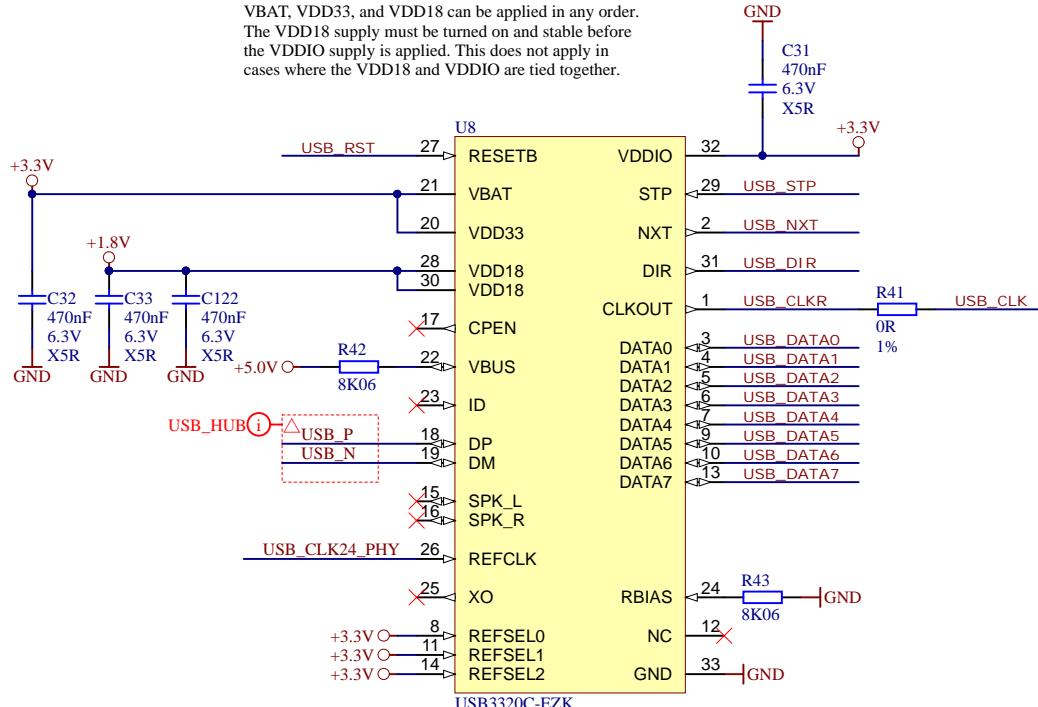
Date: * Copyright: Trenz Electronic GmbH
Drawn by: * Filename: USB-HUB.SchDoc

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A

A

VBAT, VDD33, and VDD18 can be applied in any order.
 The VDD18 supply must be turned on and stable before
 the VDDIO supply is applied. This does not apply in
 cases where the VDD18 and VDDIO are tied together.



B

B

C

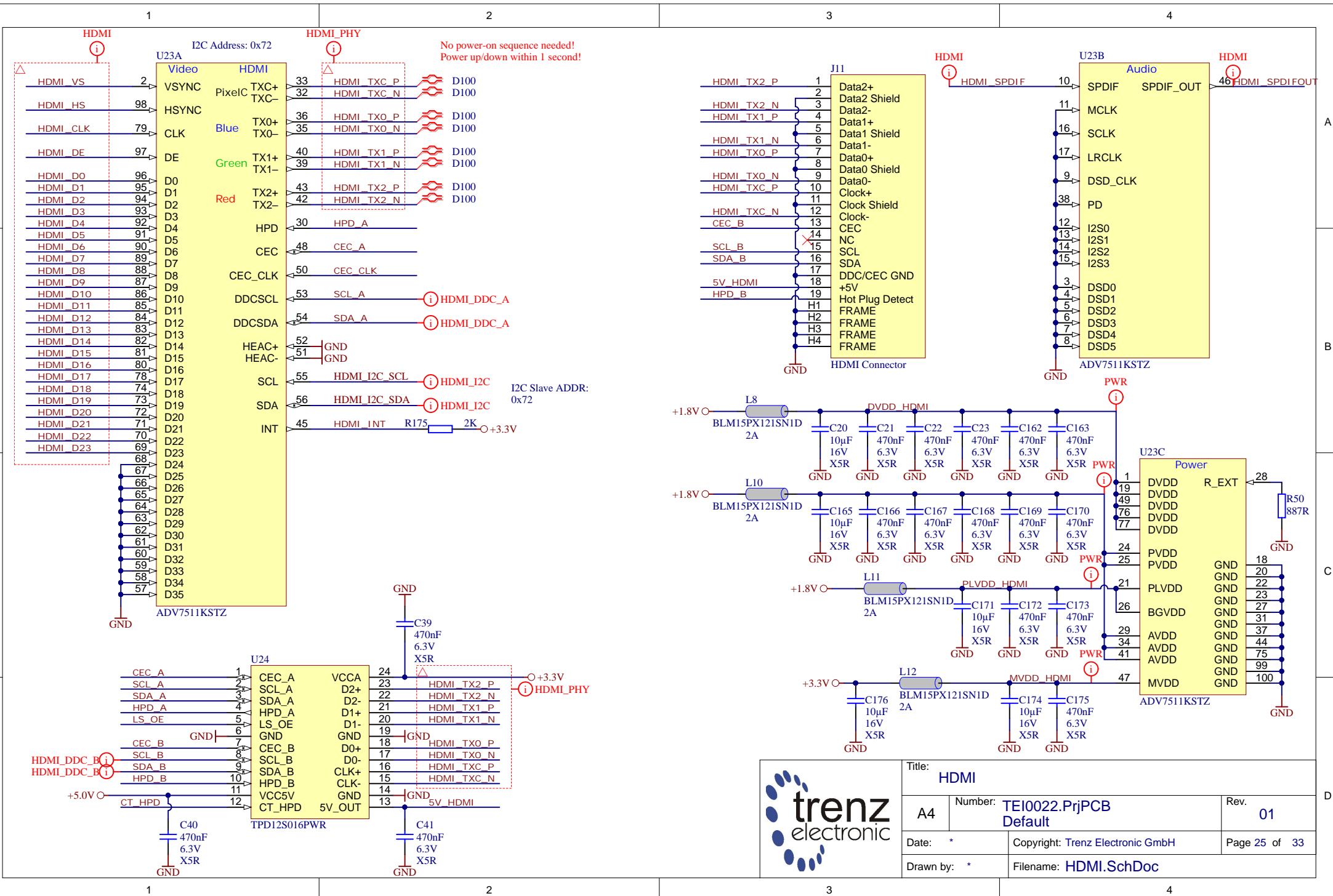
C

D

D

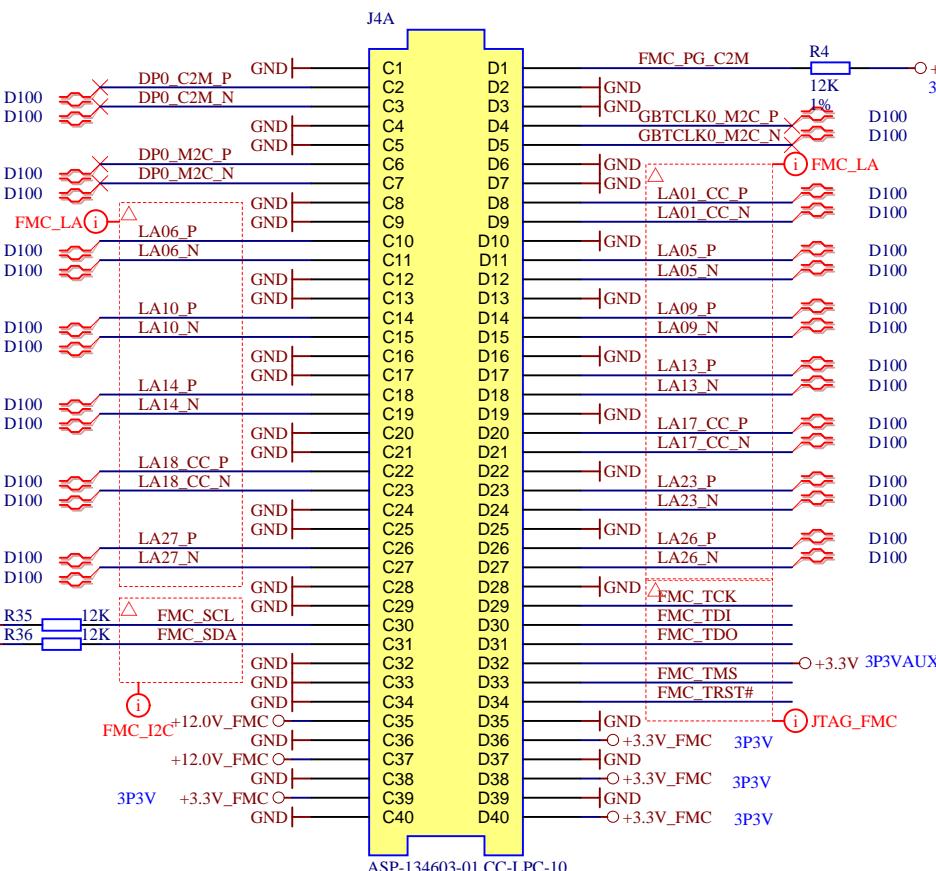


Title: USB-PHY		
A4	Number: TEI0022.PrjPCB Default	Rev. 01
Date: 18.09.2018	Copyright: Trenz Electronic GmbH	Page 24 of 33
Drawn by: *	Filename: USB-PHY.SchDoc	

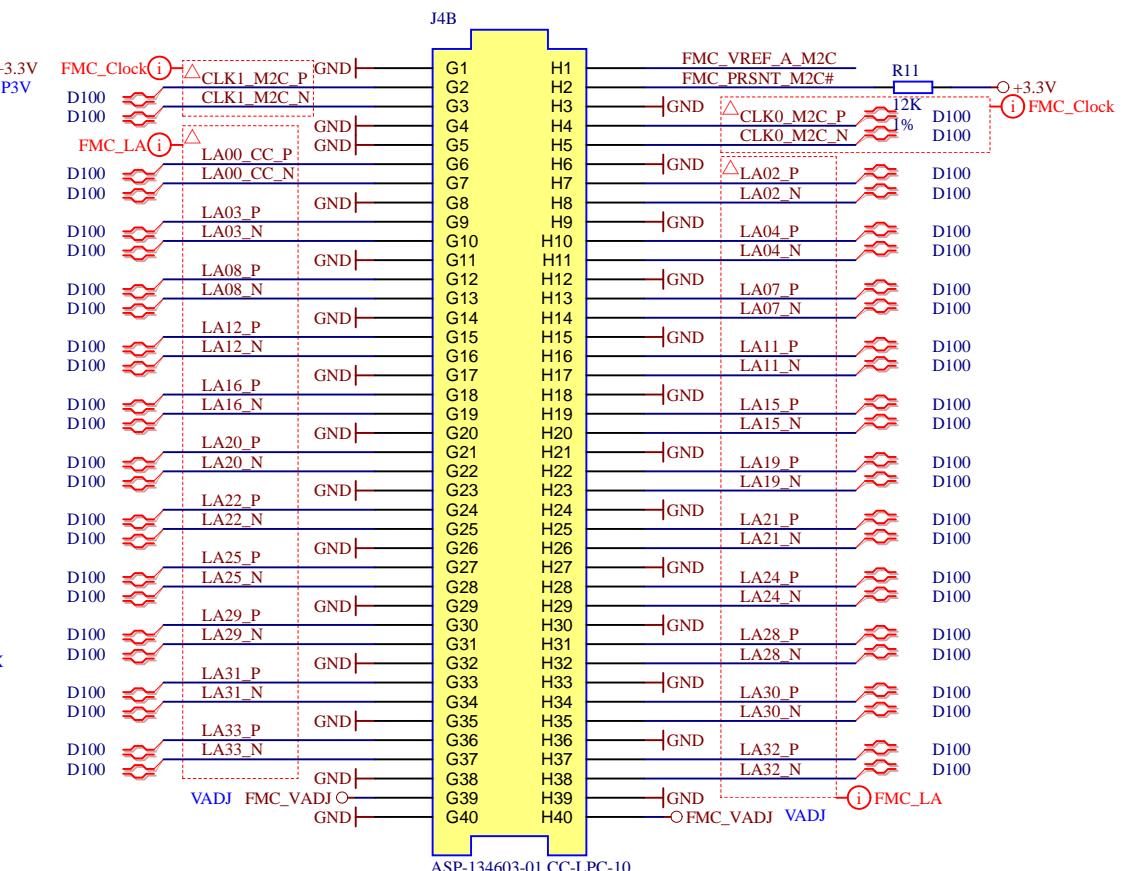


1 2 3 4

I2C Address: 0x50
Pin C34: GA[0]=0
Pin D35: GA[1]=0



FMC_VADJ	2 A	FMC_VADJ	FPGA
FMC_VREF_A_M2C	1 mA		
3P3VAUX	20 mA	+3.3 V	FPGA
3P3V	3 A	+3.3V_FMC	FPGA
+12.0V	1 A	+12.0V_FMC	



Title: FMC		
A4	Number: TEI0022.PrjPCB Default	Rev. 01
Date: 18.09.2018	Copyright: Trenz Electronic GmbH	Page 26 of 33
Drawn by: *	Filename: FMC.SchDoc	

1 2 3 4

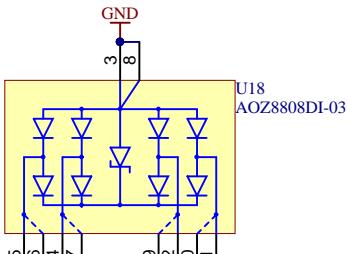
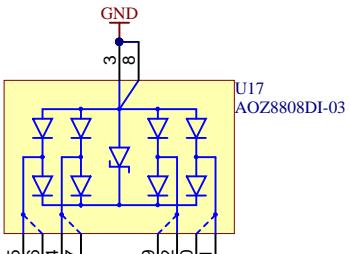
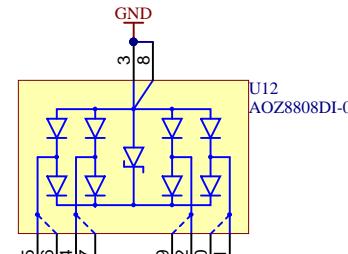
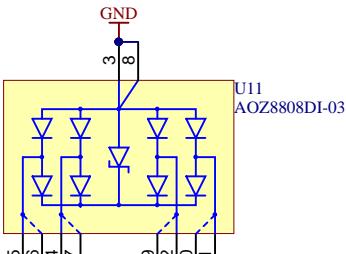
1

2

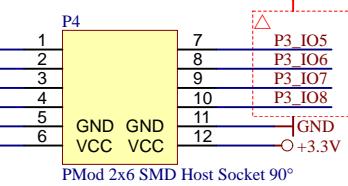
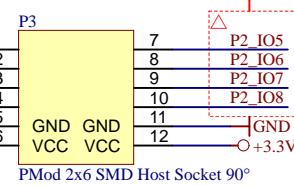
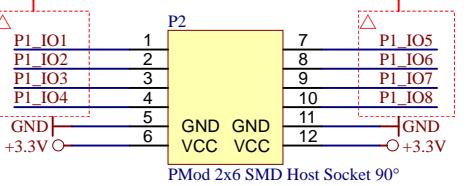
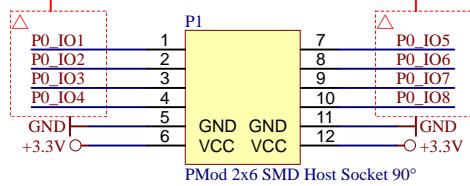
3

4

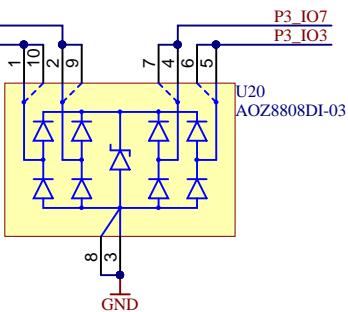
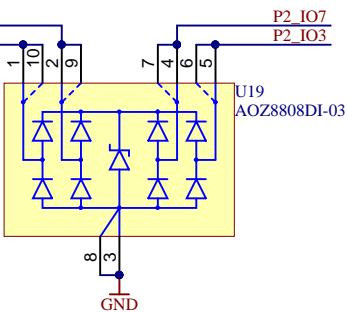
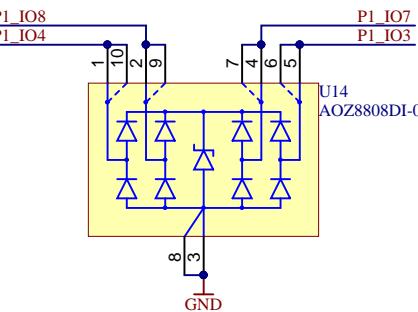
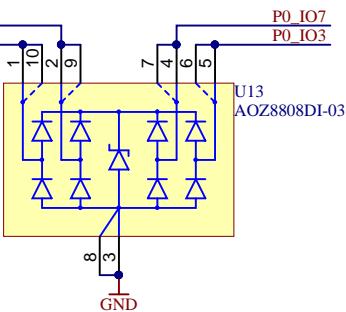
A



B



C



D



Title: PMOD	
A4	Number: TEI0022.PrjPCB Default
Date: 2017-11-21	Copyright: Trenz Electronic GmbH
Drawn by:	Page 27 of 33
	Filename: PMOD.SchDoc

1

2

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4

A

B

C

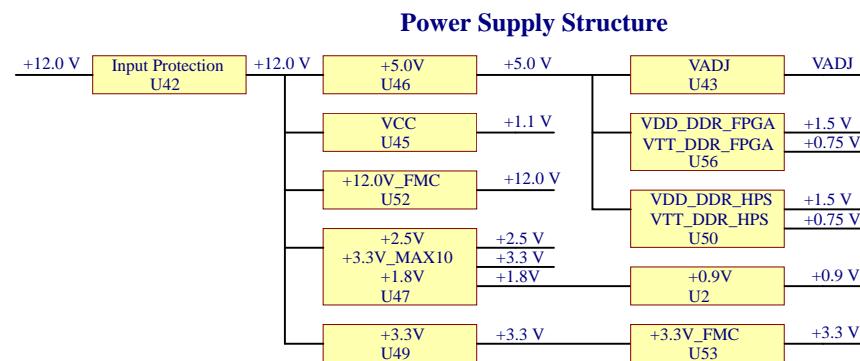
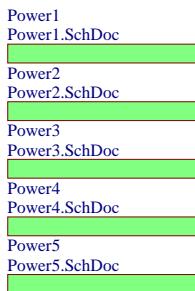
D

1

2

3

4



A

B

B

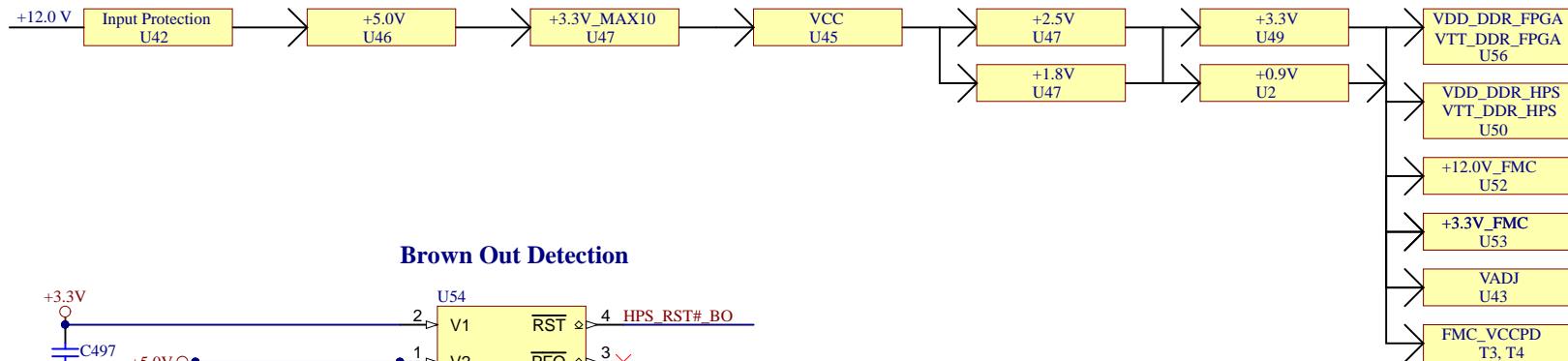
C

C

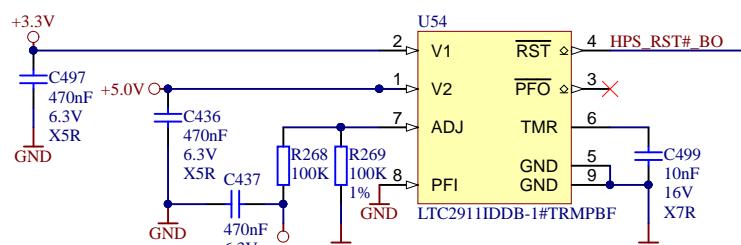
D

D

Power Supply Sequencing



Brown Out Detection



Title: TEB0911

A4 Number: TEI0022.PrjPCB Default Rev. 04

Date: 18.09.2018 Copyright: Trenz Electronic GmbH

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Drawn by: * Filename: Power.SchDoc

1

2

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4

A

A

B

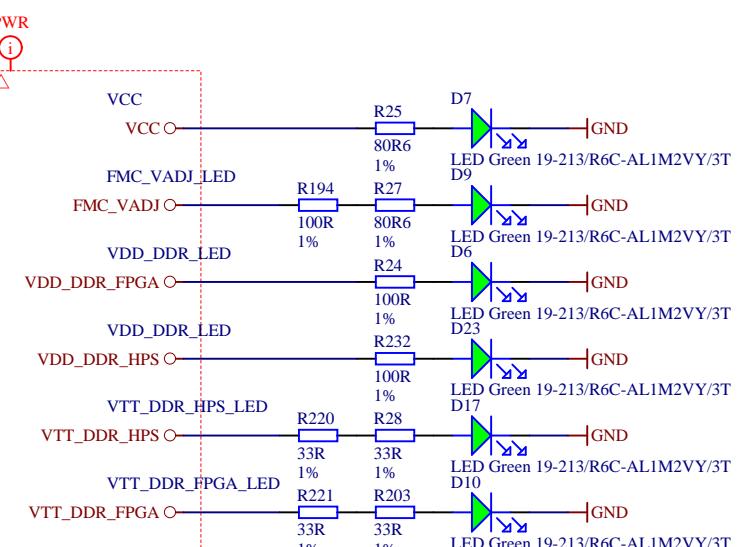
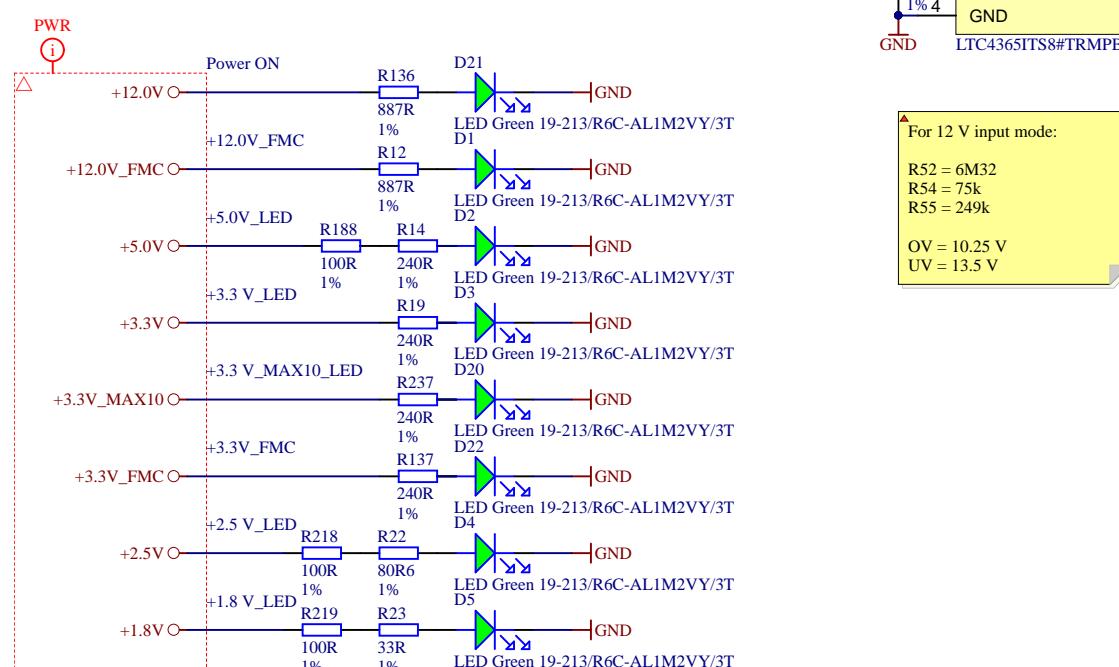
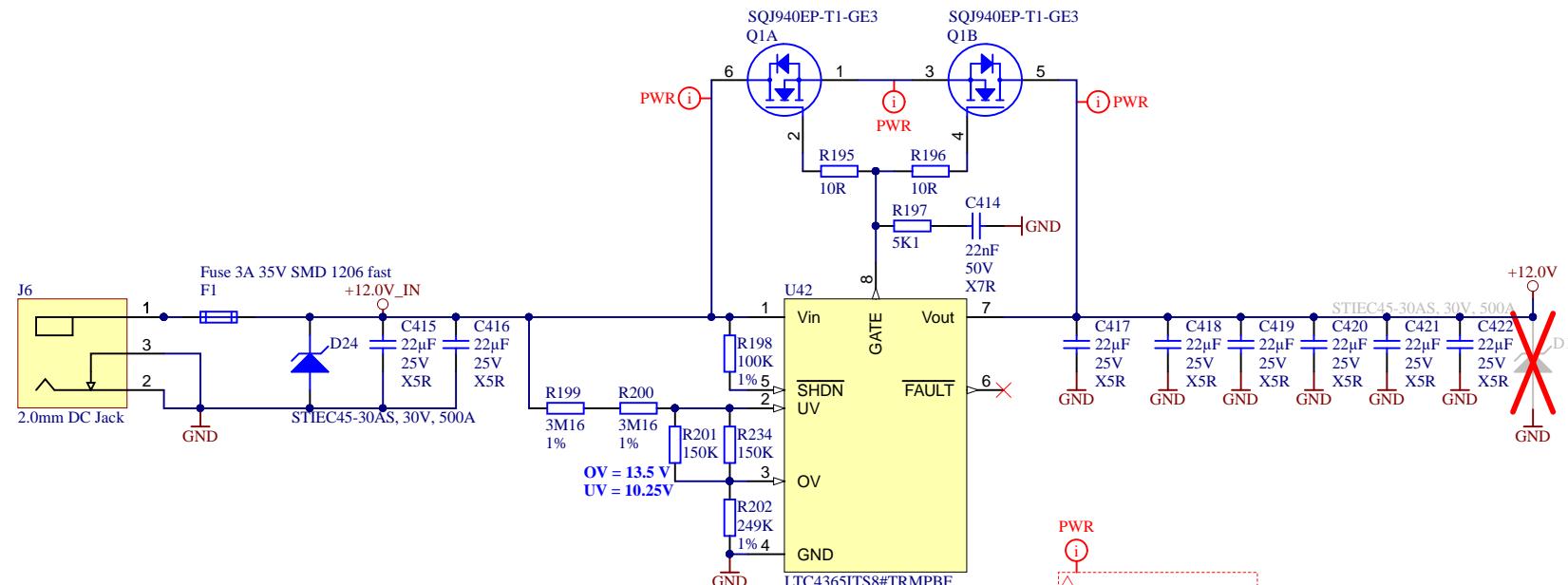
B

C

C

D

D



Title: Power1

A4 Number: TEI0022.PrjPCB Default

Rev. 01

Date: 18.09.2018 Copyright: Trenz Electronic GmbH

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Drawn by: * Filename: Power1.SchDoc

1

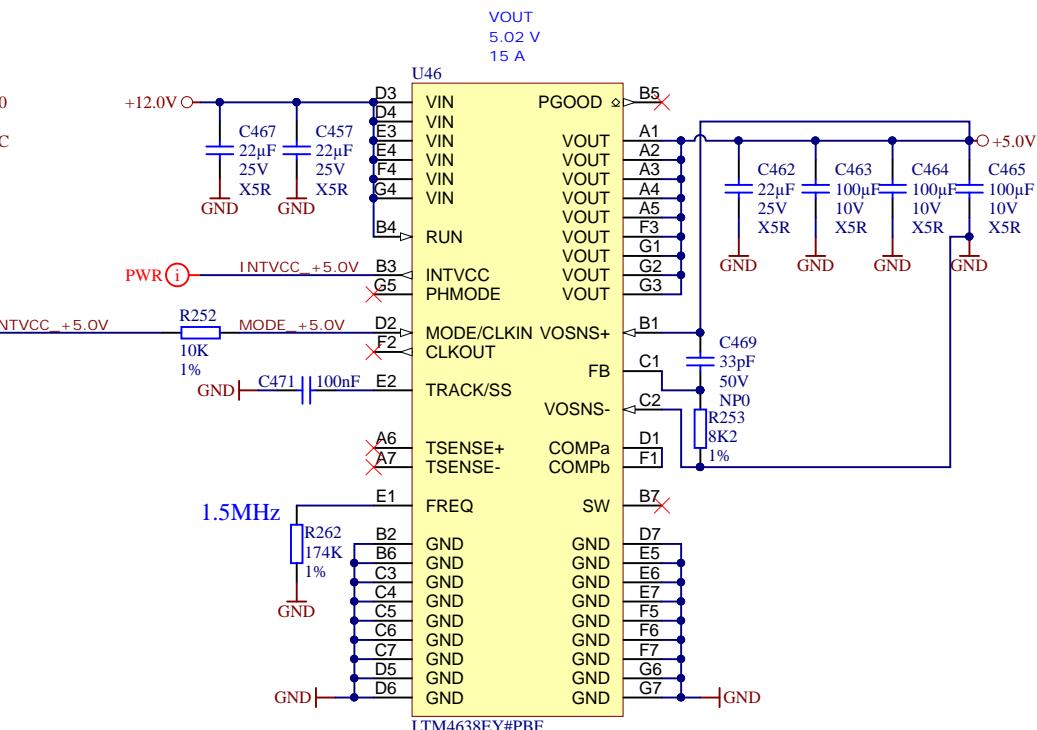
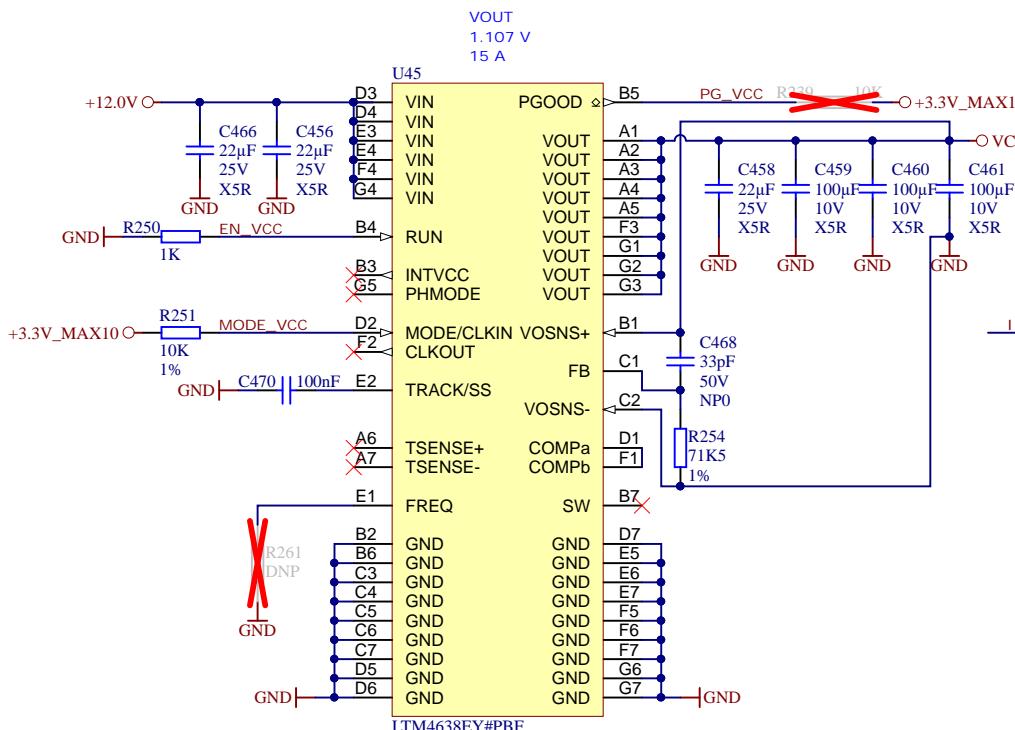
2

3

4

A

A



Title: Power2

A4 Number: TEI0022.PrjPCB
Default

Rev. 01

Date: 18.09.2018 Copyright: Trenz Electronic GmbH
Drawn by: * Filename: Power2.SchDoc

1

2

3

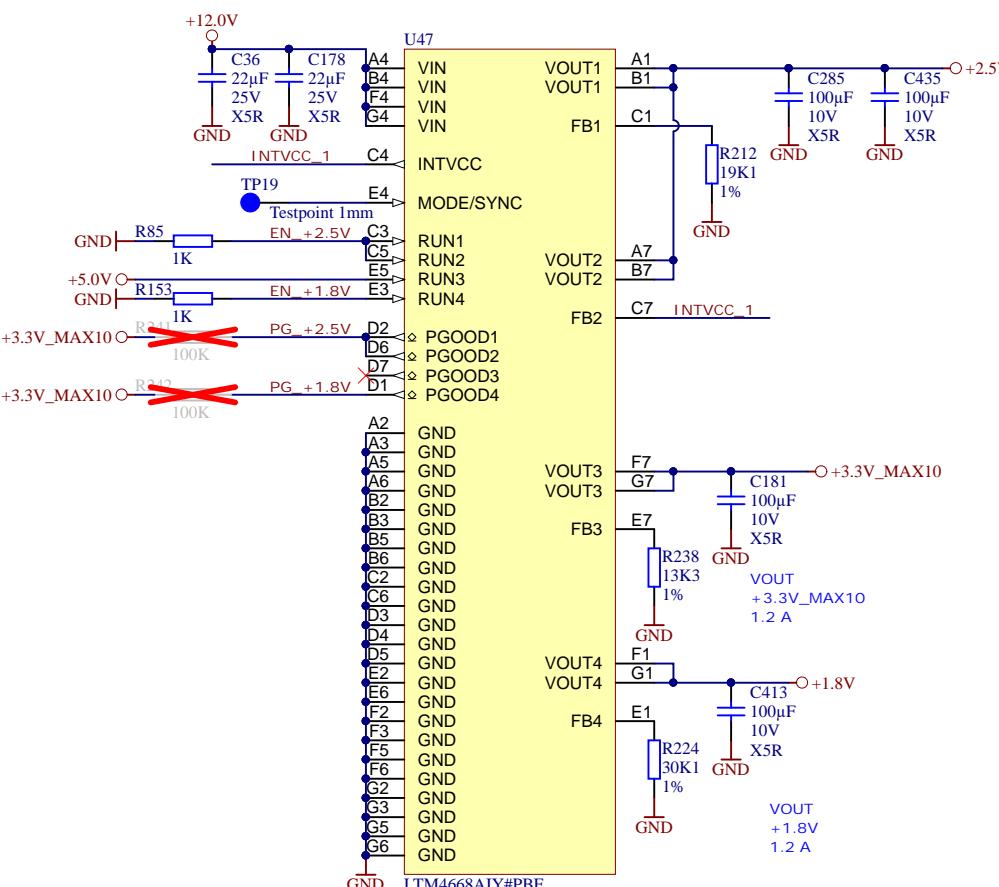
4

D

D

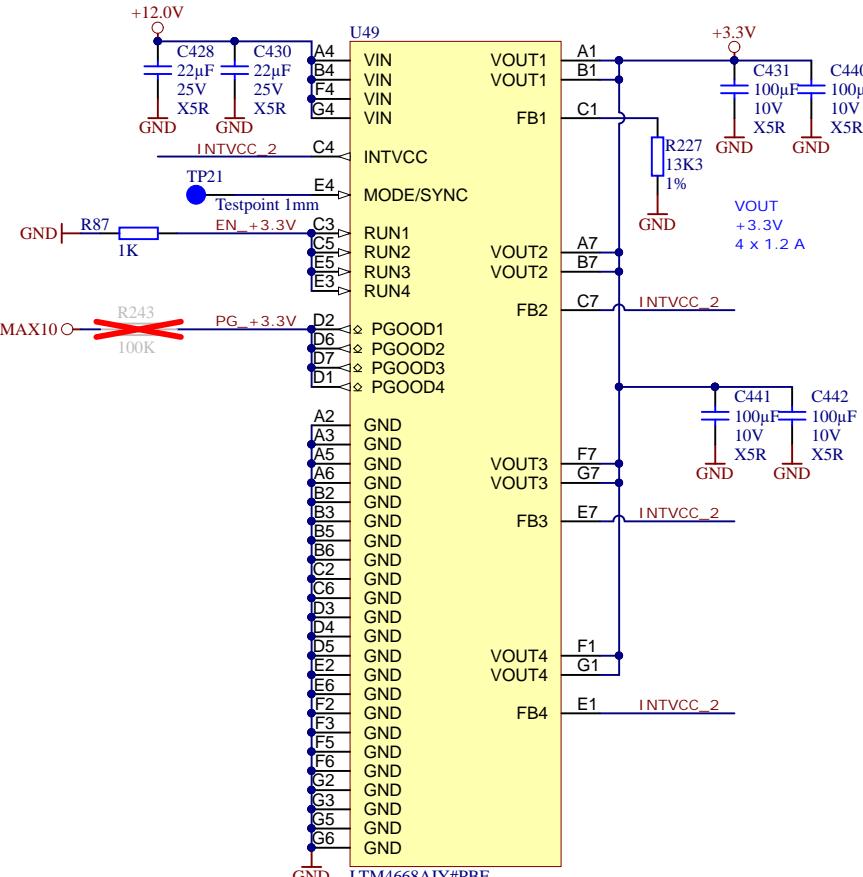
1 2 3 4

A



B

GND LTM4668AIY#PBF



C

1 2 3 4



Title: Power3

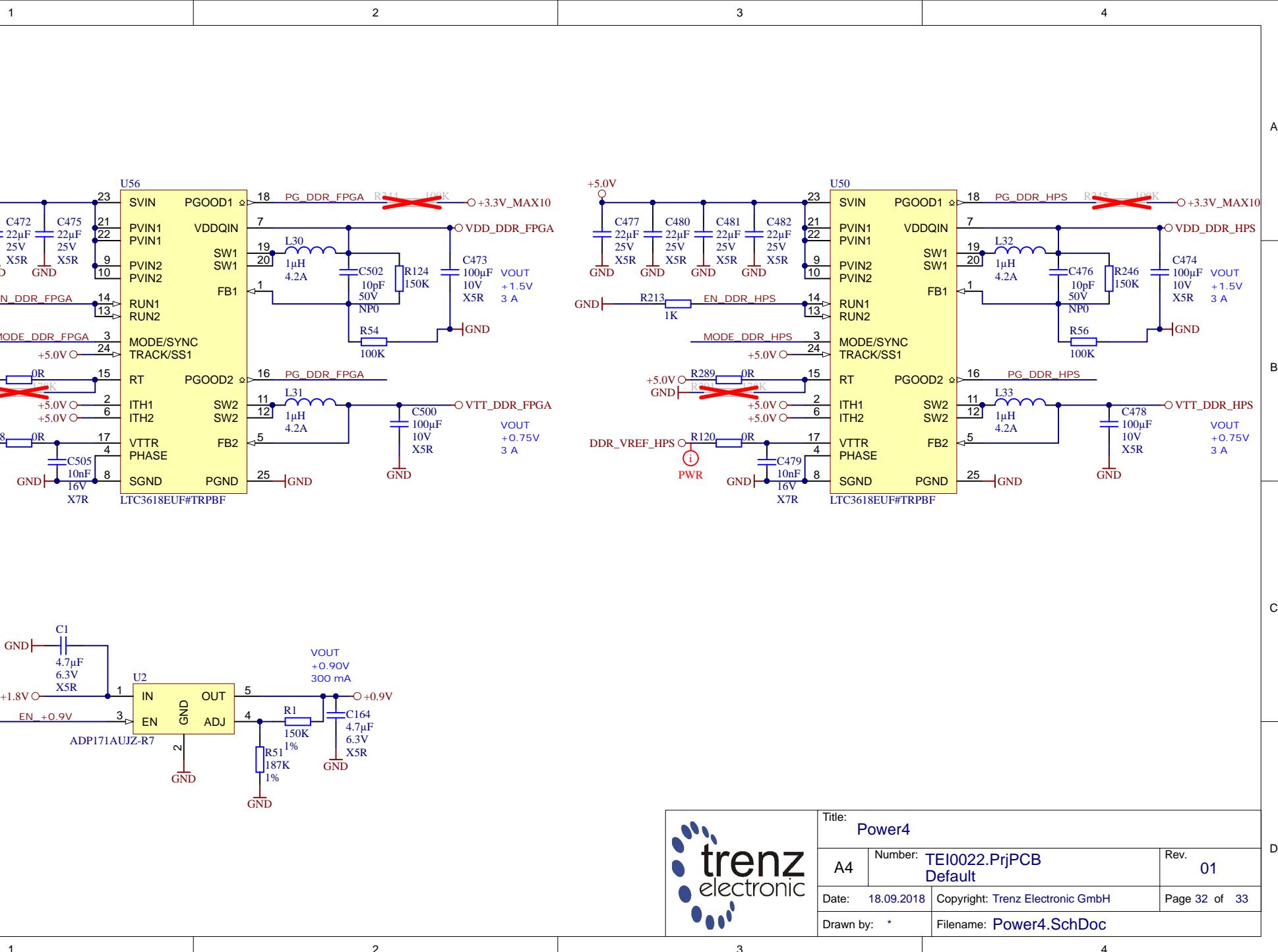
A4 Number: TEI0022.PrjPCB Default

Rev. 01

Date: 18.09.2018 Copyright: Trenz Electronic GmbH

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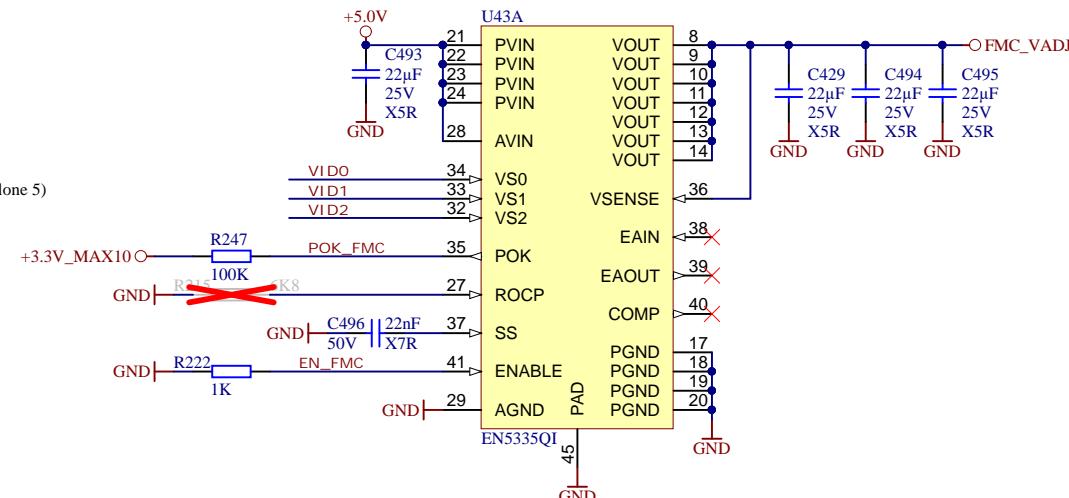
Drawn by: * Filename: Power3.SchDoc



1 2 3 4

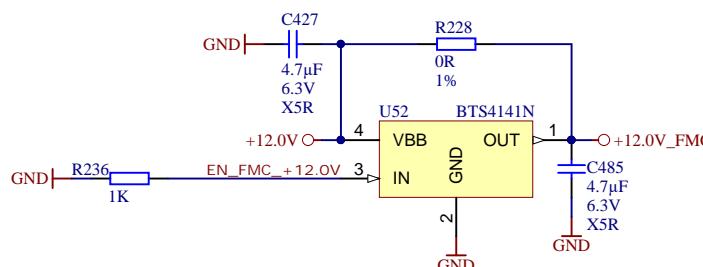
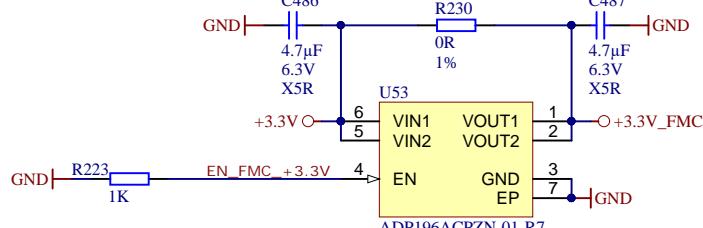
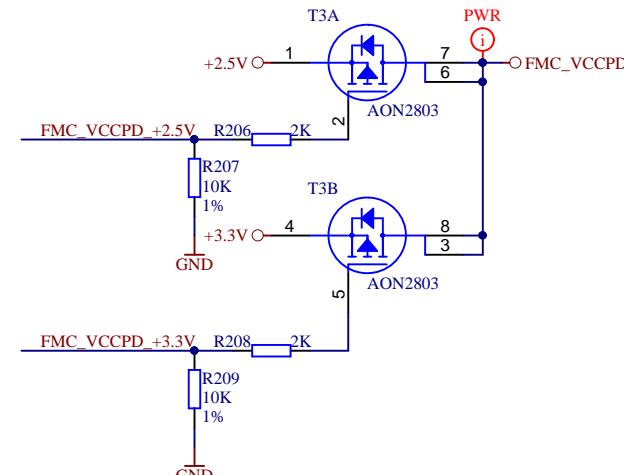
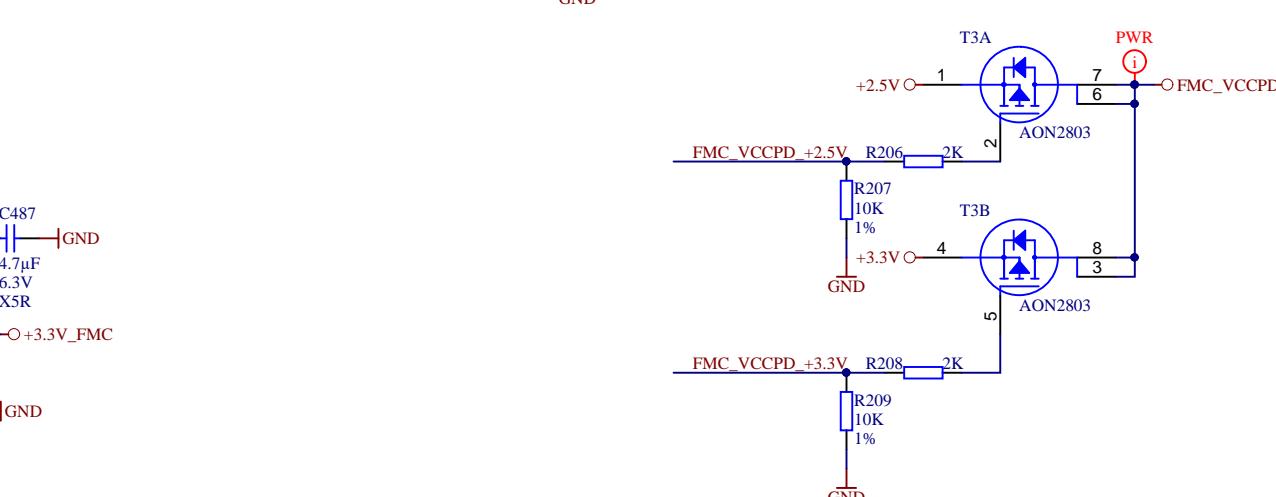
A VS2 | VS1 | VS0 | Output Voltage

0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V (not supported by Intel Cyclone 5)



1	NC
2	NC
3	NC
7	NC
16	NC
25	NC
26	NC
30	NC
31	NC
42	NC
43	NC
44	NC
4	NC(SW)
5	NC(SW)
6	NC(SW)
15	NC(SW)

EN5335QI



Title: Power5

A4 Number: TEI0022.PrjPCB
Default

Rev. 01

Date: 18.09.2018 Copyright: Trenz Electronic GmbH
Drawn by: * Filename: Power5.SchDoc

1 2 3 4