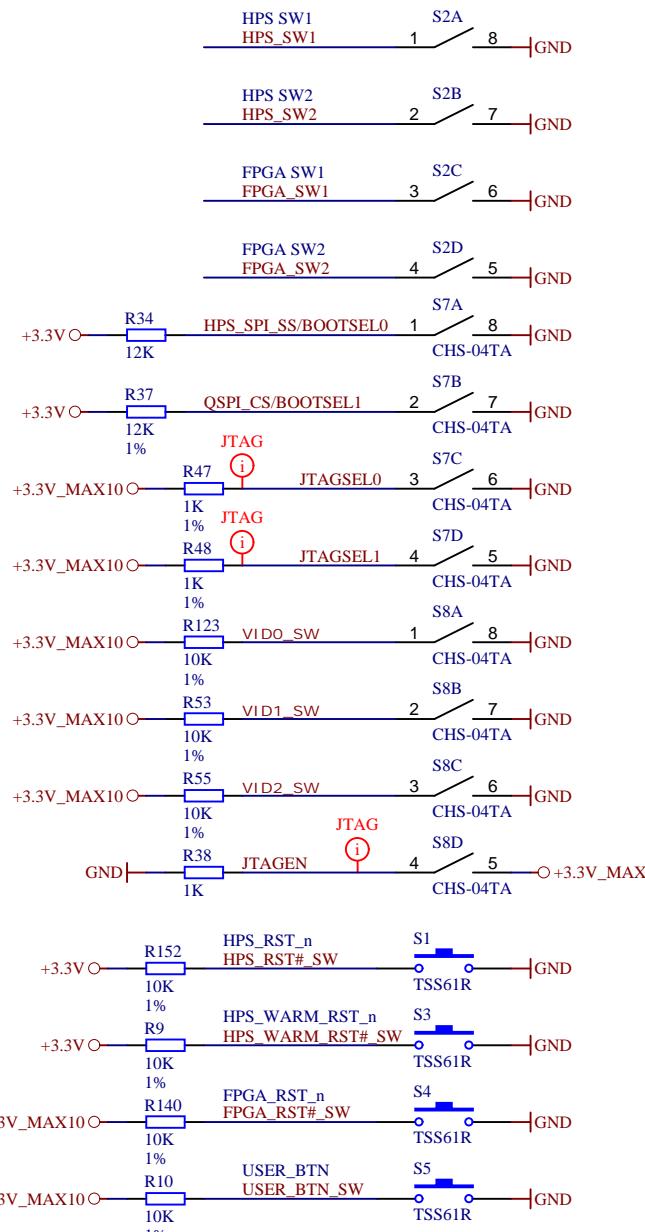


1 2 3 4

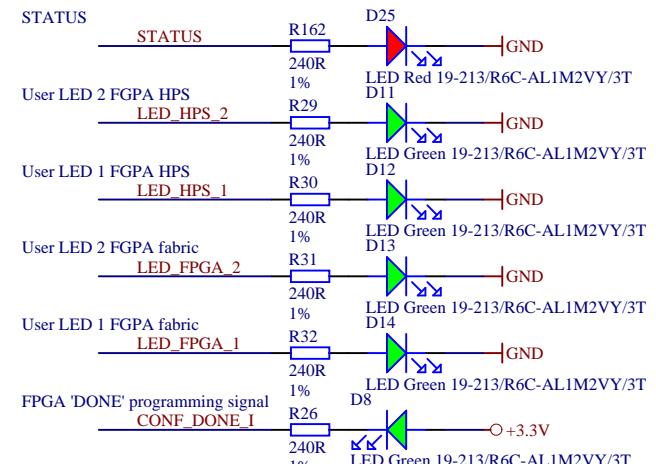
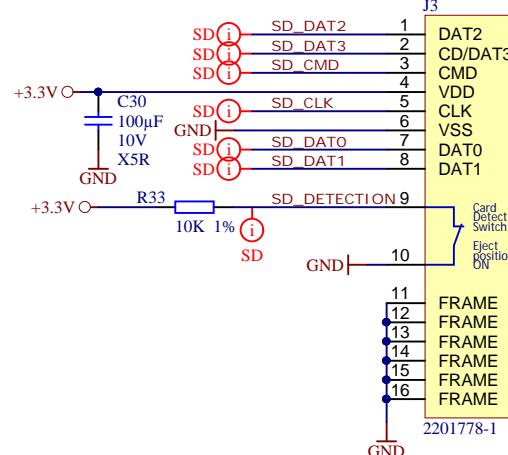


BOOTSEL0 | BOOTSEL1 | BOOTSEL2 | Boot Select

0		0		1		FPGA
1		0		1		SD/MMC (3.3V)
1		1		1		SPI(3.3V)

JTAGSEL0 | JTAGSEL1 | JTGEN | JTAG Selection

X		X		- (ON) MAX10
0 - (ON)		0 - (ON)		0 - (OFF) CYCLONE V HPS
0 - (ON)		1 - (OFF)		0 - (OFF) CYCLONE V FPGA
1 - (OFF)		0 - (ON)		0 - (OFF) FMC



Title: FrontPanel

A4 Number: TEI0022.PrjPCB Default

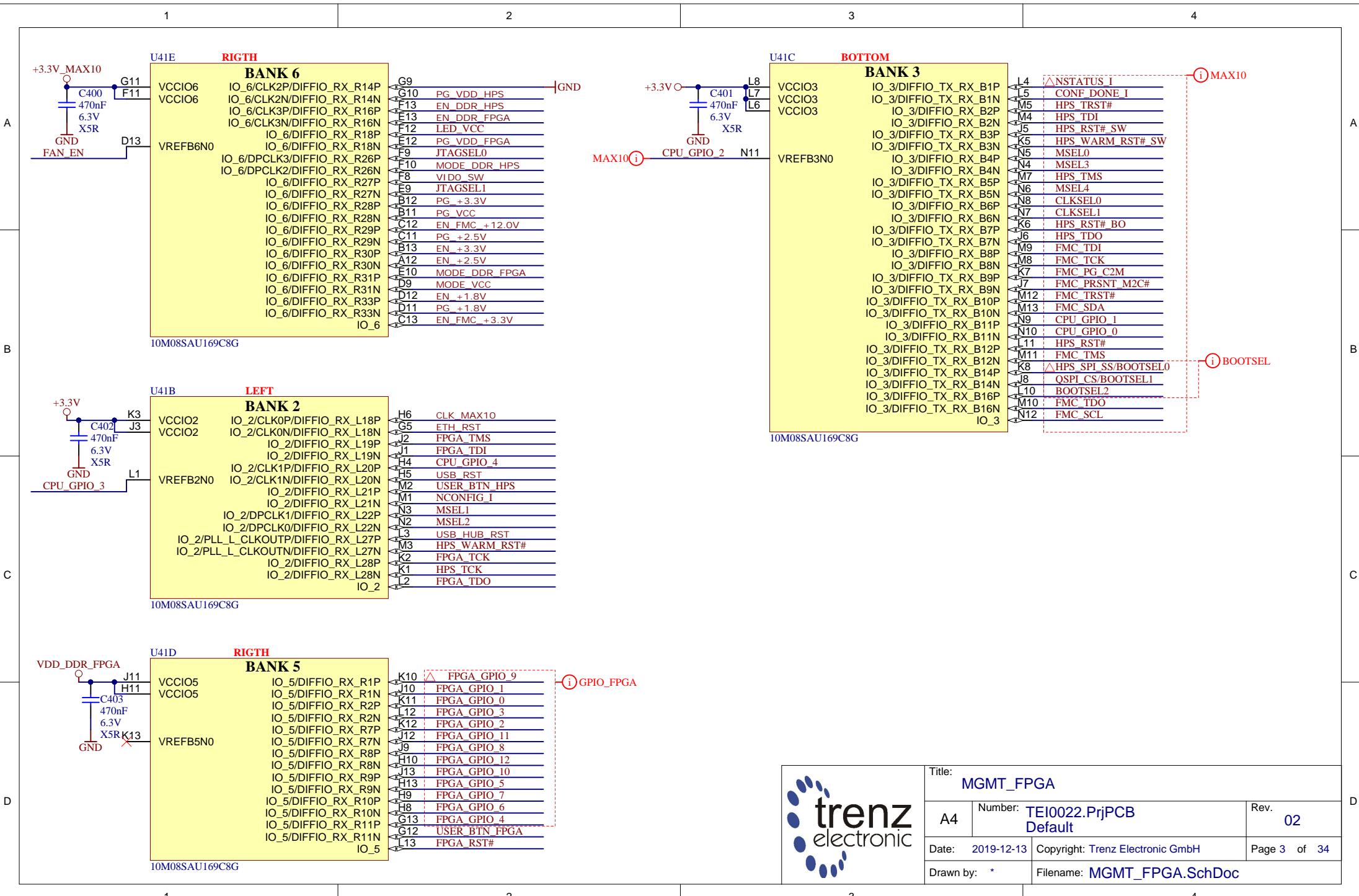
Rev. 02

Date: 2019-12-13 Copyright: Trenz Electronic GmbH

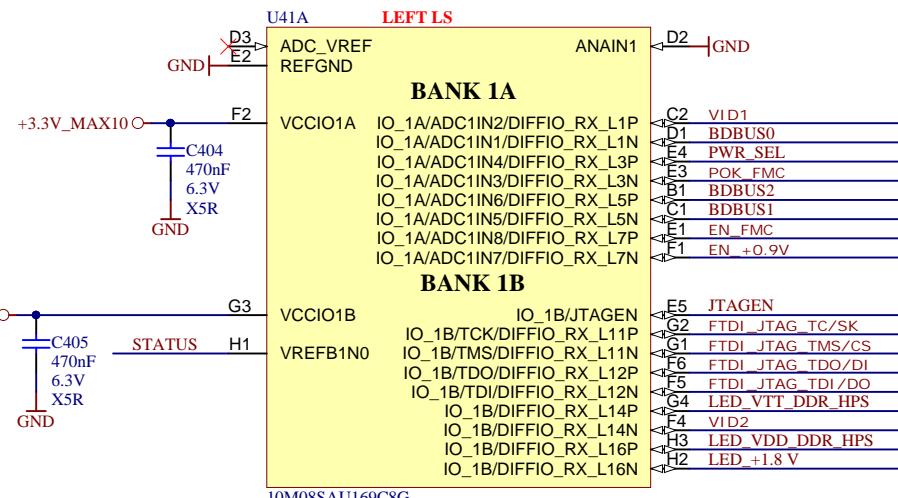
Page 2 of 34

Drawn by: * Filename: FrontPanel.SchDoc

1 2 3 4



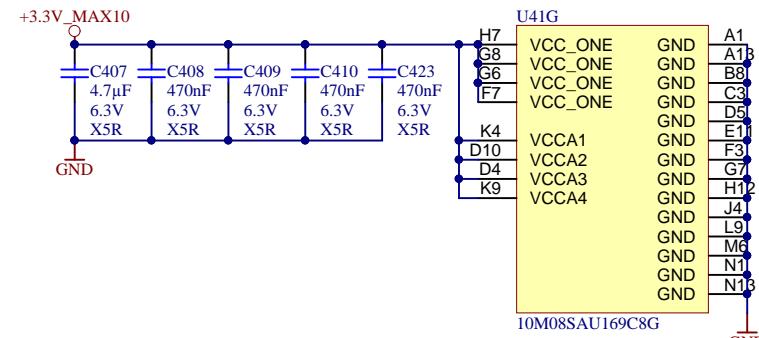
A



B



C



D

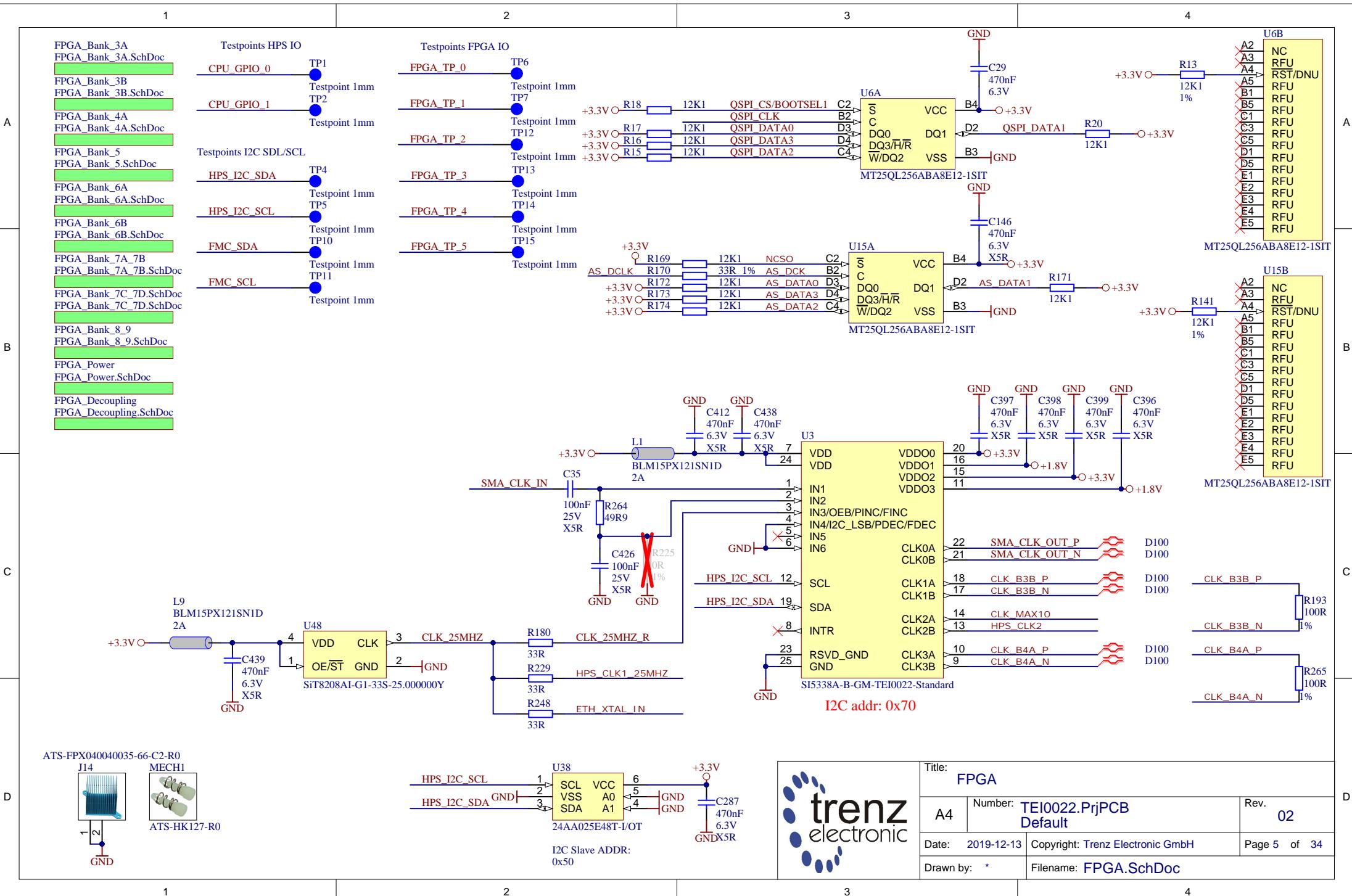


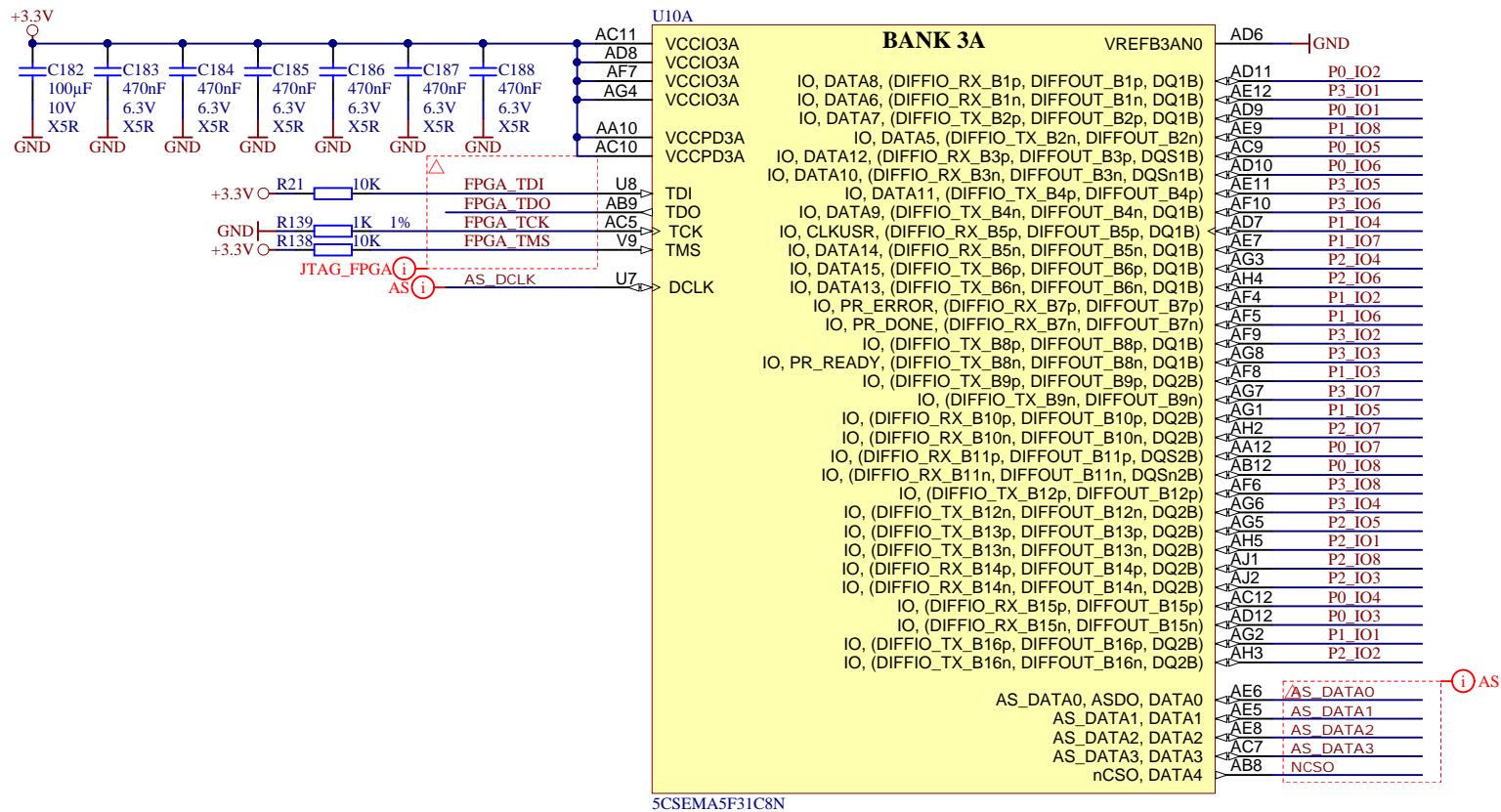
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A4 Number: TEI0022.PrjPCB Default Rev. 02

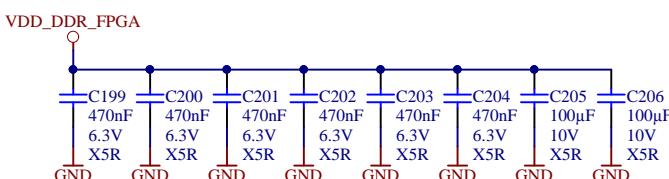
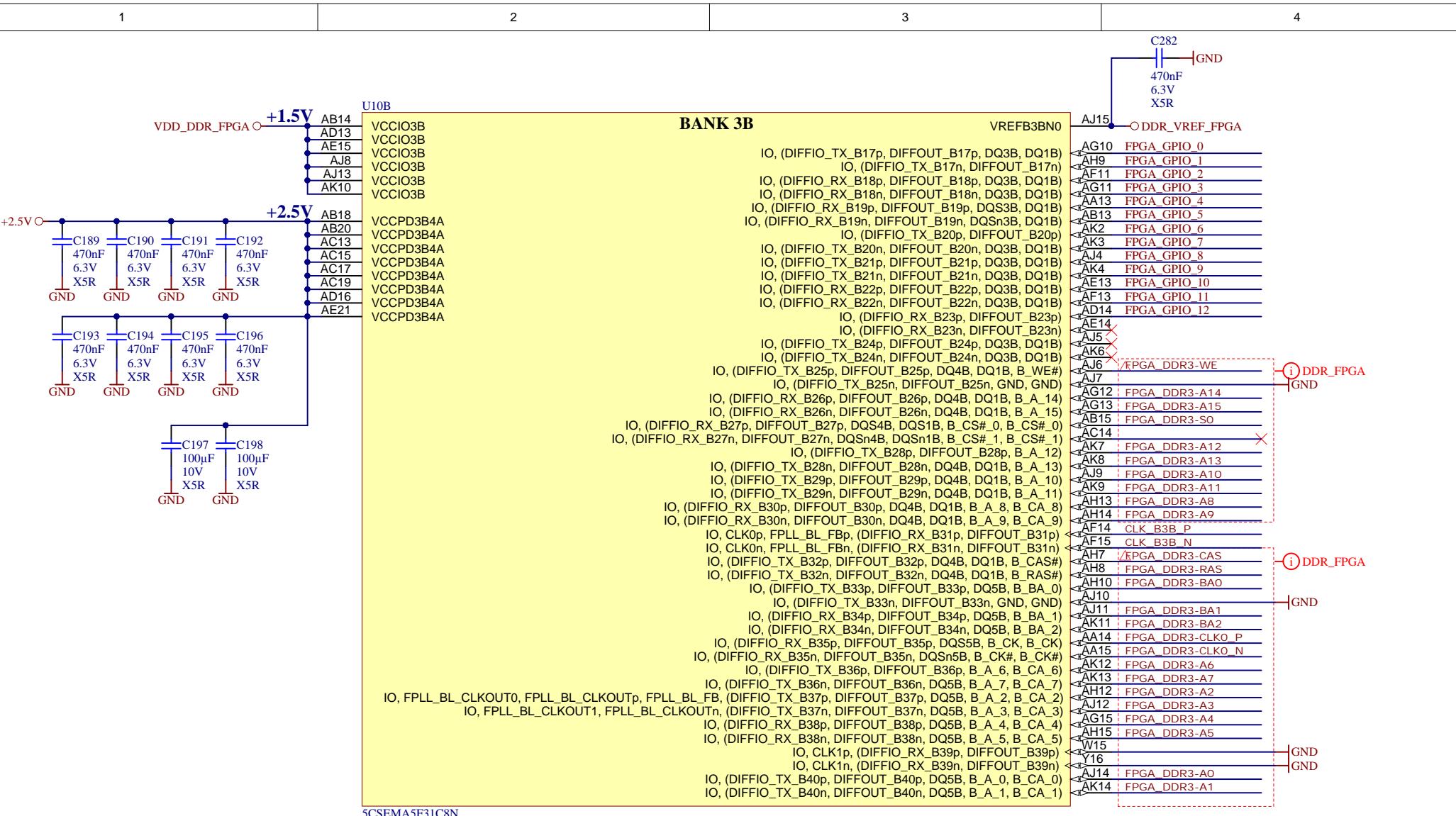
Date: 2019-12-13 Copyright: Trenz Electronic GmbH

Drawn by: * File: MGMT_FPGA_Misc.SchDoc

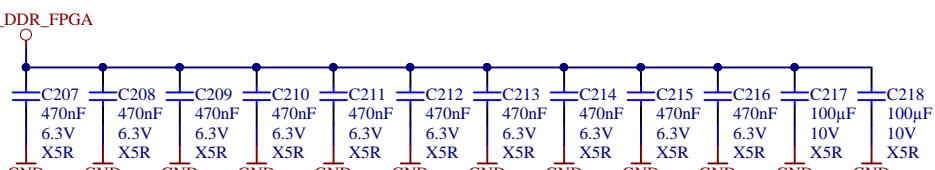
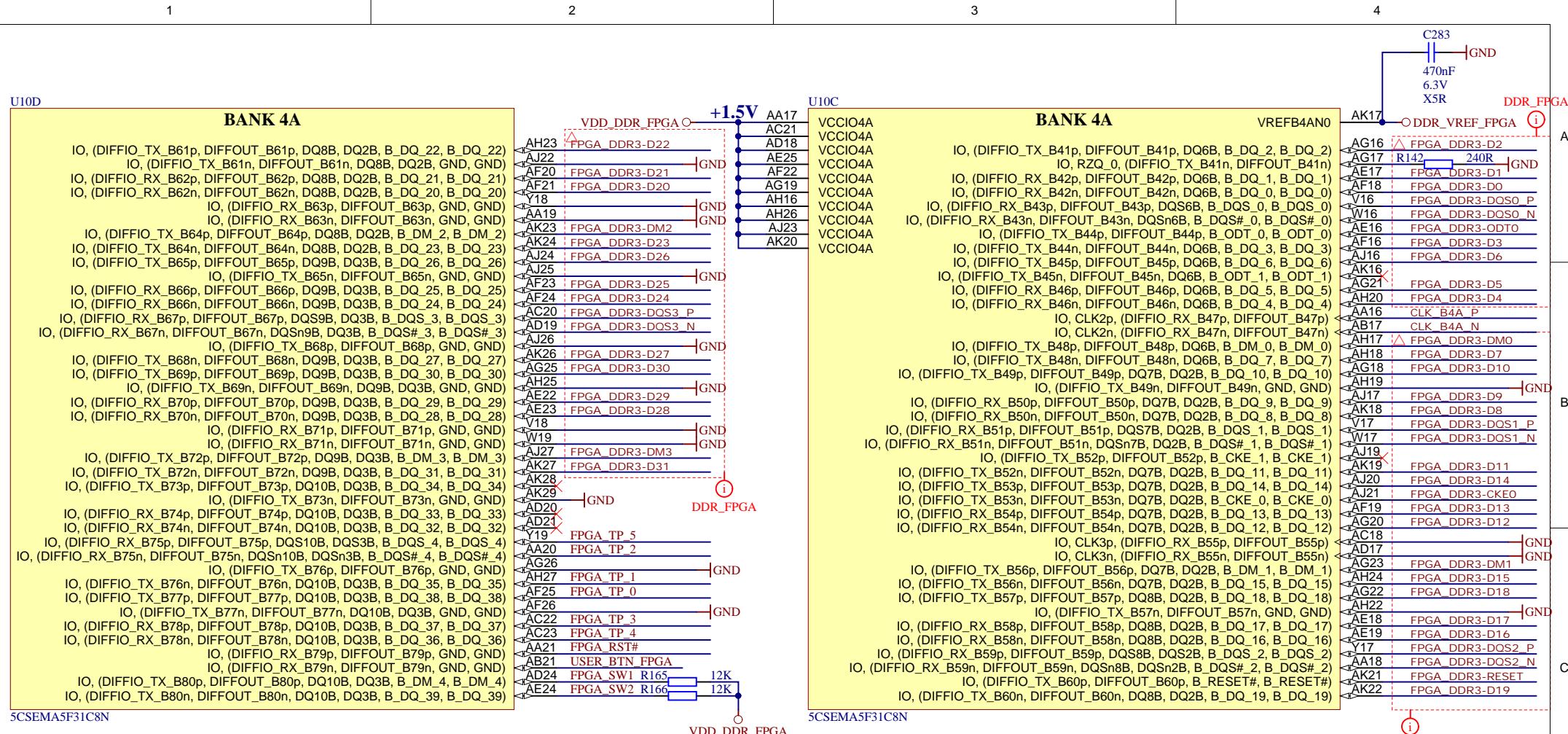




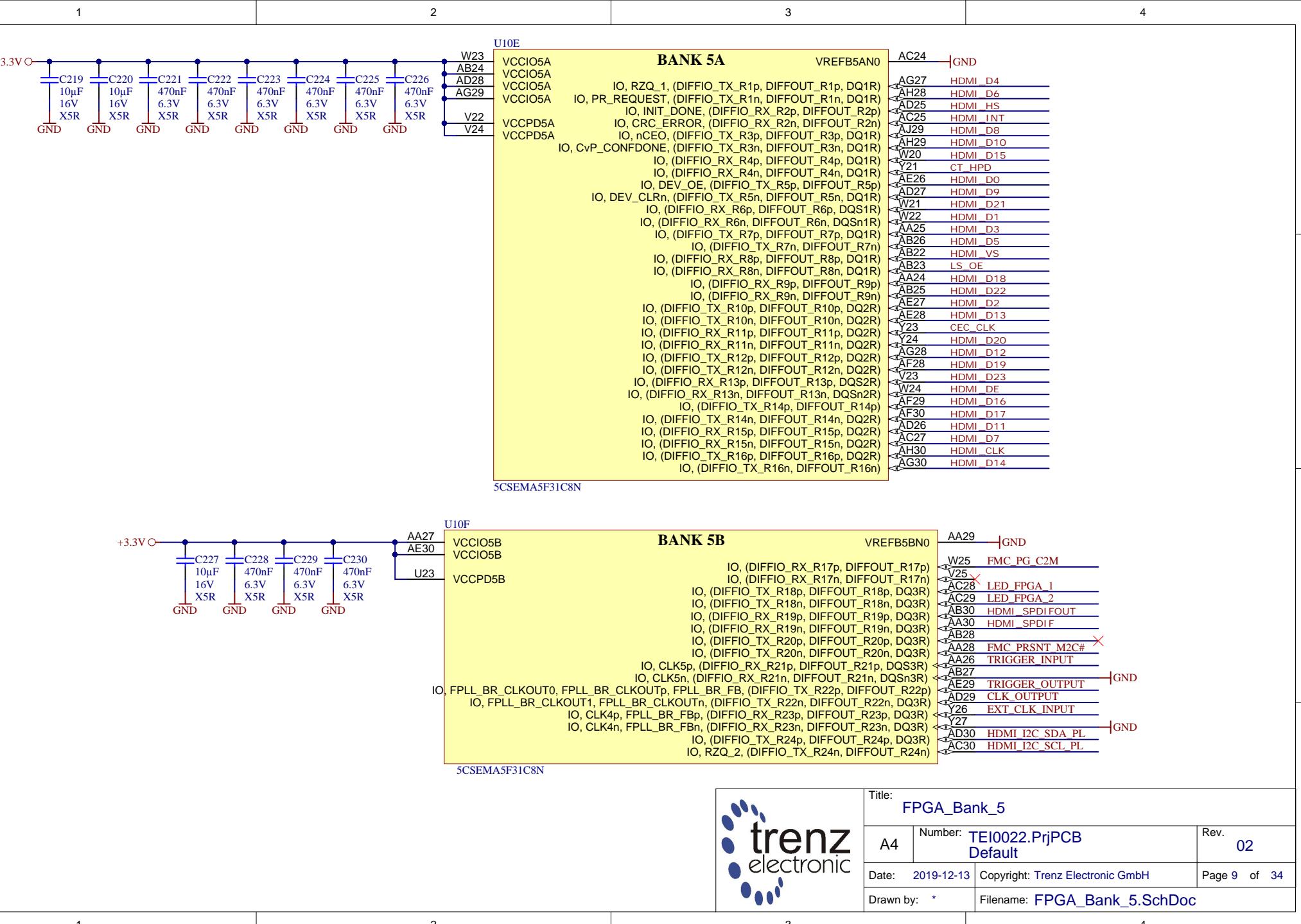
Title: FPGA_Bank_3A		
A4	Number: TEI0022.PrjPCB Default	Rev. 02
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 6 of 34
Drawn by: *	Filename: FPGA_Bank_3A.SchDoc	



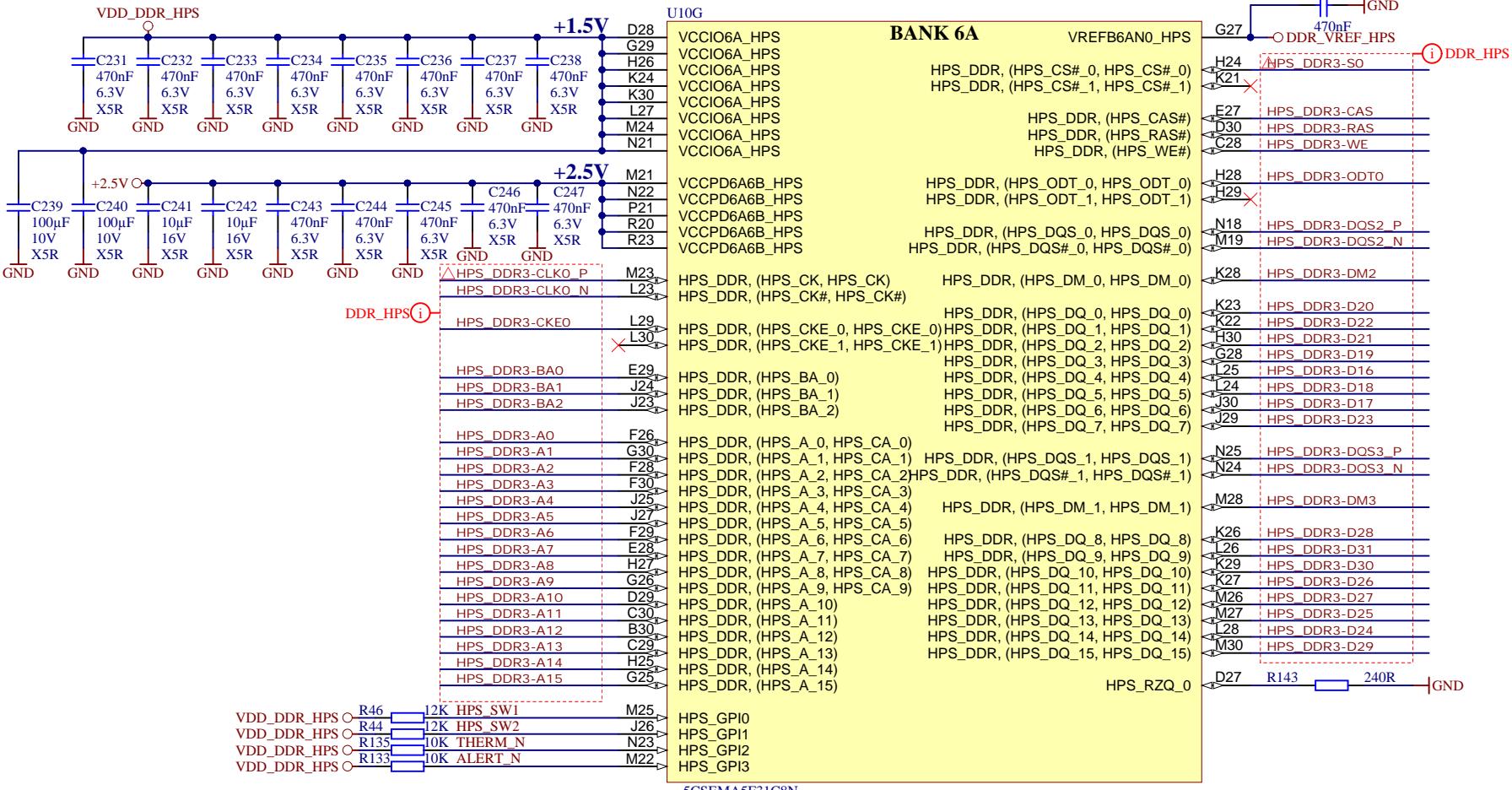
Title: FPGA_Bank_3B		
A4	Number: TEI0022.PrjPCB Default	Rev. 02
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 7 of 34
Drawn by: *	Filename: FPGA_Bank_3B.SchDoc	



Title: FPGA_Bank_4A		
A4	Number: TEI0022.PrjPCB Default	Rev. 02
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 8 of 34
Drawn by: *	Filename: FPGA_Bank_4A.SchDoc	



A



A

B

C

D



Title: FPGA_Bank_6A

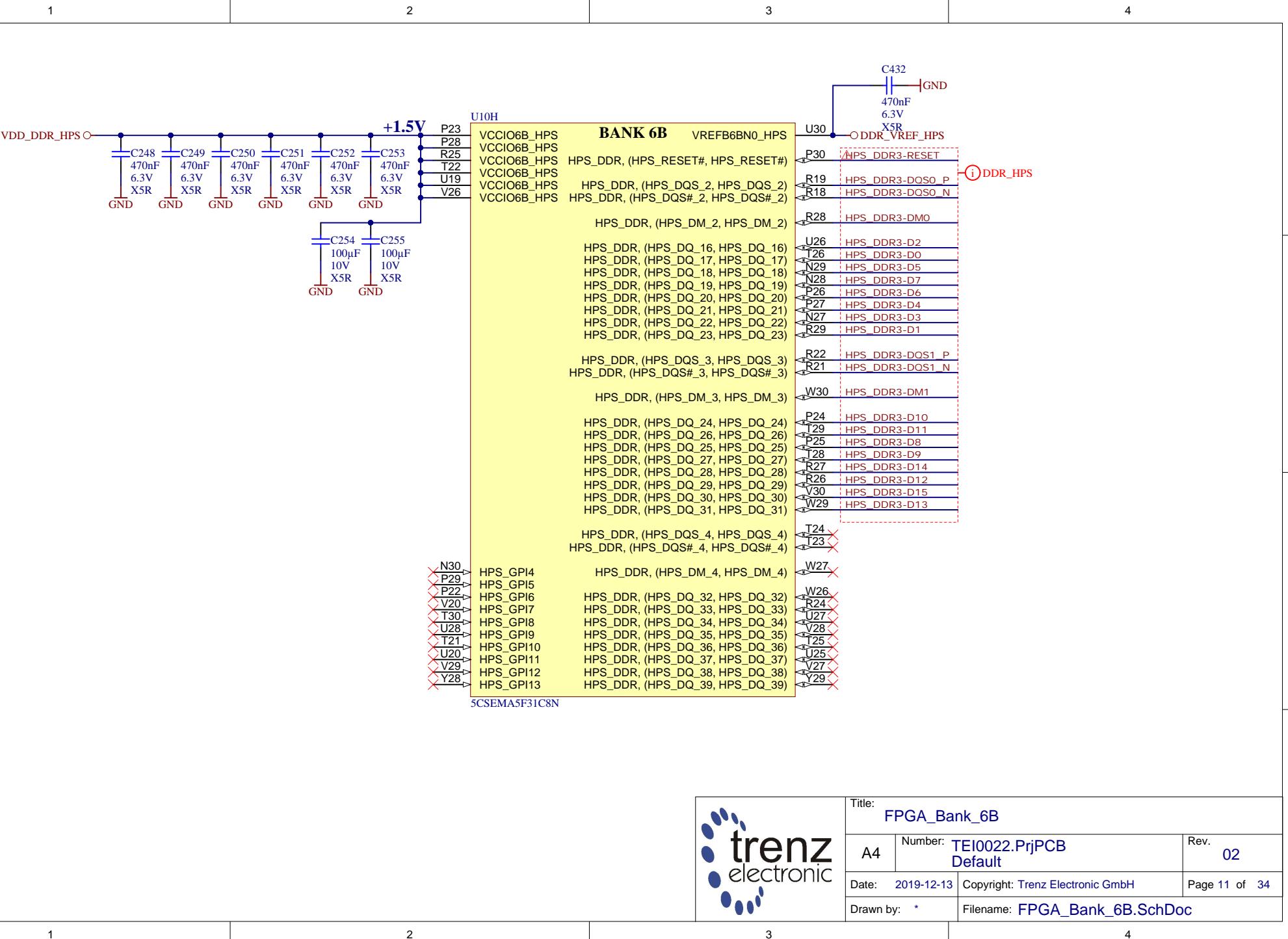
A4 Number: TEI0022.PrjPCB Default

Rev. 02

Date: 2019-12-13 Copyright: Trenz Electronic GmbH

Page 10 of 34

Drawn by: * Filename: FPGA_Bank_6A.SchDoc



A

B

C

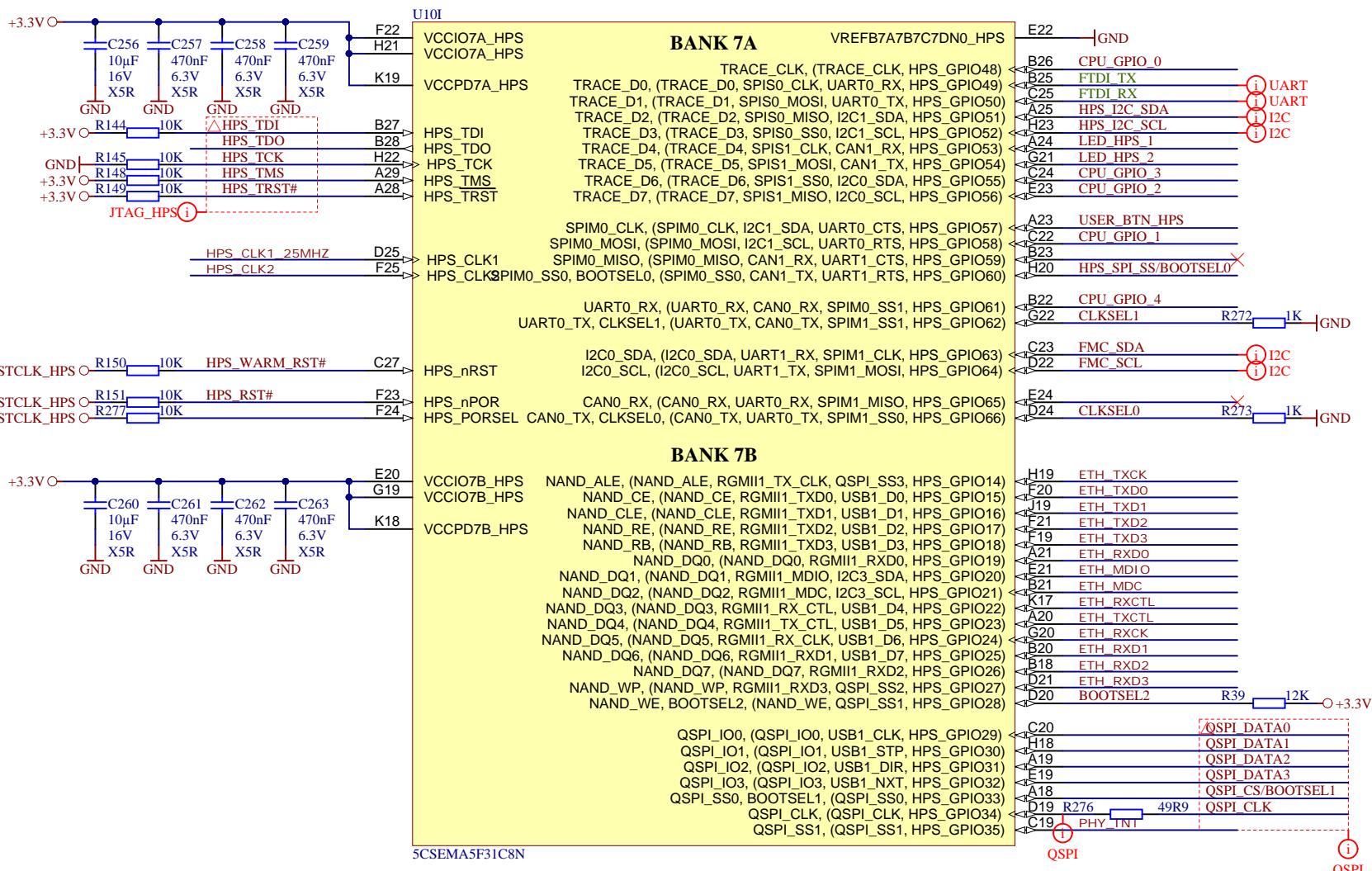
D

A

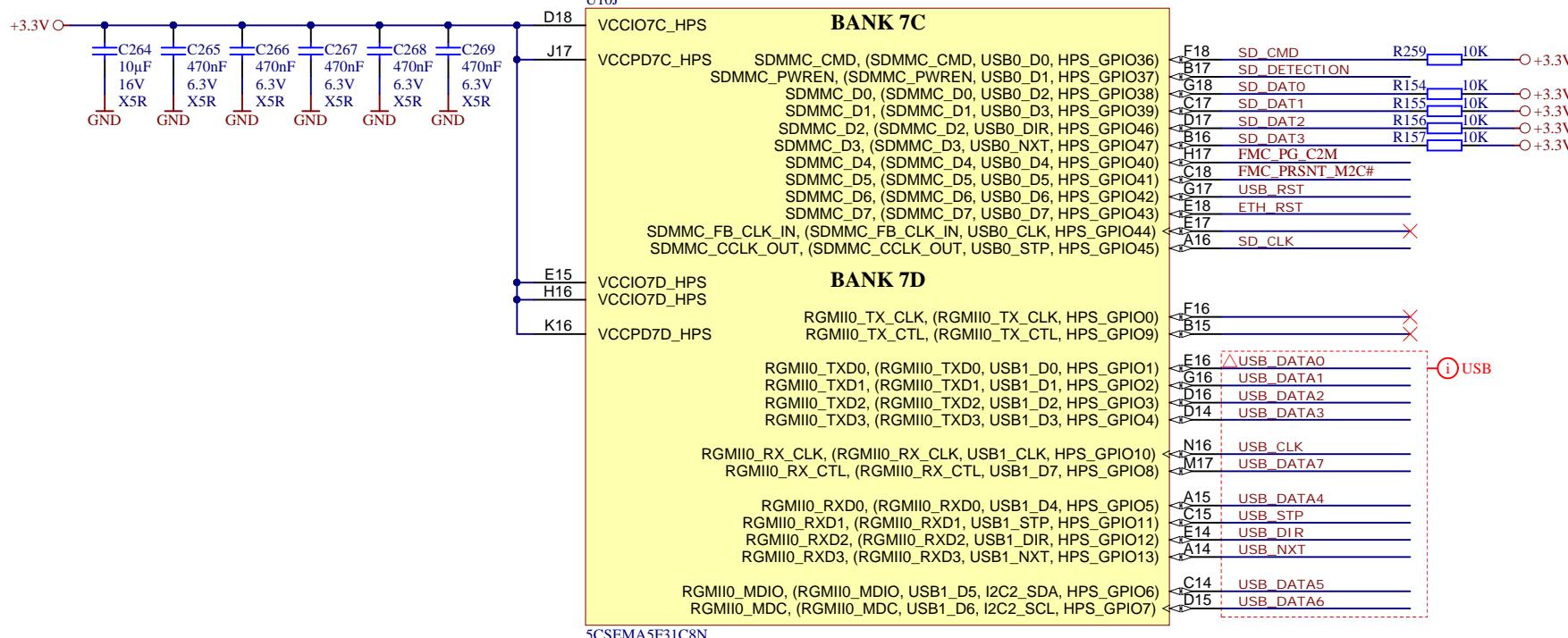
B

C

D

Title: **FPGA_Bank_7A_7B**A4 Number: **TEI0022.PrjPCB Default** Rev. **02**Date: **2019-12-13** Copyright: **Trenz Electronic GmbH**Drawn by: * File: **FPGA_Bank_7A_7B.SchDoc**

A



Title: FPGA_Bank_7C_7D		
A4	Number: TEI0022.PrjPCB Default	Rev. 02
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 13 of 34
Drawn by: *	Filename: FPGA_Bank_7C_7D.SchDoc	

A

B

C

D

A U10L

BANK 8A (cont.)

IO, (DIFFIO_RX_T21p, DIFFOUT_T21p, DQS3T, DQ1T)
 IO, (DIFFIO_RX_T21n, DIFFOUT_T21n, DQSn3T, DQ1T)
 IO, (DIFFIO_TX_T22p, DIFFOUT_T22p)
 IO, (DIFFIO_TX_T22n, DIFFOUT_T22n, DQ3T, DQ1T)
 IO, (DIFFIO_RX_T23p, DIFFOUT_T23p, DQ3T, DQ1T)
 IO, (DIFFIO_RX_T23n, DIFFOUT_T23n, DQ3T, DQ1T)
 IO, (DIFFIO_TX_T24p, DIFFOUT_T24p, DQ3T, DQ1T)
 IO, (DIFFIO_RX_T24n, DIFFOUT_T24n)
 IO, (DIFFIO_RX_T25p, DIFFOUT_T25p)
 IO, (DIFFIO_RX_T25n, DIFFOUT_T25n)
 IO, (DIFFIO_RX_T26p, DIFFOUT_T26p, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T26n, DIFFOUT_T26n, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T27p, DIFFOUT_T27p, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T27n, DIFFOUT_T27n, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T28p, DIFFOUT_T28p, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T28n, DIFFOUT_T28n, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T29p, DIFFOUT_T29p, DQS4T, DQS2T)
 IO, (DIFFIO_RX_T29n, DIFFOUT_T29n, DQSn4T, DQSn2T)
 IO, (DIFFIO_RX_T30p, DIFFOUT_T30p)
 IO, (DIFFIO_RX_T30n, DIFFOUT_T30n, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T31p, DIFFOUT_T31p, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T31n, DIFFOUT_T31n, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T32p, DIFFOUT_T32p, DQ4T, DQ2T)
 IO, (DIFFIO_RX_T32n, DIFFOUT_T32n)
 IO, (DIFFIO_RX_T33p, DIFFOUT_T33p)
 IO, (DIFFIO_RX_T33n, DIFFOUT_T33n)
 IO, (DIFFIO_RX_T34p, DIFFOUT_T34p, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T34n, DIFFOUT_T34n, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T35p, DIFFOUT_T35p, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T35n, DIFFOUT_T35n, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T36p, DIFFOUT_T36p, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T36n, DIFFOUT_T36n, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T37p, DIFFOUT_T37p, DQS5T, DQ2T)
 IO, (DIFFIO_RX_T37n, DIFFOUT_T37n, DQSn5T, DQ2T)
 IO, (DIFFIO_RX_T38p, DIFFOUT_T38p)
 IO, (DIFFIO_RX_T38n, DIFFOUT_T38n, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T39p, DIFFOUT_T39p, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T39n, DIFFOUT_T39n, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T40p, DIFFOUT_T40p, DQ5T, DQ2T)
 IO, (DIFFIO_RX_T40n, DIFFOUT_T40n)

5CSEMA5F31C8N

U10K

FMC_VADJ

H13 LA05_P RX
 H12 LA05_N RX
 D5 LA22_P TX
 C4 LA22_N TX
 F11 LA07_P RX
 E11 LA07_N RX
 E8 LA10_P TX
 D7 LA10_N TX
 J7 LA29_P RX
 H7 LA29_N RX
 B2 LA28_P TX
 B1 LA28_N TX
 B6 LA13_P RX
 B5 LA13_N RX
 C3 LA24_P TX
 B3 LA24_N TX
 K12 LA03_P RX
 J12 LA03_N RX
 D2 LA30_P TX
 C2 LA30_N TX
 G12 LA23_P RX
 G11 LA23_N RX
 E4 TX
 D4 TX
 K7 LA33_P RX
 K8 LA33_N RX
 E3 TX
 E2 TX
 G10 LA27_P RX
 F10 LA27_N RX
 E1 LA32_P TX
 D1 LA32_N TX
 J10 LA31_P RX
 J9 LA31_N RX
 E7 TX
 E6 TX
 F9 LA11_P RX
 F8 LA11_N RX
 G7 TX
 F6 TX

FMC_VCCPD

L14

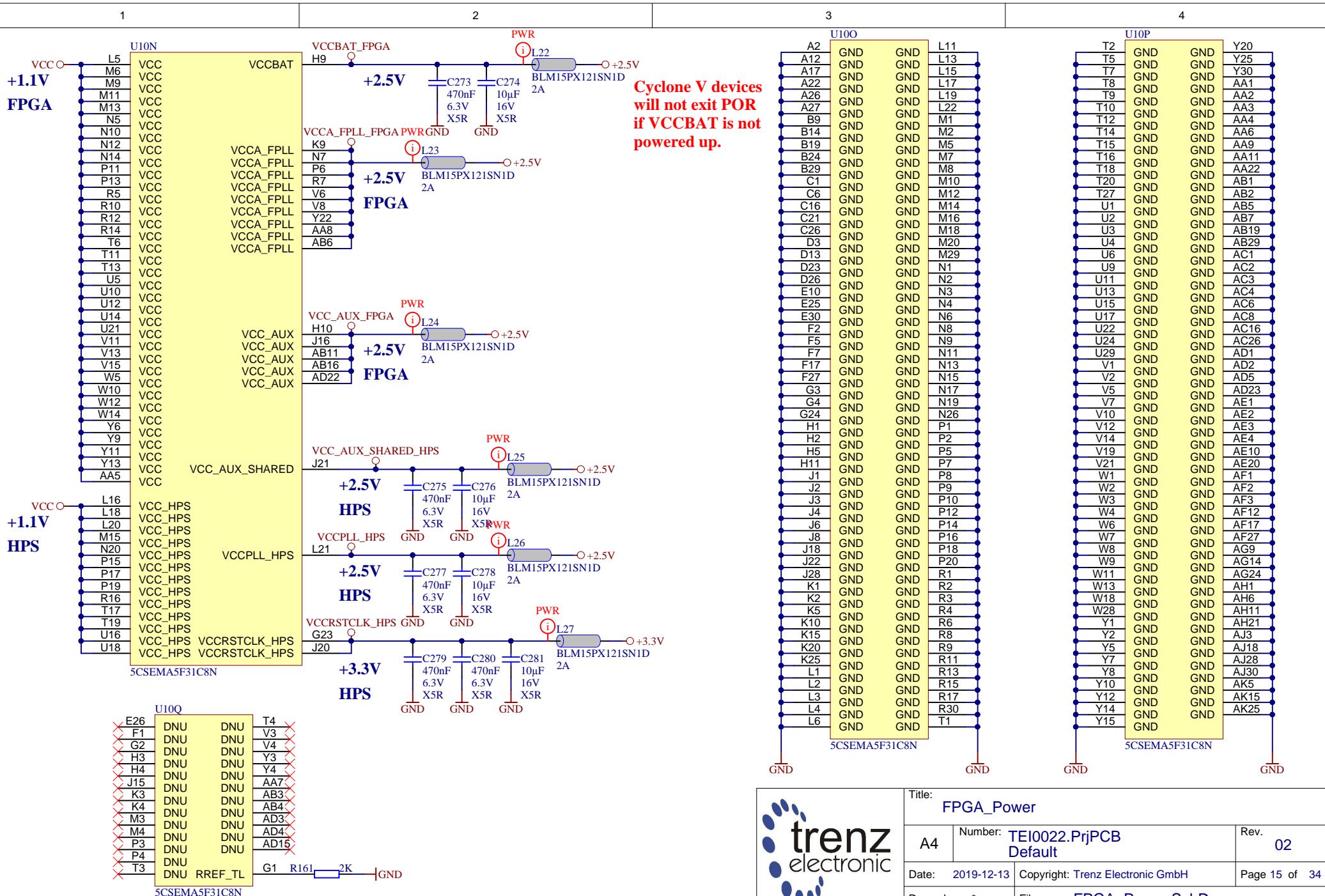
L12

L10

K11

K13

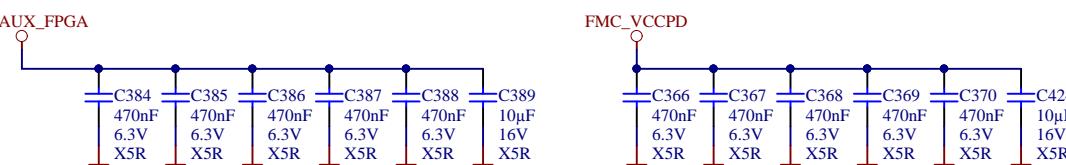
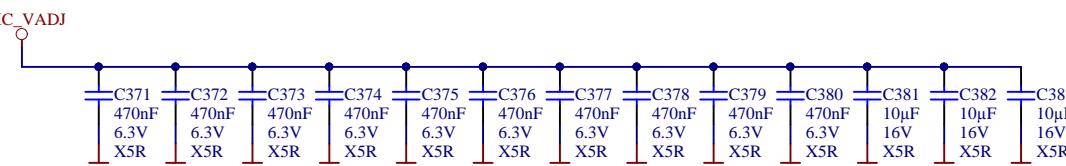
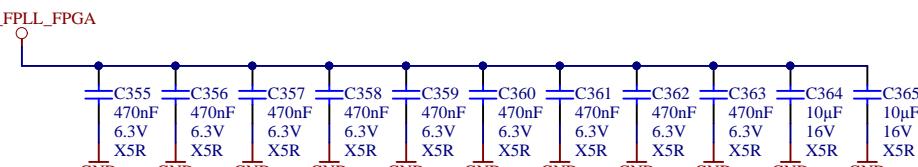
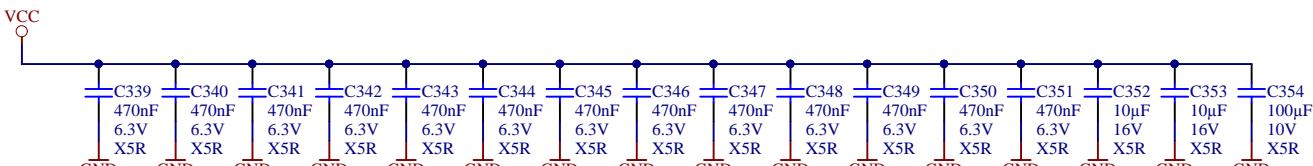
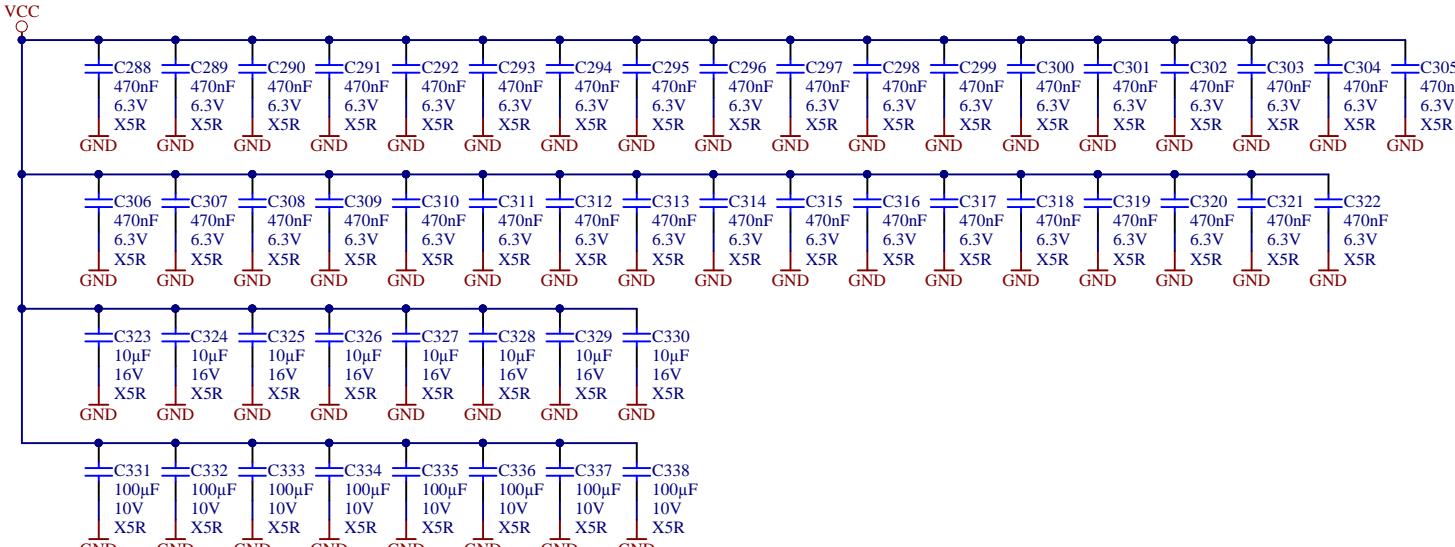
VCCPD8A



Title:

FPGA_Power

Default
Date: 2019-12-13 Copyright: Trenz Electronic GmbH Page 15 of 15
Drawn by: * Filename: FPGA_Power_SchDoc



Title: **FPGA_Decoupling**

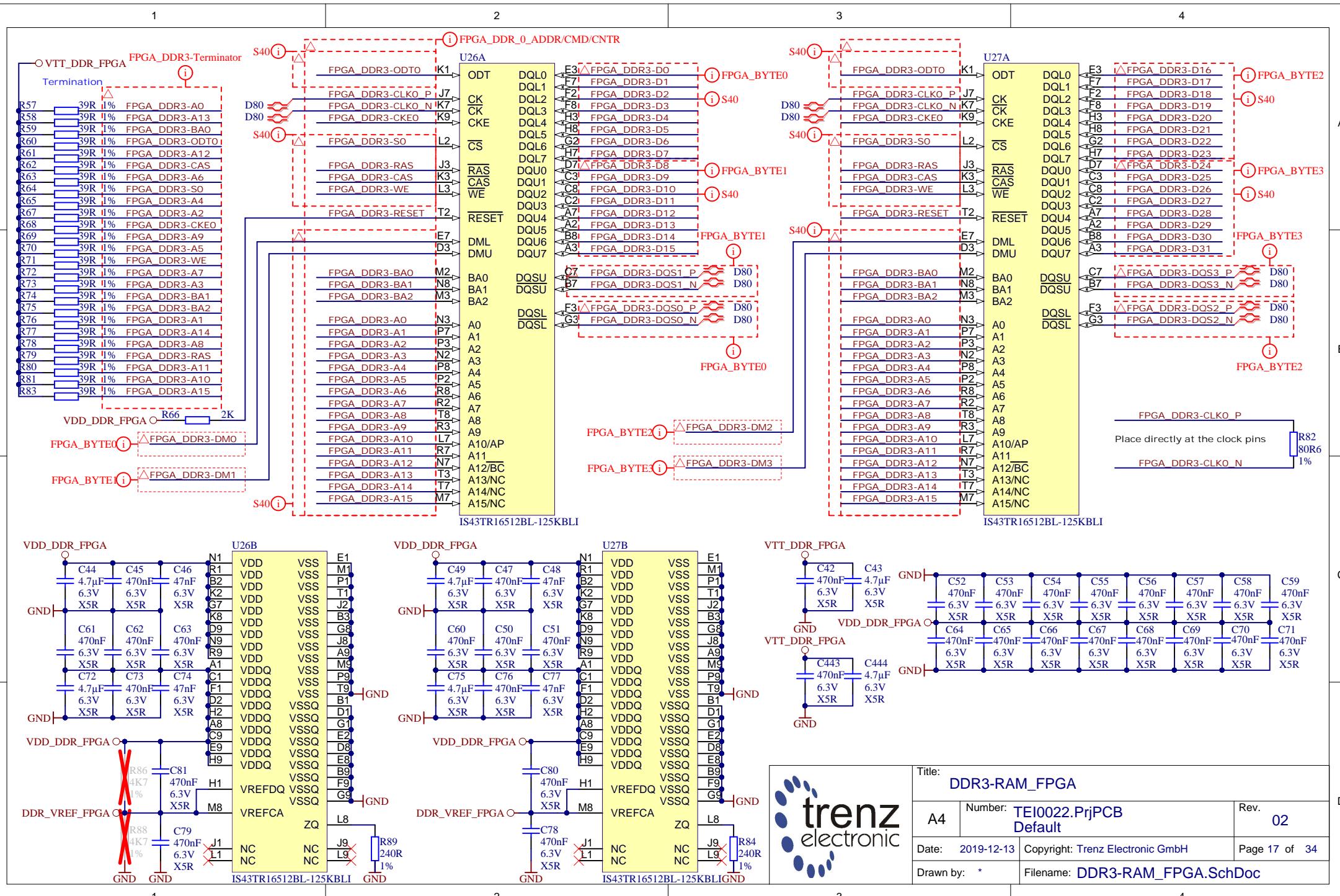
A4 Number: **TEI0022.PrjPCB Default**

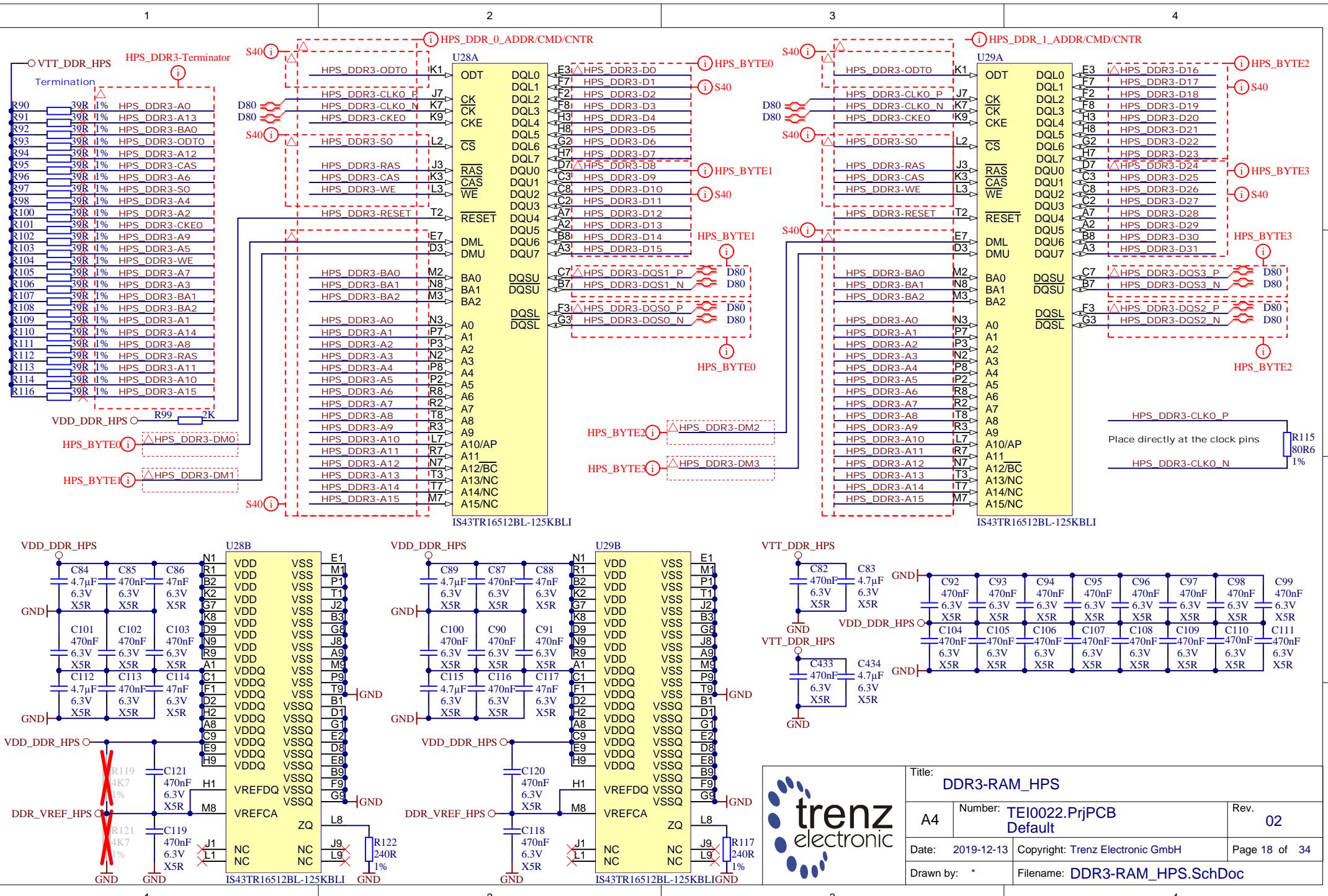
Rev. **02**

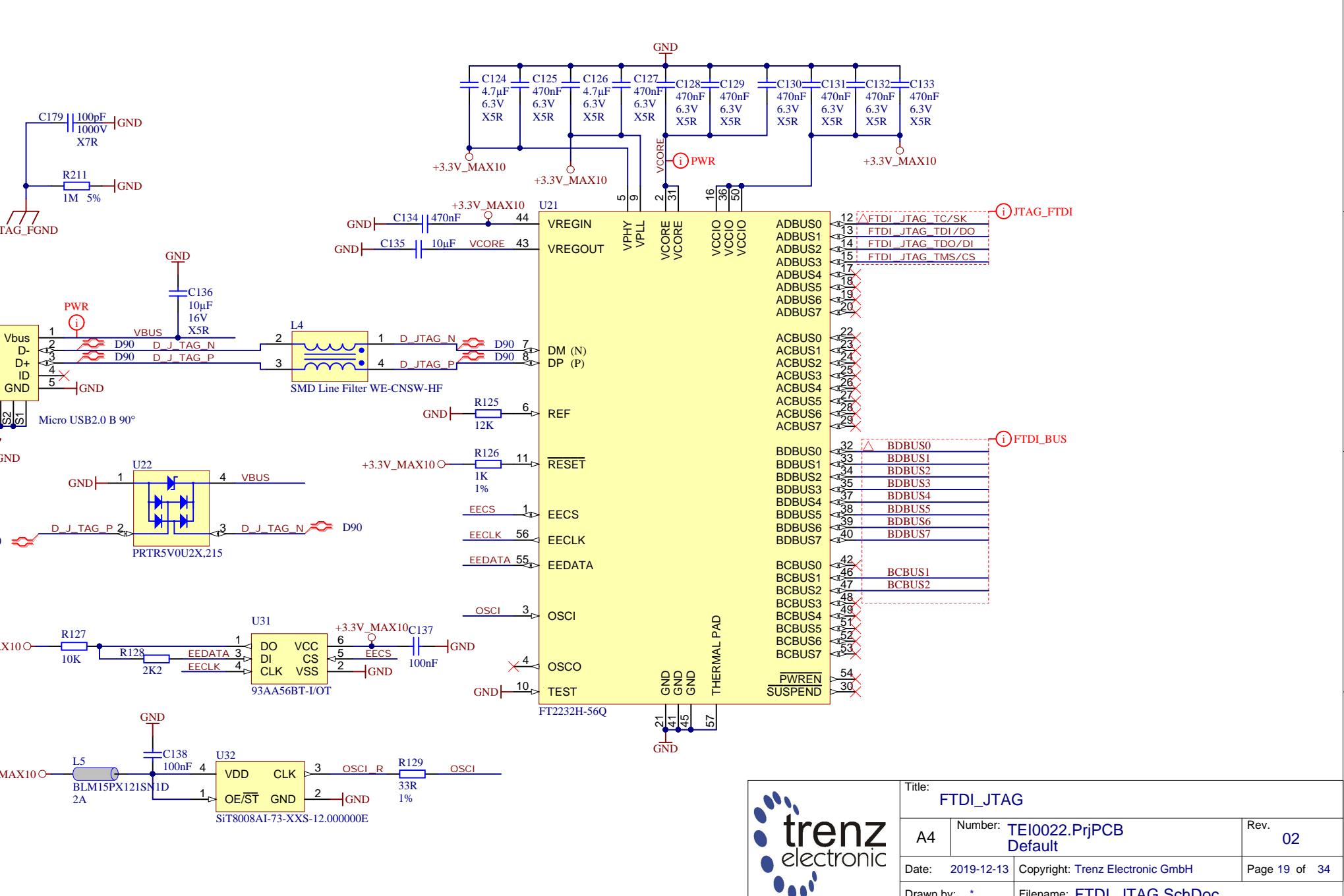
Date: **2019-12-13** Copyright: **Trenz Electronic GmbH**

Page **16** of **34**

Drawn by: * Filename: **FPGA_Decoupling.SchDoc**







Title: FTDI_JTAG

A4 Number: TEI0022.PrjPCB Default

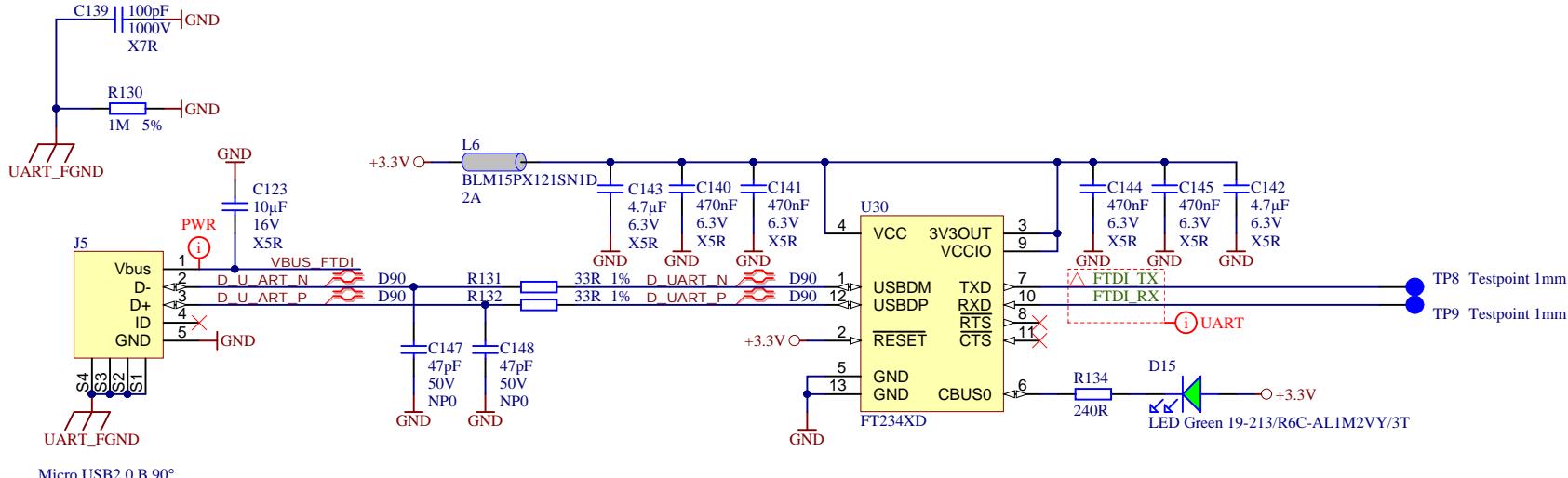
Rev. 02

Date: 2019-12-13 Copyright: Trenz Electronic GmbH

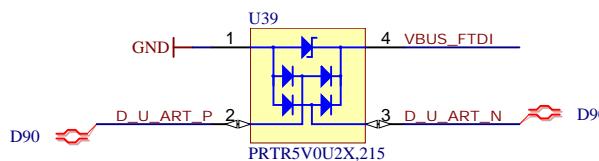
Page 19 of 34

Drawn by: * Filename: FTDI_JTAG.SchDoc

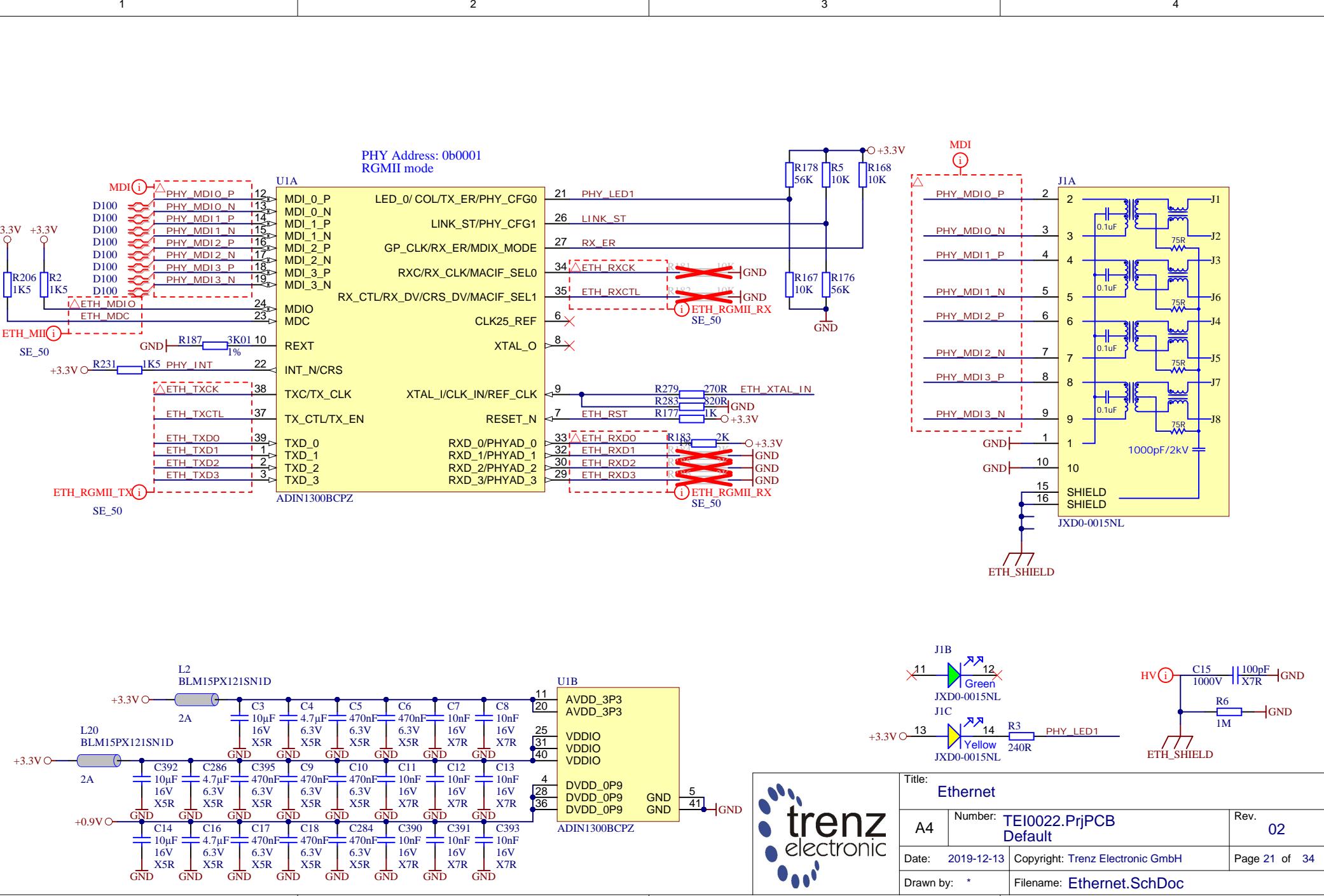
USB/UART Bridge



Micro USB2.0 B 90°



Title: FTDI_UART		
A4	Number: TEI0022.PrjPCB Default	Rev. 02
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 20 of 34
Drawn by: *	Filename: FTDI_UART.SchDoc	



The logo for trenz electronic consists of a stylized blue graphic of three overlapping ovals in the upper left corner, followed by the company name "trenz electronic" in a lowercase, sans-serif font.

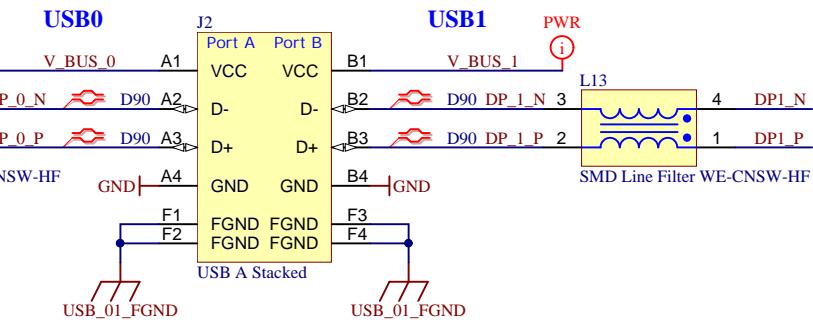
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2

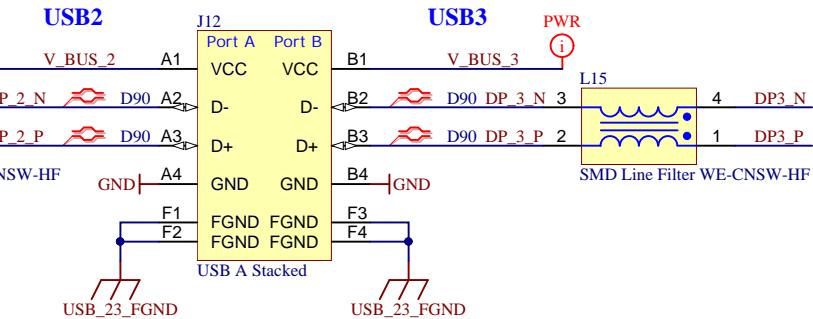
3

4

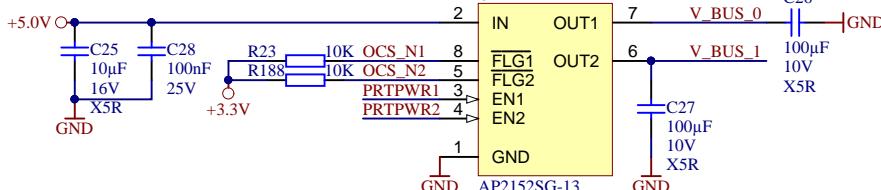
A



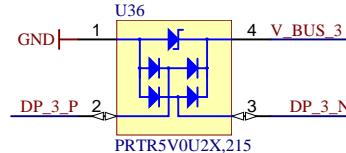
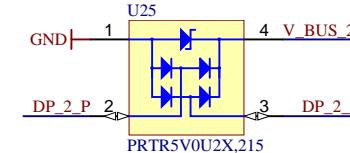
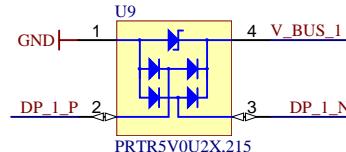
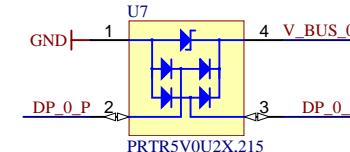
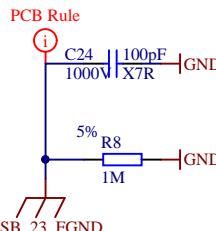
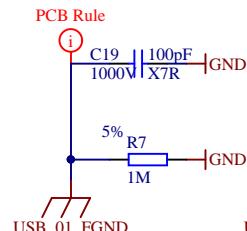
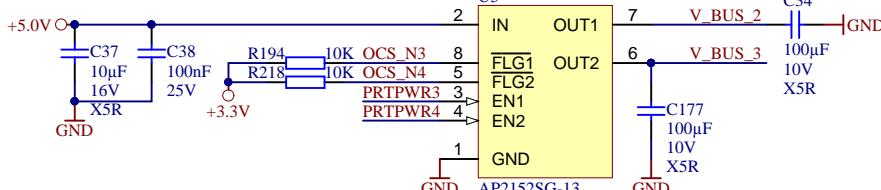
B



C



D

Title: **USB**A4 | Number: **TEI0022.PrjPCB Default**Rev. **02**

Date: 2019-12-13 | Copyright: Trenz Electronic GmbH

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Drawn by: * | Filename: **USB.SchDoc**

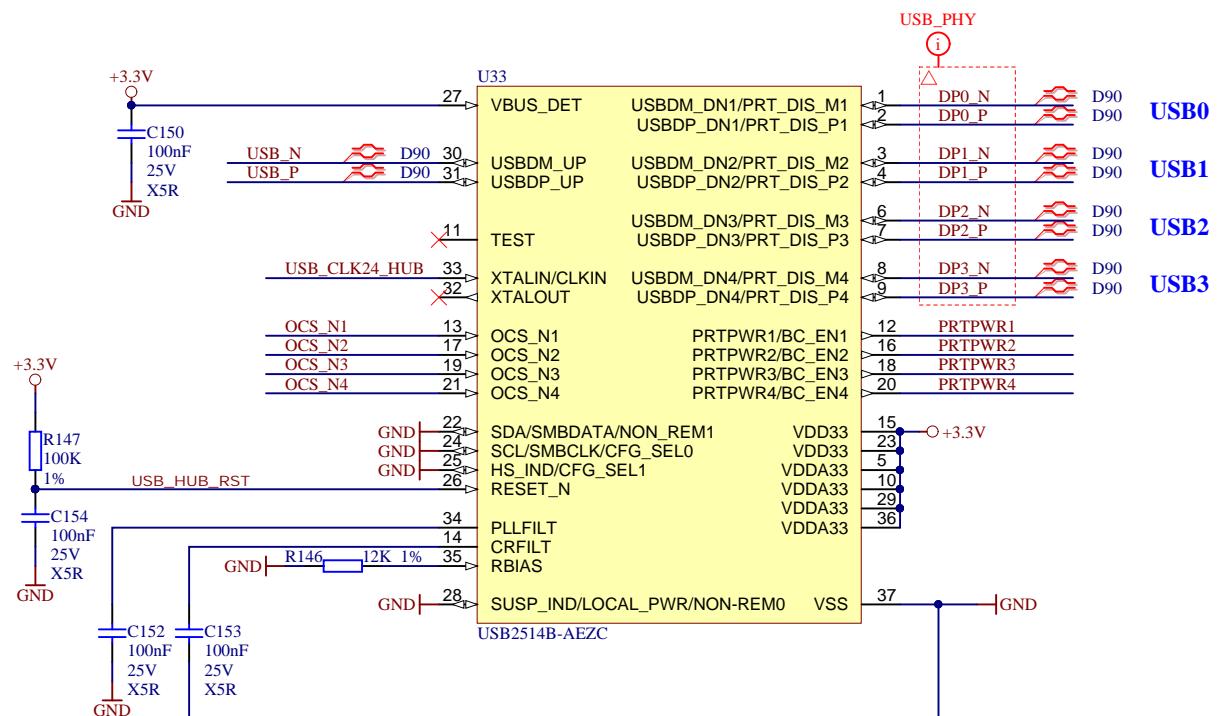
1

2

3

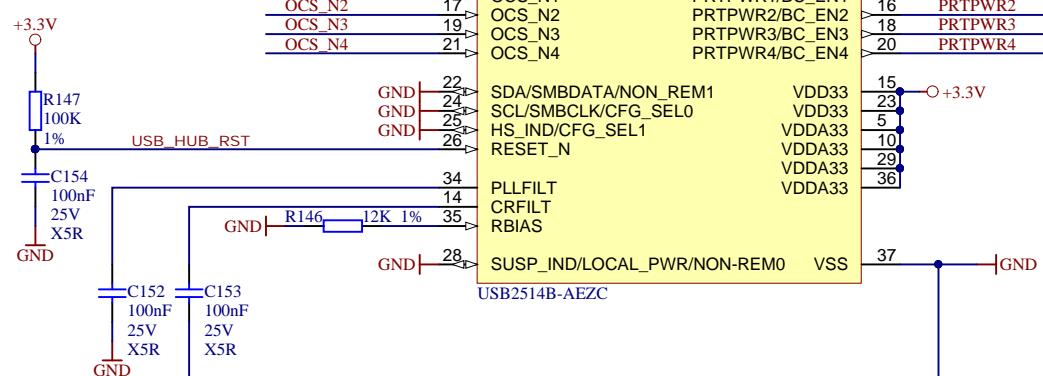
4

A



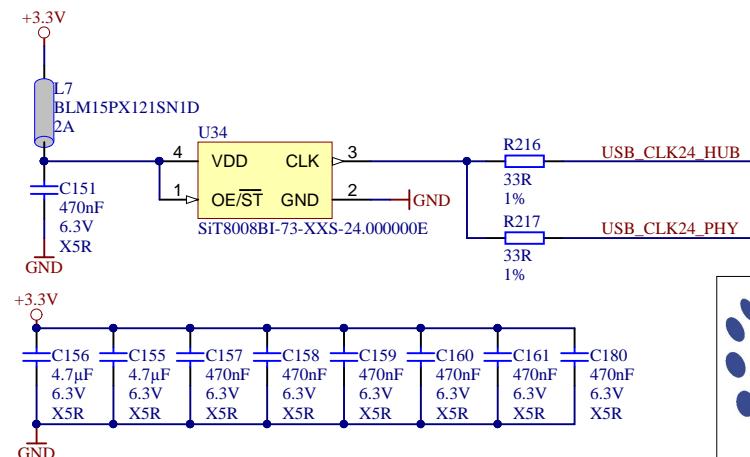
A

B



B

C



C

D



Title: **USB-HUB**

A4 Number: **TEI0022.PrjPCB Default** Rev. **02**

Date: **2019-12-13** Copyright: **Trenz Electronic GmbH** Page **23 of 34**
Drawn by: * Filename: **USB-HUB.SchDoc**

A

A

B

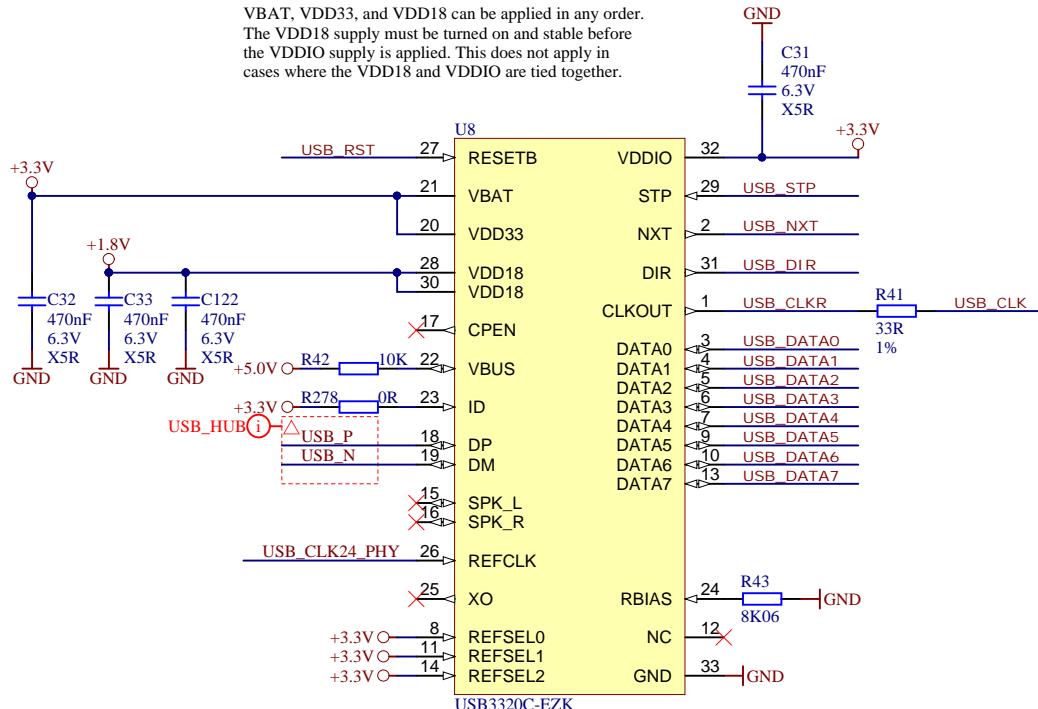
B

C

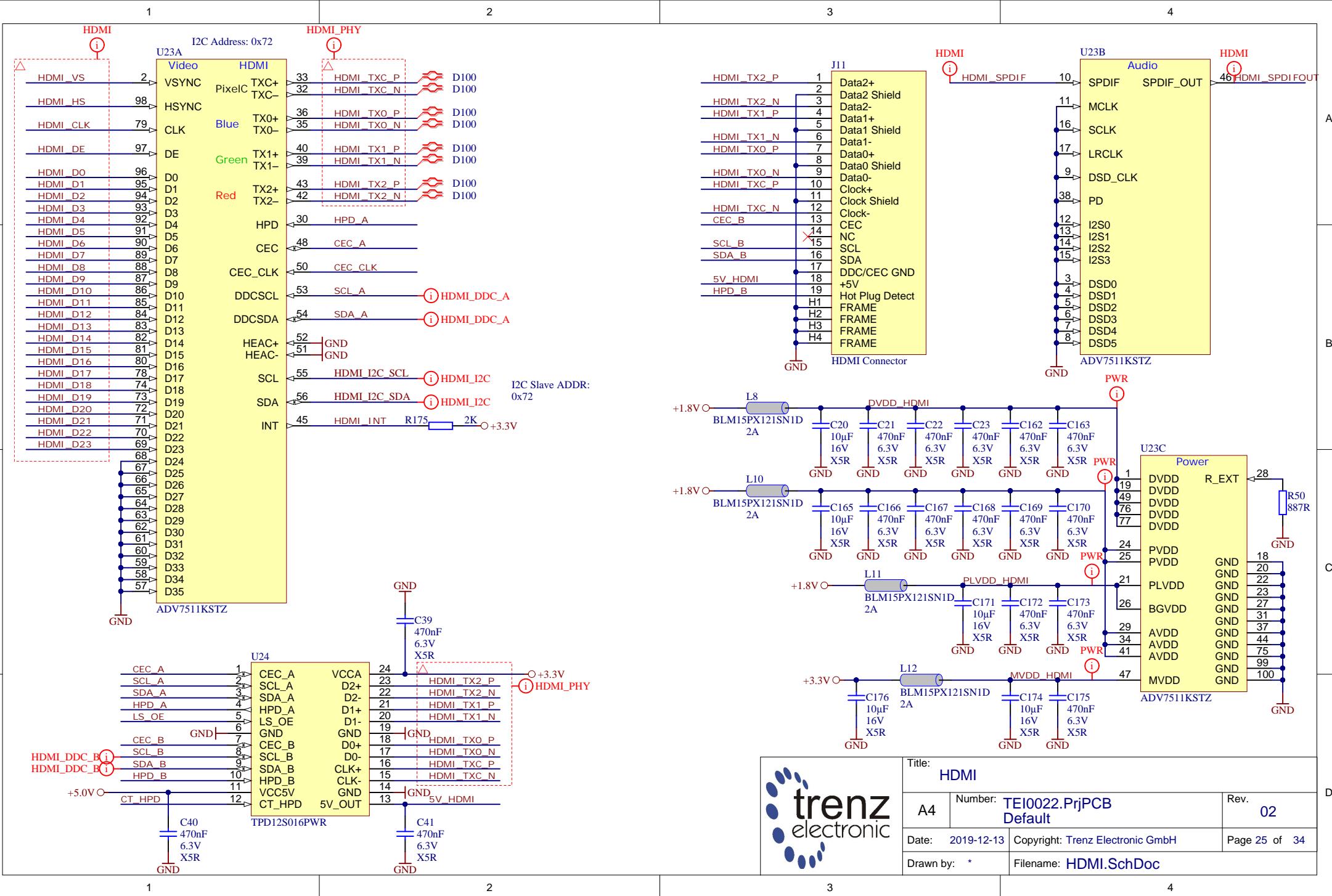
C

D

D



Title: USB-PHY		
A4	Number: TEI0022.PrjPCB Default	Rev. 02
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 24 of 34
Drawn by: *	Filename: USB-PHY.SchDoc	



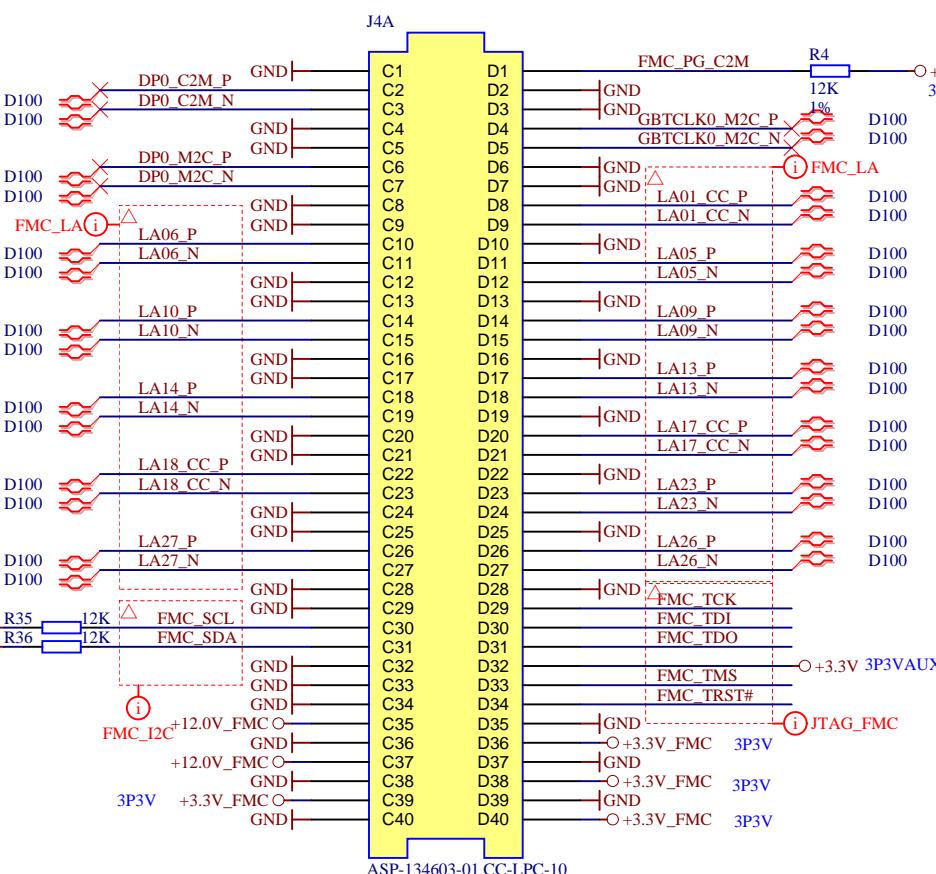
1

2

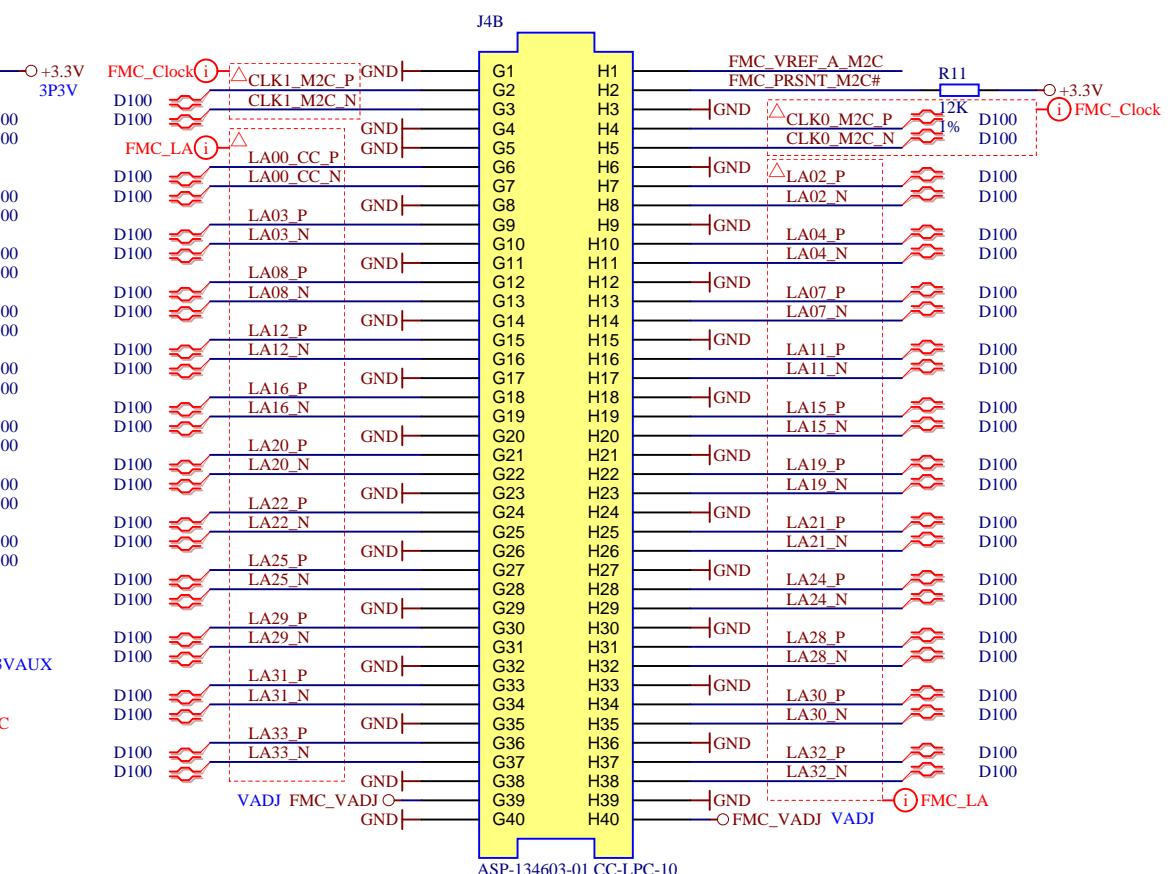
3

4

I2C Address: 0x50
Pin C34: GA[0]=0
Pin D35: GA[1]=0



FMC_VADJ	2 A	FPGA
FMC_VREF_A_M2C	1 mA	
3P3VAUX	20 mA	
3P3V	3 A	+3.3 V FPGA
+12.0V	1 A	+3.3V_FMC FPGA
		+12.0V_FMC



Title: FMC		
A4	Number: TEI0022.PrjPCB Default	Rev. 02
Date: 2019-12-13	Copyright: Trenz Electronic GmbH	Page 26 of 34
Drawn by: *	Filename: FMC.SchDoc	

1

2

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4

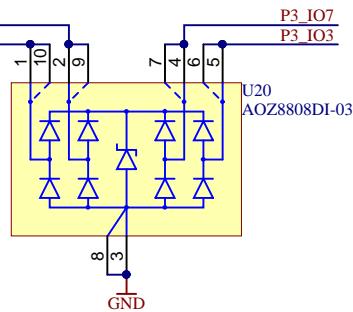
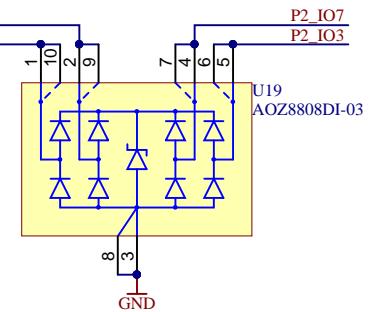
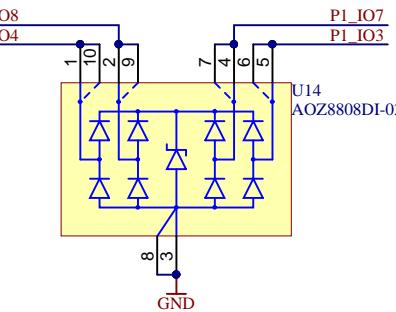
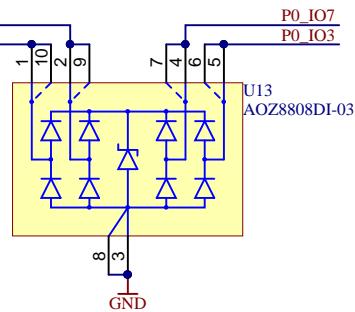
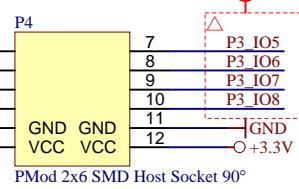
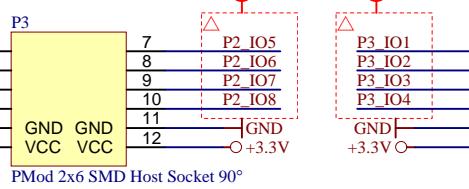
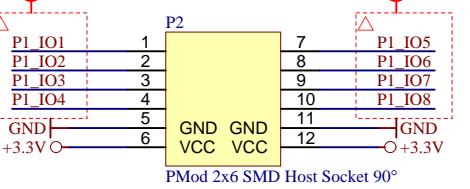
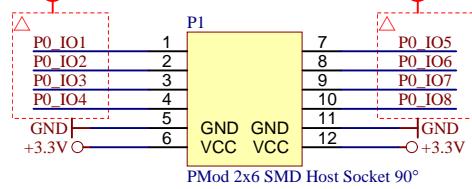
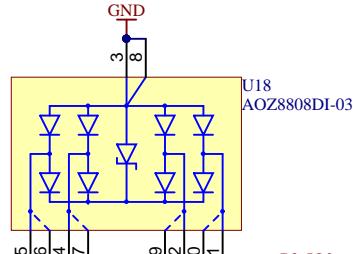
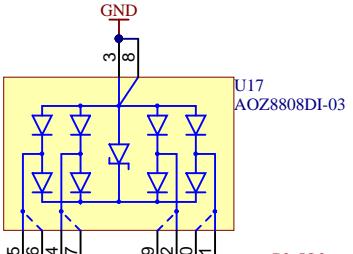
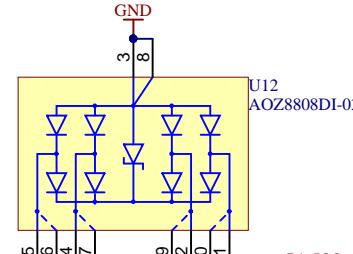
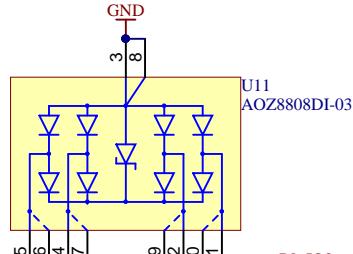
1

2

3

4

A



Title: PMOD		
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1

2

3

4

A

B

C

D

1 2 3 4

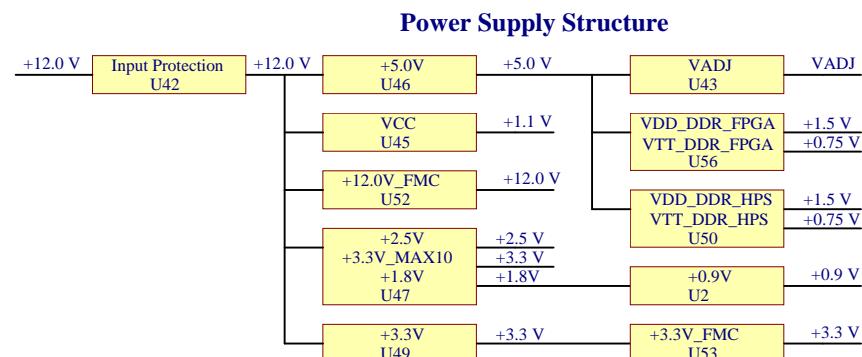
Power1
Power1.SchDoc

Power2
Power2.SchDoc

Power3
Power3.SchDoc

Power4
Power4.SchDoc

Power5
Power5.SchDoc



A

A

B

B

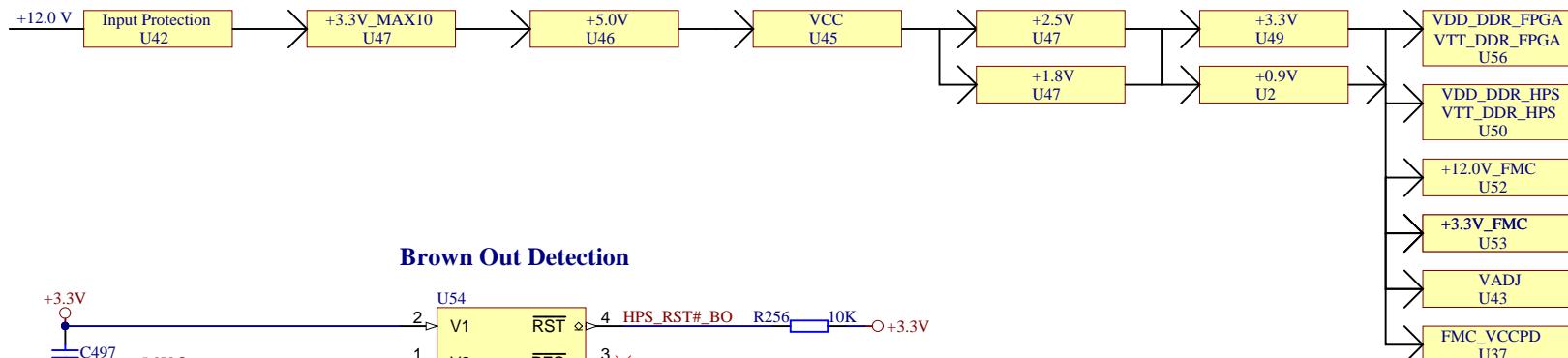
C

C

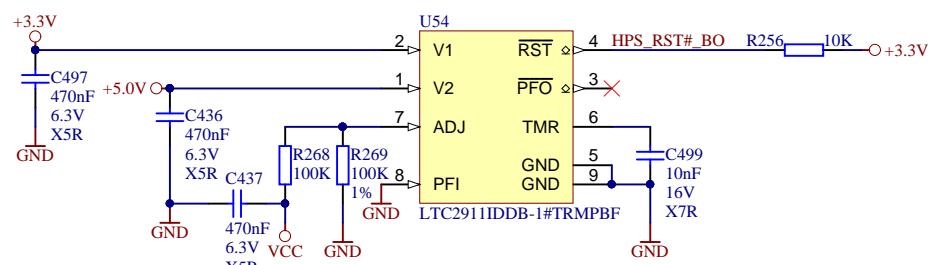
D

D

Power Supply Sequencing



Brown Out Detection



VADJ-Threshold: 1.0 V



Title: TEB0911

A4 Number: TEI0022.PrjPCB Default

Rev. 02

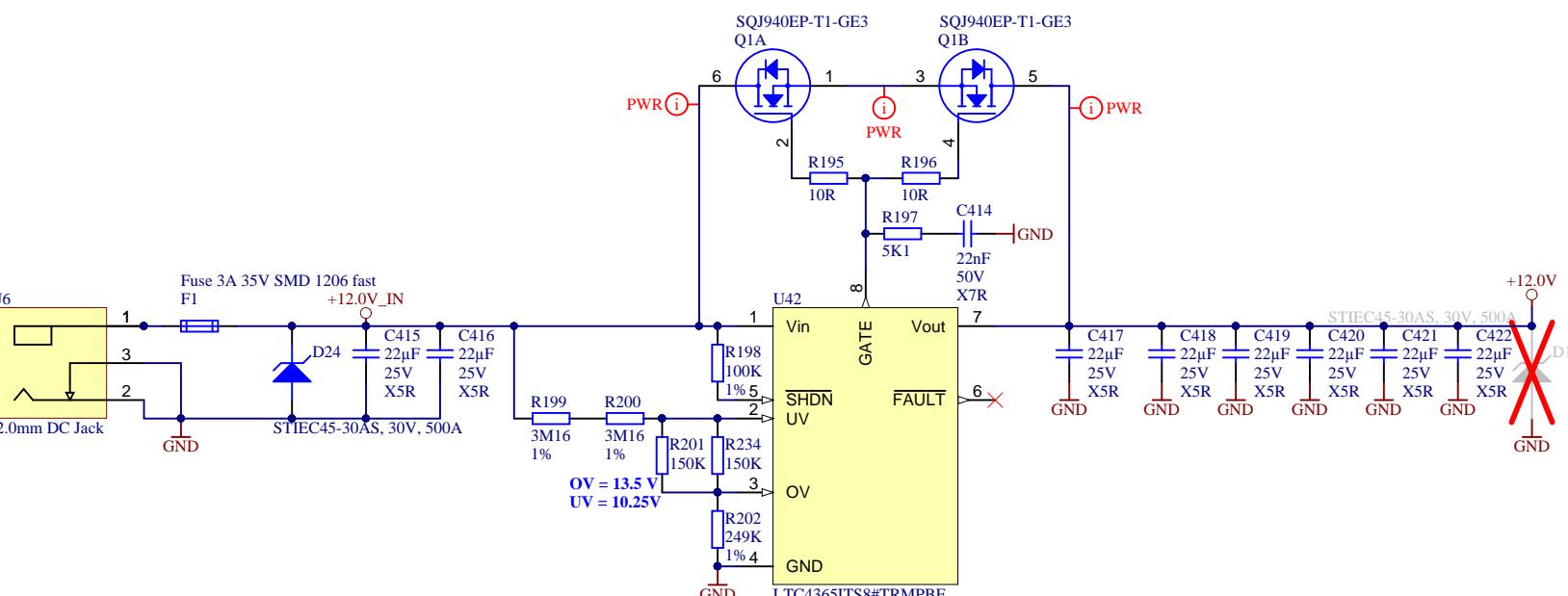
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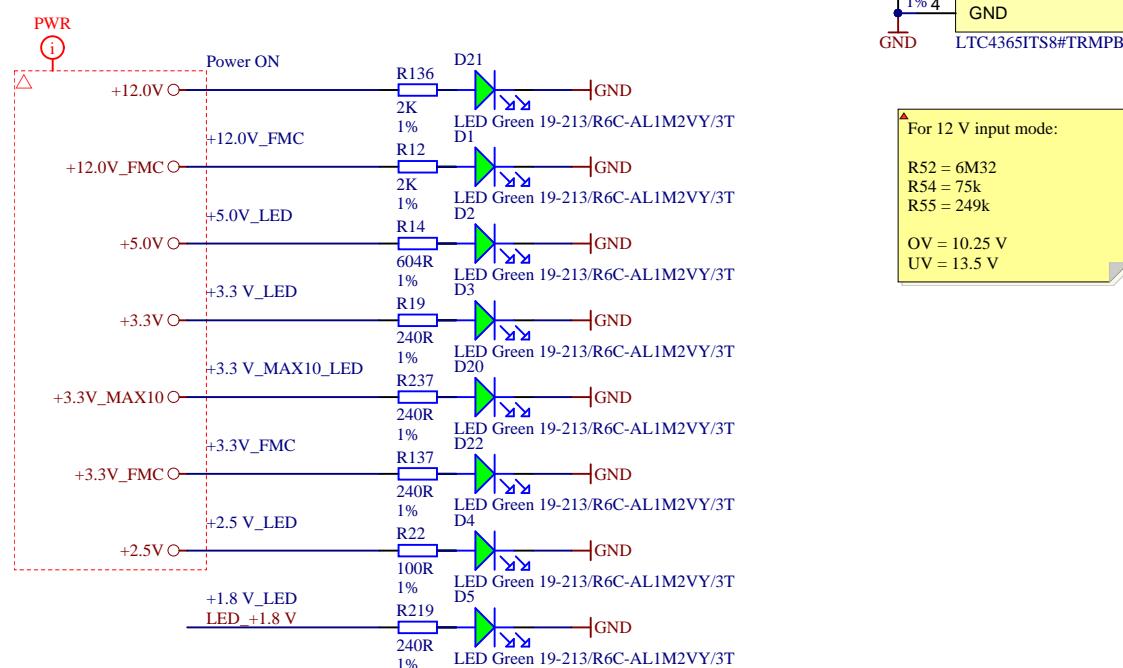
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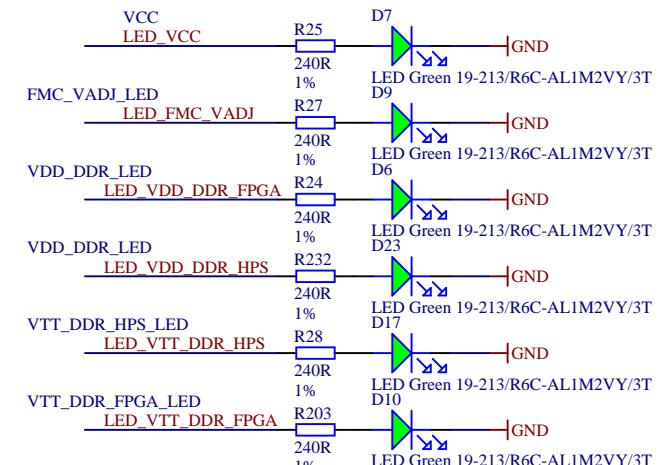
A



B



A



B



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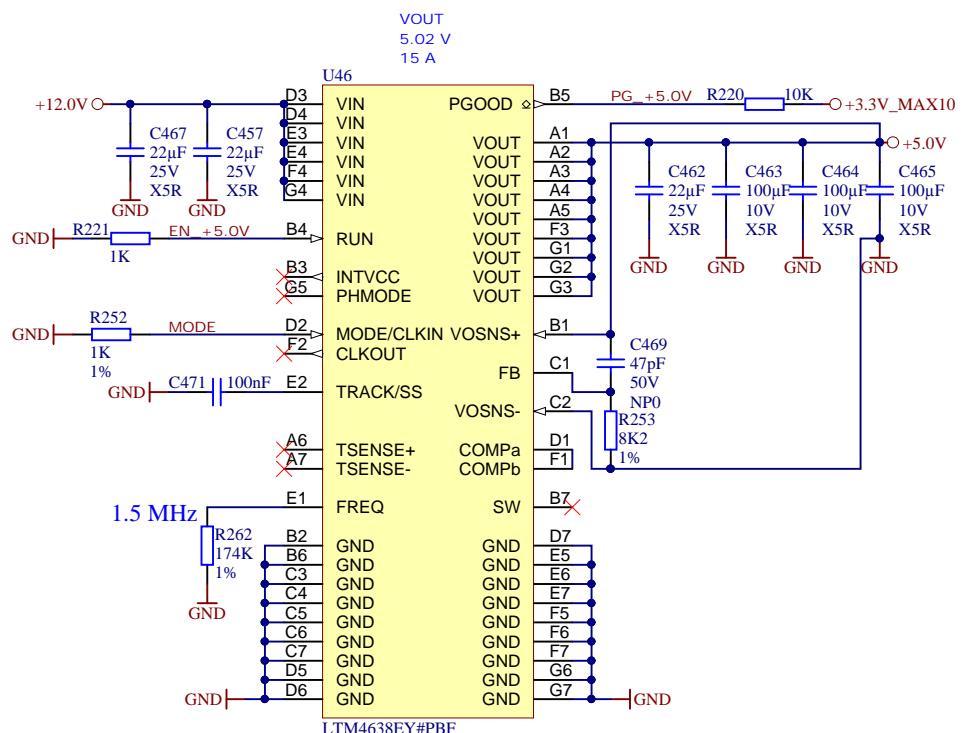
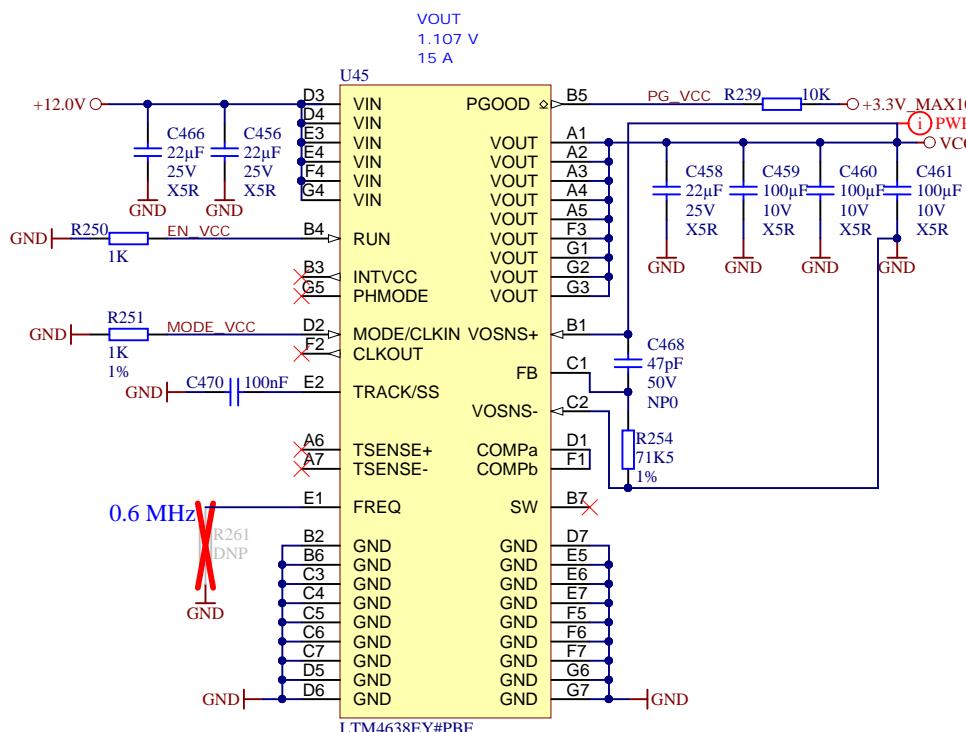
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2

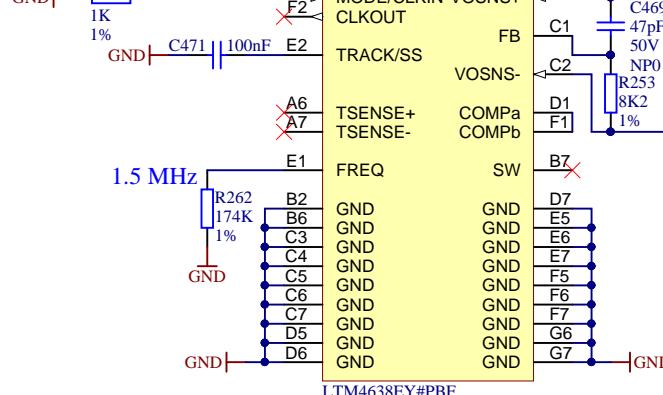
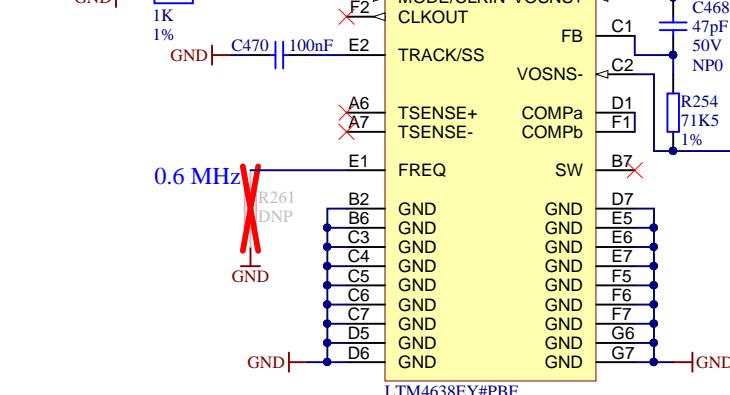
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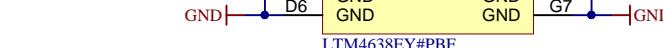
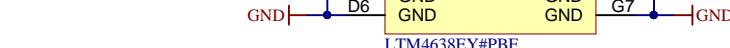
A



B



C



D



Title: Power2		
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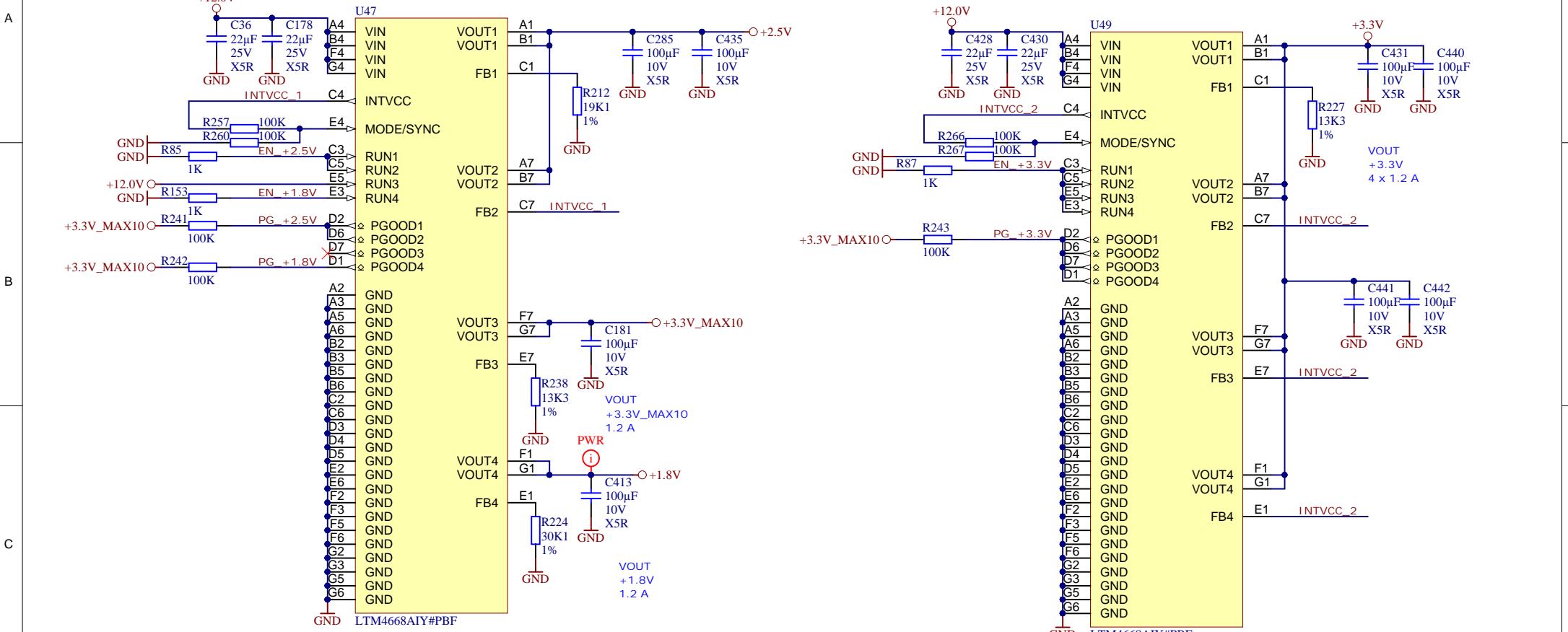
1

2

3

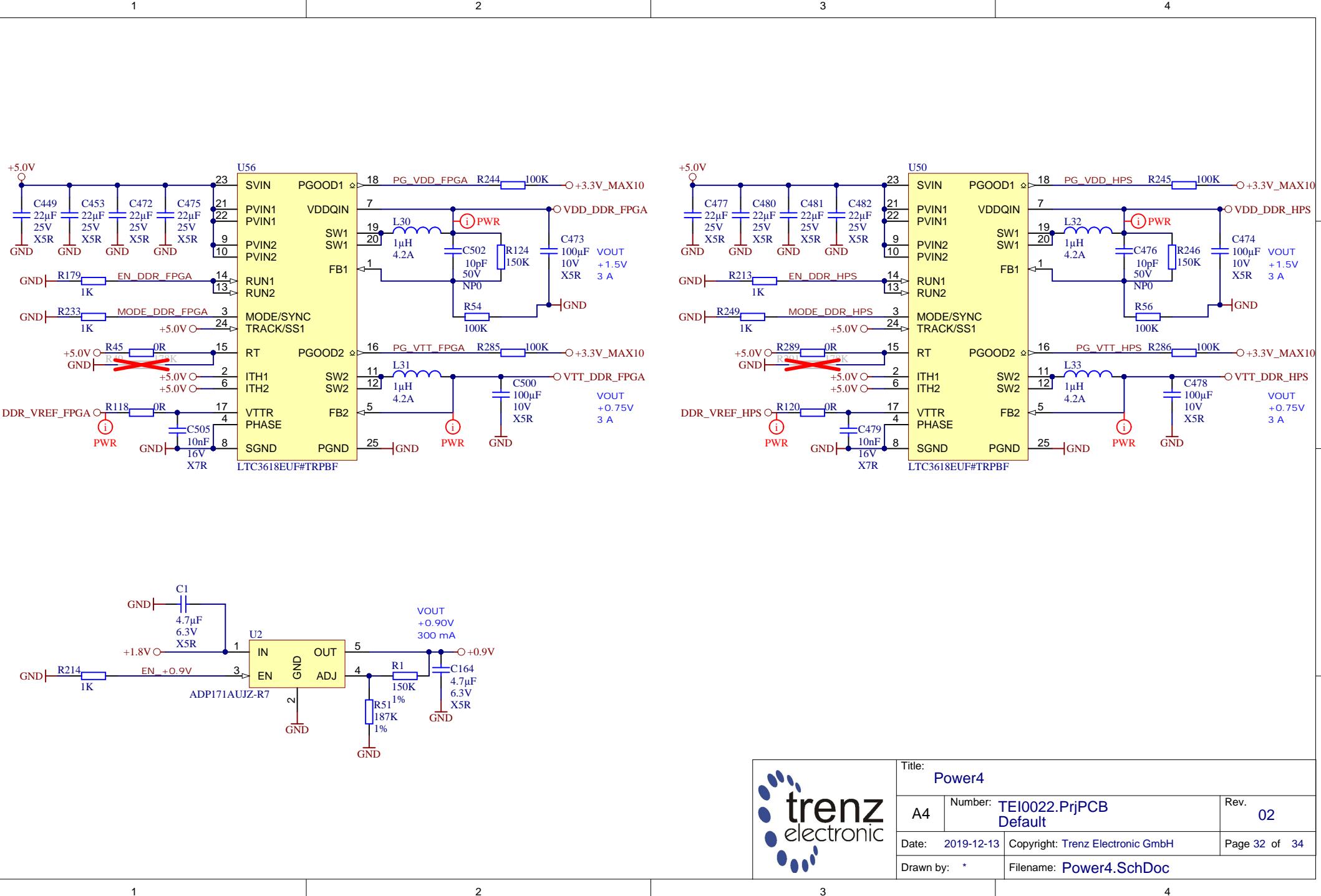
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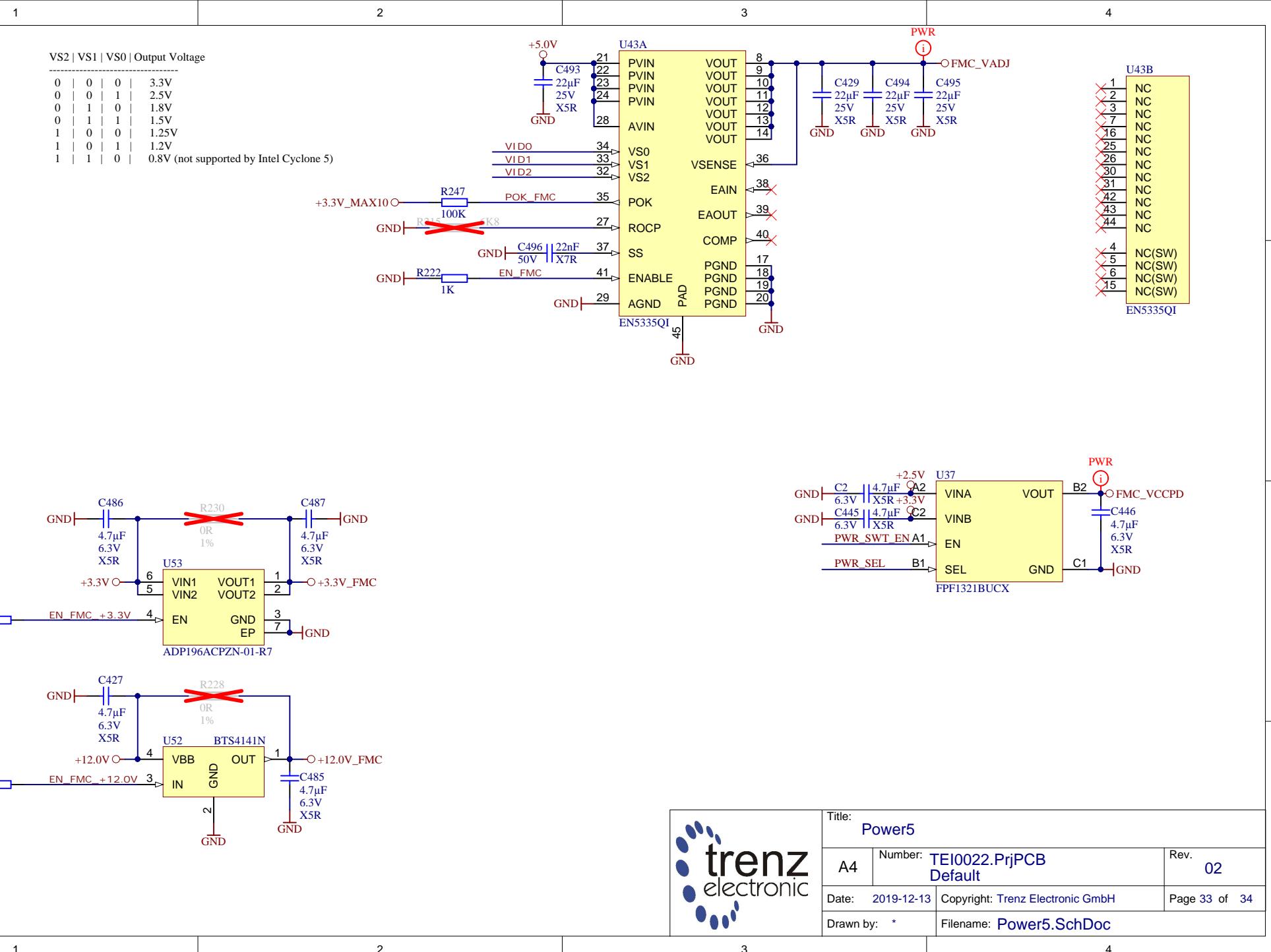
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1 2 3 4





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CHANGES REV01 to REV02

- Added "Revision_Changes.SchDoc"
 - Swapped FTDL_JTAG_TMS/CS and FTDL_JTAG_TDI/DO at MAX10 (JIRA GT-1064)

- Added "+12 V" comment in PCB
 - Added power in symbol and attention symbol in PCB
 - LED circuits changed (JIRA GT-1062)
 - FTDL LED polarity and resistors changed
 - Added pull-ups at OCS_N1...4 to "+3.3V"
 - Changed net name CLK_50MHz_MAX10 to CLK_MAX10
 - Changed net name HPS_CLK2_25MHz to HPS_CLK2
 - Changed C468 and C469 from 33 pF to 47 pF
 - Connected PG from U46 to MAX10
 - Pulled the MODE pins from U45, U46, U50, and U56 down
 - Changed net name "INTVCC_+5.0V" to "MODE"
 - Deleted nets "INTVCC_+5.0V"

- Disconnect nets "Link_ST", and "RX_ER" from Cyclone V
 - Inserted net "EN_+5.0V" for controlling DCDC U46
 - Changed the Power Supply Sequencing
 - Changed resistors for LEDs

- Changed MODE pin circuit from U47 and U49 (JIRA GT-1077)

- Added pull up for net "HPS_RST#_BO"
 - Added pull downs for net "MODE_DDR_HPS" and "MODE_DDR_FPGA"
 - Change pull down of net "FPGA_DDR_RESET" to pull up to "VDD_DDR_FPGA"
 - Change pull down of net "HPS_DDR_RESET" to pull up to "VDD_DDR_FPGA"
 - Deleted 100 Ohm resistor between nets "SMA_CLK_OUT_p" and "SMA_CLK_OUT_n"
 - Added zero Ohm resistor at U3 pin 2.
 - Added pull up for U2 pin HPS_PORSEL

- Changed resistor values from signals CONF_DONE_I, nCONFIG_I, and nSTATUS from 12k to 10k
 - Changed voltage divider resistor values of R268 and R269

- Connected ID of U8 to +3.3V via a 0 Ohm resistor

- Changed R42 from 8k06 Ohm to 10k Ohm

- Added resistor divider (R279 and R283) for Ethernet clock input

- Connected Ethernet reset to Intel MAX10

- Added cooler attachment (JIRA GT-1070)

- Changed transistor T3 circuit to component U37

- Swapped HDMI pins (JIRA GT-1079)

- Changed programmable clock (U3) to project specific clock

- Connected net "QSPI_RST" from Cyclone V to "+3.3V" via pull-up resistor

- Connected net "AS_RST" from Cyclone V to "+3.3V" via pull-up resistor

- Added pull-up resistor for net "ETH_MDC"

- Connect nets "GPIO2", "GPIO3", and "GPIO4" between MAX10 and Cyclone V

- Connect nets "THERM_N" and "ALERT_N" to Cyclone V bank 6A and changed pull-up to net "VDD_DDR_HPS"

- Connect nets "FPGA_RST#_SW" and "USER_BTN_SW" to MAX10 bank 8 and changed pull-up to net "+3.3V_MAX10"

- Delete nets "BCBUS4", "BCBUS5", "BCBUS6", and "BCBUS7"

- Connect USB HUB reset to MAX10 with net "USB_HUB_RST"

- Increased size of "ARROW" logo on PCB

- Add boxes for LEDs on PCB

- Change address on PCB

- Change revision on PCB

- Changed RJ45 connector

- Changed assembly option of C35, C80, C81, C120, C121, C426, D26, D29, D32, R210, R228, R230, R255, R264, R225, R239, R193, R265, R241, R242, R243, R244, R245, and R226

- Changed D11, D12, D13, D14, D18, D19, and D25 from active-low to active-high

- Change resistor value of R41 from 0 Ohm to 33 Ohm

- Connect net "USB_RST" to MAX10

- Insert resistors R207, R208, R209, and R284 to connect I2C HDMI with I2C HPS optionally

- Change net "PG_VDD_HPS" to "PG_DDR_HPS" and "PG_VDD_HPS"

- Insert R286 as pull-up for net "PG_VDD_HPS"

- Change net "PG_VDD_FPGA" to "PG_DDR_FPGA" and "PG_VDD_FPGA"

- Insert R285 as pull-up for net "PG_VDD_FPGA"

- Delete nets "BCBUS0" and "BCBUS3"



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