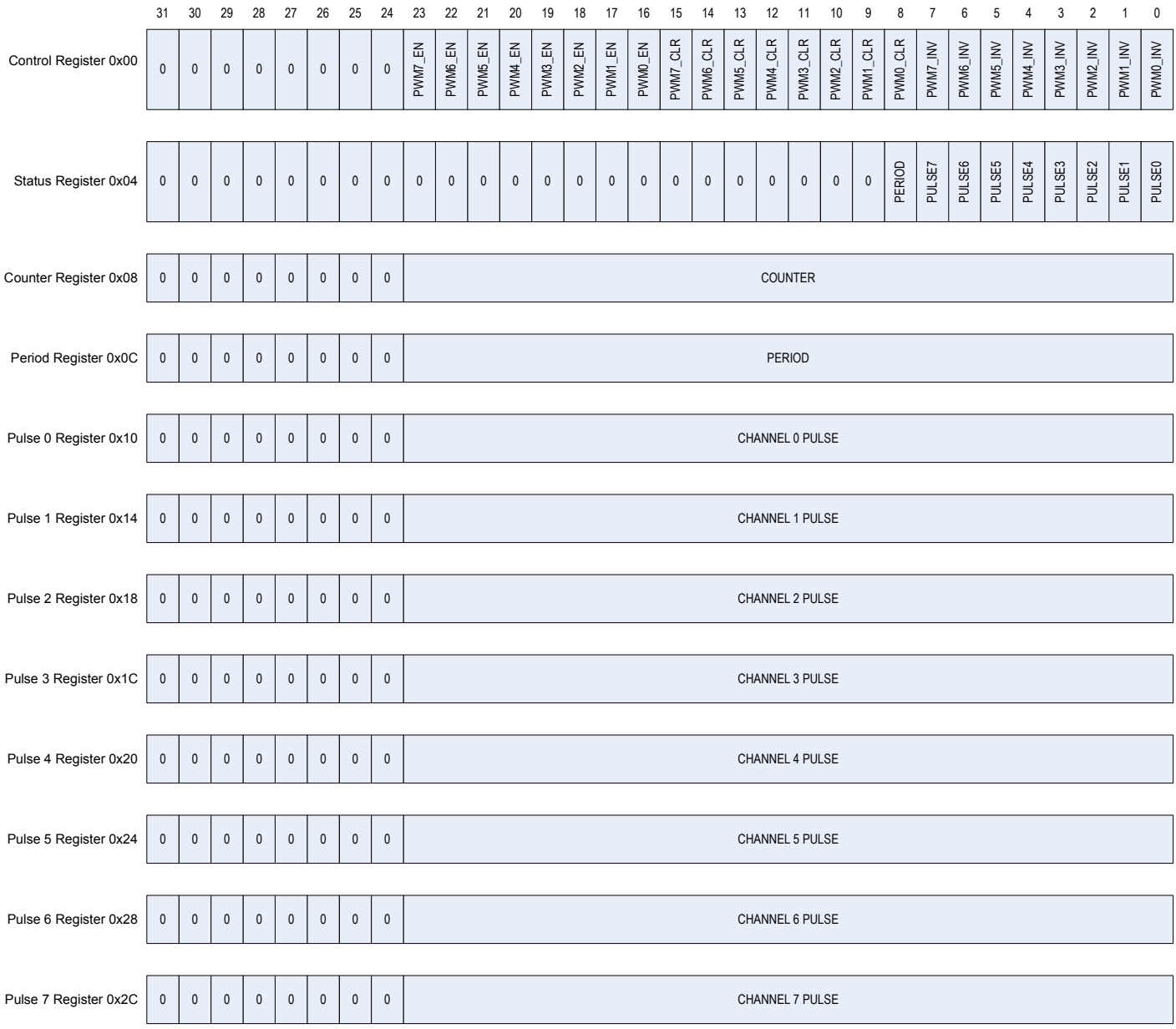

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Control Register 0x00	0	0	0	0	0	0	0	0	PWM7_EN	PWM6_EN	PWM5_EN	PWM4_EN	PWM3_EN	PWM2_EN	PWM1_EN	PWM0_EN	PWM7_CLR	PWM6_CLR	PWM5_CLR	PWM4_CLR	PWM3_CLR	PWM2_CLR	PWM1_CLR	PWM0_CLR	PWM7_INV	PWM6_INV	PWM5_INV	PWM4_INV	PWM3_INV	PWM2_INV	PWM1_INV	PWM0_INV
Status Register 0x04	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PERIOD	PULSE7	PULSE6	PULSE5	PULSE4	PULSE3	PULSE2	PULSE1	PULSE0
Counter Register 0x08	0	0	0	0	0	0	0	0	COUNTER																							
Period Register 0x0C	0	0	0	0	0	0	0	0	PERIOD																							
Pulse 0 Register 0x10	0	0	0	0	0	0	0	0	CHANNEL 0 PULSE																							
Pulse 1 Register 0x14	0	0	0	0	0	0	0	0	CHANNEL 1 PULSE																							
Pulse 2 Register 0x18	0	0	0	0	0	0	0	0	CHANNEL 2 PULSE																							
Pulse 3 Register 0x1C	0	0	0	0	0	0	0	0	CHANNEL 3 PULSE																							
Pulse 4 Register 0x20	0	0	0	0	0	0	0	0	CHANNEL 4 PULSE																							
Pulse 5 Register 0x24	0	0	0	0	0	0	0	0	CHANNEL 5 PULSE																							
Pulse 6 Register 0x28	0	0	0	0	0	0	0	0	CHANNEL 6 PULSE																							
Pulse 7 Register 0x2C	0	0	0	0	0	0	0	0	CHANNEL 7 PULSE																							

Status Register bits are cleared by writing a ‘1’ to them.