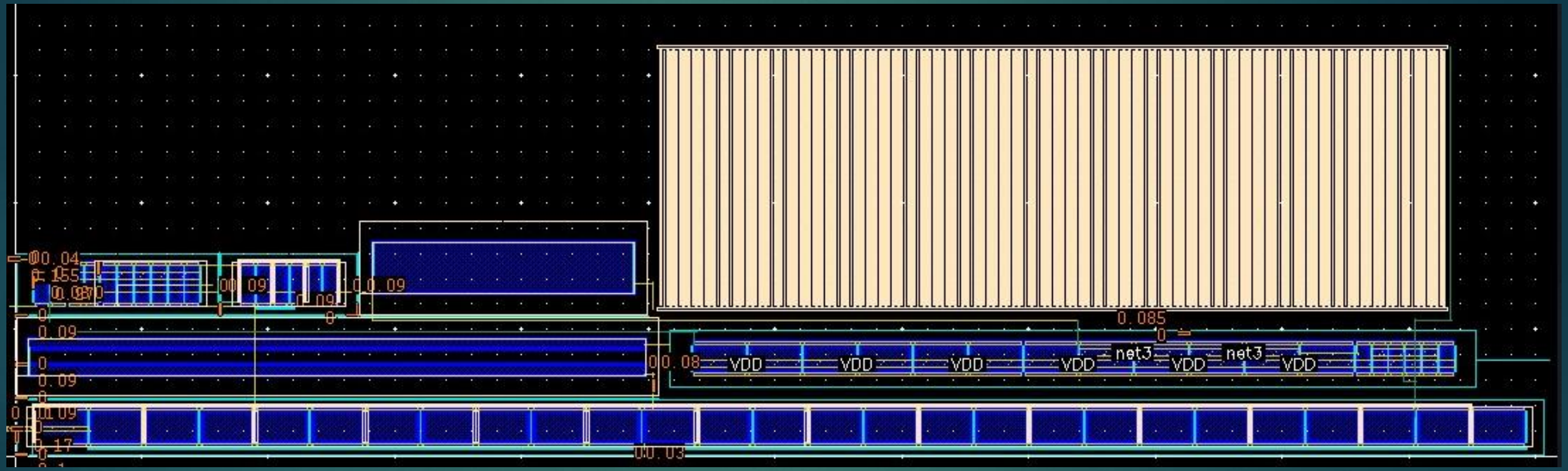
# LDO - Week 2

Previous Week:

- Met with Tal to discuss layout issues.
- Mostly completed the OTA layout design.
- The OTA layout passed LVS and DRC, except for one remaining error, which we are working with Tal to resolve.
- Extracted QRC but the OTA output is stuck at 0V in simulations.

This Week:

- Resolving the outstanding DRC issue.
- Finalizing the BGR layout.
- Running simulations to verify the layout.


0.085
0.08
VDD
VDD
VDD
VDD
net3
VDD
net3
VDD
0.09
0.09
0.09
0.09
0.09
0.09
0.04
0.03

```
##################################################
##                                              ##
##        C A L I B R E   S Y S T E M           ##
##                                              ##
##            L V S   R E P O R T               ##
##                                              ##
##################################################
```

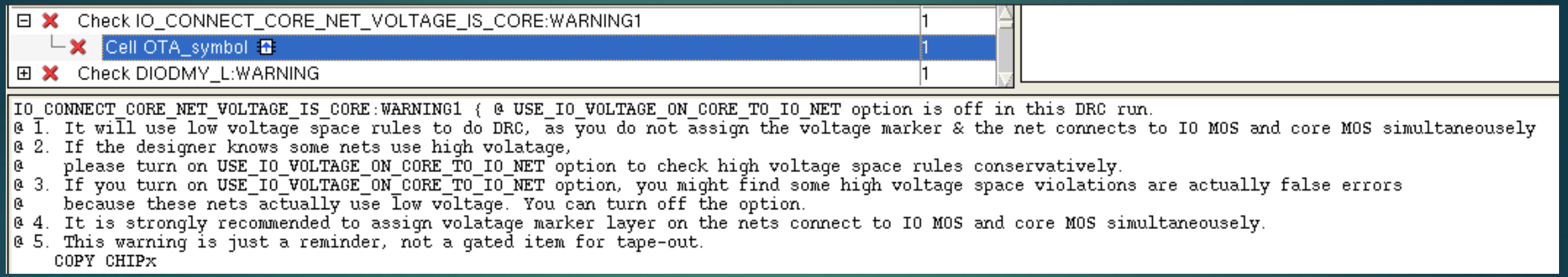
```
REPORT FILE NAME:         OTA.lvs.report
LAYOUT NAME:              OTA.sp ('OTA')
SOURCE NAME:              OTA.src.net ('OTA')
RULE FILE:                _DFM_LVS_RC_CALIBRE_N28HP_1p9M_5X1Y1Z1U_ALRDL.v1.0_3p_
CREATION TIME:            Wed Mar 26 19:10:41 2025
CURRENT DIRECTORY:        /project/tsmc28mmwave/users/yaishorf/ws/calibrelvs/OTA
USER NAME:                yaishorf
CALIBRE VERSION:          v2022.1_36.16    Tue Mar 1 14:26:36 PST 2022
```

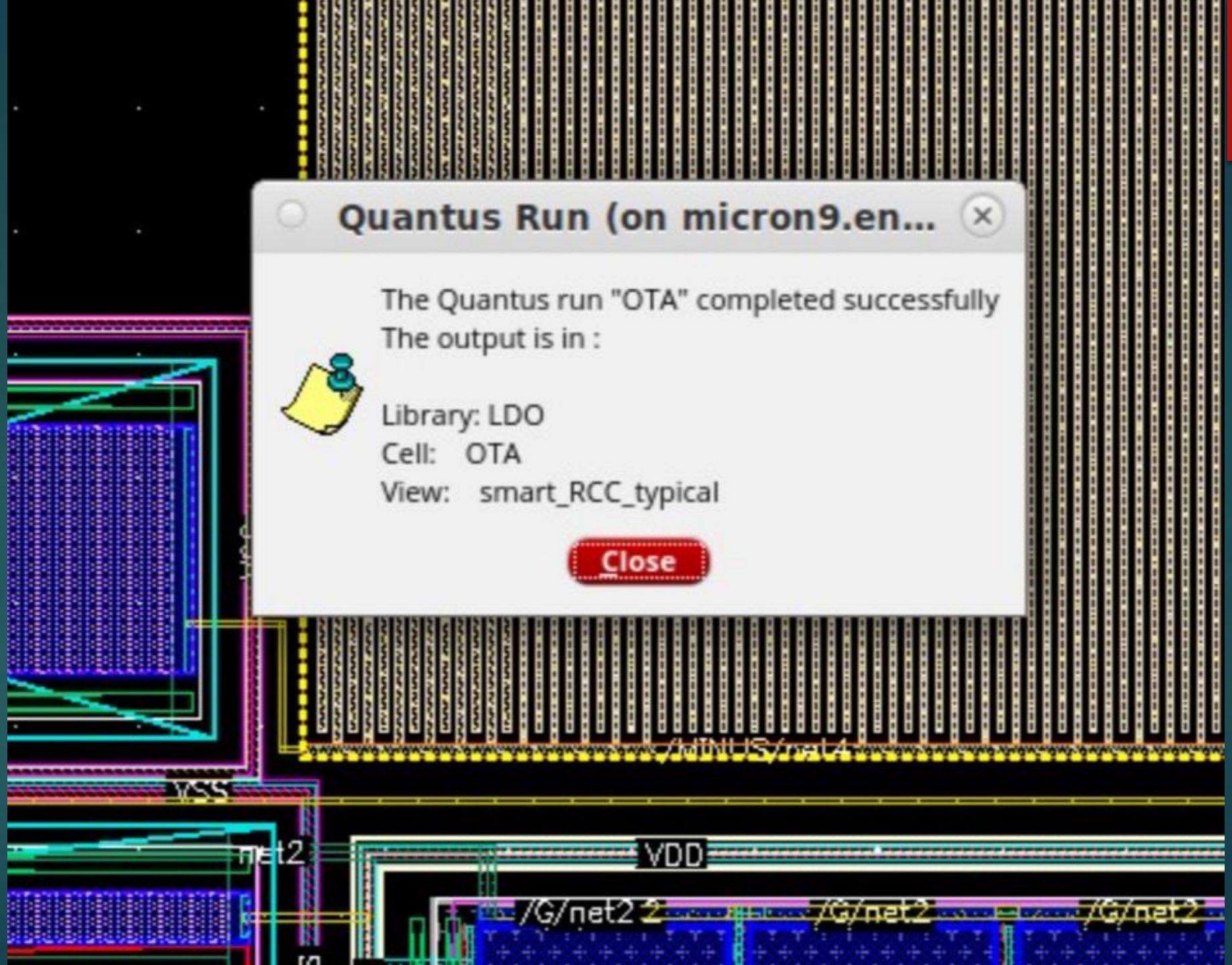
OVERALL COMPARISON RESULTS


```
*****************************************************************************************************************
                                        CELL  SUMMARY
*****************************************************************************************************************

  Result          Layout                        Source
  -----------     -----------                   --------------
  CORRECT         OTA                           OTA


*****************************************************************************************************************
                                        LVS PARAMETERS
*****************************************************************************************************************
```


Check IO_CONNECT_CORE_NET_VOLTAGE_IS_CORE:WARNING1
1
Cell OTA_symbol
1
Check DIODMY_L:WARNING
1
IO_CONNECT_CORE_NET_VOLTAGE_IS_CORE:WARNING1 { @ USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option is off in this DRC run.
@ 1. It will use low voltage space rules to do DRC, as you do not assign the voltage marker & the net connects to IO MOS and core MOS simultaneously
@ 2. If the designer knows some nets use high volatage,
@ please turn on USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option to check high voltage space rules conservatively.
@ 3. If you turn on USE_IO_VOLTAGE_ON_CORE_TO_IO_NET option, you might find some high voltage space violations are actually false errors
@ because these nets actually use low voltage. You can turn off the option.
@ 4. It is strongly recommended to assign volatage marker layer on the nets connect to IO MOS and core MOS simultaneously.
@ 5. This warning is just a reminder, not a gated item for tape-out.
COPY CHIPx


Quantus Run (on micron9.en...
The Quantus run "OTA" completed successfully
The output is in :
Library: LDO
Cell: OTA
View: smart_RCC_typical
Close
VSS
net2
VDD
/G/net2
/G/net2
/G/net2