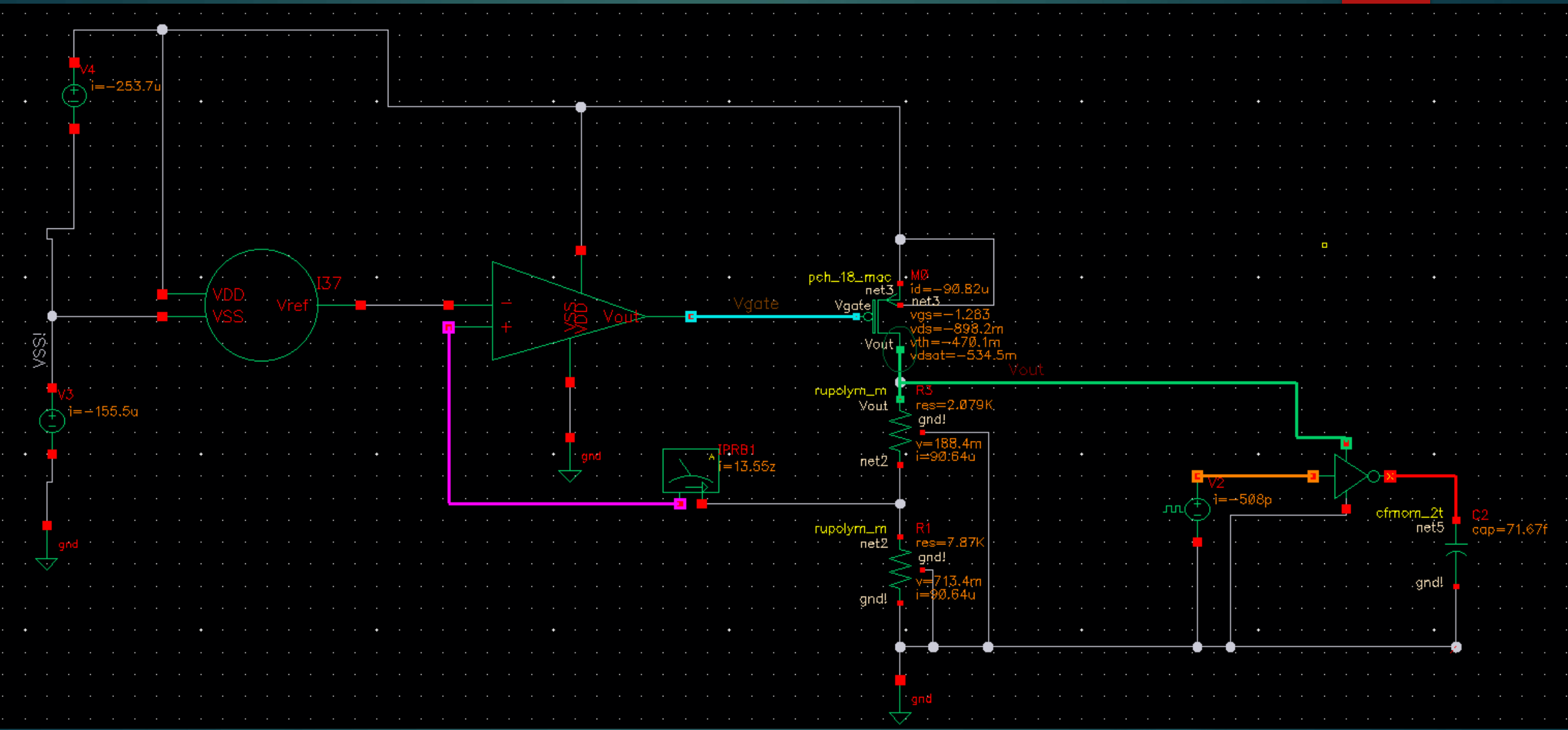
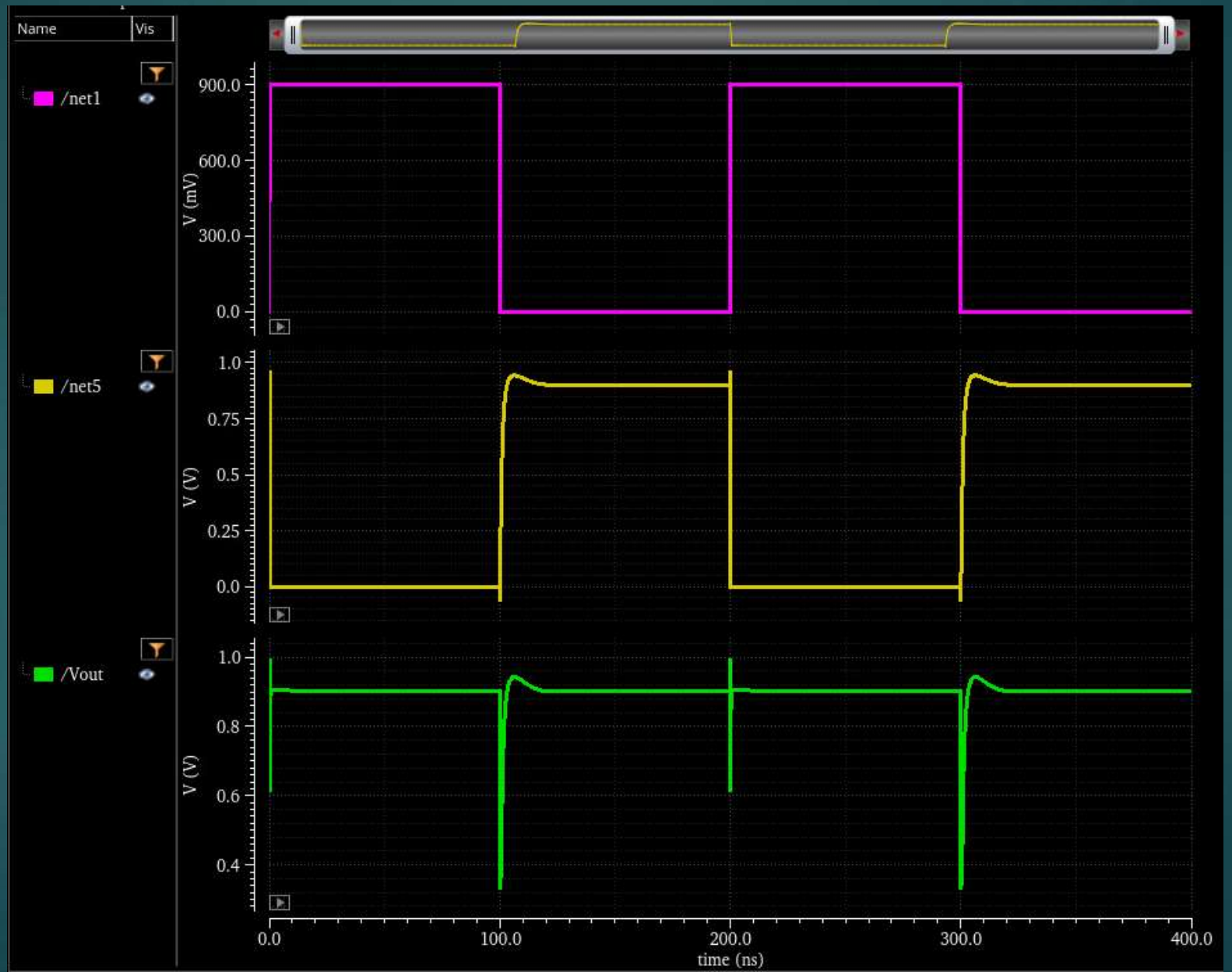
LDO

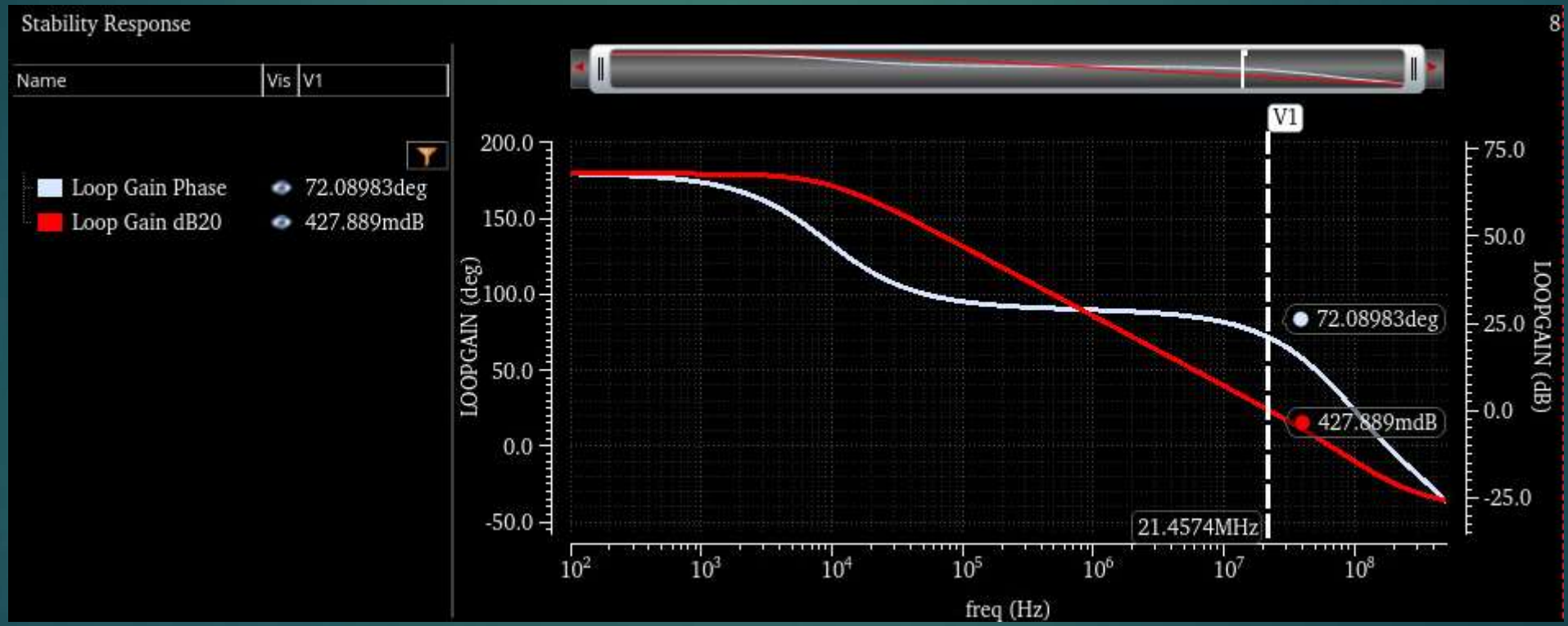

V4
i=-253.7u
VDD
VSS
Vref
I37
VSS!
V3
i=-155.5u
gnd
gnd
Vout
Vgate
pch_18_mac
M0
id=-90.82u
net3
Vgate
net3
vgs=-1.283
vds=-898.2m
Vout
vth=-470.1m
vdsat=-534.5m
Vout
rupolym_m
R3
Vout
res=2.079K
gnd!
v=188.4m
i=90.64u
net2
IPRB1
i=13.55z
rupolym_m
R1
net2
res=7.87K
gnd!
v=713.4m
i=90.64u
gnd!
gnd
V2
i=-508p
cfmom_2t
net5
C2
cap=71.67f
gnd!

LDO – Transient Response

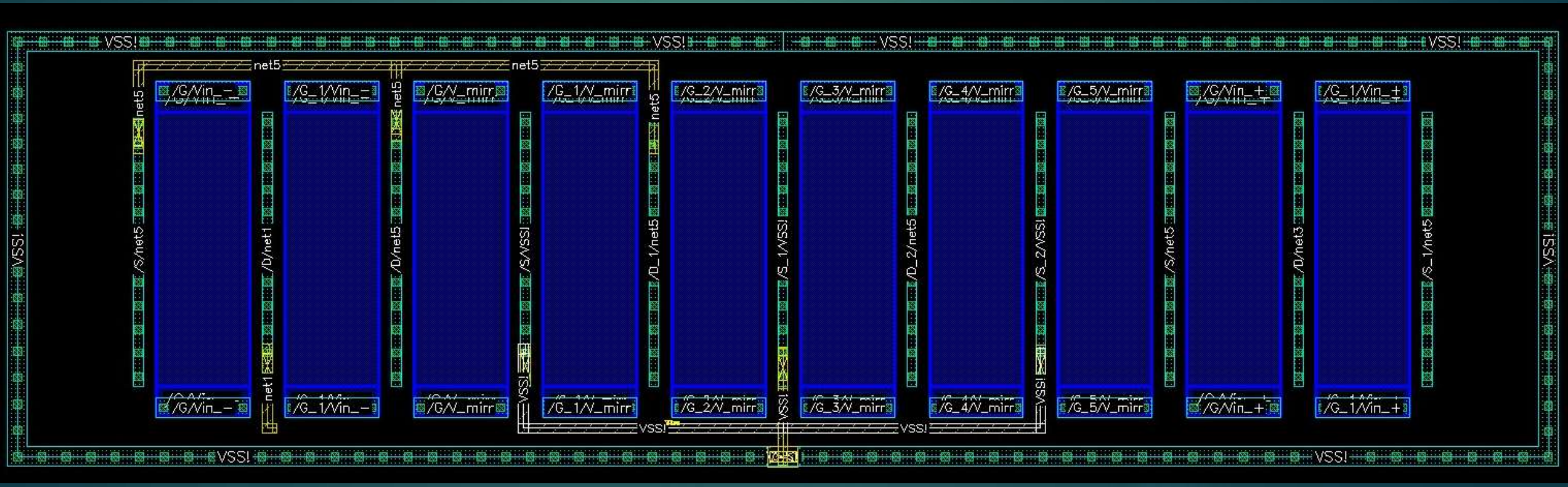


LDO – Frequency Response

Phase Margin = 71.37 (Deg) @ freq = 22.34M (Hz)
Gain Margin = 19.9 (dB) @ freq = 177.8M (Hz)



- What is the maximum switching frequency? In GHz?
- What should be the average current of the LDO? What is the maximal current?

OTA

Started working on the layout of the OTA.
Currently trying to abut all transistors, still encountering some difficulties in matching their widths.
Objective now is to complete OTA & BGR layouts until mid-late Feb.