LDO

Previous Week:

• Completed a preliminary layout design of the LDO. Results were tolerable but IR drop of 5mV impaired load regulation.

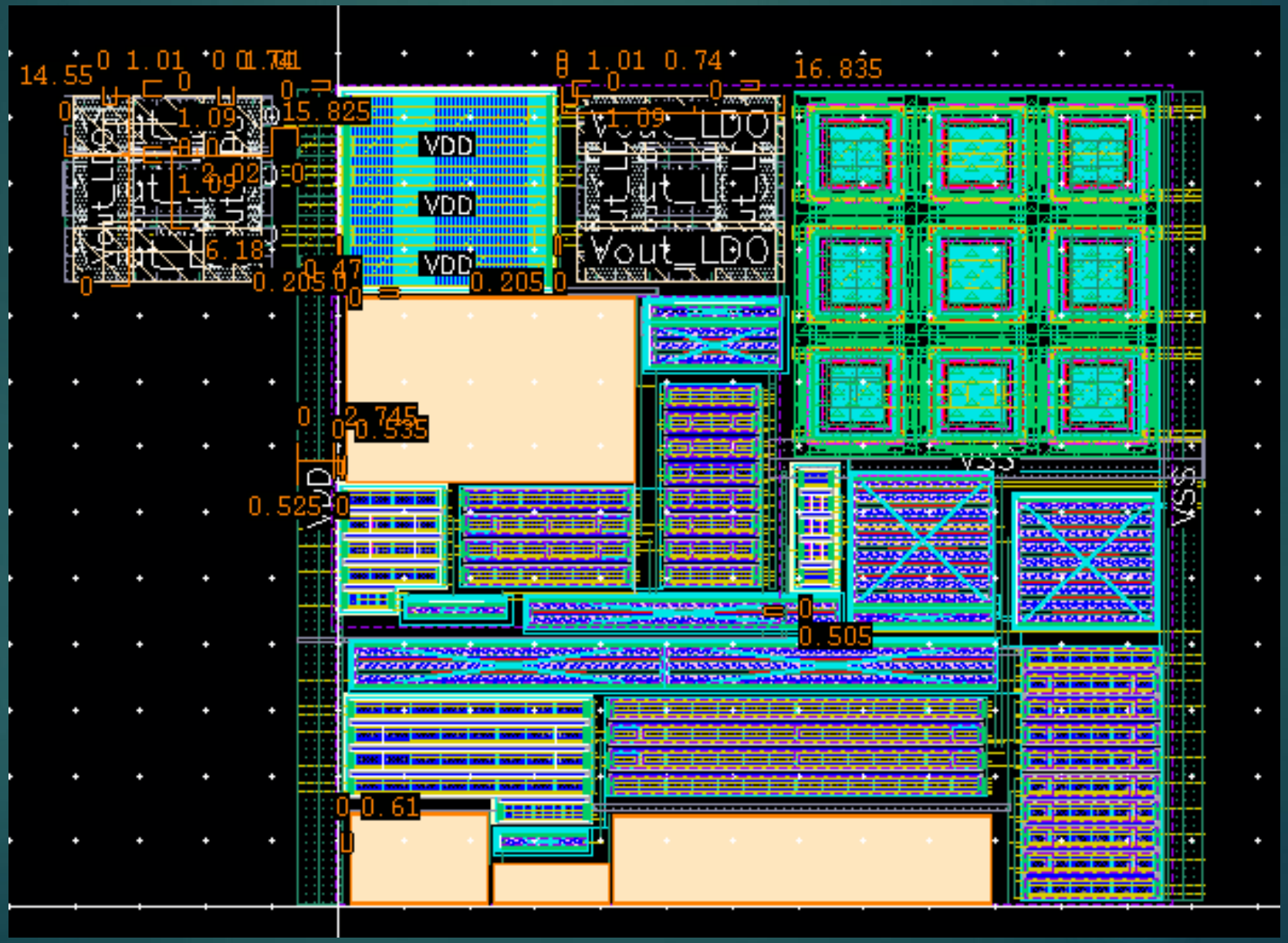
• Met with Pini to review the layout — need to redo the pass transistor part more carefully.

Next:

• Improving the LDO layout to minimize IR drop.

LDO - Layout

69 x 63



LDO – Results Comparison

LDO_TC_TEST	/LDO_Vout				
LDO_TC_TEST	Vout_vs_Temp	926.7u			
LDO_TC_TEST	av_Vout_vs_Temp	900.3m			
LDO_TC_TEST	TC	6.239	< 60		pass
LDO_TC_TEST_layout	Vout_vs_Temp	1.216m			
LDO_TC_TEST_layout	av_Vout_vs_Temp	895.9m			
LDO_TC_TEST_layout	TC	8.229	< 60		pass
LDO_TC_TEST_layout	/LDO_Vout_1				
LDO_Line_Reg_TEST	/LDO_Vout				
LDO_Line_Reg_TEST	Vout_vs_VDD	873.4u			
LDO_Line_Reg_TEST	av_Vout_vs_VDD	900m			
LDO_Line_Reg_TEST	LINE_REG	1.456m	< 0.01		pass
LDO_Line_Reg_TEST_layout	/LDO_Vout_1				
LDO_Line_Reg_TEST_layout	Vout_vs_VDD_1	769.1u			
LDO_Line_Reg_TEST_layout	av_Vout_vs_VDD...	895.6m			
LDO_Line_Reg_TEST_layout	LINE_REG_1	1.282m	< 0.01		pass
LDO_Load_Reg_TEST	/LDO_Vout_LOAD				
LDO_Load_Reg_TEST	Vout_vs_LOAD	130.4u			
LDO_Load_Reg_TEST	av_Vout_vs_LOAD	900.1m			
LDO_Load_Reg_TEST	LOAD_REG	2.173m	< 0.1		pass
LDO_Load_Reg_TEST_layout	/LDO_Vout_LOA...				
LDO_Load_Reg_TEST_layout	Vout_vs_LOAD_1	5.44m			
LDO_Load_Reg_TEST_layout	av_Vout_vs_LOA...	897.5m			
LDO_Load_Reg_TEST_layout	LOAD_REG_1	90.66m	< 0.1		pass