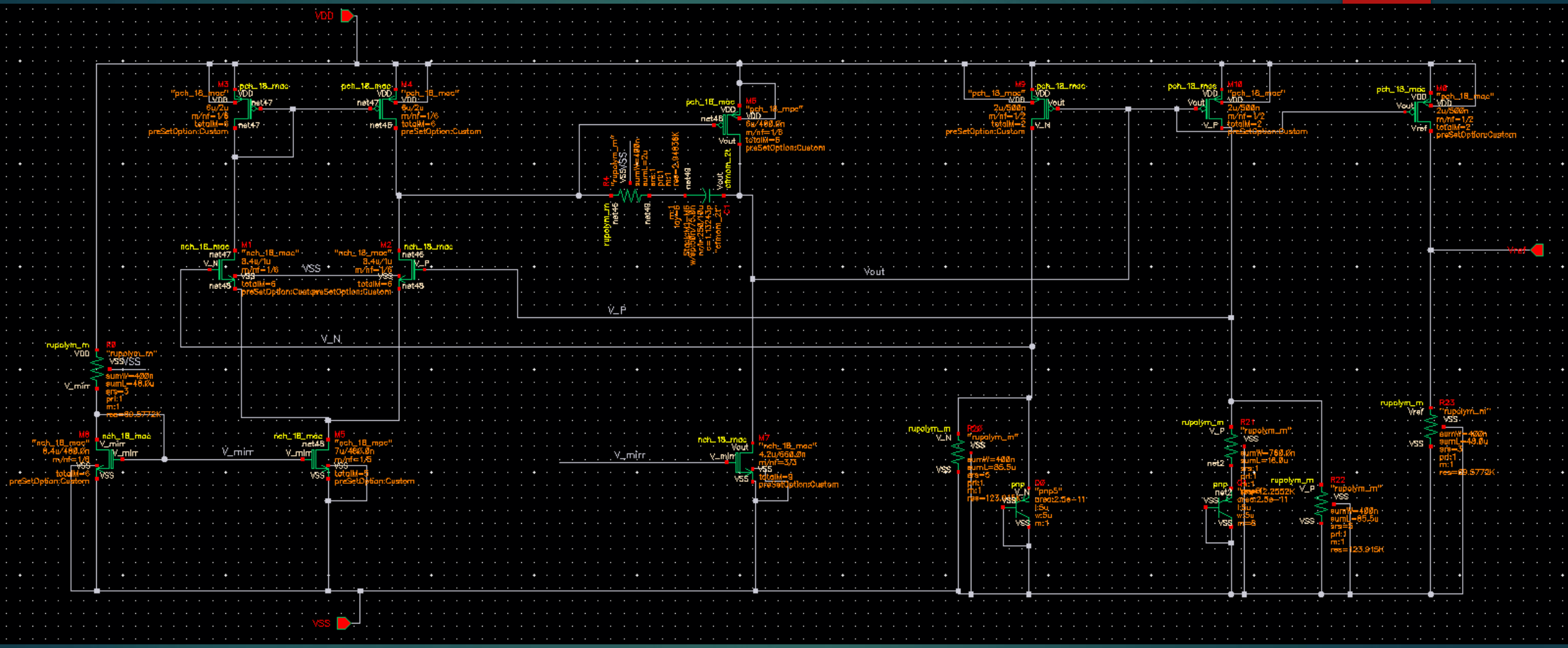
LDO

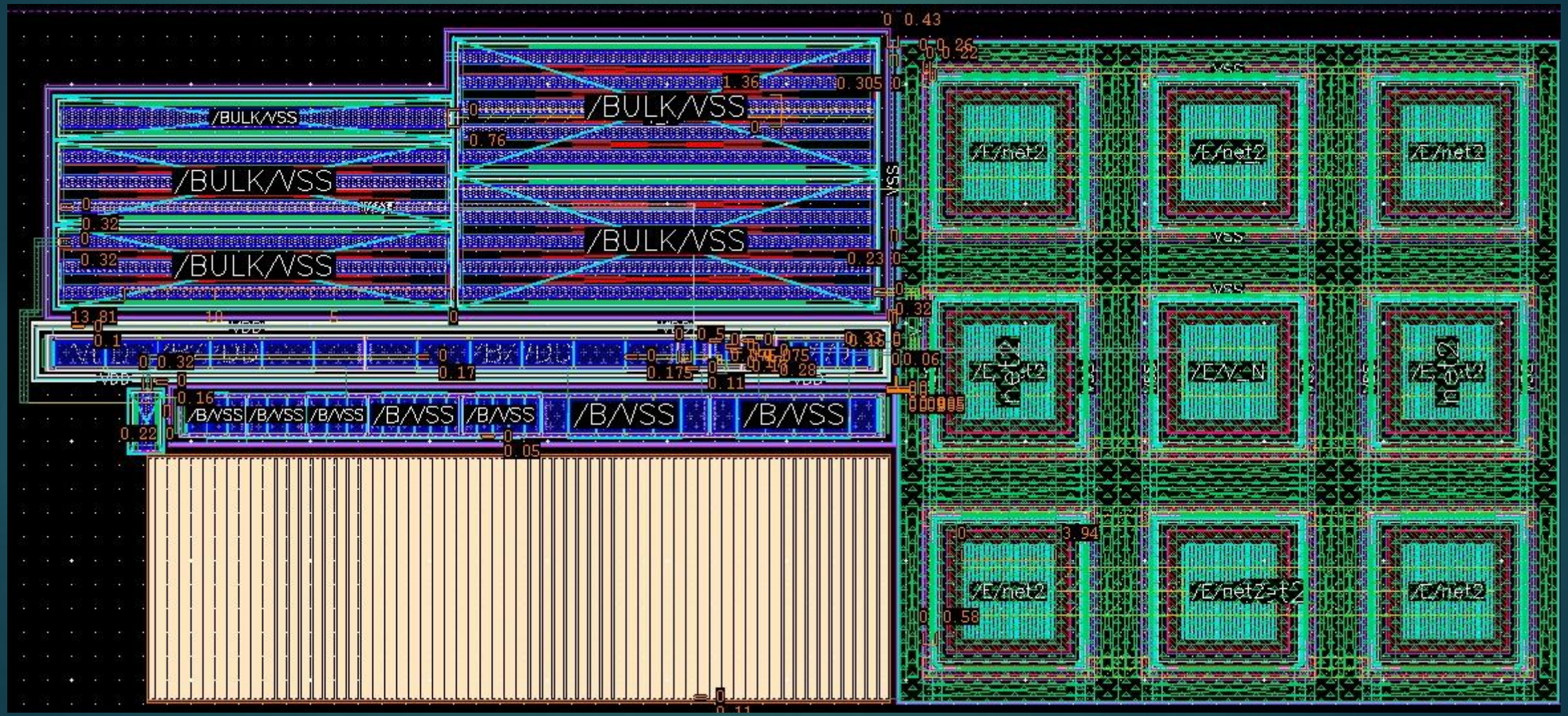
Previous Week:

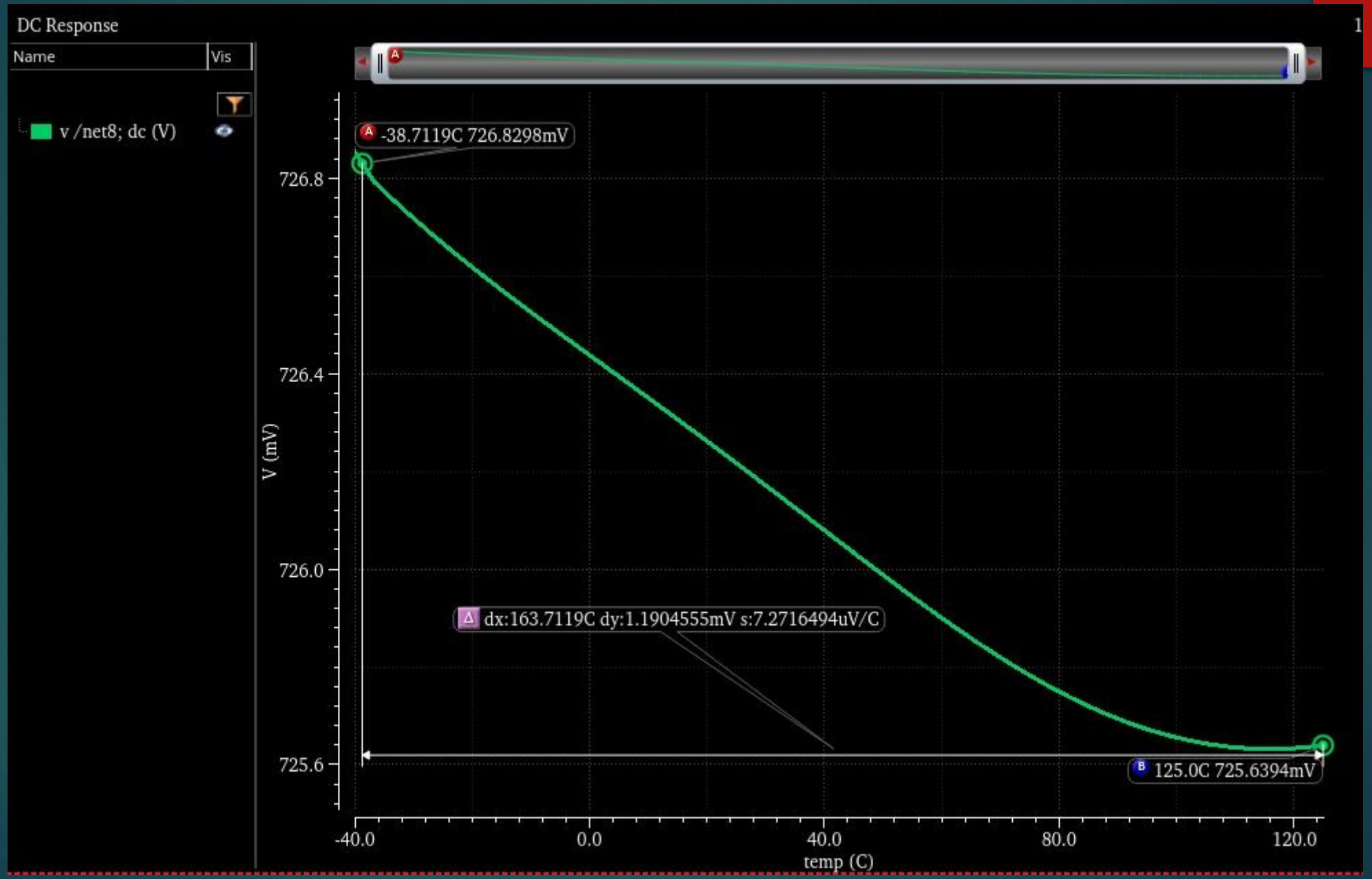
- Completed two additional OTA layouts, focusing on placing dummy transistors to improve matching and ensure symmetry between devices, as well as keeping metals as direct as possible with minimal bends. Simulation results post-layout were poor.
- Met with Pini to analyze possible causes — advised further layout improvements and additional dummies.
- Question – VSS?

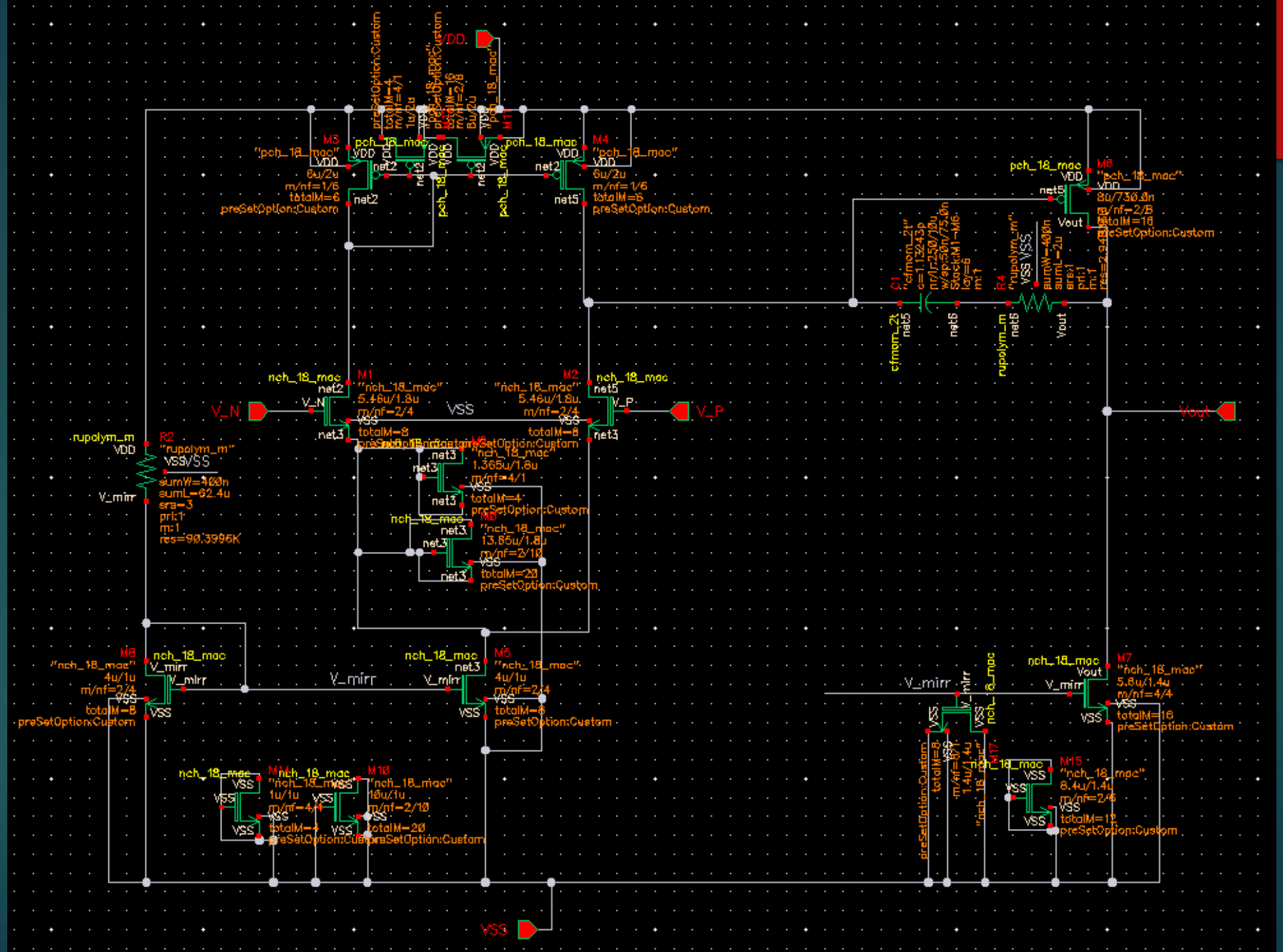
Next:

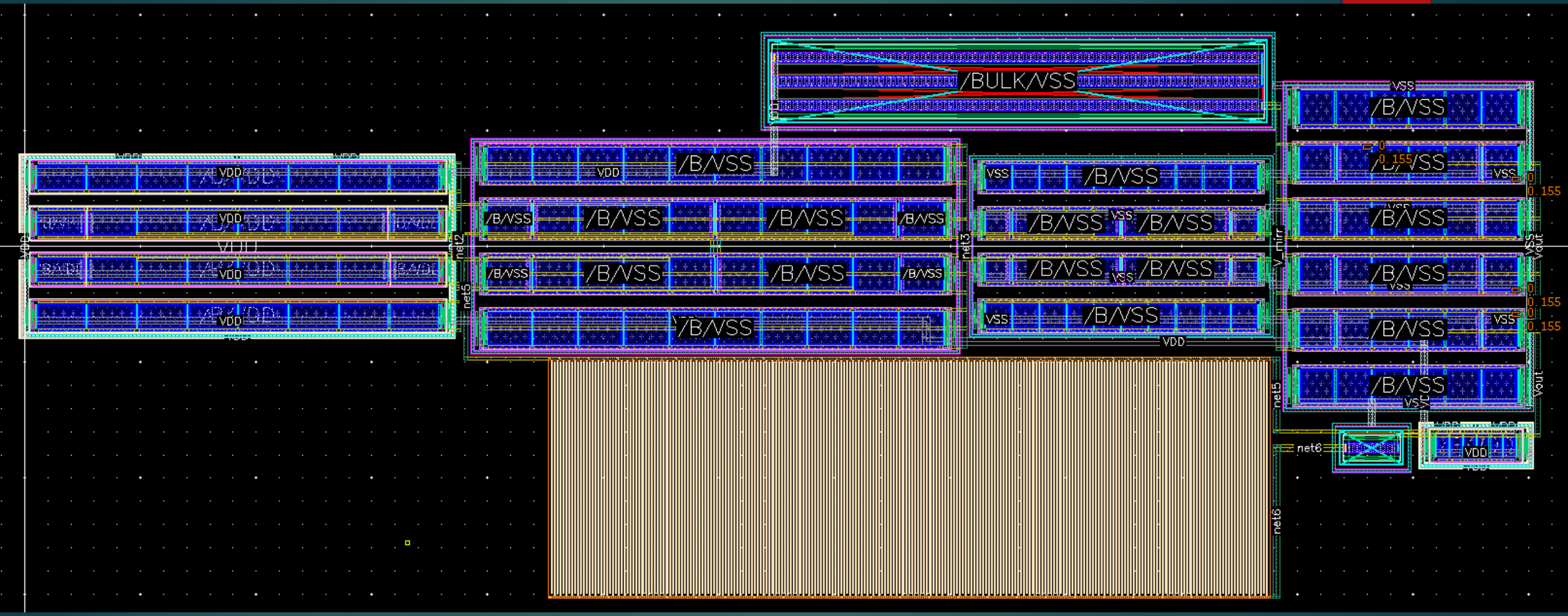
- Continue refining OTA and BGR layouts to improve post-layout performance.

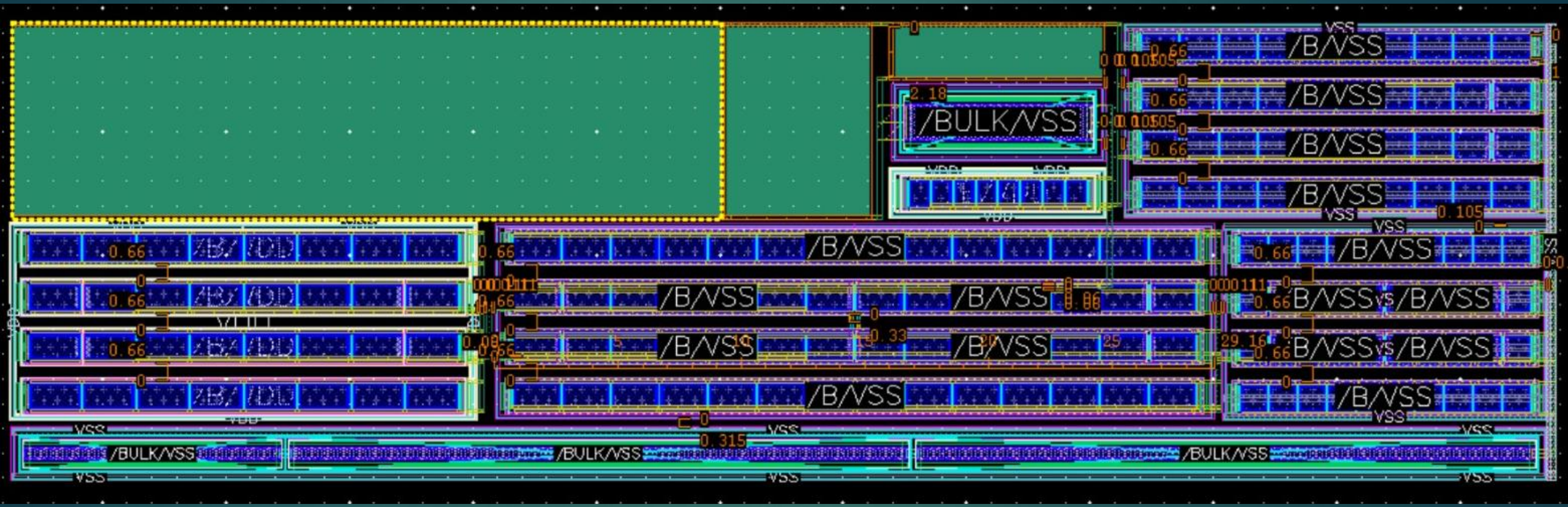

VDD
VSS
Vout
V_P
V_N
V_mirr
Vref
M1 "nch_18_mac" 8.4u/1u m/nf=1/6 totalM=6 preSetOption:Custom
M2 "nch_18_mac" 8.4u/1u m/nf=1/6 totalM=6 preSetOption:Custom
M3 "pch_18_mac" 6u/2u m/nf=1/6 totalM=6 preSetOption:Custom
M4 "pch_18_mac" 6u/2u m/nf=1/6 totalM=6 preSetOption:Custom
M5 "pch_18_mac" 6u/400.0n m/nf=1/6 totalM=6 preSetOption:Custom
M6 "nch_18_mac" 4.2u/660.0n m/nf=3/3 totalM=6 preSetOption:Custom
M7 "nch_18_mac" 4.2u/660.0n m/nf=3/3 totalM=6 preSetOption:Custom
M8 "nch_18_mac" 8.4u/400.0n m/nf=1/6 totalM=6 preSetOption:Custom
M9 "pch_18_mac" 2u/500n m/nf=1/2 totalM=2 preSetOption:Custom
M10 "pch_18_mac" 2u/500n m/nf=1/2 totalM=2 preSetOption:Custom
M11 "pch_18_mac" 2u/500n m/nf=1/2 totalM=2 preSetOption:Custom
R0 "rupolym_m" sumW=400n sumL=46.0u srs=3 prl:1 m:1 res=29.5772K
R20 "rupolym_m" sumW=400n sumL=85.5u srs=5 prl:1 m:1 res=123.915K
R21 "rupolym_m" sumW=760.0n sumL=16.0u srs=1 prl:1 m:1 res=412.2552K
R22 "rupolym_m" sumW=400n sumL=85.5u srs=5 prl:1 m:1 res=123.915K
R23 "rupolym_m" sumW=400n sumL=46.0u srs=3 prl:1 m:1 res=29.5772K
D0 "pnp5" area=2.5e-11 l=5u w=5u m=1
D1 "pnp5" area=2.5e-11 l=5u w=5u m=6


/BULK/VSS
/BULK/VSS
/BULK/VSS
/BULK/VSS
/BULK/VSS
/E/net2
/E/net2
/E/net2
/E/net2
/E/net2
/E/net2
/E/net2
/E/net2
/E/net2
VSS
VSS
VSS
VDD
VDD
/B/VSS
/B/VSS
/B/VSS
/B/VSS
/B/VSS
/B/VSS
/B/VSS


DC Response
Name
Vis
v /net8; dc (V)
A -38.7119C 726.8298mV
726.8
726.4
726.0
725.6
V (mV)
Δ dx:163.7119C dy:1.1904555mV s:7.2716494uV/C
B 125.0C 725.6394mV
-40.0
0.0
40.0
80.0
120.0
temp (C)


VDD
M3
"pch_18_mac"
6u/2u
m/nf=1/6
totalM=6
preSetOption:Custom
M4
"pch_18_mac"
6u/2u
m/nf=1/6
totalM=6
preSetOption:Custom
M8
"pch_18_mac"
80/730.8n
m/nf=2/8
totalM=16
preSetOption:Custom
C1
"cfmom_2t"
c=1.13243p
nr/lr=250/10u
wsp:50n/75.8n
Stack:M1-M6
lay=6
m:1
R4
"rupolym_m"
sumW=400n
sumL=2u
are:1
pri:1
m:1
res=2.944K
cfmom_2t
net5
net6
rupolym_m
net6
Vout
V_N
V_P
Vout
M1
"nch_18_mac"
5.46u/1.8u
m/nf=2/4
totalM=8
M2
"nch_18_mac"
5.46u/1.8u
m/nf=2/4
totalM=8
R2
"rupolym_m"
sumW=400n
sumL=62.4u
sra=3
pri:1
m:1
res=90.3996K
V_mirr
M9
"nch_18_mac"
1.365u/1.8u
m/nf=4/1
totalM=4
preSetOption:Custom
M10
"nch_18_mac"
13.65u/1.8u
m/nf=2/10
totalM=20
preSetOption:Custom
M6
"nch_18_mac"
4u/1u
m/nf=2/4
totalM=8
preSetOption:Custom
M7
"nch_18_mac"
5.8u/1.4u
m/nf=4/4
totalM=16
preSetOption:Custom
M14
"nch_18_mac"
1u/1u
m/nf=4/4
totalM=4
preSetOption:Custom
M10
"nch_18_mac"
10u/1u
m/nf=2/10
totalM=20
preSetOption:Custom
M15
"nch_18_mac"
8.4u/1.4u
m/nf=2/6
totalM=12
preSetOption:Custom
VSS


/BULK/VSS
VDD
/B/VSS
VSS
net2
net3
net5
net6
V_mirr
Vout
0.155


/BULK/VSS
/B/VSS
VSS
VDD
0.66
0.105
0.315
2.18