LDO

Previous Week:

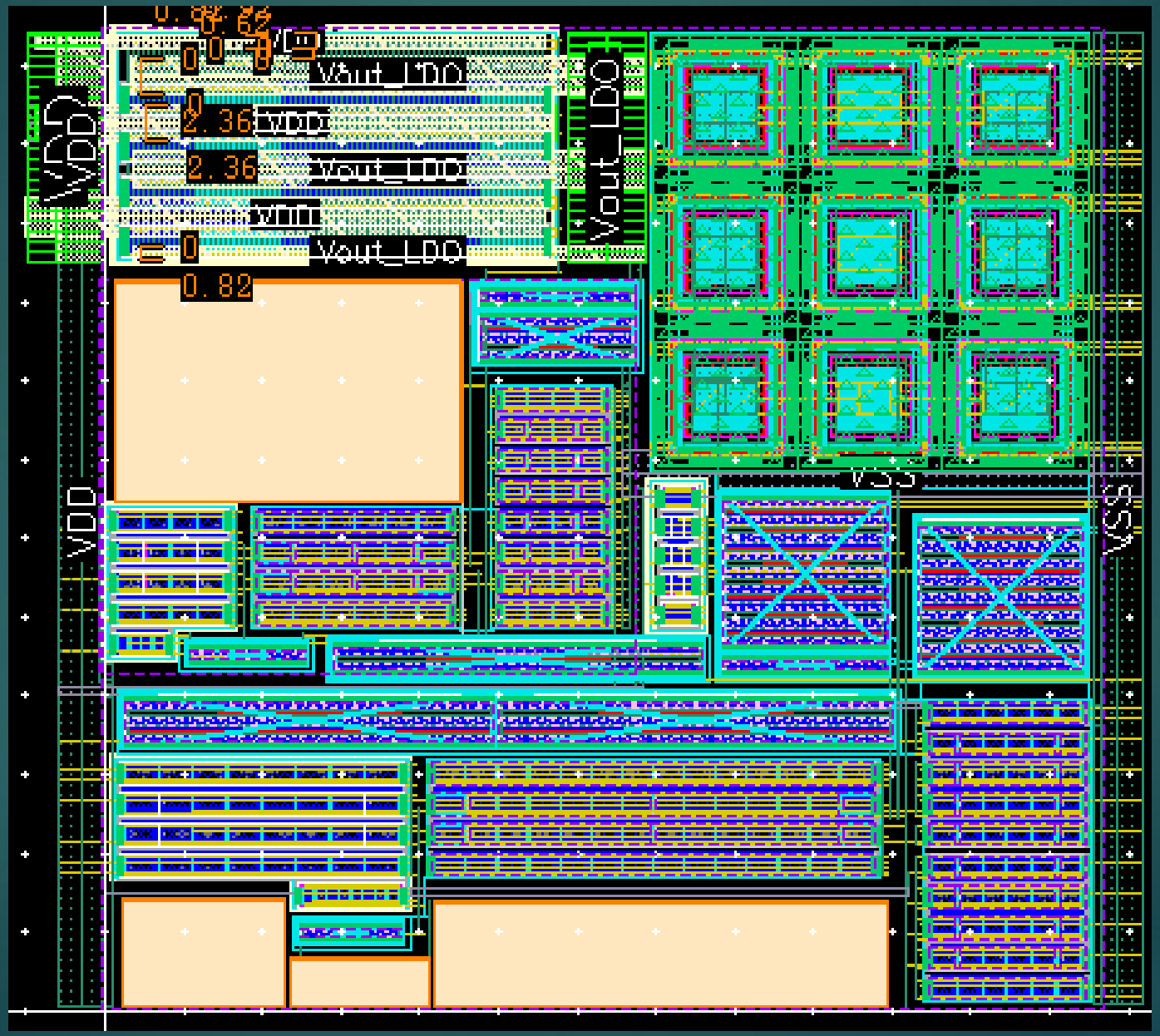
- Implemented metal stacking to decrease the IR Drop in the LDO layout. Voltage drop performance improved threefold.
- Verified dynamic parameters – PSRR, output noise, and transient stability using a 10ps pulse (1.8V to 0V) on VDD to check settling time.

Next:

- Finishing project deliverables and documentation.

LDO - Layout

71 x 62



LDO – Results

Parameter	This Work	Schematic
Process	28nm	28nm
Layout Area (mm^2)	0.0044	N/A
Supply Voltage V_{DD} (V)	1.38–3	1.2–3
Output Voltage V_{OUT} (V)	0.9	0.9
Load Current I_{Load} (mA)	55.5	55.5
Quiescent Current I_Q (μA)	80	80
Line Regulation (mV/V)	0.9	0.9
Load Regulation (mV/mA)	0.032	0.002
Temperature Coefficient (ppm/°C)	6.4	6.2
PSRR (dB @1kHz)	-60.8	-60.7
Output Noise (nV/$\sqrt{Hz}$ @100kHz)	672	–
Settling Time - Worst Case (μs)	0.7	–