LDO

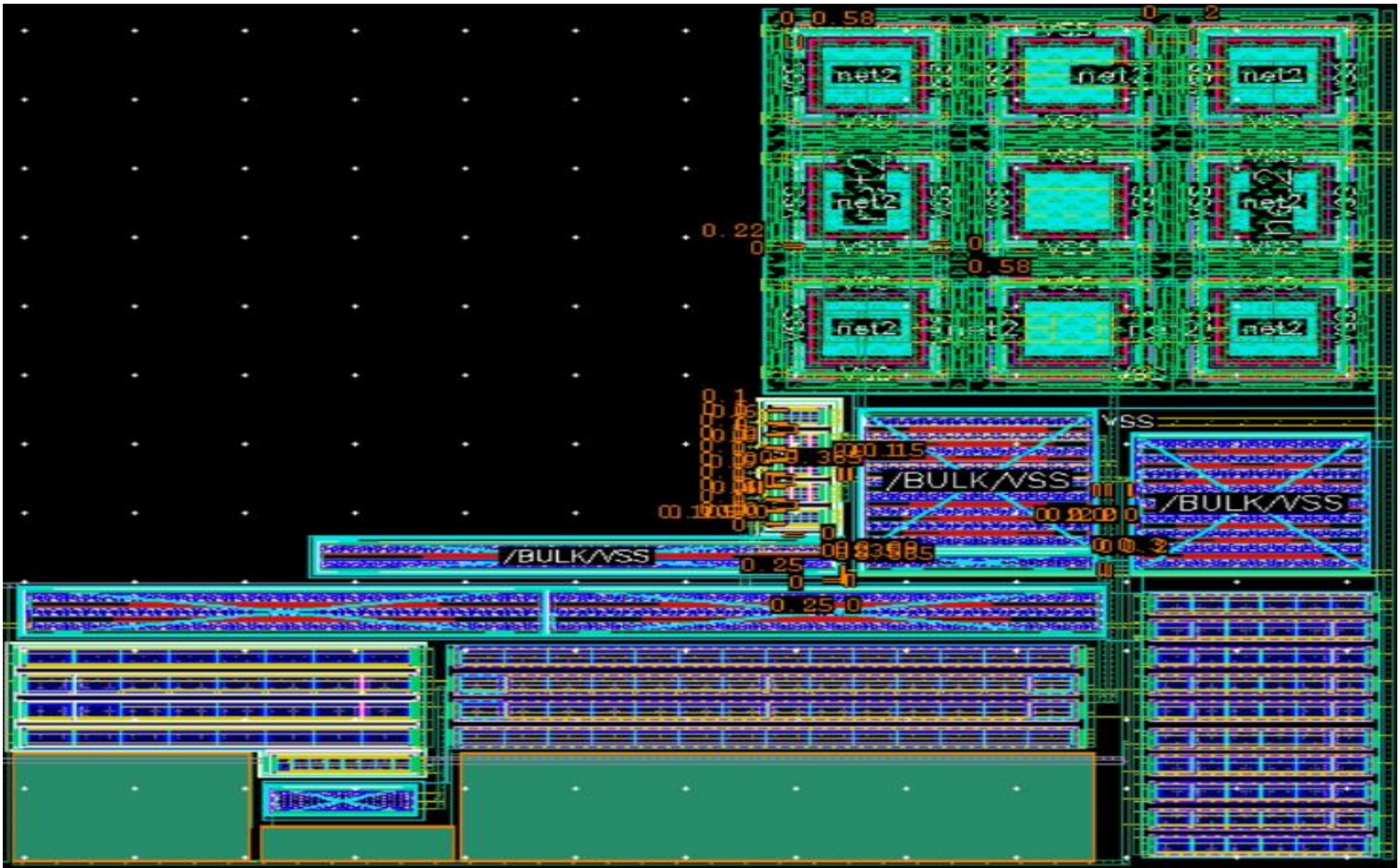
Previous Week:

- Completed the bandgap layout. The extracted results were very similar to the schematic results.
- Designed the project poster.

Next:

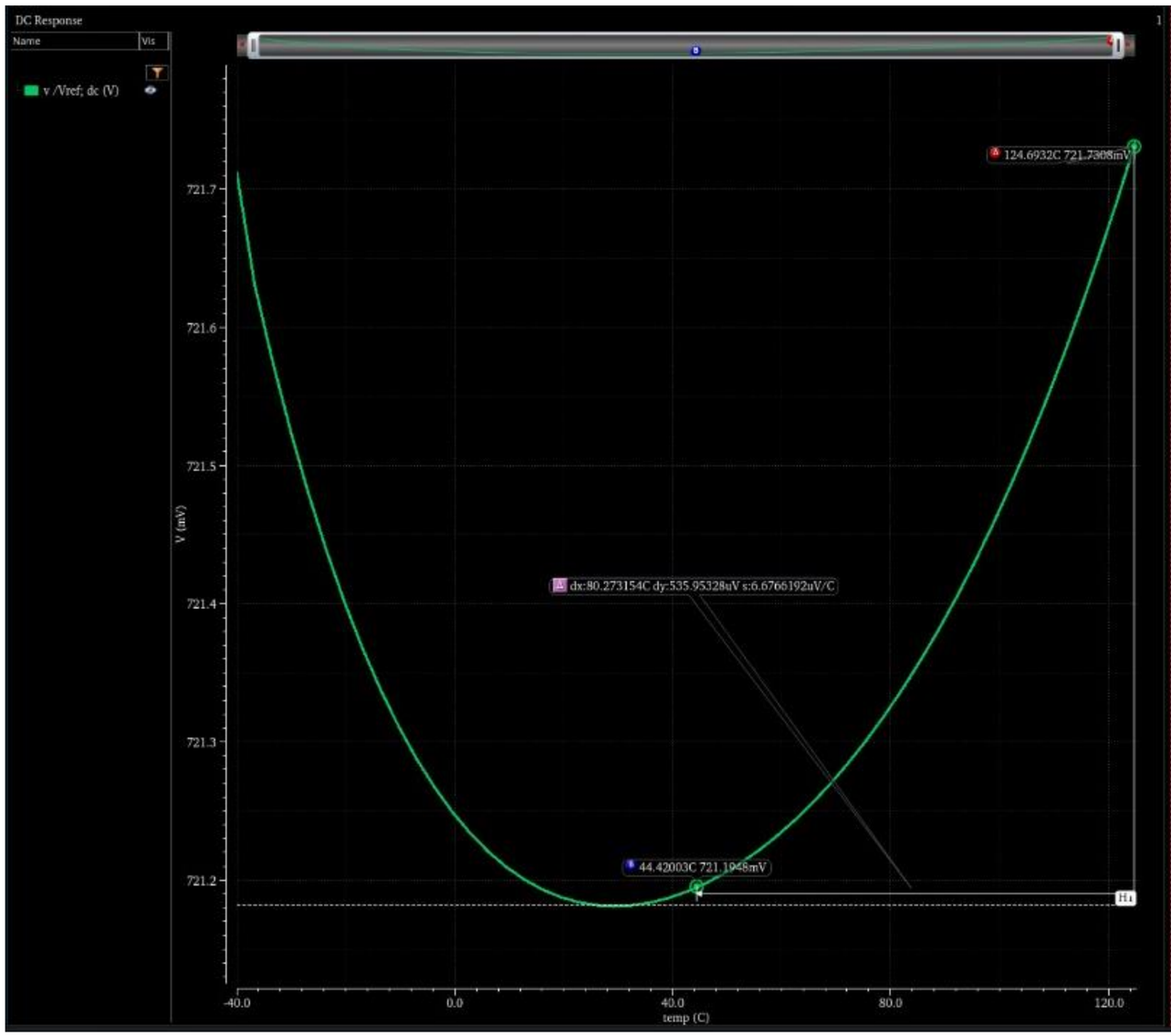
- Focus on optimizing the LDO performance.
- Begin layout design for the LDO.

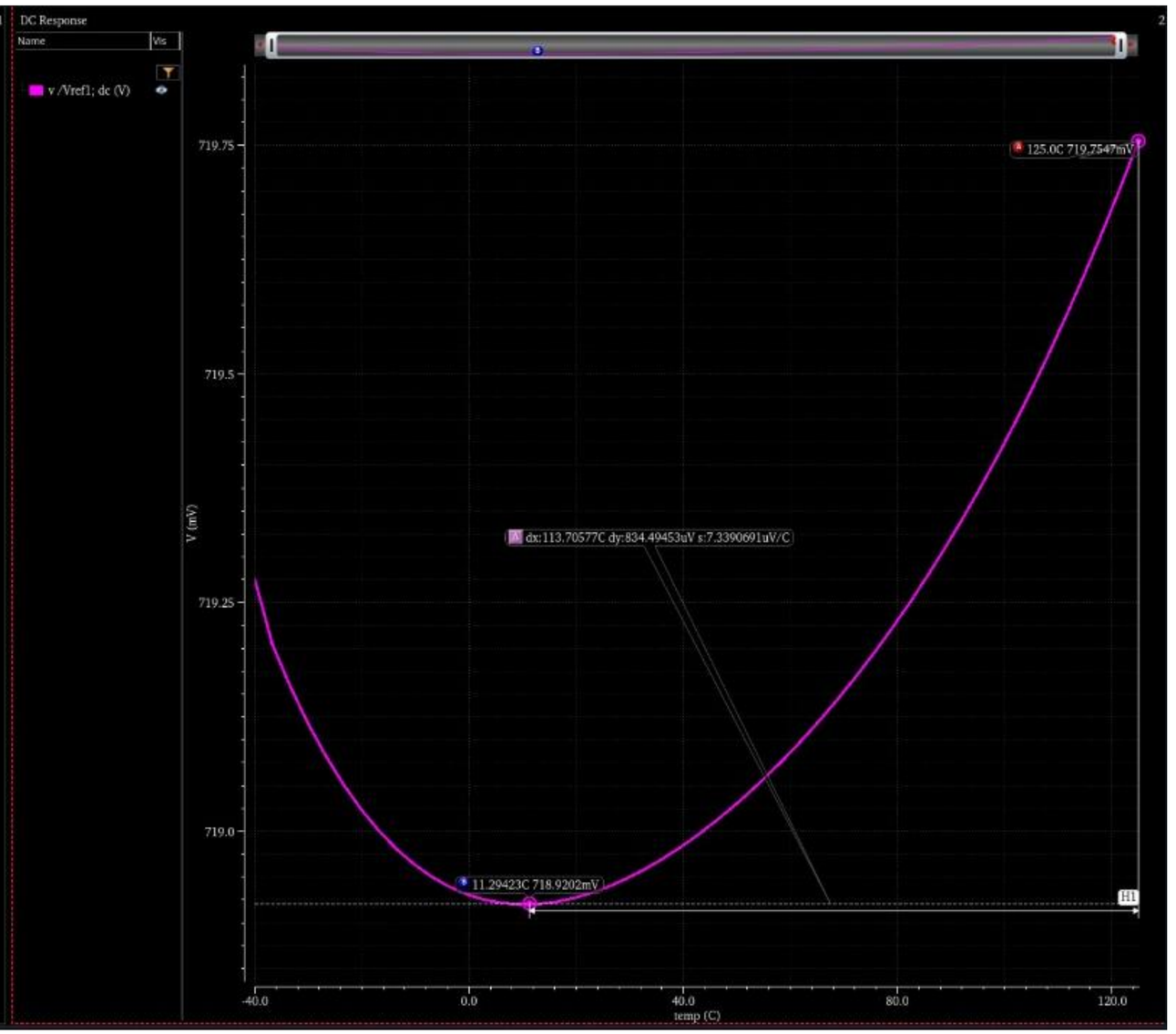
BGR Layout



BGR Results Post Layout

V_{ref} slightly decreased from 721mV to 719mV.
TC of 6. 7 $\frac{ppm}{°C}$ pre-layout, TC of 7.3 $\frac{ppm}{°C}$ post-layout.





LDO for a Digital High Frequency Clock Source Chip

Project Number: 24-1-1-3097

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TEL AVIV UNIVERSITY
Pursuing the Unknown

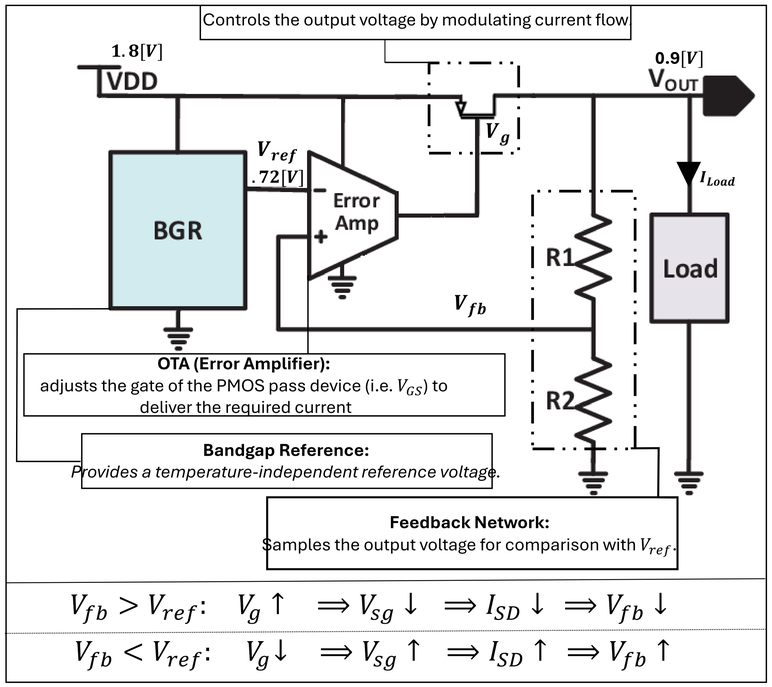
DPLL 2024/25

Motivation & Objective

To ensure low phase noise and precise timing, the DPLL needs a stable, low-noise supply. Our LDO is designed to Provide a consistent output voltage across supply and Temperature variations, tailored specifically for DPLL requirements.

Operating Principle

Internal architecture of the LDO:



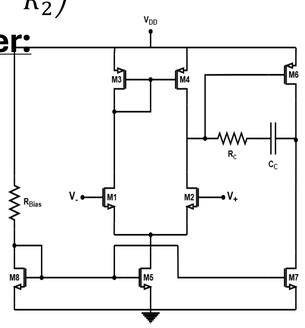
The regulated output voltage is given by:

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

Miller OTA as an Error Amplifier:

In BGR, forces $V_A = V_B$ to generate a temperature-independent current.

In LDO, used as a current regulator that stabilizes V_{out}. High gain ($\sim 80dB$) improves accuracy and regulation.



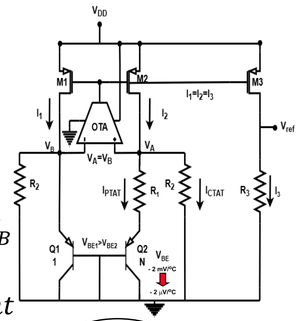
The Bandgap Reference

The bandgap reference generates a precise, temperature-independent voltage.

$$V_A = \frac{kT}{q} ln\left(\frac{I}{N \times I_s}\right) + IR_1 = \overbrace{\frac{kT}{q} ln\left(\frac{I}{I_s}\right)}^{V_{BE1} = V_{CTAT}} = V_B$$

$$I = \frac{V_{BE1} - V_{BE2}}{R_1} = \frac{kT}{qR_1}\ln(N) \rightarrow PTAT\ current$$

$$V_{ref} = R_3(I_{PTAT} + I_{CTAT}) = R_3\left(\frac{\ln(N)V_T}{R_1} + \frac{V_A}{R_2}\right) \rightarrow \frac{\partial V_{ref}}{\partial T} = 0$$



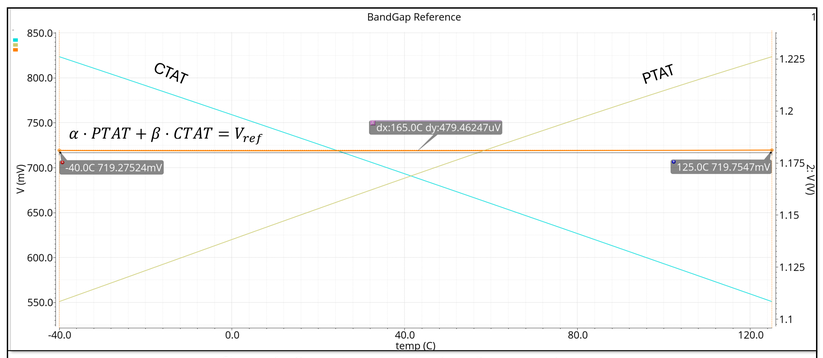


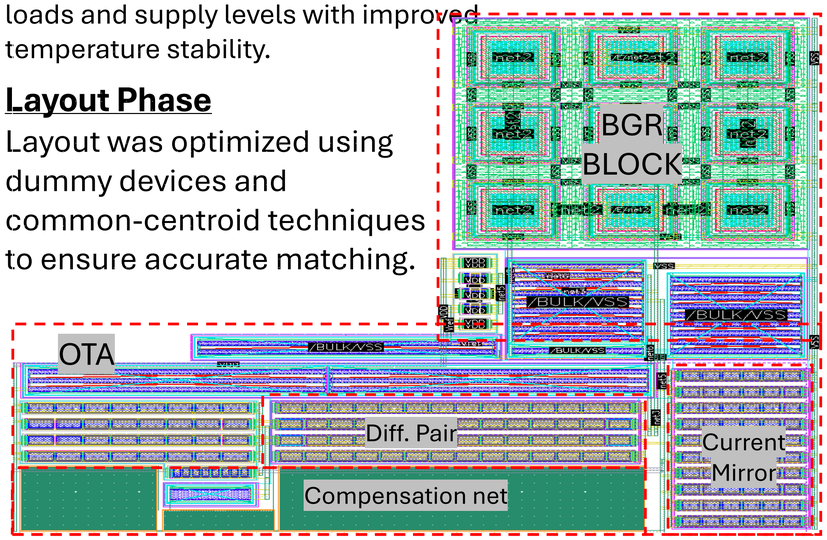
figure 1: Operating principle of the Bandgap reference
PTAT – **Proportional** to temperature coefficient ; CTAT – **Complementary** to temperature coefficient

Implementation

The LDO, designed in TSMC 28nm with a two-stage OTA and modified bandgap (0.72V), reliably regulates 0.9V across varying loads and supply levels with improved temperature stability.

Layout Phase

Layout was optimized using dummy devices and common-centroid techniques to ensure accurate matching.



Results

The following table summarizes three critical performance metrics of the LDO:

Metric	Definition	Requirement	Achieved
Temperature Coefficient	$\frac{dV_{out}}{dT}$ (ppm/°C) Stability against temperature variation	< 60	5.8 (↑10.3×)
Line Regulation	$\frac{\Delta V_{out}}{\Delta V_{DD}}$ (V/V) Stability against supply variation	< 0.01	0.001 (↑10×)
Load Regulation	$\frac{\Delta V_{out}}{\Delta I_{load}}$ (mV/mA) Stability against load current variation	< 0.1	0.0044 (↑22.7×)

Table 1: Summary of the three critical performance metrics of the LDO.

Our LDO maintains excellent output stability across a wide operating range:

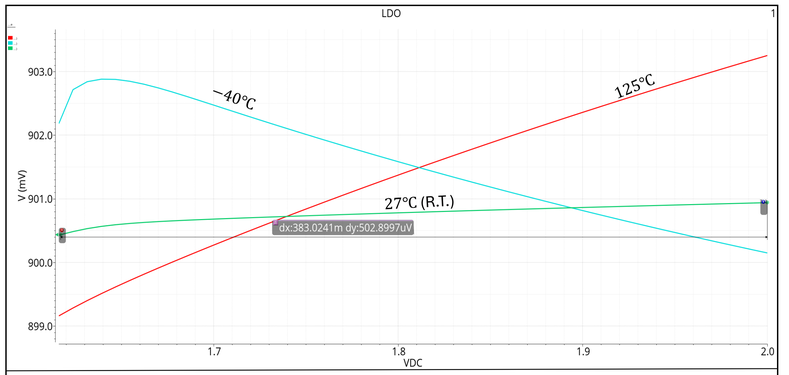


figure 2: V_{out} against Supply Voltage for a different temperature

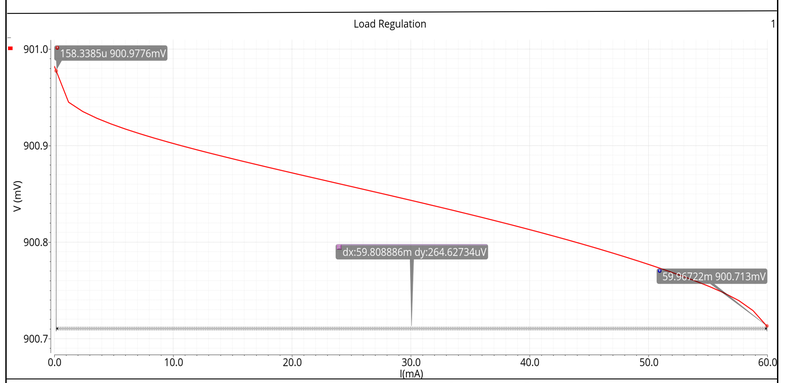


figure 3: V_{out} against I_{load} $[0 - 60mA]$