LDO

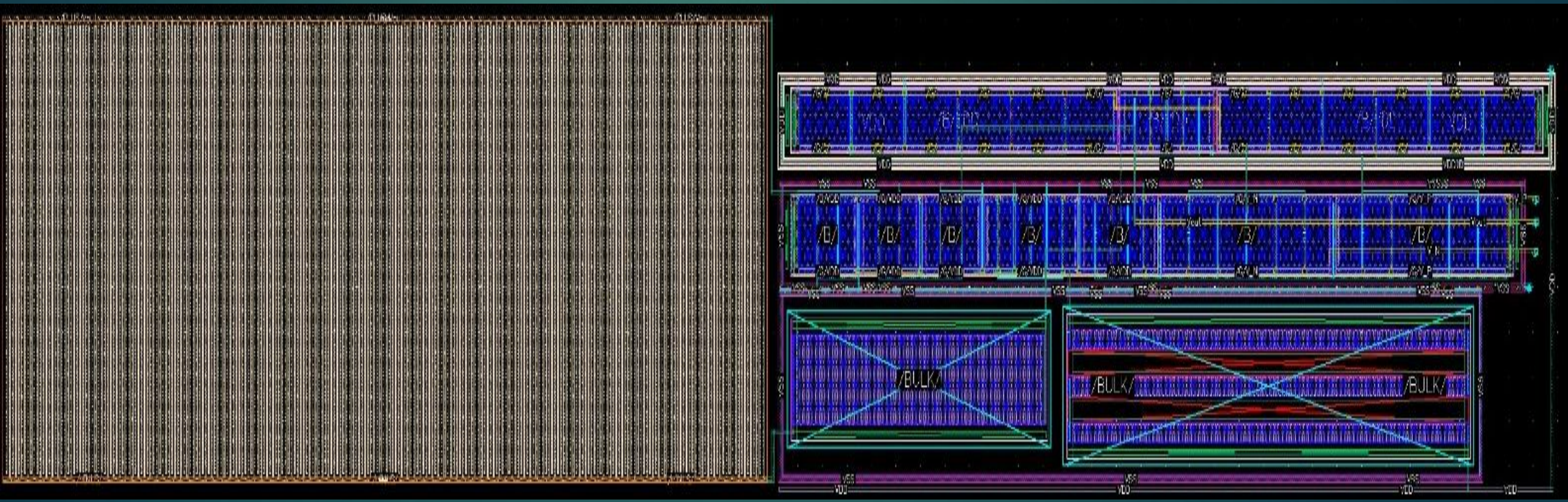
Previous Weeks:

- Fixed the post layout simulation of the OTA, The issue was that the VDS of the tail transistor was too close to VDSAT. Resizing some transistors fixed it and slightly improved the schematic performance.
- Redesigned the OTA layout several times to improve post-layout performance. The OTA now works in post-layout simulation, but the Vref output in the BGR increased from 713 mV to 733 mV.
- Still unsure how to fix the DRC problem regarding metal layers.

This Week:

- Fixing the OTA layout.
- Finishing the BGR layout.

OTA – Current Layout



OTA – Layout AC Response