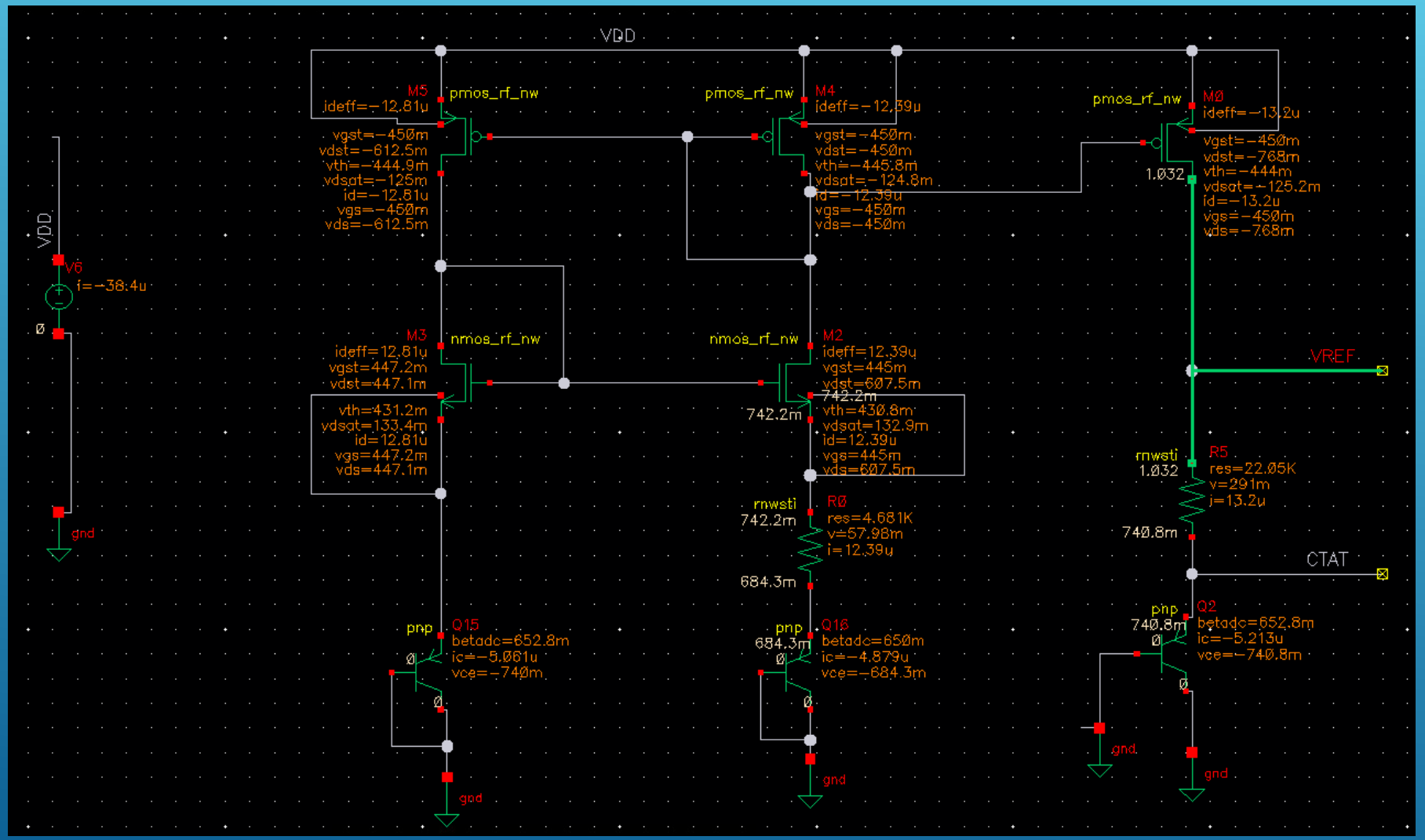
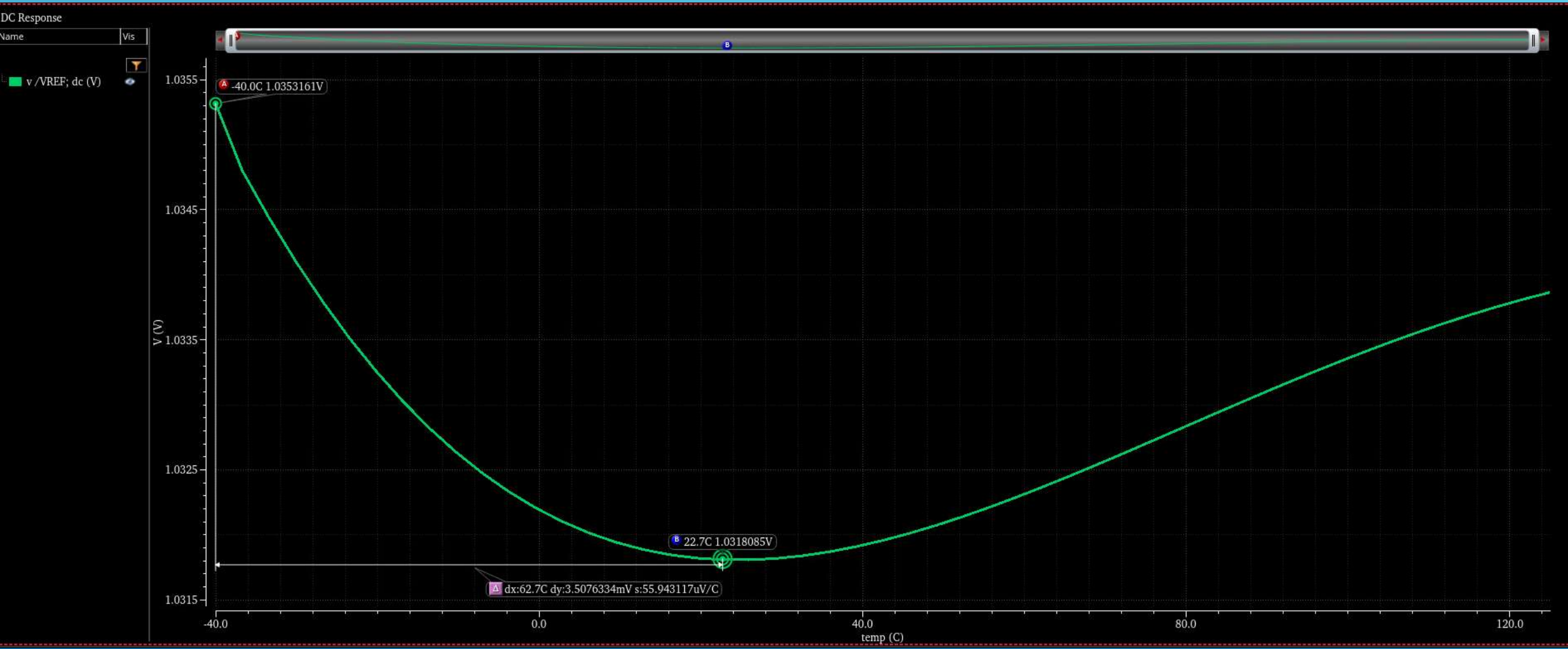
This Week:

Implemented two topologies of the BGR, the first one with a current mirror



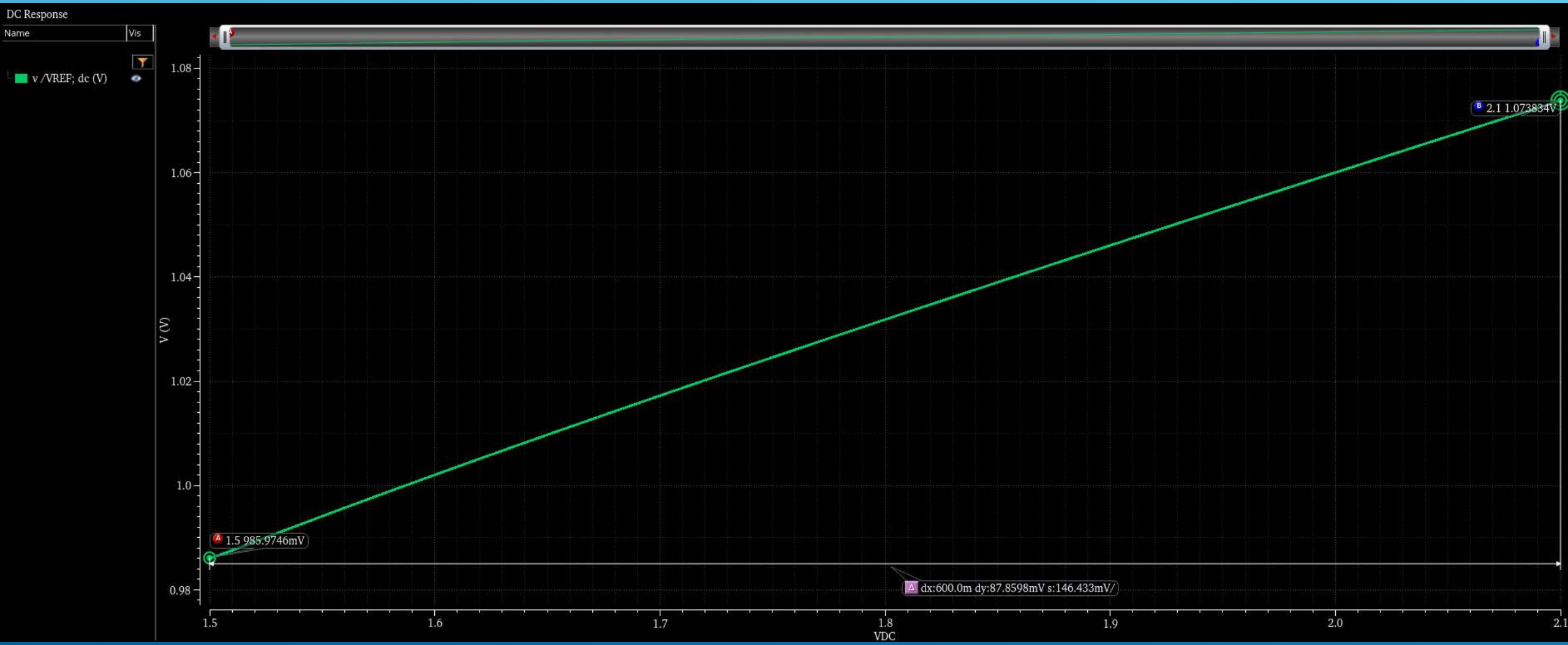
Vref across temperatures (-40 degrees to 125 degrees Celsius)

Max deviation is 3.5mV, approx. $\frac{V_{ref_{max}} - V_{ref_{min}}}{V_{ref_{avg}} * \Delta T} * 10^6 = 20.5 \frac{ppm}{°C}$

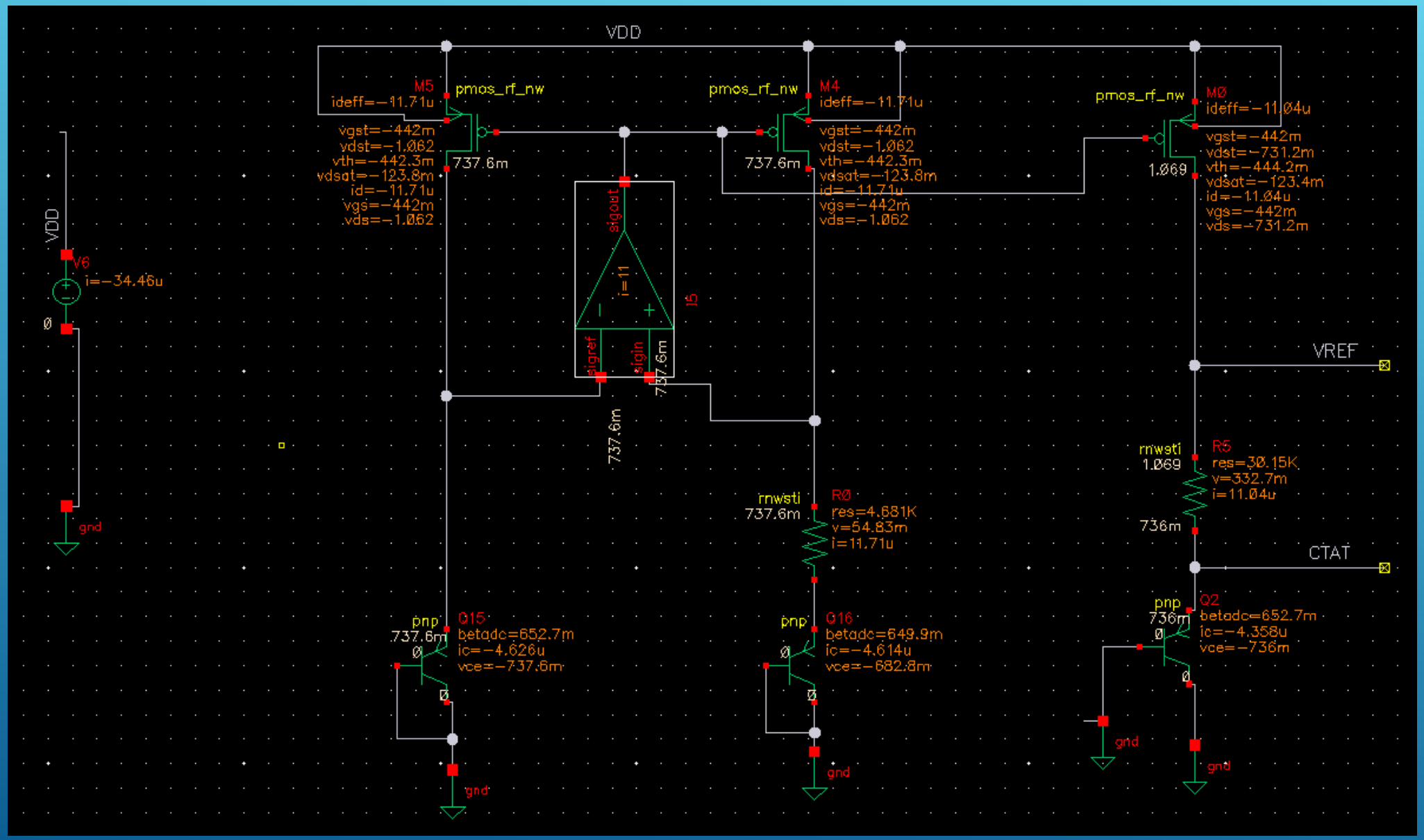


Vref across VDD variations (1.5V to 2.1V)

Max deviation is 85.9mV, terrible PSSR $= 20log\left(\frac{\Delta V_{DD}}{\Delta V_{ref}}\right)$ =17dB

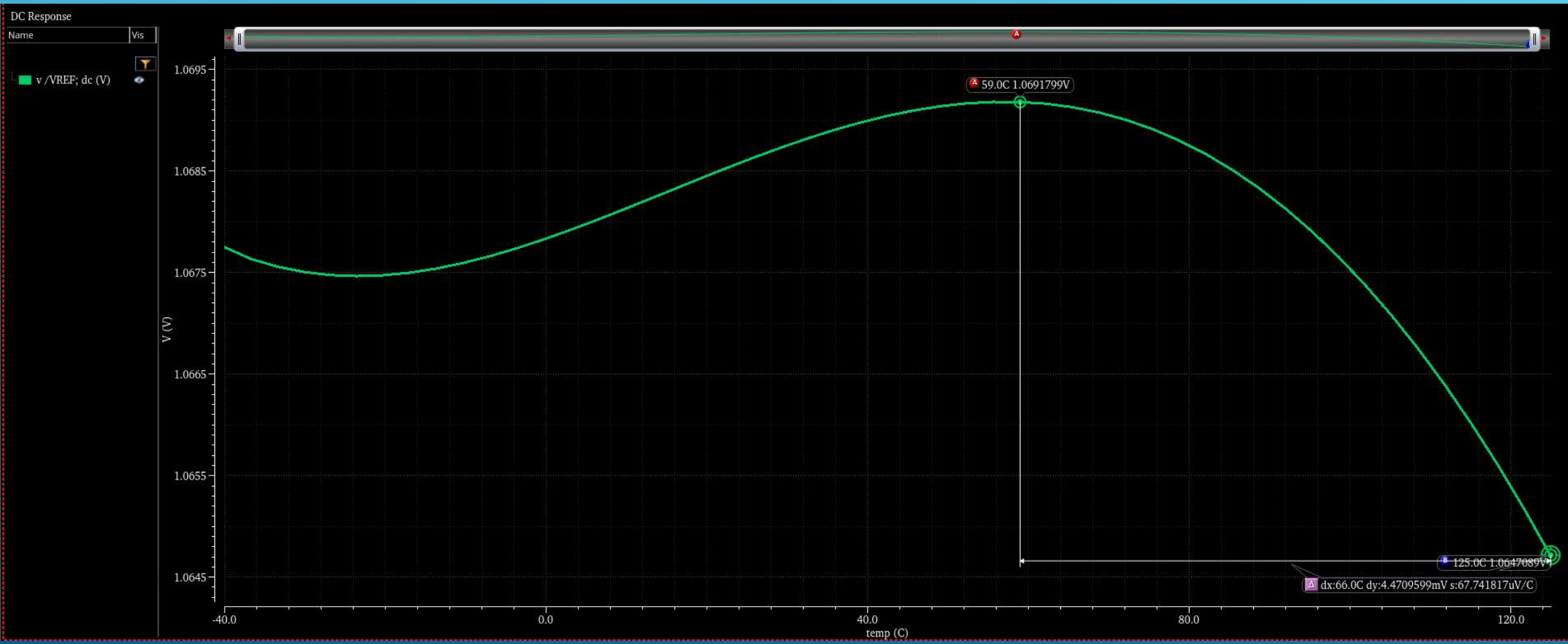


Second implementation with an ideal OTA – operational transconductance amplifier



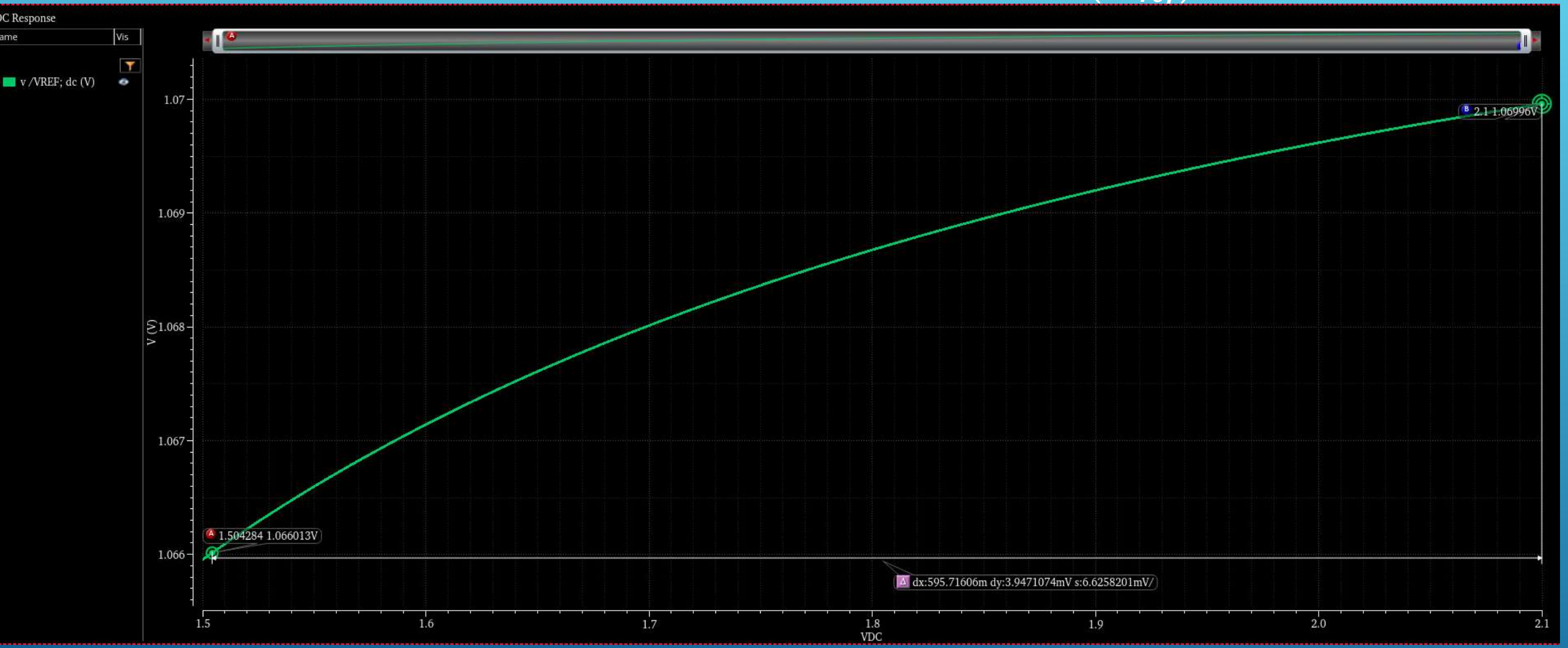
Vref across temperatures (-40 degrees to 125 degrees Celsius)

Max deviation is 4.5mV, approx. $\frac{V_{ref_{max}} - V_{ref_{min}}}{V_{ref_{avg}} * \Delta T} * 10^6 = 25 \frac{ppm}{°C}$



Vref across VDD variations (1.5V to 2.1V)

Max deviation is 4mV, reasonable PSSR $= 20log\left(\frac{\Delta V_{DD}}{\Delta V_{ref}}\right) =$ 43dB



Tried implementing a BGR with a cascode current mirror to improve current matching across branches, Vref didn't stabilize until a VDD of 3V, can be fixed

Instead, working on designing a Miller CMOS OTA with the following specs:
GBW = 2-10MHz
DC gain > 60dB (70-80dB if possible)
SR = 1-5 V/usec
PM=60
$C_L = 1pF$
Input common mode voltage range from 0.6V to 1.5V
Power$\leq 500uW$