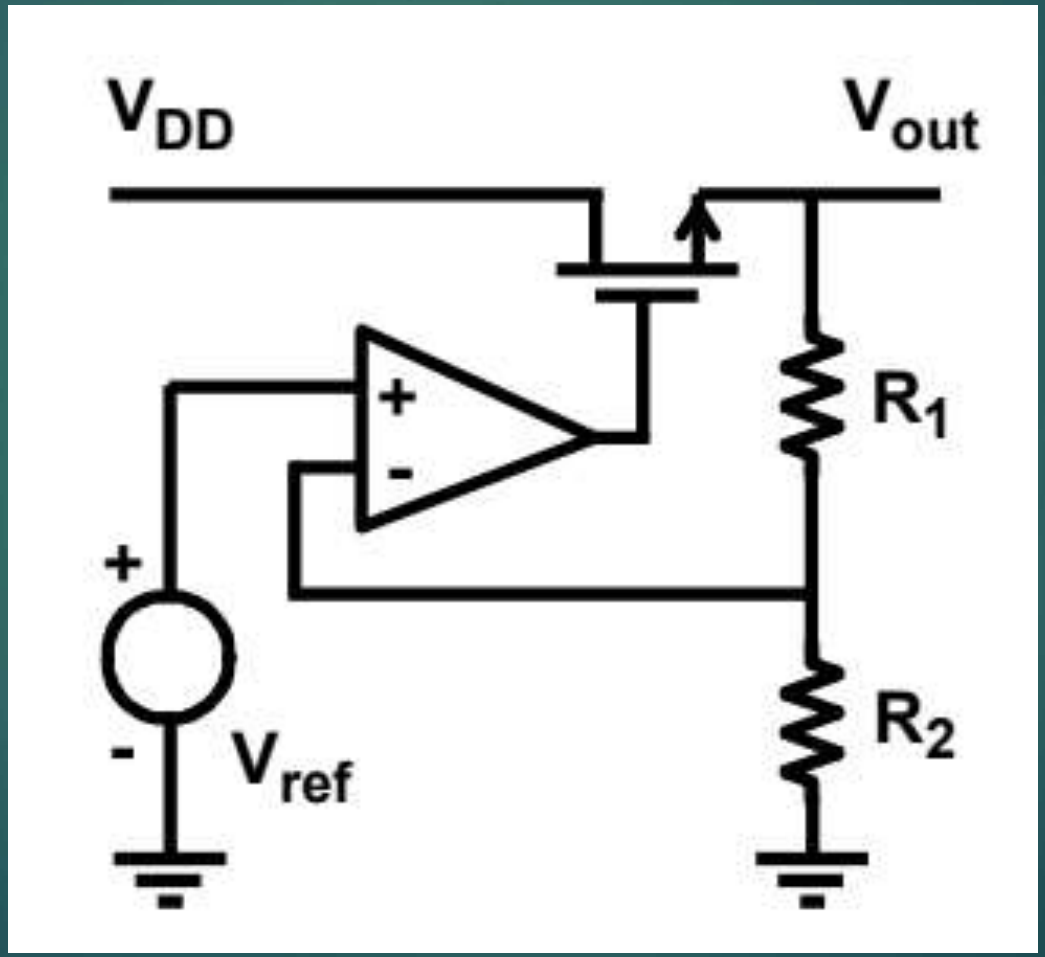
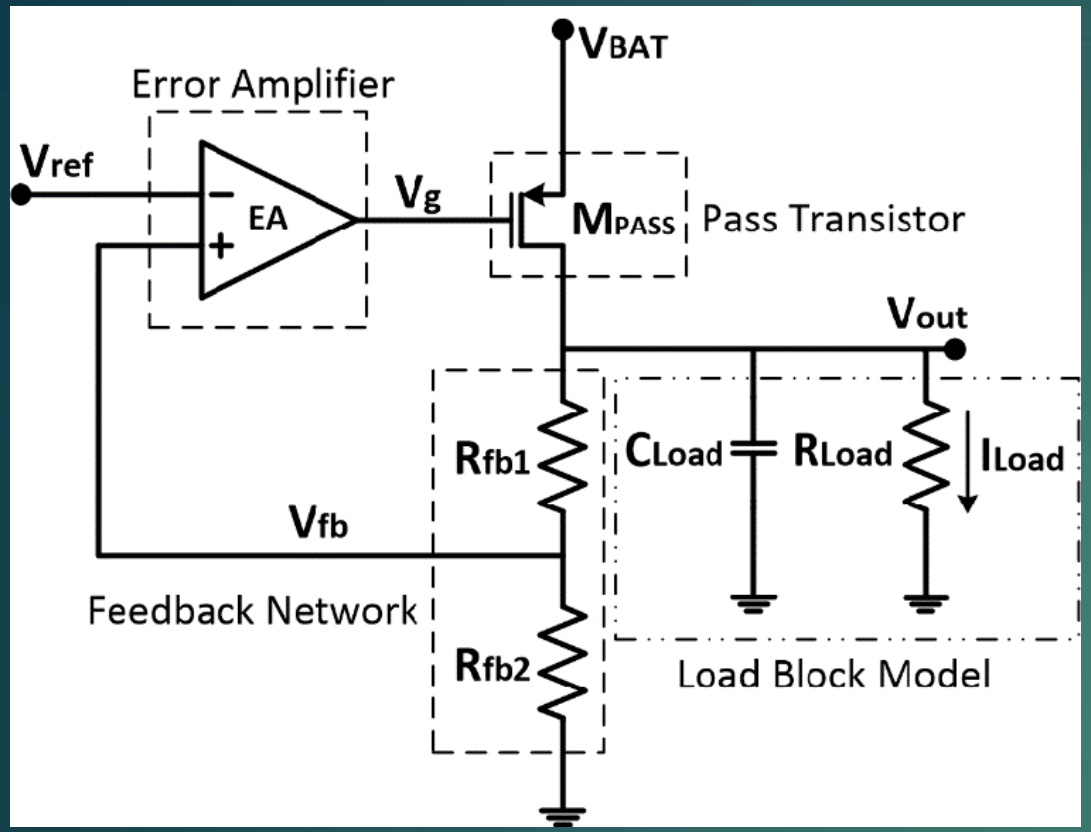
LDO – Low Dropout Voltage Regulator

Arsen & Or



LDO – Low Dropout Voltage Regulator



$$V_{fb} = V_{ref} = V_{out}\frac{R_{fb2}}{R_{fb1}+R_{fb2}}$$

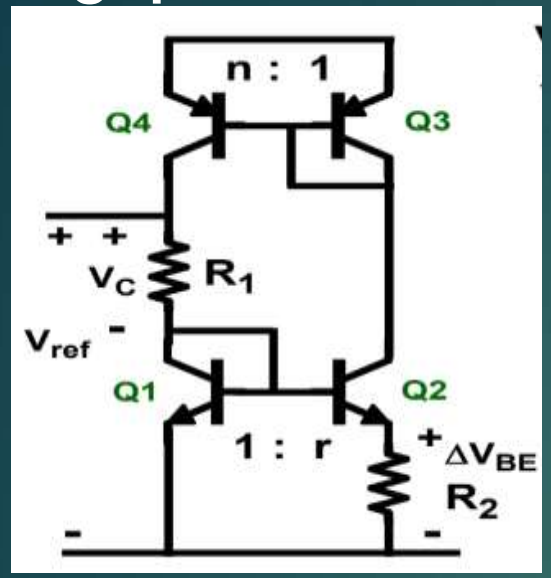
$$V_{out} = V_{ref}\frac{R_{fb1}+R_{fb2}}{R_{fb2}}$$

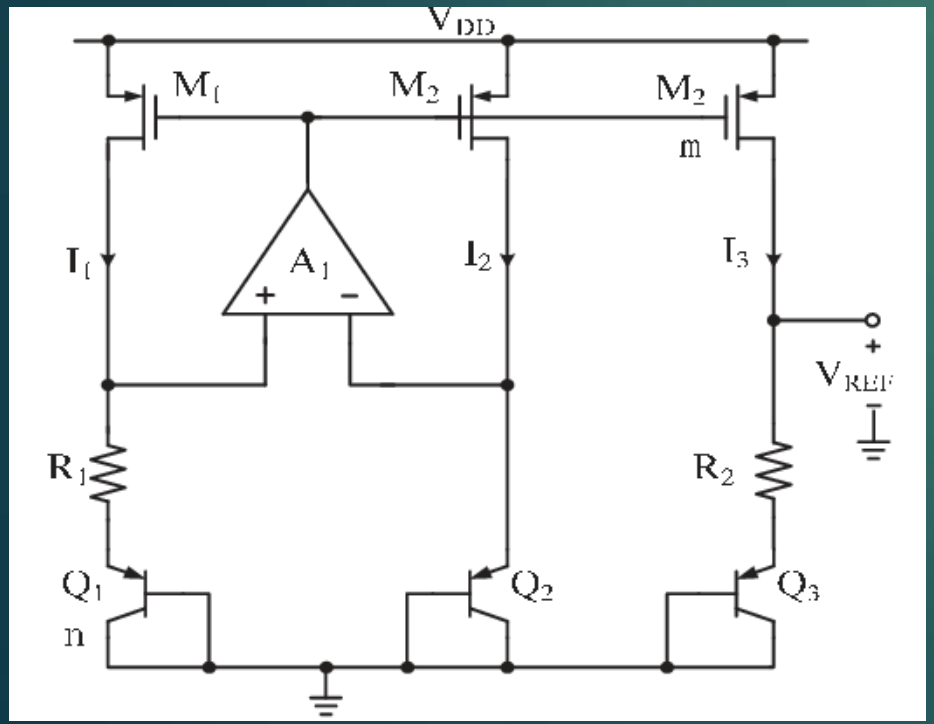
- Low dropout indicates that it can regulate Vout with a very small difference (dropout) between VDD and Vout. Typically, 50-200mV.
- Regulator's purpose is to stabilize the voltage and maintain it constant across a range of supply voltage and load fluctuations.
- Vref is given by the bandgap reference circuit and is stable across a wide temperature range: -40 to 125 degrees.
- The circuit consists of:
  - PMOS pass transistor in SAT mode – gate voltage sets current through the feedback network and the load.
  - Feedback network – two resistors that form a voltage divider.
  - OTA – compares feedback system with the ref voltage and generates the error signal to control the output voltage.

$$\text{If } V_{fb} > V_{ref} \rightarrow V_g\uparrow \rightarrow V_{sg}\downarrow \rightarrow I_{SD}\downarrow \rightarrow V_{fb}\downarrow$$
$$\text{If } V_{fb} < V_{ref} \rightarrow V_g\downarrow \rightarrow V_{sg}\uparrow \rightarrow I_{SD}\uparrow \rightarrow V_{fb}\uparrow$$

$$I_{SD}=k(V_{GS}-V_t)^2(1+\lambda V_{SD})$$

Bandgap Reference Circuit



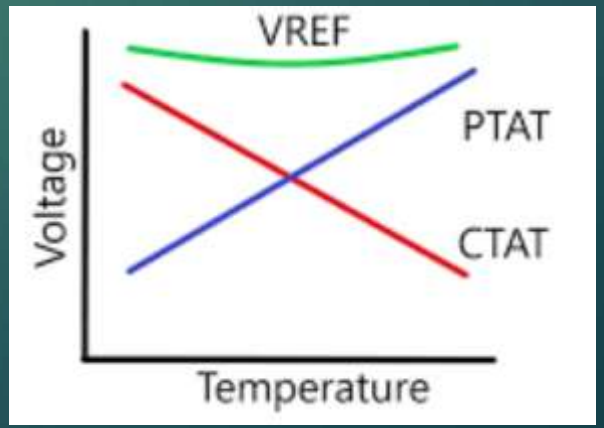


- The bandgap reference circuit provides a fixed output voltage independent of VDD and temperature. Widely used in LDO's, ADC, DAC circuits.
- We want a fixed voltage reference, but such component doesn't exist in nature.

- The circuit consists of:
  - CTAT – a negatively proportional to absolute temperature component, in this case the base-emitter junction voltage of a BJT transistor in FA mode.

  - PTAT – a positively proportional to absolute temperature component (with the same temperature coefficient), in this case the resistor (not every resistor!).

  - Combined, the output voltage remains constant across this temperature range.



CTAT

- A diode or the BE junction in a FA BJT is a natural CTAT.
- As the temperature increases, V_{BE} decreases
- The slope is around -1.6$\frac{mV}{K}$, however this is not a constant value, but an approximation for 300K.

- The current through a PN diode is given by:

$$I = I_s \cdot e^{\frac{V_D}{V_T}}$$

- I_s is the saturation current, V_D is the voltage across the diode, and V_T is the thermal voltage (26mV at 300K).
- The voltage across the PN diode is:

$$V_D = V_T \cdot ln(\frac{I}{I_s})$$

- We want to find the dependency of V_D on T, so we must find $\frac{dV_D}{dT}$. We already know it's a CTAT and should be around -1.6$\frac{mV}{K}$.
- But first we remember that $V_T = \frac{kT}{q}$, hence $\frac{dV_T}{dT} = \frac{k}{q} > 0$, so this is a PTAT!

- Before we find dV_D/dT, we must find $\frac{dI_s}{dT}$, $\frac{dI}{dT}$.
- The saturation current is given by:
- $I_S = A \cdot q \cdot n_i^2 \cdot \mu \cdot \frac{D_p}{L_p}$
- μ is the carrier mobility, in silicon $\mu(T) \propto T^{-1.5}$
- n_i^2 is the intrinsic carrier concentration squared, approx. $n_i^2(T) \propto T^3 e^{-\frac{E_g}{kT}}$
- D_p is the diffusion coefficient and L_p is the diffusion length, approx. $\frac{D_p}{L_p}(T) \propto T$
- A is the cross-sectional area of the junction and q is the electronic charge, both constant with temperature
- Thus, we found that $I_s(T) \propto C \cdot T^{2.5} e^{-\frac{E_g}{kT}}$.
- Calculating the derivative gives:

$$\frac{dI_s}{dT} = I_s \cdot (\frac{E_g}{kT^2} + \frac{2.5}{T})$$

- The current through the diode is given by (explanation later):

$$I = \frac{V_T ln(n)}{R}$$

- R dependency on temperature will be neglected since it is weak

$$R(T) = R_0[1 + \alpha(T - T_0)] \text{ where } \alpha = 0.001$$

- We've already seen that $\frac{dV_T}{dT} = \frac{k}{q} = \frac{V_T}{T}$
- Therefore: $\frac{dI}{dT} = \frac{ln(n)V_T}{RT} = \frac{I}{T}$

- Now we can finally find $\frac{dV_D}{dT}$:

$$\frac{dV_D}{dT} = \frac{d}{dT}(V_T \cdot ln\left(\frac{I}{I_S}\right) = \frac{d}{dT}(V_T \cdot (ln(I) - ln(I_S)) = V_T \cdot \left(\frac{1}{I} \cdot \frac{dI}{dT} - \frac{1}{I_S} \cdot \frac{dI_S}{dT}\right) + ln(\frac{I}{I_S}) \cdot \frac{dV_T}{dT}$$

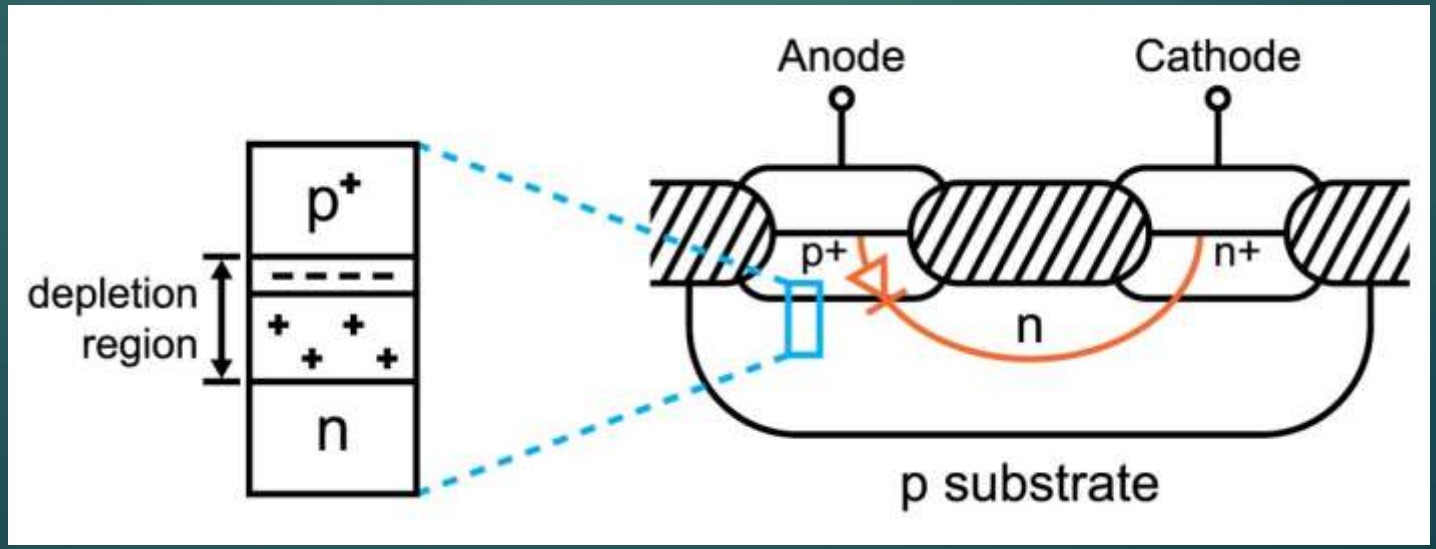
- Substituting in $\frac{dI_S}{dT}$, $\frac{dV_T}{dT}$ to get:

$$\frac{dV_D}{dT} = \frac{V_D - 1.5V_T - \frac{E_g}{q}}{T}$$

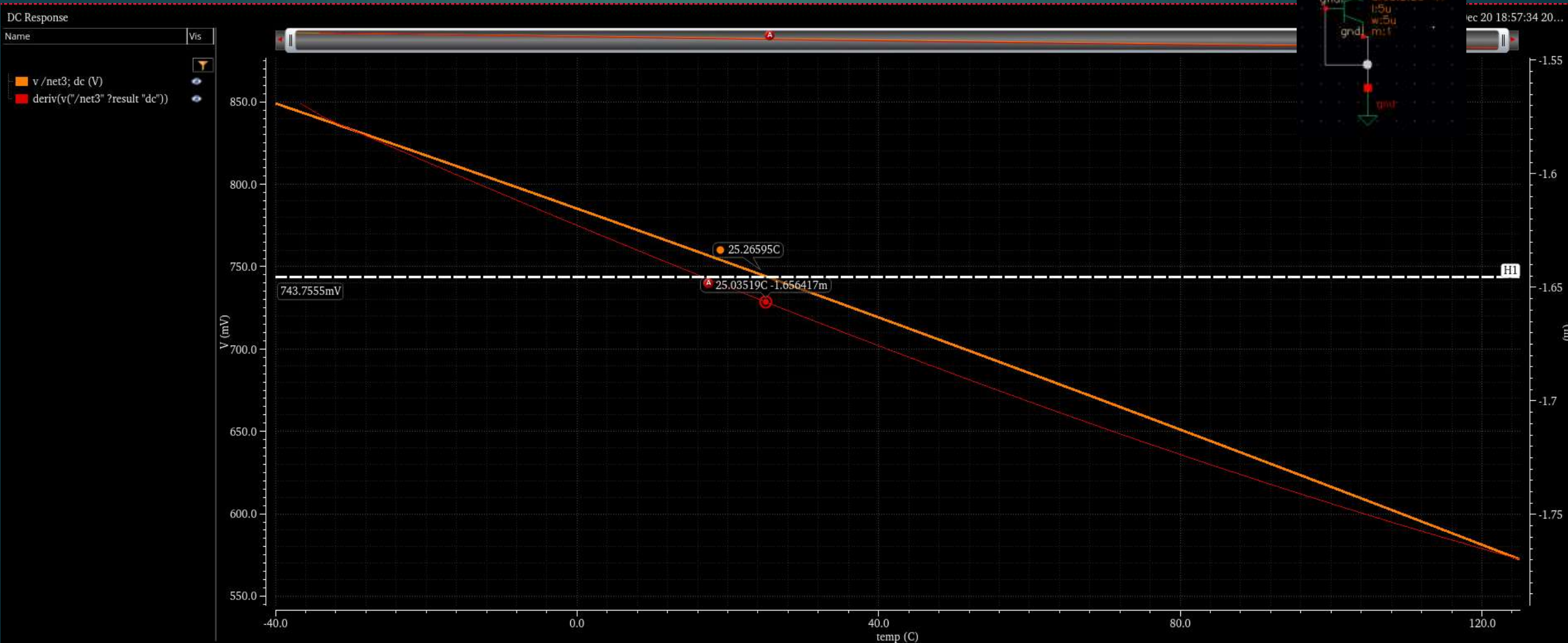
- Plugging in typical values for T=300K to obtain:

$$\frac{dV_D}{dT}(300K) = \frac{0.7 - 1.5 \cdot 0.026 - 1.12}{300} = -1.53\frac{mV}{K}$$

- In CMOS, a parasitic lateral BJT cannot be avoided,
- V_{BE} in FA changes with respect to temperature just as V_D does. Hence, the diodes will be implemented with diode connected PNPs/NPNs.

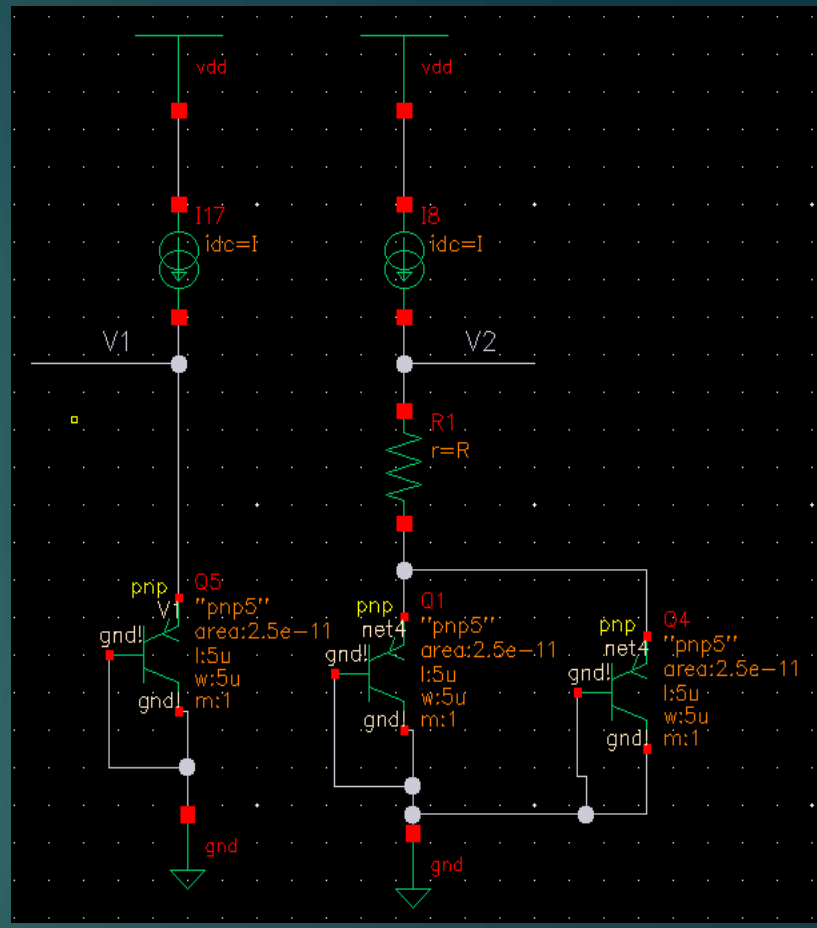


- We verified this through a simulation in Virtuoso and got a very similar result of $\frac{dV_{BE}}{dT}(300K) = -1.65mV$



PTAT

- We have seen that $V_T = \frac{kT}{q}$, hence $\frac{dV_T}{dT} = \frac{k}{q} = 86.25\mu > 0$, so this is a PTAT but a very weak one!
- We saw that $V_D = V_T \cdot ln(\frac{I}{I_s})$ and the CTAT term dominates! We want to cancel the strong CTAT and only get the PTAT term.
- This can be done with the circuit shown. The two PNPs in parallel are equivalent to one BJT with a BE junction area with double the size. In practice the multiplier will not be 2, but larger usually.
- For this to work we assume:
  1) Current through both branches is equal (use a current mirror)
  2) V1=V2 (can be done with either a current mirror or an OTA)
- How is the CTAT term cancelled here?



$$V_1 = V_T \cdot ln(\frac{I}{I_s})$$

$$I_{Q1} = I_{Q2} = \cdots = I_{Qn} = I_s \cdot e^{\frac{V_{BE}}{V_T}} \quad \rightarrow \quad I = n \cdot I_{Q1} = n \cdot I_s \cdot e^{\frac{V_E}{V_T}}$$

$$V_E = V_T \cdot ln(\frac{I}{n \cdot I_s})$$

- Hence: $V_R = V_1 - V_E = V_T \cdot \left(ln\left(\frac{I}{I_s}\right) - ln\left(\frac{I}{nI_s}\right) \right) = V_T \cdot ln\left(\frac{I \cdot n \cdot I_s}{I_s \cdot I}\right) = V_T \cdot ln(n) = \frac{k}{q} ln(n) \cdot T = Const \cdot T$
- The voltage on the resistor is now a PTAT: $V_R = Const \cdot T$
- The current through the resistor is given by: $V_R = IR = V_T \cdot ln(n) \quad \rightarrow \quad I = \frac{V_T ln(n)}{R}$

Combining PTAT with CTAT

- We want to duplicate this PTAT current to a third branch with a new diode connected PNP Q3 sized the same as Q1 so we can change the voltage across the resistor without affecting the current in the main branch.
- The voltage across this new resistor is given by:

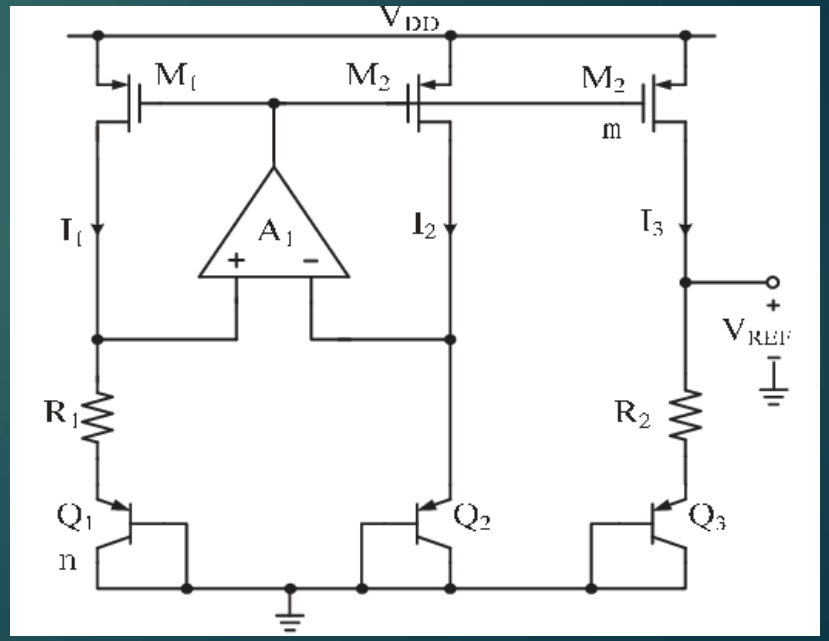
$$V_{R2} = I \cdot R_2 = \frac{R_2}{R_1} ln(n) \cdot V_T$$

- Let's find out how much the voltage on this resistance changes with respect to temperature:

$$\frac{dV_{R2}}{dT} = \frac{R_2}{R_1} ln(n) \cdot \frac{dV_T}{dT}$$

$$\frac{dV_T}{dT} = \frac{k}{q} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}} = 86.25 \frac{\mu V}{K}$$

- The value above is fixed and very low compared to the $-1.65 \frac{mV}{K}$ found for CTAT. We must scale it up by changing $\frac{R_2}{R_1} ln(n)$ to obtain
- $V_{ref} = V_{R2} + V_{Q3}$ fixed across a wide temperature range



Verifying in simulation the PTAT:

Not exactly what we obtained analytically, possibly because of small current mismatches between the branches and the resistor dependance on the temperature was neglected.

Combining PTAT with CTAT

- So, we found in simulation that $\frac{dV_{BE}}{dT} = -1.656\frac{mV}{K}$, $\frac{dV_{R2}}{dT} = 178.39\frac{\mu V}{K}$. We must scale the PTAT up by changing $\frac{R_2}{R_1}ln(n)$ to obtain:
- $V_{ref} = V_{R2} + V_{Q3}$ fixed across a wide temperature range
- So $\frac{dV_{ref}}{dT} = 0 \rightarrow \frac{R_2}{R_1}ln(n) \cdot \left(178.39\frac{\mu V}{K}\right) - 1.656\frac{mV}{K} = 0$

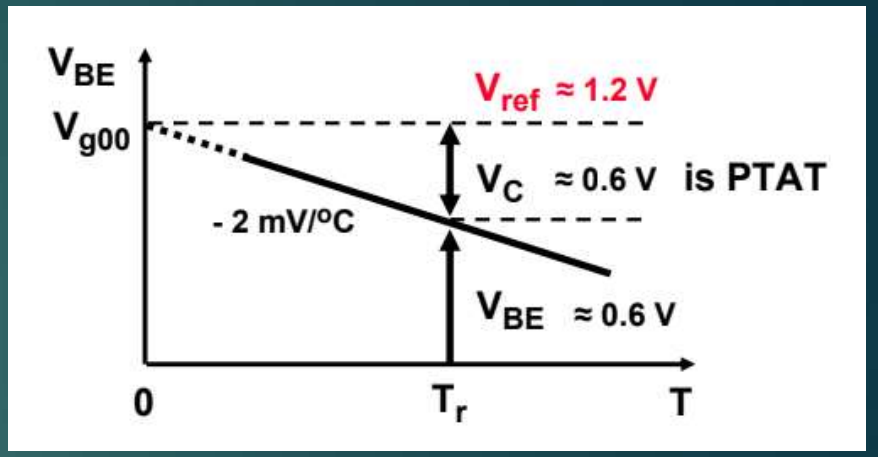
$$\frac{R_2}{R_1}ln(n) = \frac{1.656m}{178.39\mu} = 9.283$$

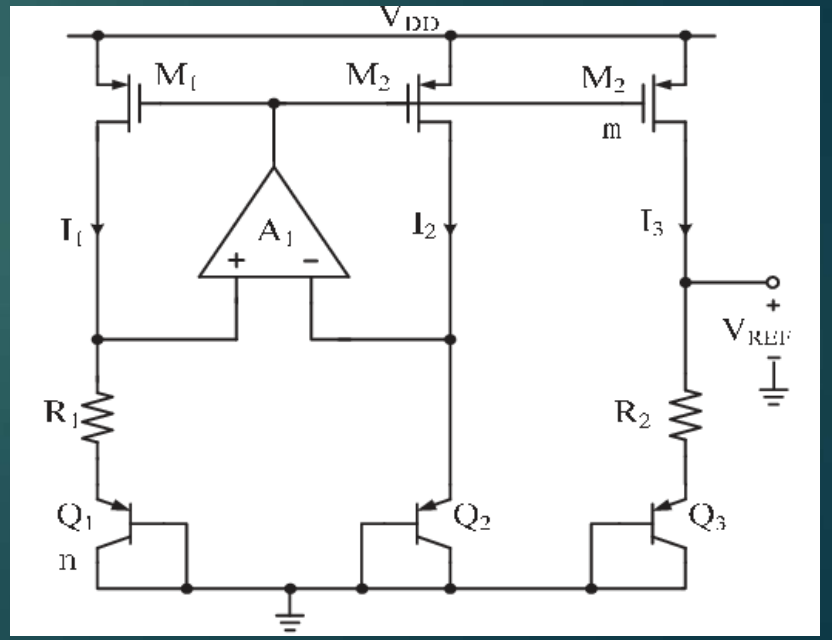
- Therefore, for $\frac{dV_{ref}}{dT} = 0$, $V_{ref} = 9.283V_T + 0.743 = 0.984V$

$$\frac{R_2}{R_1}ln(n) = \frac{1.65m}{86.25\mu} = 9.283$$

- R_1 sets the current in the left branch, so it cannot be changed.
- N=8 was picked in the design.
- Hence R_2 is already set to get the desired $\frac{dV_{ref}}{dT} = 0$:

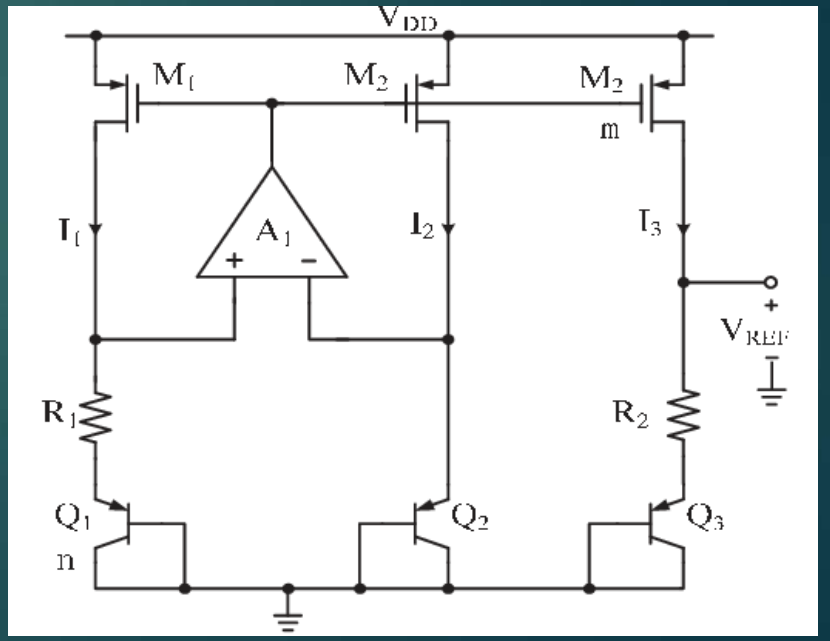
$$R_2 = \frac{9.283R_1}{ln(n)}$$





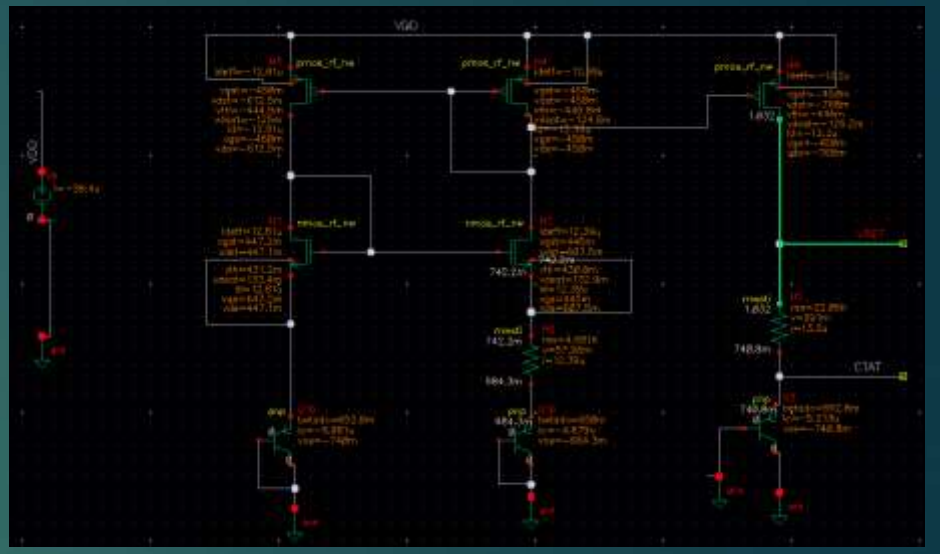
The Design Process

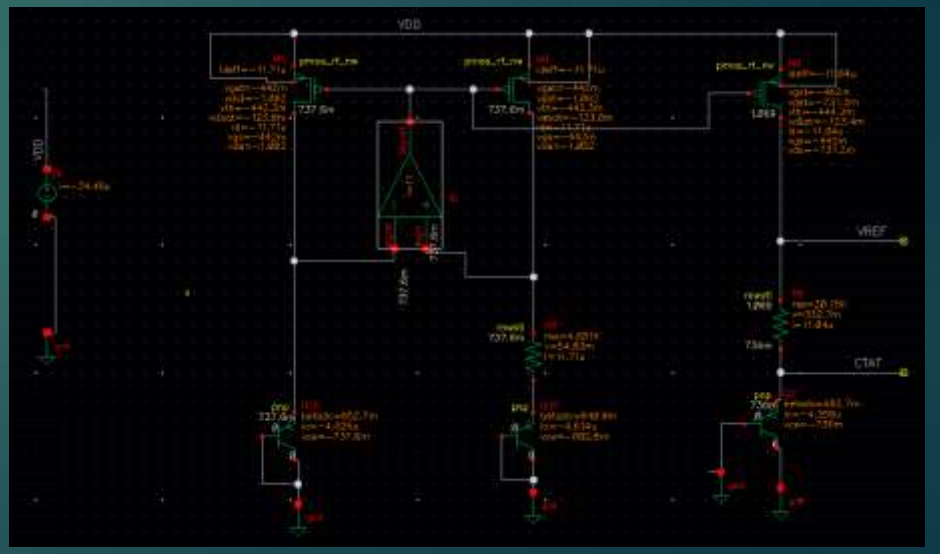
- We wanted the current in all branches to be around $12\mu A$. Hence from $\boldsymbol{I = \frac{V_T ln(n)}{R} \rightarrow R_1 = \frac{V_T ln(n)}{I} = \frac{0.026 ln(8)}{10\mu} = 4.5k}$
- n=8 was picked to minimize R_2 value but also not too high to not make the layout too big. Also, this value allows to implement a common centroid layout, which can minimize mismatch in matched components caused by process gradients and temperature variations.
- The PNP transistors Q1 and Q3 are sized the same, and Q2 BE junction area is multiplied by n=8.
- The PMOS transistors length was chosen to be 240nm (max possible size) to minimize the short channel modulation effect ($\lambda \propto \frac{1}{\mathrm{L}}$) and reduce the sensitivity of I_D to changes in V_{DS}. However, requires more size to drive same current.
- The PMOS transistors M1, M2 width were decreased to 400nm to increase V_{GS} and ensure they're in saturation (at first the fixed current in the branches forced V_{OV} to be near zero because their size was too big).
- The size of M3 was set to 420nm to have better current matching in all branches (its V_{DS} is noticeably lower).



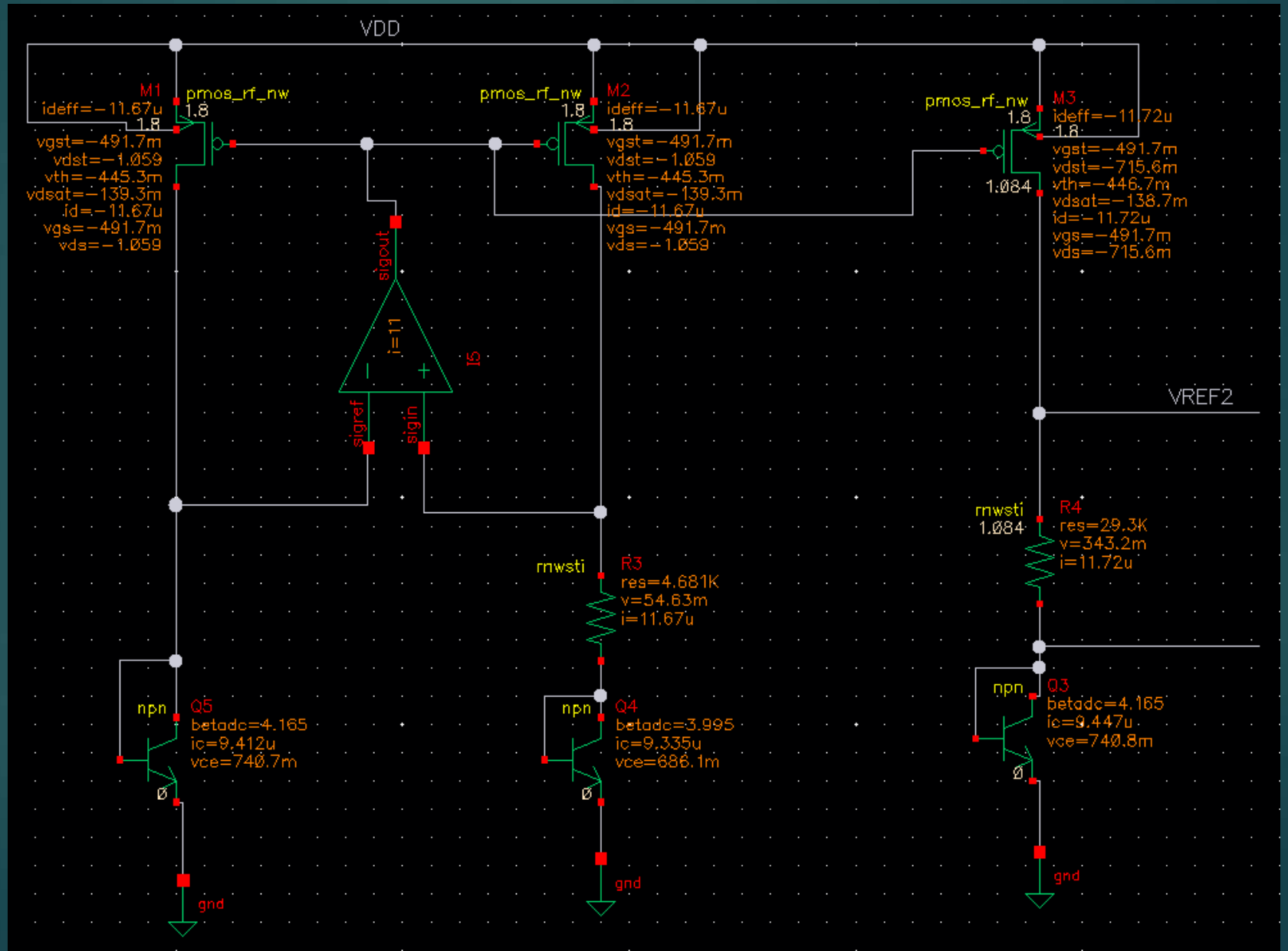
The Design Process

- To force $V_1 = V_2$, we tried using an NMOS current mirror first. Because the current is fixed and their gate voltage is identical, if their sizes match then their source voltage should be identical as well.
- Next, we tried using an ideal OTA to force $V_1 = V_2$, and settled for it because as presented last week, its PSSR was much better (43dB vs 17dB). This is because it matches the voltages much more accurately.
- Next, we calculated $\boldsymbol{R_2 = \frac{9.283R_1}{ln(n)} = 20.9K\Omega}$ to get a fixed V_{ref}. However, in the simulation V_{ref} had a CTAT behavior so we increased R_2 to get V_{ref} constant and settled on $R_2 = 28.9K\Omega$.
- It was confirmed in simulation that the scaling up of the resistor changed its temperature coefficient.
- This gave us $\boldsymbol{V_{ref} = 12.92V_T + 0.743 = 1.08V}$



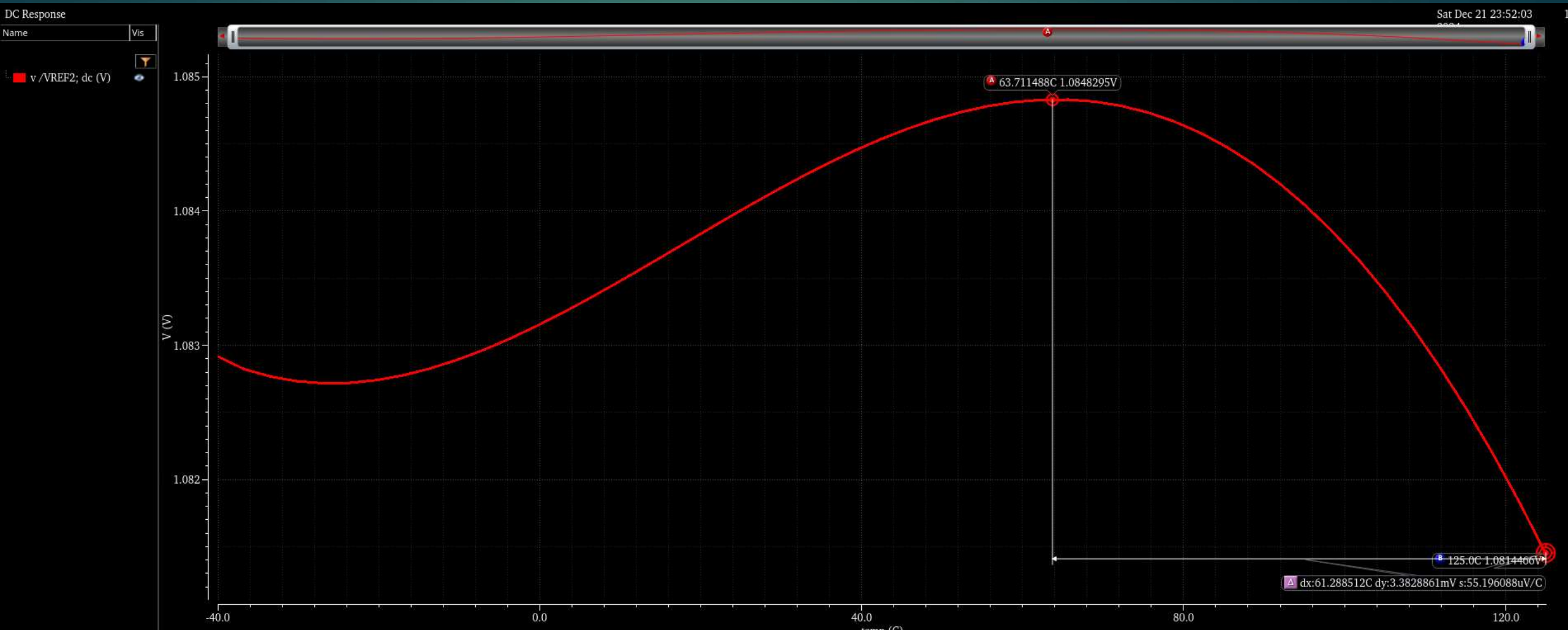


DC Operating Point – Ideal OTA



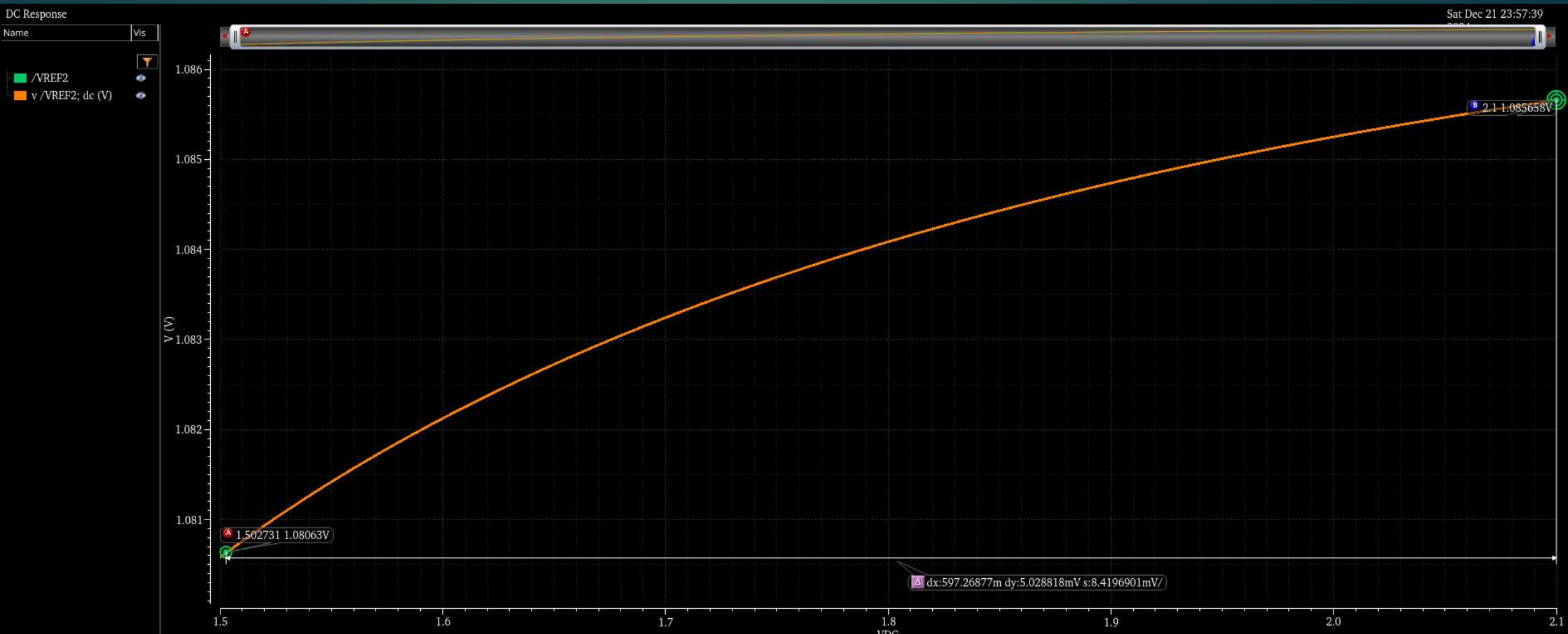
V_{ref} across temperature – Ideal OTA

Max deviation is 3.382mV, approx. $\frac{V_{ref_{max}} - V_{ref_{min}}}{V_{ref_{avg}} * \Delta T} * 10^6 = 21 \frac{ppm}{°C}$



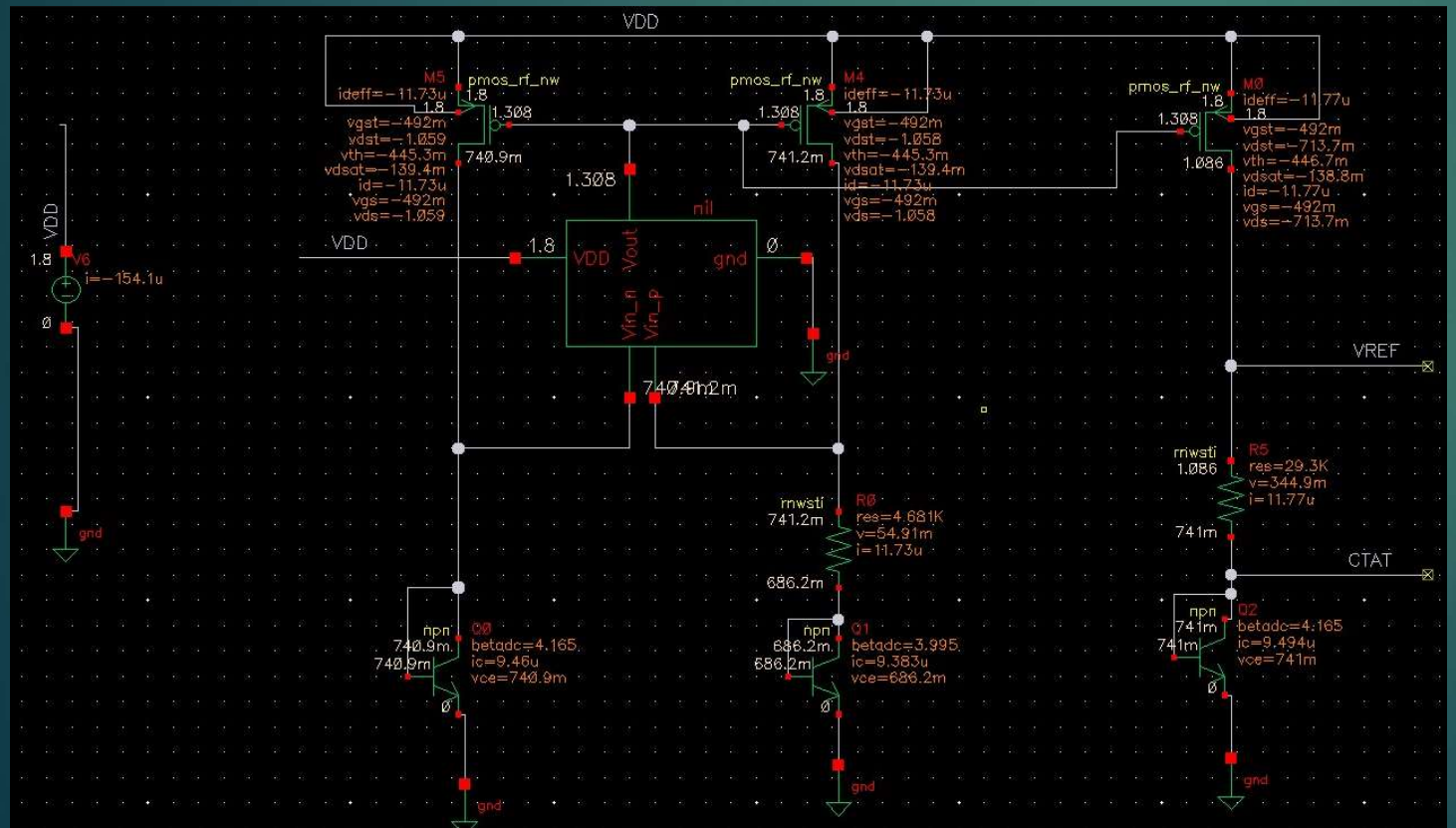
V_{ref} across VDD variation – Ideal OTA

Max variation is 5mV, $PSSR = 20log10\left(\frac{\Delta V_{DD}}{\Delta V_{ref}}\right)$ =41.58dB.



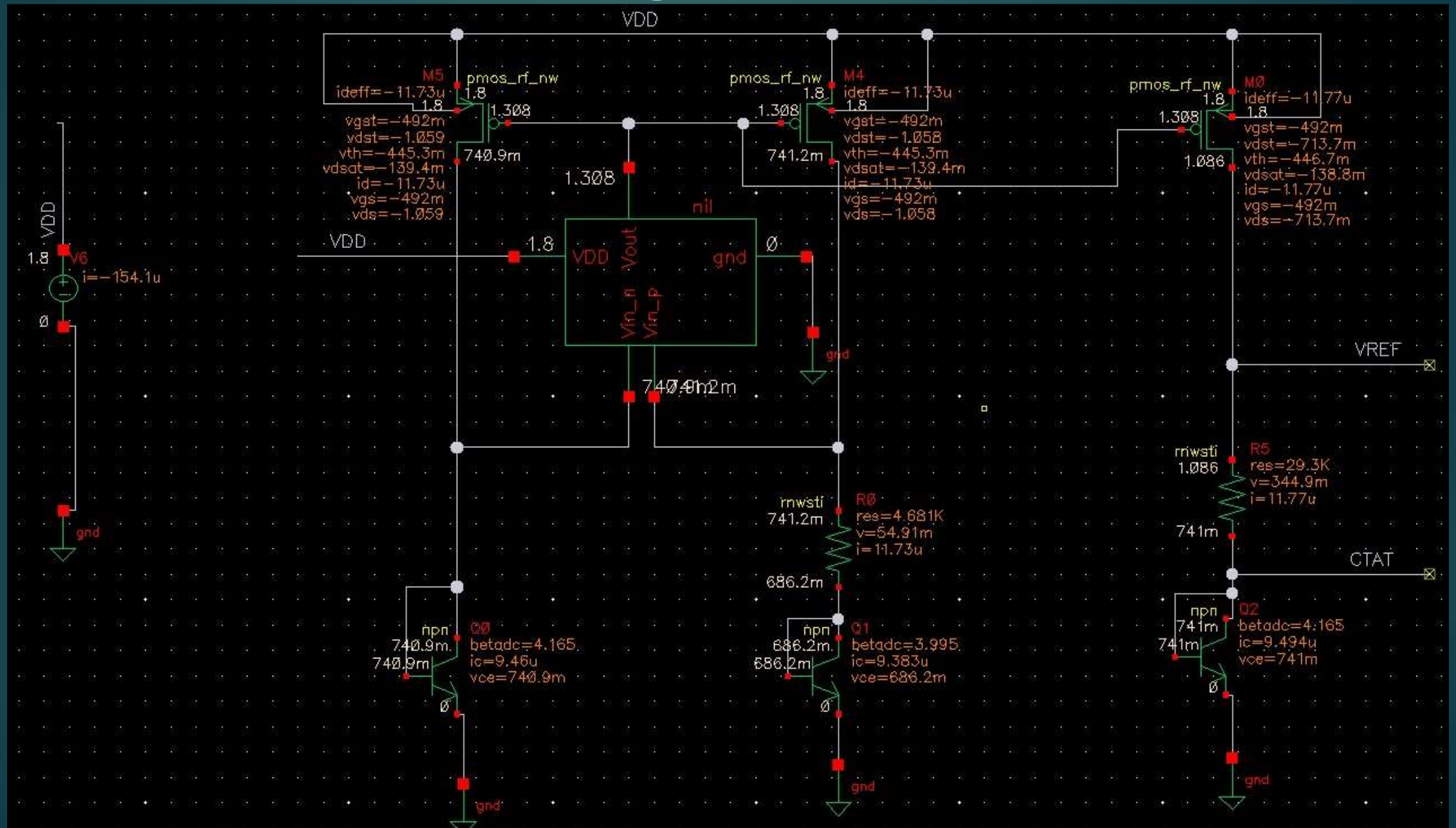
BGR with a real OTA

- This week we implemented our own CMOS Miller OTA and replaced the ideal OTA. Our results were very similar.
- The non-inverting input of the OTA was connected to V_2 to ensure negative feedback and stable operation.
- When V_2 increases above V_1, then V_G also increases, because these are PMOS transistors, $V_{SG} = V_{DD} - V_G$ decreases, hence the current in the branch will decrease and V_2 will decrease.



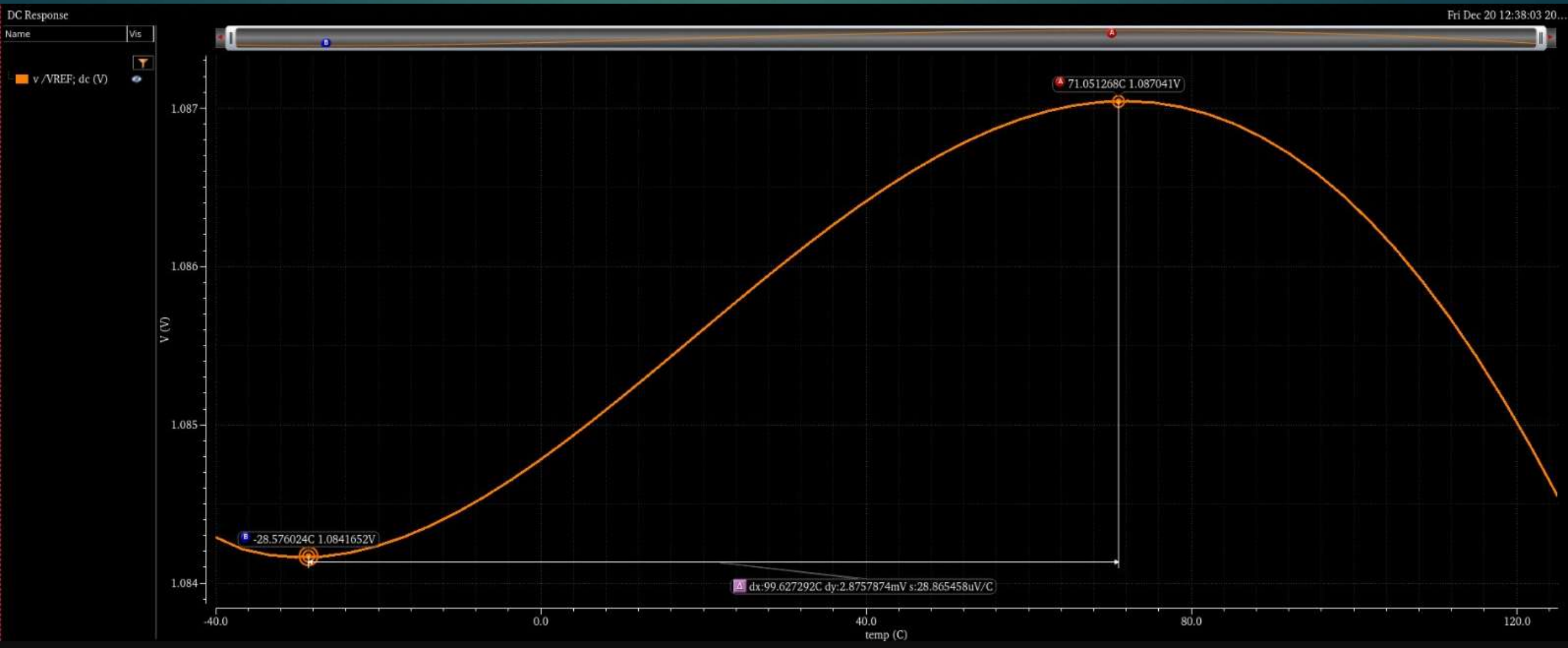
Specification	Desired	Reached
PSSR	>40	41.2
Power (μW)	<300	154
Variation Across T	<60 $\frac{ppm}{°C}$	16 $\frac{ppm}{°C}$

DC Operating Point – Our OTA



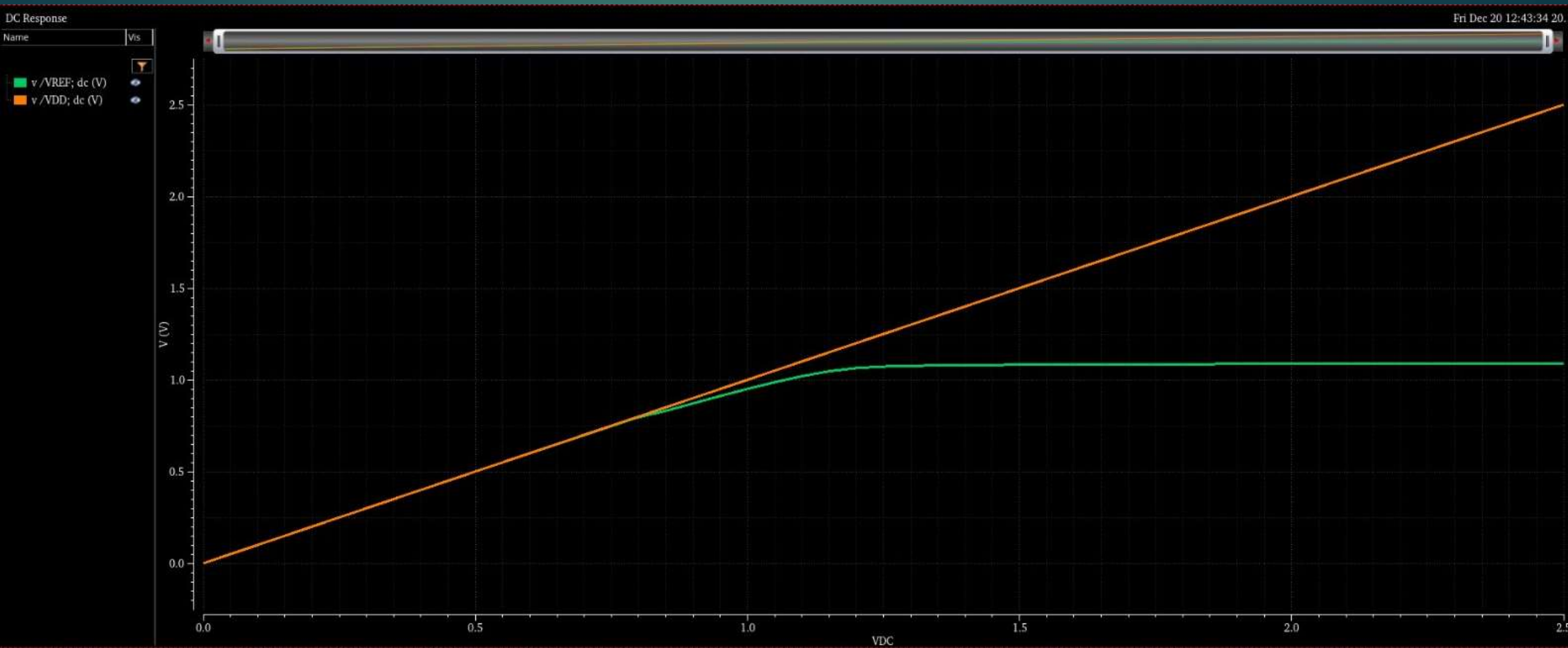
V_{ref} across temperature (-40-125°C)

Max deviation is 2.875mV, approx. $\frac{V_{ref_{max}} - V_{ref_{min}}}{V_{ref_{avg}} * \Delta T} * 10^6 = 16 \frac{ppm}{°C}$



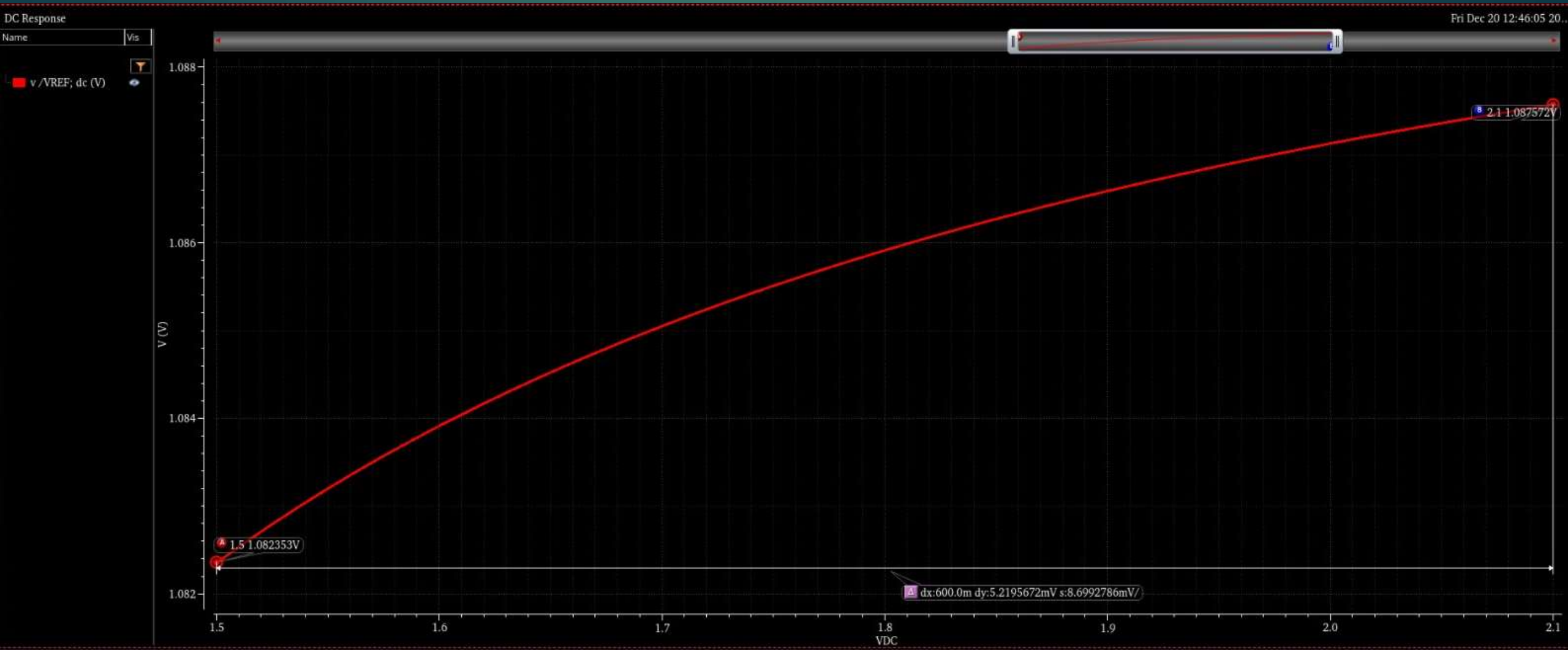
V_{ref} across VDD variation ($0V - 2.5V$)

Once V_{DD} reaches 1.25V, V_{ref} becomes nearly constant for any variation of V_{DD}



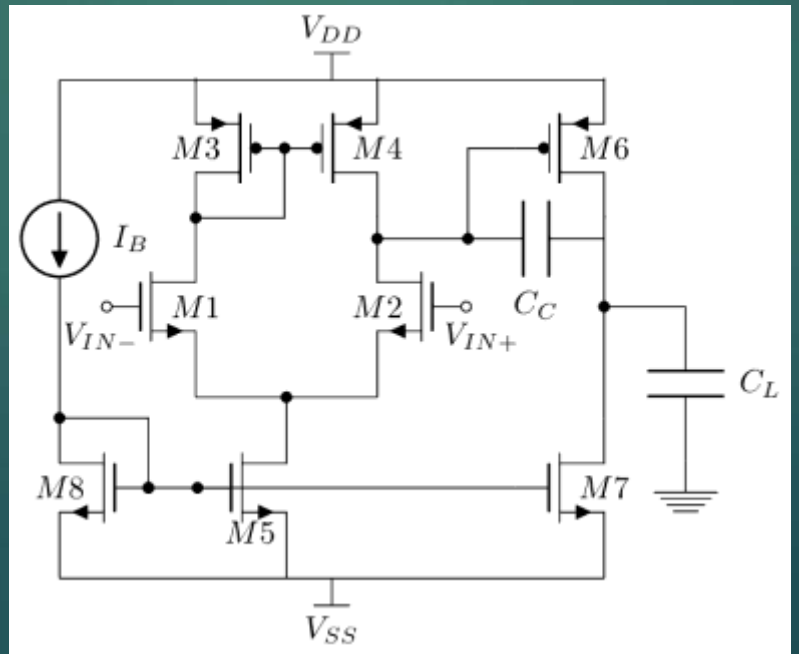
V_{ref} across VDD variation (1.5V – 2.1V)

Max variation is 5.2mV, $PSSR = 20log10\left(\frac{\Delta V_{DD}}{\Delta V_{ref}}\right)$ =41.21dB.



CMOS Miller OTA

- Consists of two stages:
- Input stage – differential amplifier, with a DC current mirror biasing it and an active load M5. The gain achieved by this stage was around 36dB.
- Gain stage – a CS stage to boost the gain north of 60dB.
- OTA's are transconductance ($\frac{i_{out}}{v_{in}}$) amplifiers, hence their output impedance is naturally high ($\frac{r_{ds}}{2}$ in this topology). Therefore, these amplifiers are perfect for driving capacitive loads (like a gate of a MOS transistor like in the cases of the BGR and the LDO).
- To drive resistive loads, a third buffer stage is needed to provide a low output impedance. Then this becomes a typical three stage op-amp topology like the 741 op-amp.



CMOS Miller OTA – Design Specs

- Last week we presented the intended specifications. The design specifications reached during the design process are:

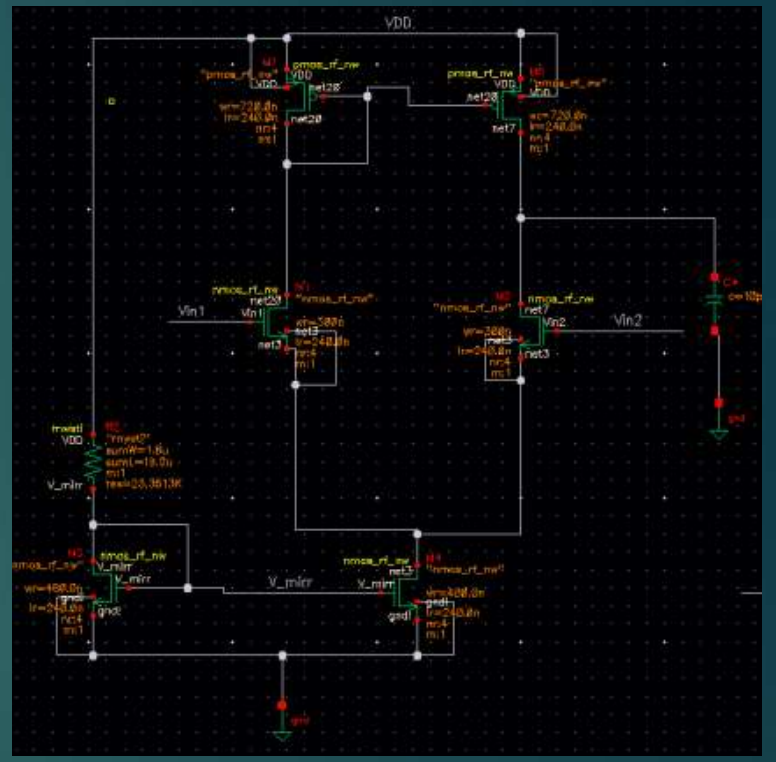
Specification	Intended	Reached
DC Gain (dB)	>60 (70 if possible)	67.5-68dB
GBW (MHz)	5-10MHz	13.5-14MHz
Slew Rate ($\frac{V}{\mu s}$)	1-5	16
Phase Margin (°)	60	63-64
C_L (pF)	10pF	10pF
Power (μW)	500	480-495
Input Common Mode Range (V)	0.6V-1.5V	0.75V-1.2V(1.6V)

- The input common mode range is the voltage range for which all transistors in the circuit are guaranteed to stay in saturation.
- This range is sufficient because in the BGR both inputs to the OTA are expected to be around 0.75V and for the LDO both inputs are expected to be around 0.9V.

CMOS Miller OTA – Design Process

- First, we designed the first stage of the Miller OTA – the diff. amp.

Specification	Intended	Reached
DC Gain (dB)	40	35.8
GBW (MHz)	10MHz	9.3MHz
Slew Rate $(\frac{V}{\mu s})$	10	9.9
C_L (pF)	5pF	5pF
Power (μW)	<300	180
Input Common Mode Range (V)	0.6V-1.5V	0.75V-1.2V(1.6V)



- We will size all transistors to ensure all of them are in saturation mode for all voltages in the ICM range.

CMOS Miller OTA – Design Process

- SR is the max rate of change of the output voltage. This is the scenario when all the current flows through one branch only, hence

$$I_0 = SR \cdot C_L = 10M \cdot 10p = 50\mu A$$

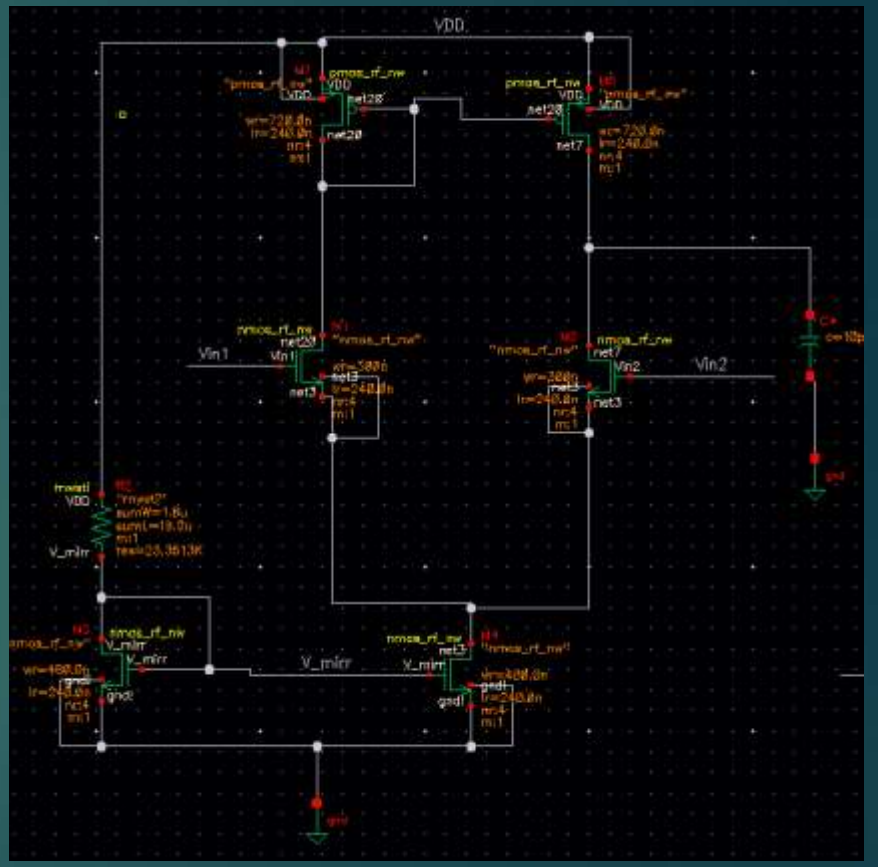
- Next, we found $V_{t,n} = 500mv, V_{t,p} = 500\text{mV}, \mu_n C_{ox} = 1935\frac{\mu A}{V^2}, \mu_p C_{ox} = 2125\frac{\mu A}{V^2}$ through simulations
- What is the max V_{in} for M_1 to not go into linear mode?

$$V_{D1} > V_G - V_{t1} \quad \rightarrow \quad V_{D1} > 1.2 - 0.5 = 0.7V$$

- We want $V_{D1} = 1.2V$, since $I_3 = 25\mu A$ we can find $\left(\frac{W}{L}\right)_{3,4}$:

$$I_3 = 25\mu A = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)_3 (V_{GS} - V_t)$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{25 \cdot 2}{2125 \cdot (0.6 - 0.5)^2} = 2.352 \rightarrow \left(\frac{W}{L}\right)_{3,4} = 3 = \frac{720n}{240n}$$



CMOS Miller OTA – Design Process

- We see that the gain of the stage is:

$$A_v = -g_{m2}(r_{ds2}||r_{ds5})$$

- The bandwidth of the stage is:

$$BW = \frac{1}{2\pi R_{out} C_L} = \frac{1}{2\pi(r_{ds2}||r_{ds5})C_L}$$

- Hence the GBW is given by:

$$GBW = A_v \cdot BW = \frac{g_{m1,2}}{2\pi C_L} = 10MHz \;\rightarrow\; g_{m1,2} = 314\mu$$

$$g_{m1,2}^2 = 2I_1 \cdot \mu_n C_{ox}\left(\frac{W}{L}\right)_{1,2} \rightarrow \left(\frac{W}{L}\right)_{1,2} = \frac{(314\mu)^2}{50\mu \cdot \mu_n C_{ox}} \approx 1$$

$$\left(\frac{W}{L}\right)_{1,2} = \left(\frac{300n}{240n}\right)$$

- What is the min V_{in} for M_4 to not go into linear mode?

$$V_{in,min} > V_{DSAT5} + V_{GS1}$$

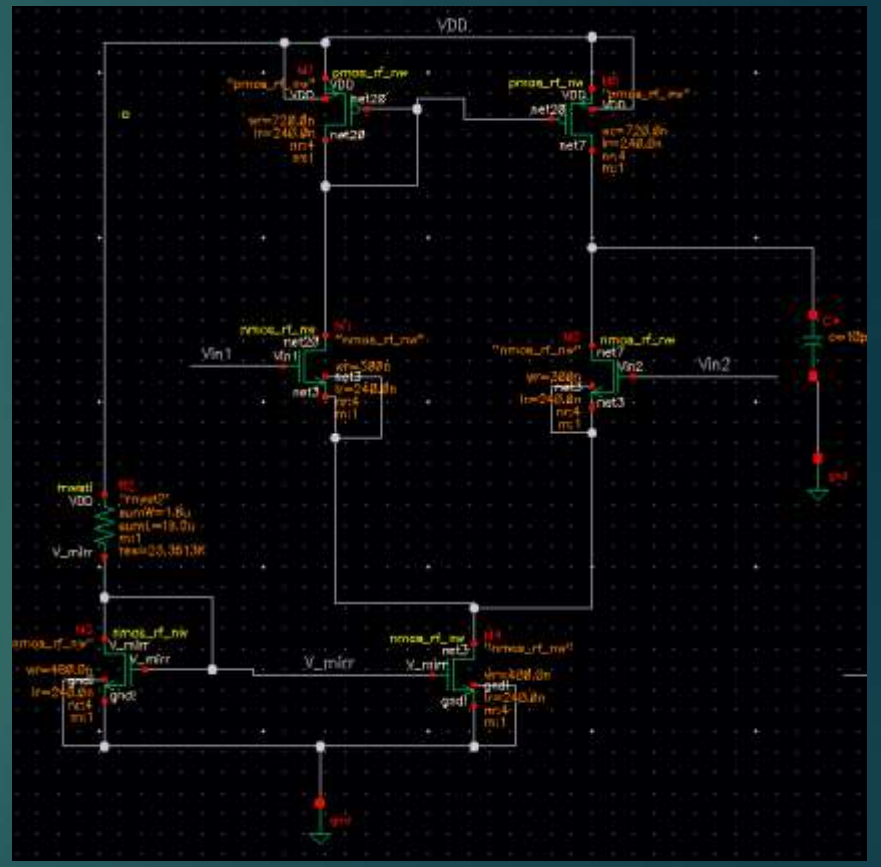
$$I_{D1} = 25\mu = \frac{1935\mu}{2} \cdot 1.25 \cdot (V_{GS} - 0.4)^2 \rightarrow V_{GS1} = 0.55V$$

- We find $V_{DSAT,5} = 0.18V$ from the simulation

$$V_{in,min} > 0.55V + 0.18V = 0.73V$$

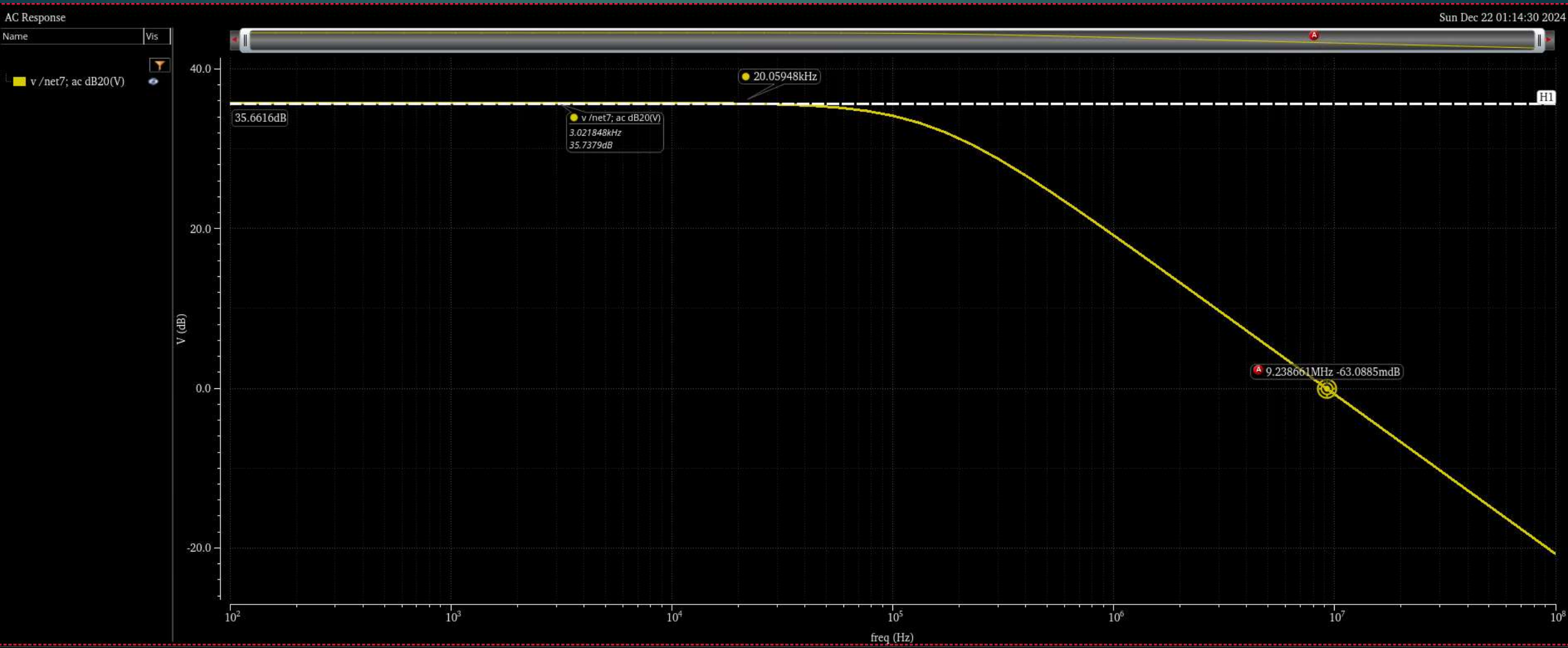
$$I_5 = 50\mu A = \frac{1935\mu}{2} \cdot \left(\frac{W}{L}\right)_{5,6} \cdot 0.2^2 \rightarrow \left(\frac{W}{L}\right)_{5,6} = 1.3 \rightarrow (W_L)_{5,6} = \left(\frac{480n}{240n}\right)$$

- Lastly, we sized R to 23.35kΩ to get a 50uA current in this bias branch.



$AC\ Response\ For\ V_{CM} = 0.9V$

This is a one pole system so phase drops to -90 degrees and stability isn't a matter of concern.



CMOS Miller OTA – Design Process

- Now we design the second stage to boost the total gain

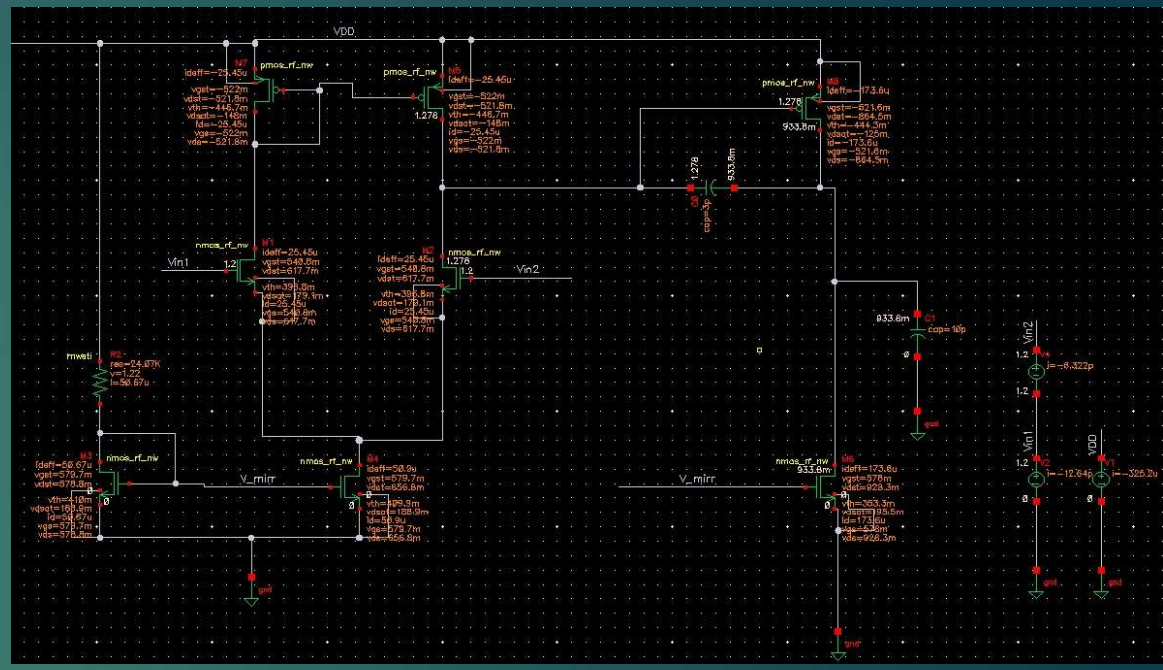
$$A_{v2} = -g_{m7}(r_{ds7}||r_{ds8})$$

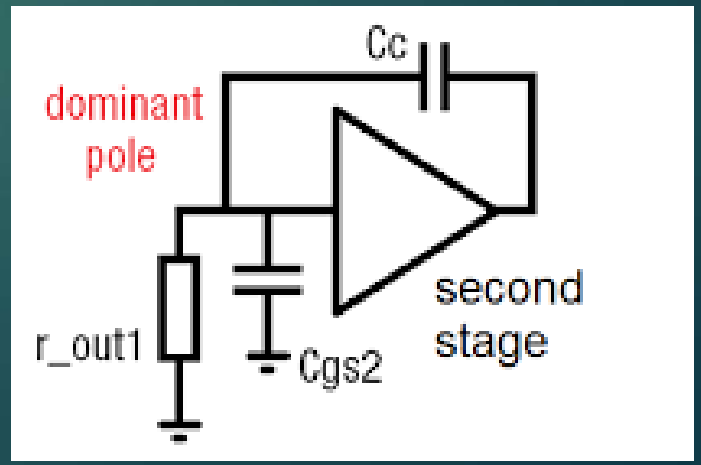
- The bandwidth of the stage is:

$$BW = \frac{1}{2\pi R_{out} C_L} = \frac{1}{2\pi (r_{ds7}||r_{ds8}) C_L}$$

- Very similar to the first stage, hence the poles of both stages almost coincide which means the phase is going to drop to -180 degrees very fast and the PM at the f_{co} is going to be very small or negative! The system might not be stable.
- Thus, we use a compensating capacitor to decrease the pole of the first stage and increase the non dominant pole beyond the GBW to have effectively a 1 pole system.
- Instead of intentionally adding a large C_C, we utilize Miller effect.
- The first pole now is:

$$P_1 = \frac{1}{R_{out1} \cdot (C_{par} + (1 + A)C_C)}$$

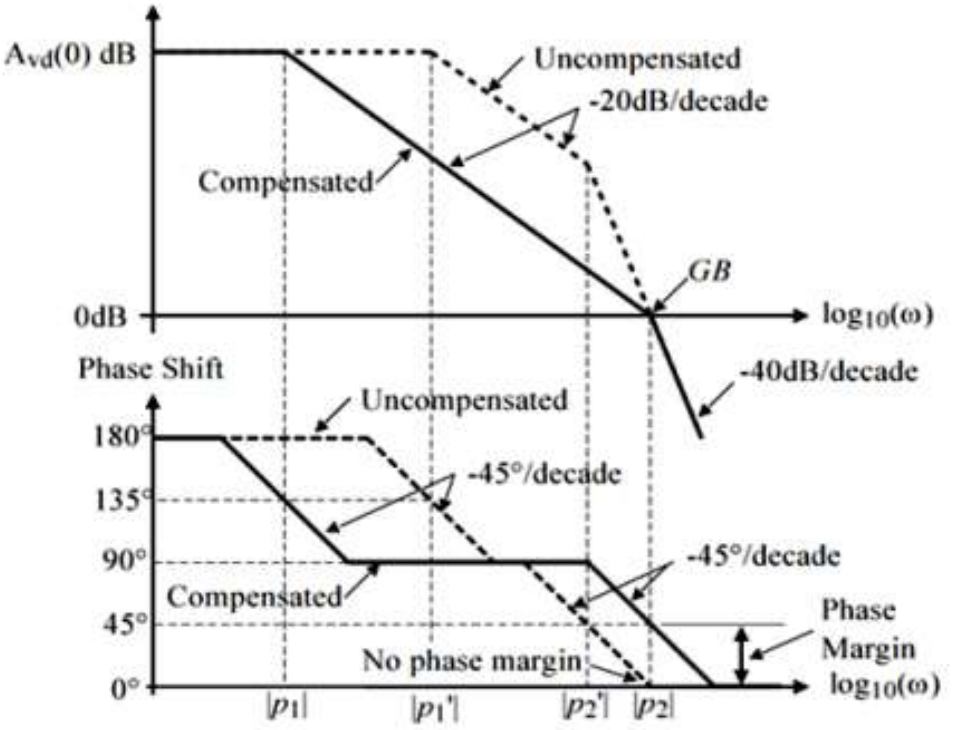




CMOS Miller OTA – Design Process

- The TF of the circuit is:
- $\frac{V_{out}}{V_{in}} = \frac{g_{m1}R_{out1}g_{m2}R_{out2}\left(1-\frac{C_C s}{g_{m2}}\right)}{s^2\left(R_{out1}R_{out2}\left(C_{par}C_C+C_{par}C_C+C_LC_C\right)+s\left(R_{out2}\left(C_C+C_L+R_{out1}\left(C_C+C_{par}\right)+g_{m2}R_{out1}R_{out2}C_C\right)+1\right.\right.}$
- We can extract:
  DC gain=$g_{m1}g_{m2}R_{out1}R_{out2}$
  Dominant pole $P_1 \approx \frac{1}{C_C R_{out1} g_{m2} R_{out2}}$
  Non dominant pole $P_2 \approx \frac{g_{m2}}{C_L}$
  RHP zero $Z = \frac{g_{m2}}{C_C}$ - also drops phase by 90 degrees

- $GBW = DC\ gain \cdot P_1 = \frac{g_{m1}}{C_C}$
- To minimize the effect of the zero we want
- $Z = 10GBW$
- $\measuredangle \frac{V_{out}}{V_{in}}(\omega_{0dB}) = -\tan^{-1}\left(\frac{GBW}{P_1}\right) - \tan^{-1}\left(\frac{GBW}{P_2}\right) - \tan^{-1}\left(\frac{GBW}{Z}\right) =$
- $= -\tan^{-1}(DC\ Gain) - \tan^{-1}\left(\frac{GBW}{P_2}\right) - \tan^{-1}(0.1) =$
- $\measuredangle \frac{V_{out}}{V_{in}}(\omega_{0dB}) - 180 + PM = -90 - \tan^{-1}\left(\frac{GBW}{P2}\right) - 5.7$



CMOS Miller OTA – Design Process

- $\angle \frac{V_{out}}{V_{in}}(\omega_{0dB}) - 180 + PM = -90 - \tan^{-1}\left(\frac{GBW}{P2}\right) - 5.7$

- $PM = 180 - 84.3 - \tan^{-1}(\frac{GBW}{P_2})$
- We want PM=60:
- $P_2 = 2GBW$
- $\frac{g_{m2}}{C_L} = 2 \cdot \frac{g_{m1}}{C_C}$
- $Z = 10GBW \rightarrow \frac{g_{m2}}{C_C} = \frac{10g_{m1}}{C_C} \rightarrow g_{m2} = 10g_{m1}$
- $\frac{10g_{m1}}{C_L} = 2\frac{g_{m1}}{C_C} \rightarrow C_C = 0.2C_L$ to get PM=60

- In the 2-stage OTA, SR is given by:
- $SR = \frac{I_5}{C_C}$

- $C_C = 0.2C_L = 2pF \rightarrow C_C = 3pF$ because C_L will also have C_{par}
- $SR = \frac{I_5}{C_C} = \frac{50u}{3p} = 16.5\frac{V}{\mu s}$

Specification	Intended	Reached
DC Gain (dB)	>60 (70 if possible)	67.5-68dB
GBW (MHz)	5-10MHz	13.5-14MHz
Slew Rate ($\frac{V}{\mu s}$)	1-5	16
Phase Margin (°)	60	63-64
C_L (pF)	10pF	10pF
Power (μW)	500	480-495
Input Common Mode Range (V)	0.6V-1.5V	0.75V-1.2V(1.6V)

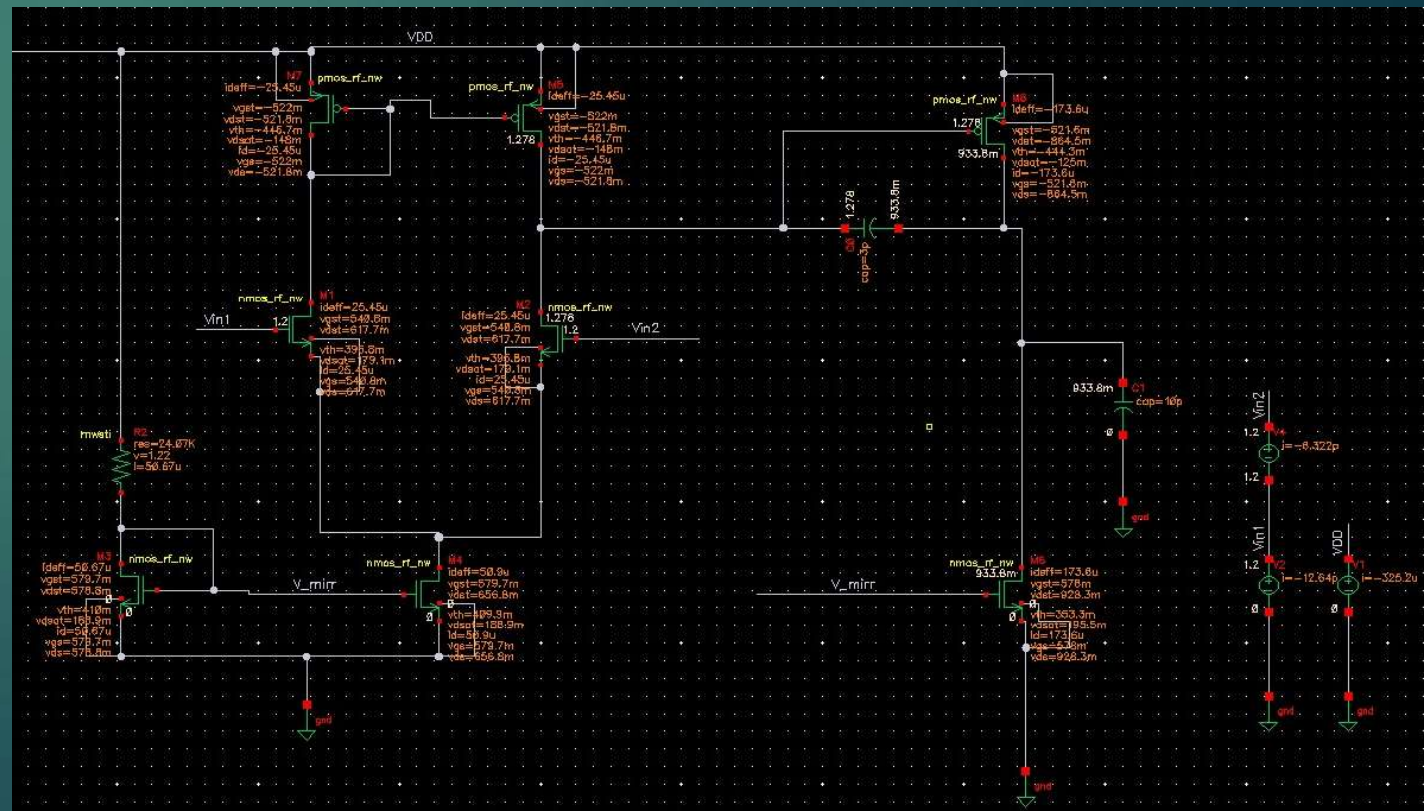
CMOS Miller OTA – Design Process

- We got $g_{m1} = 350\mu$, to get PM=60 we need:
- $g_{m6} = 10g_{m1} = 3500\mu$
- Because of the mirroring:
- $V_{DS3} = V_{DS4} = V_{DS6} \rightarrow V_{GS3} = V_{GS4} = V_{GS6}$
- Hence, the currents through M3,M4,M6 is proportional to their $(\frac{W}{L})$ ratios
- $$\frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4} = \frac{I_7}{I_4} = \frac{g_{m7}}{g_{m4}} \rightarrow \left(\frac{W}{L}\right)_7 = \frac{3500}{565} \cdot 3 = 18.6 \approx 19$$
- In this technology max width of M6 is 3μ,

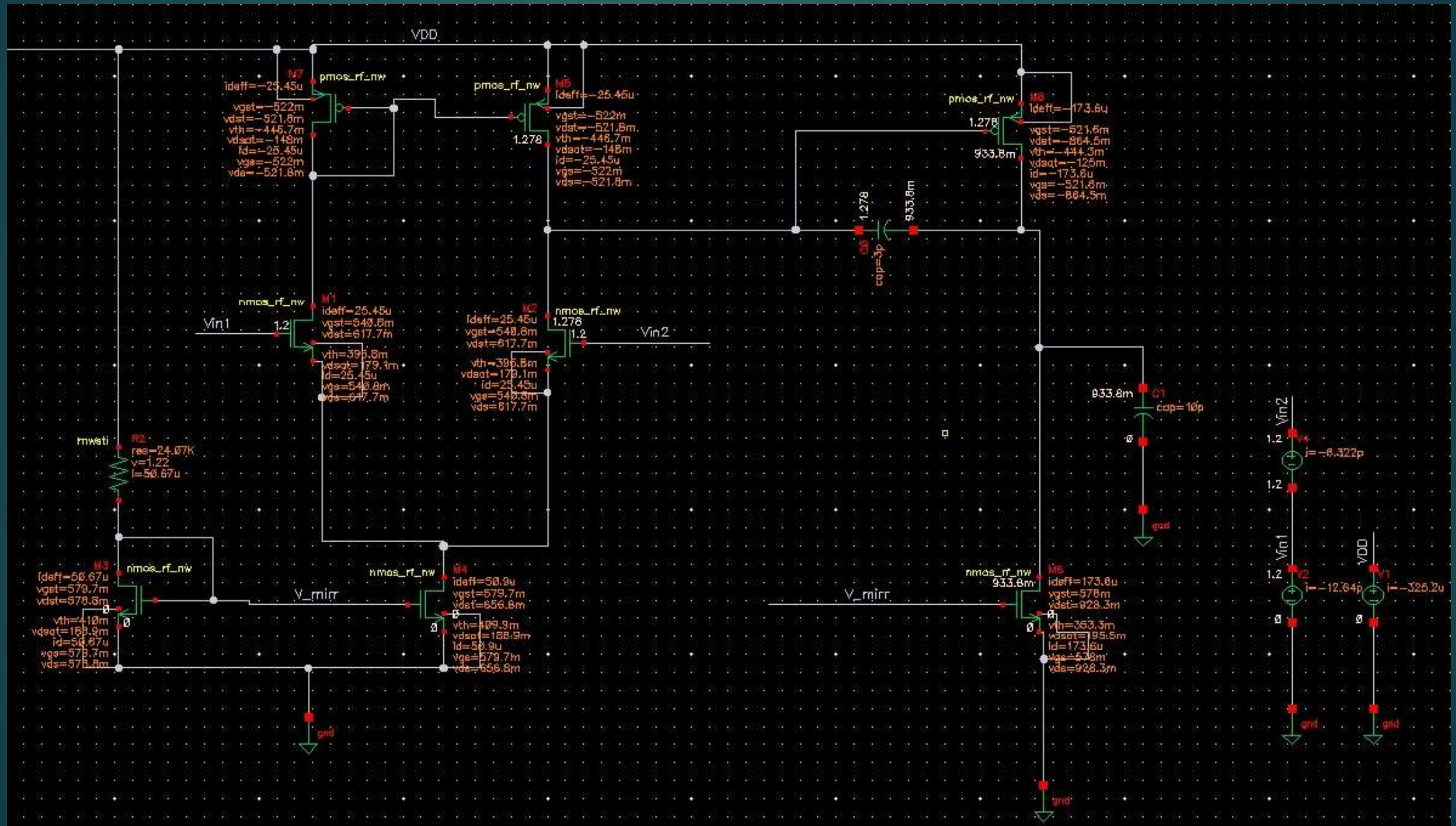
So we decrease $L_7 = 120n$ to get

$$\left(\frac{W}{L}\right)_7 = \frac{2.3u}{120n}$$

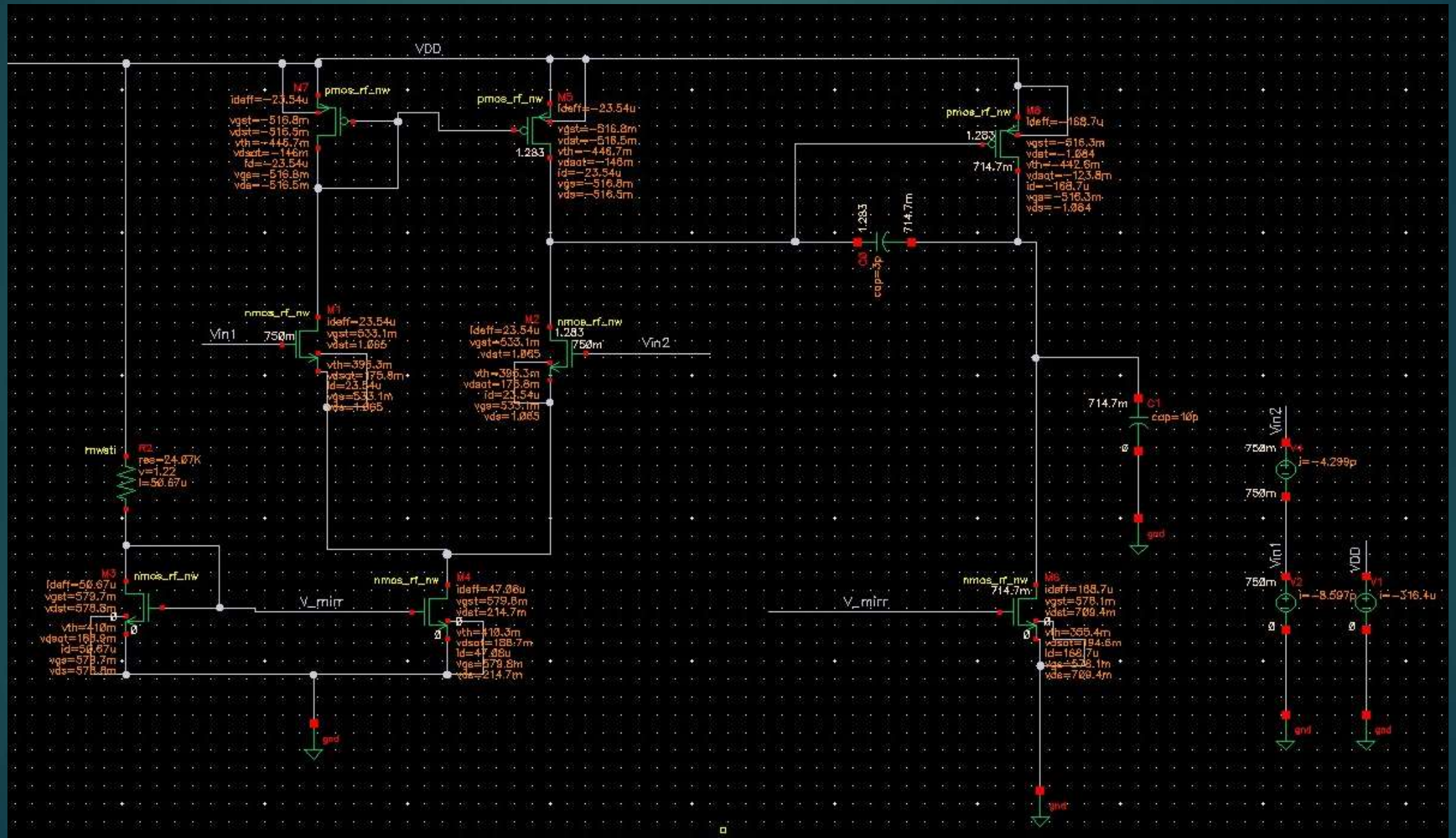
- $$\frac{I_7}{I_4} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4} \rightarrow I_7 = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_4} I_4 = \frac{19}{3} \cdot 23.81\mu = 150.8$$
- Only M8 sizing remains:
- $$\frac{I_8}{I_5} = \frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_5} \rightarrow \left(\frac{W}{L}\right)_8 = \frac{153\mu}{50\mu} \cdot 2 \approx 7$$
- The design is finished, to get a higher gain we changed $\left(\frac{W}{L}\right)_7 = \frac{1.85\mu}{120n}$



$DC\ Operation\ Point\ For\ V_{CM} = 1.2V$

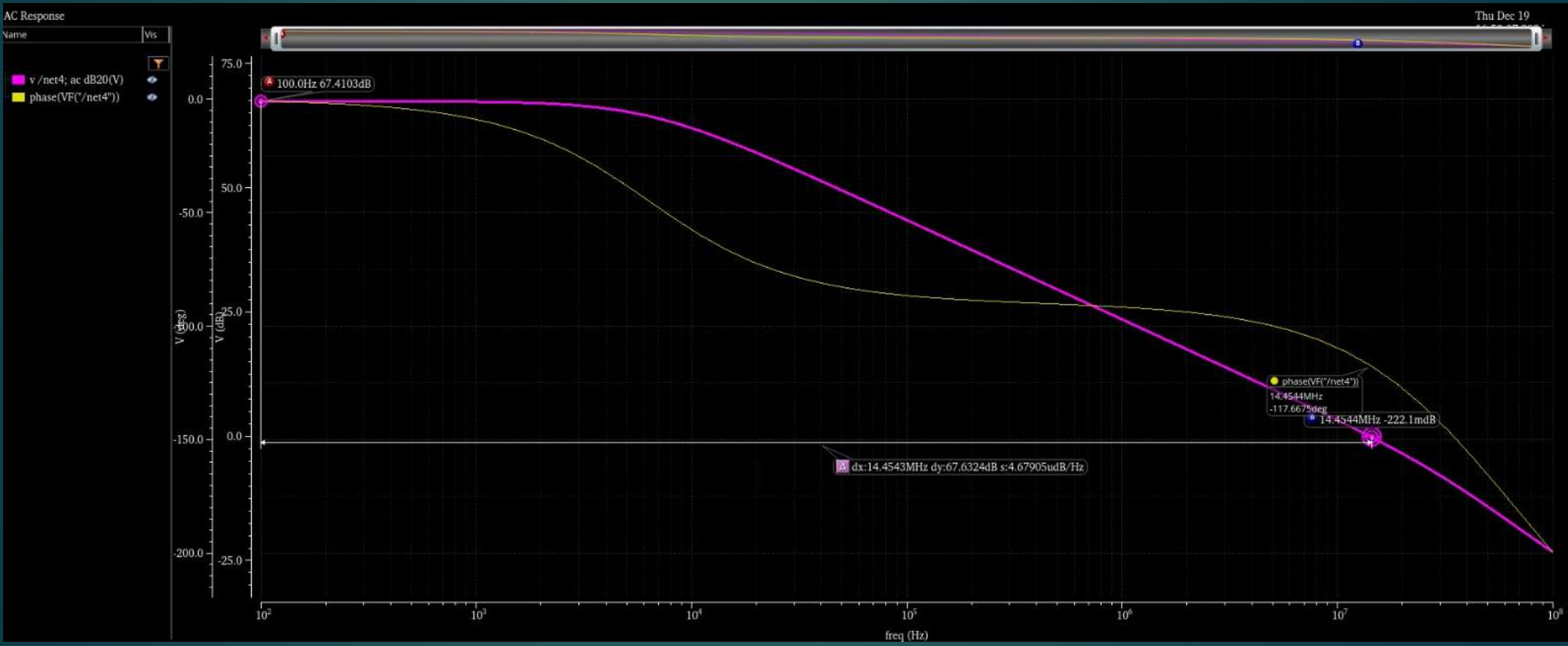


$DC\ Operation\ Point\ For\ V_{CM} = 0.75V$



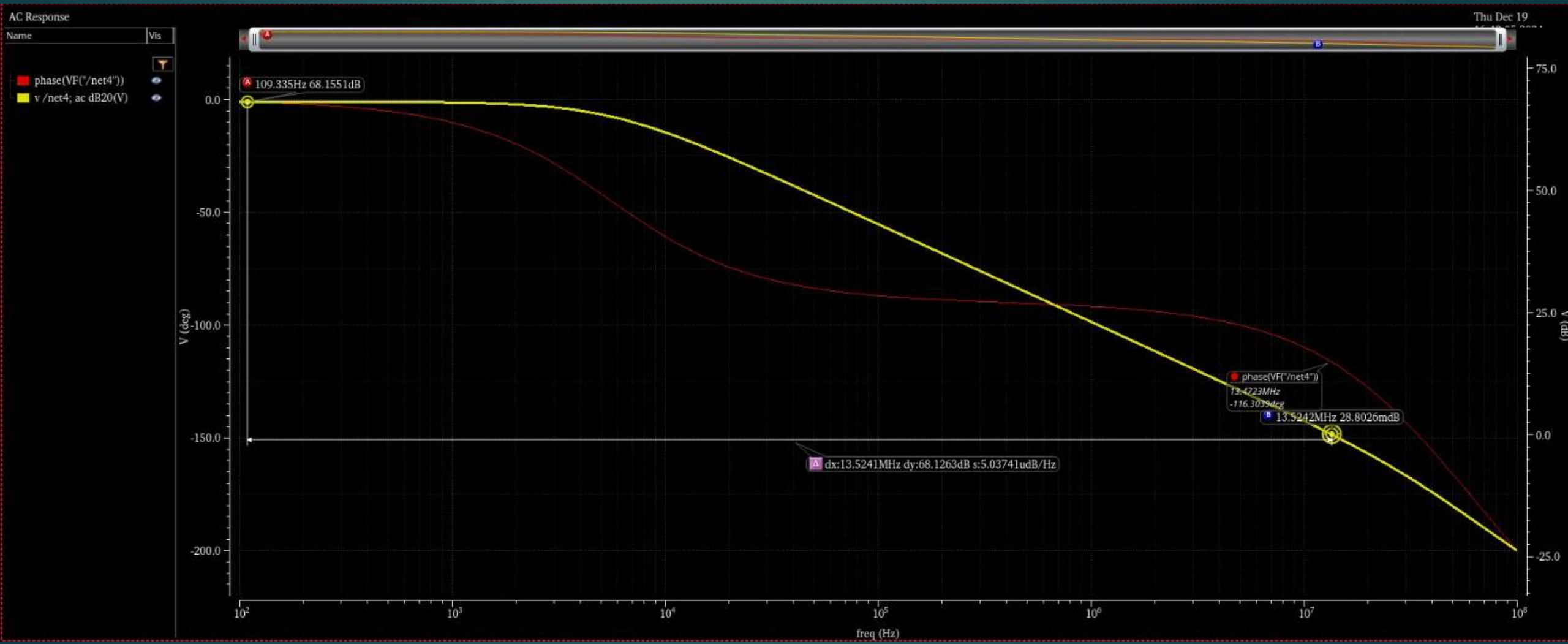
$AC\ Response\ For\ V_{CM} = 1.2V$

The AC signal is connected to the non-inverting input so no phase inversion



$AC\ Response\ For\ V_{CM} = 0.75V$

The AC signal is connected to the non-inverting input so no phase inversion



$Transient\ Response\ For\ V_{CM} = 1.2V$

AC input is a 500uV amplitude sin wave at a 1kHz to the non-inverting input

$Transient\ Response\ For\ V_{CM} = 0.75V$

AC input is a 500uV amplitude sin wave at a 1kHz to the non-inverting input