The Iby and Aladar Fleischman Faculty of Engineering
Tel Aviv University

LDO Regulator

DPLL 2024/25

Project Name: Digital High Frequency Chip – Linear Low Dropout Voltage Regulator
Project Number: 3097

Students:
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Project Instructor:
Name: Tal Elazar

Project carried out at: University

Instructor's Signature: ____Tal Elazar____

Abstract and Introduction

- The project's objective is to design an LDO for a DPLL.
- DPLLs require a highly stable voltage input for proper operation.
- Variations in supply voltage, temperature, and load current can degrade performance.
- The LDO is necessary to maintain a constant input voltage despite these variations.
- A well-designed bandgap reference circuit and a high-gain stable OTA are essential for the LDO's design.

Updated Project Requirements

- **Implementation Method:**

- Schematic design, layout design, and testing of the LDO performed exclusively in Cadence Virtuoso.

- **Project Requirements:**

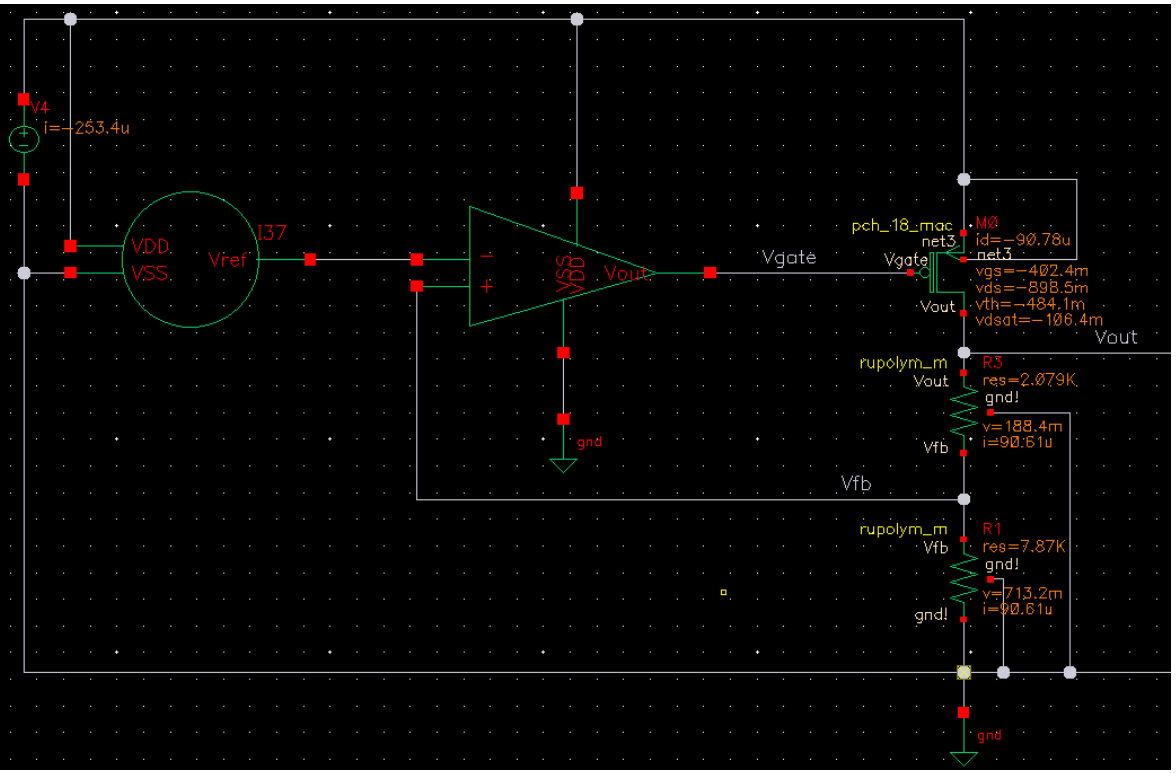
- Bandgap Reference voltage – 0.713V.
- LDO output voltage – 0.9V.
- Load current range – 0 – 50mA.
- Resistive feedback network current drawn – $< 50\mu A$.
- Output voltage temperature coefficient – $\leq 1\%$ across temperature range -40-125°C ($60\frac{ppm}{°C}$).
- Line regulation $\leq 0.01\frac{V}{V}$.
- Load regulation $\leq 0.1\frac{mV}{mA}$.

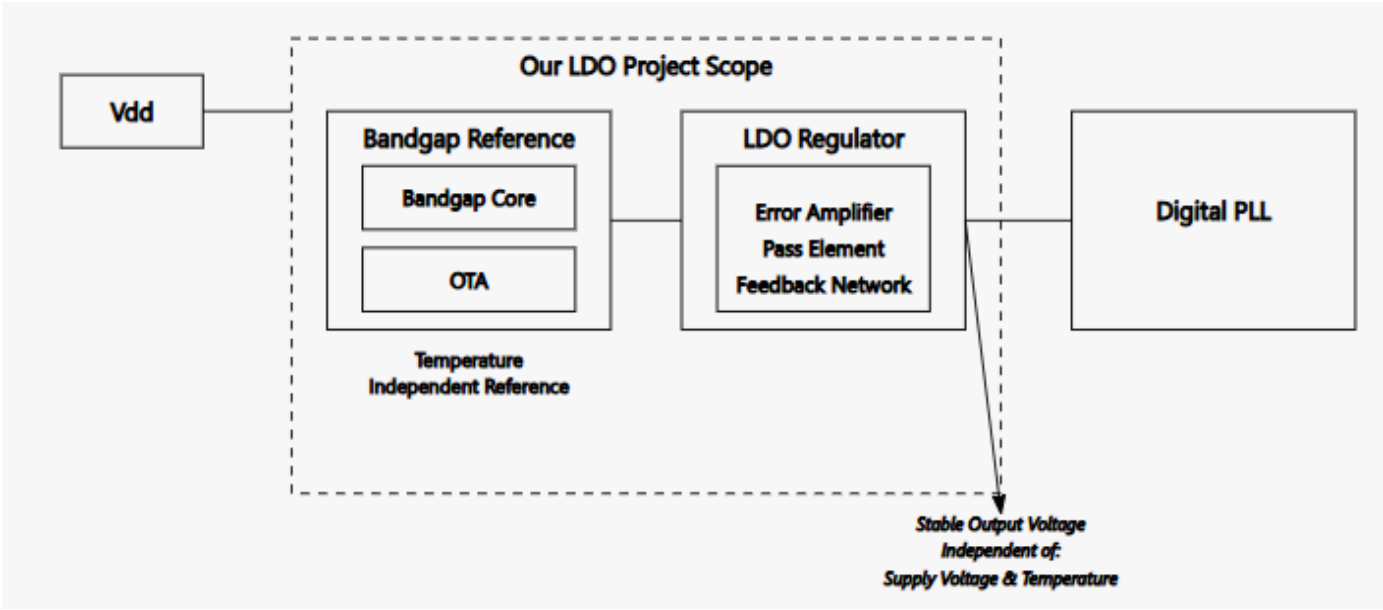
Project Deliverables

- **Project Deliverables:**

- Bandgap reference circuit – schematic design, layout design, OP simulation, line regulation simulation, temperature coefficient simulation (pre- and post-layout).
- OTA – schematic design, layout design, OP simulation, loop stability simulation (Gain & GBW & PM), transient response simulation (pre- and post-layout).
- LDO – schematic design, layout design, OP simulation, loop stability simulation, line regulation and load regulation simulations, temperature coefficient simulation (pre- and post layout).

LDO – Block Diagram



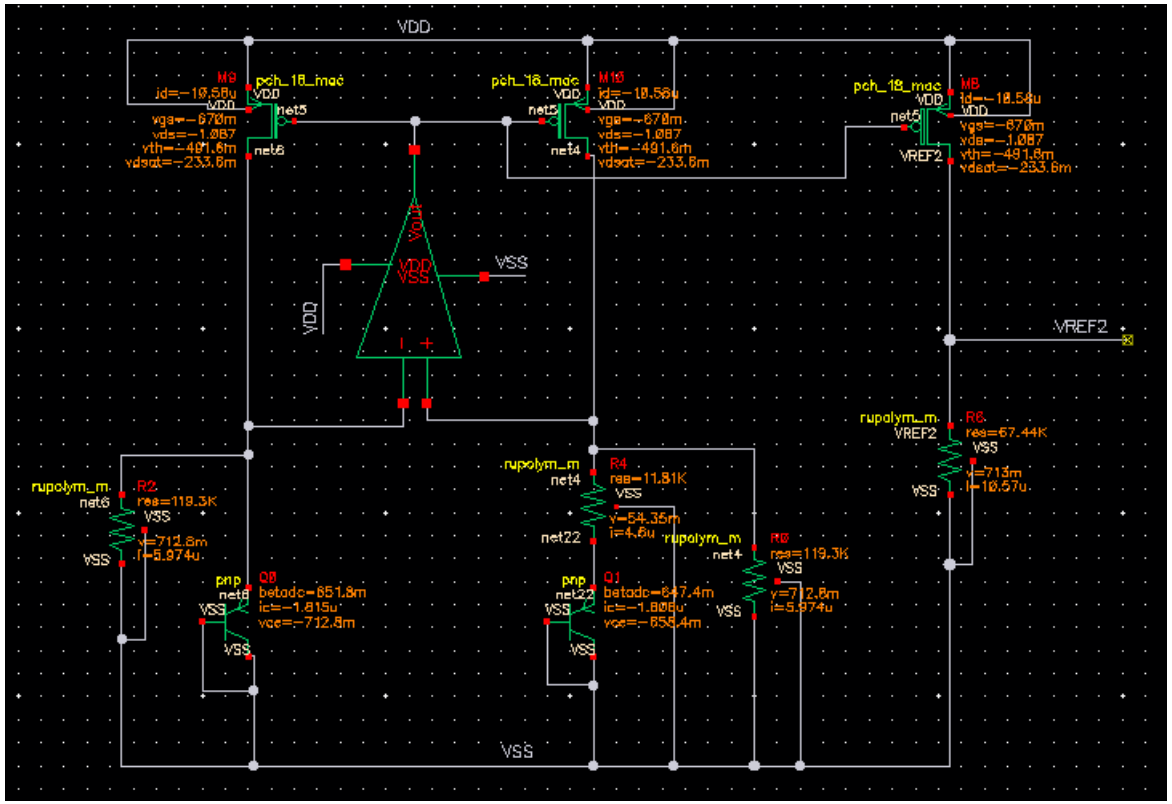


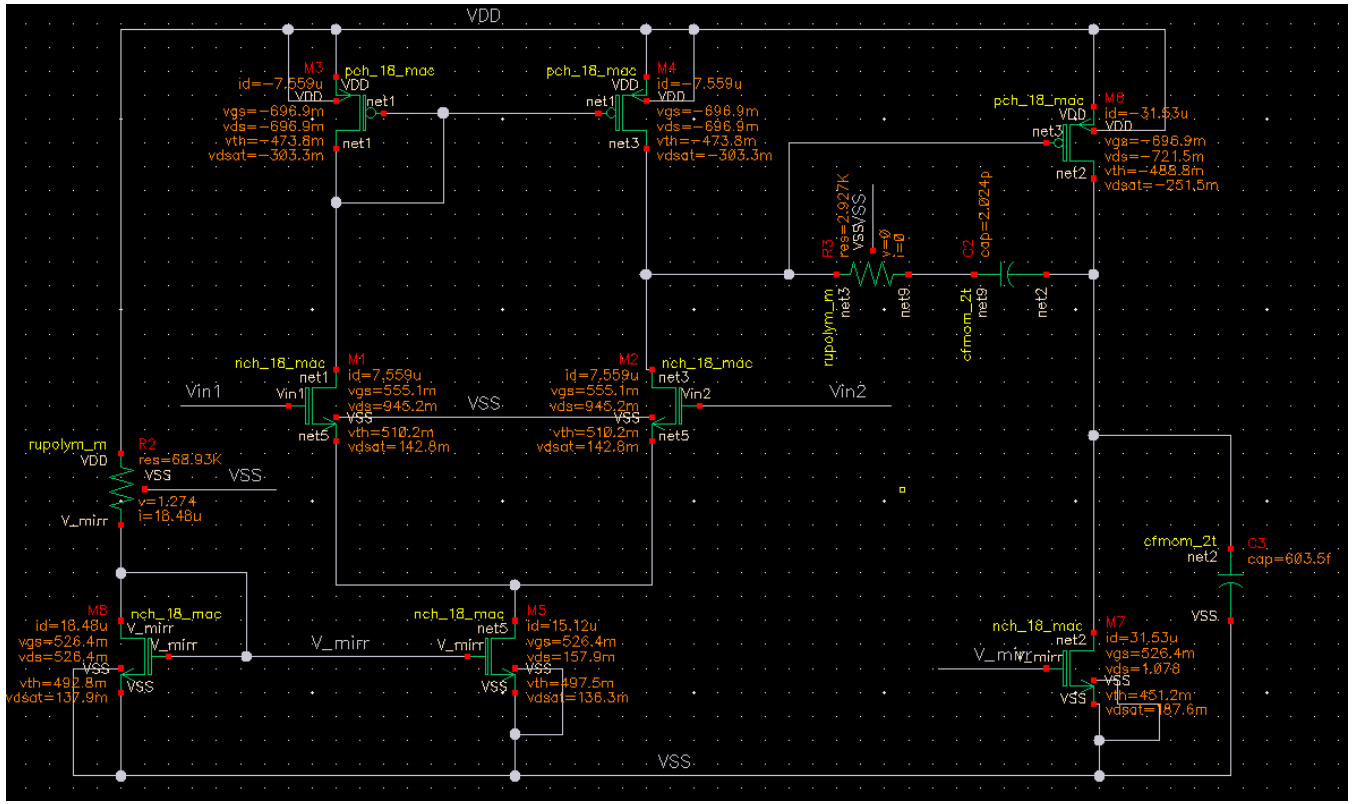
- **LDO:**

- Maintains a stable and constant output voltage despite supply voltage and load current fluctuations.
- The negative feedback loop consisting of the EA, pass transistor and resistor network regulates the output voltage.
- Designed in Virtuoso from scratch.

$$V_{fb} > V_{ref} \rightarrow V_{gate}\uparrow \rightarrow V_{sg}\downarrow \rightarrow I_{SD}\downarrow \rightarrow V_{fb}\downarrow$$
$$V_{fb} < V_{ref} \rightarrow V_{gate}\downarrow \rightarrow V_{sg}\uparrow \rightarrow I_{SD}\uparrow \rightarrow V_{fb}\uparrow$$

LDO – Block Diagram





- **BGR:**

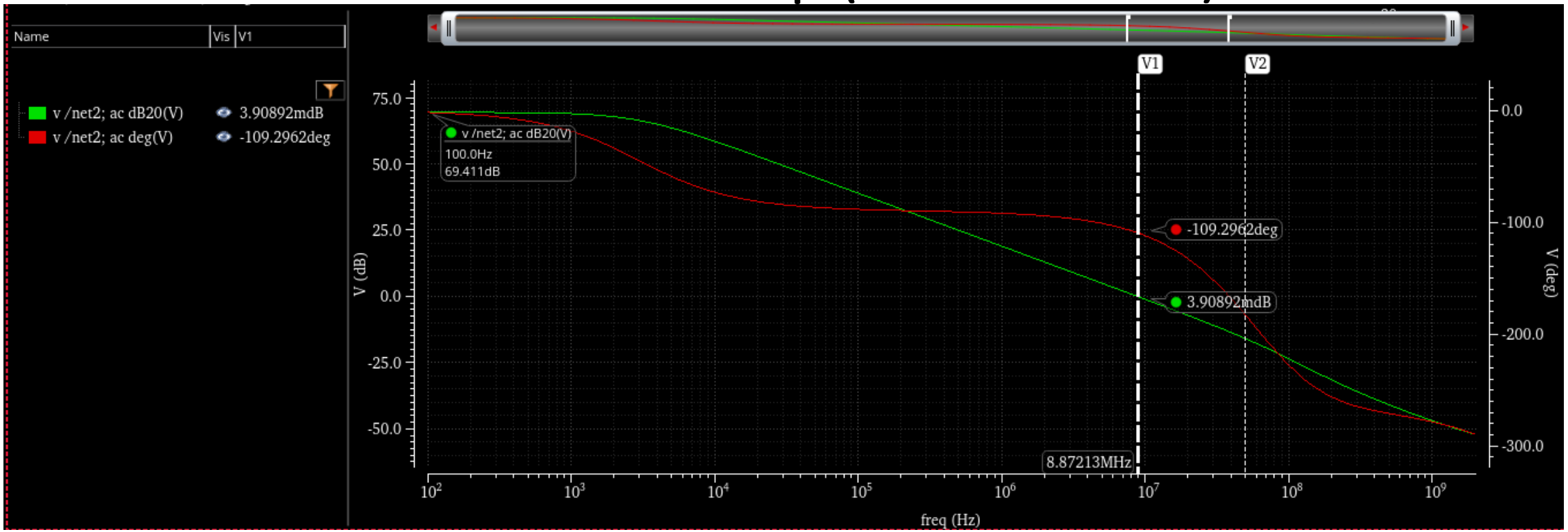
- Generates a stable reference voltage that remains constant despite temperature and supply voltage variations.
- Designed in Virtuoso from scratch.

- **OTA:**

- In BGR – balances the voltages in two branches to stabilize the reference voltage, compensating for temperature variations.
- In LDO – controls transistor's current based on sampled output voltage to maintain regulation.
- Designed in Virtuoso from scratch.

Project's Products Achieved So Far - OTA

Vout – AC Sweep (VCM=0.713V)

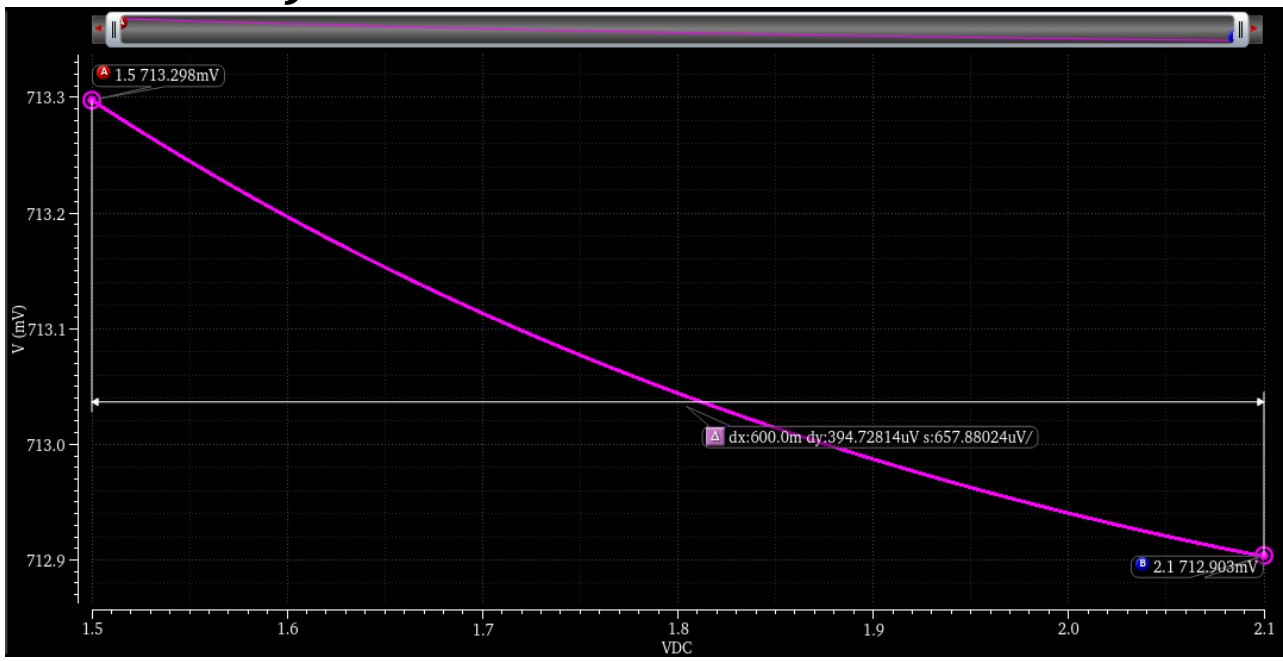


Specification	Goal	Achieved
DC Gain (dB)	>60 (70 if possible)	69.4
GBW (MHz)	5-10	8.9
PM (°)	>60	70
Power (µW)	Minimize	120

Project's Products Achieved So Far - BGR

V_{ref} across temperatures

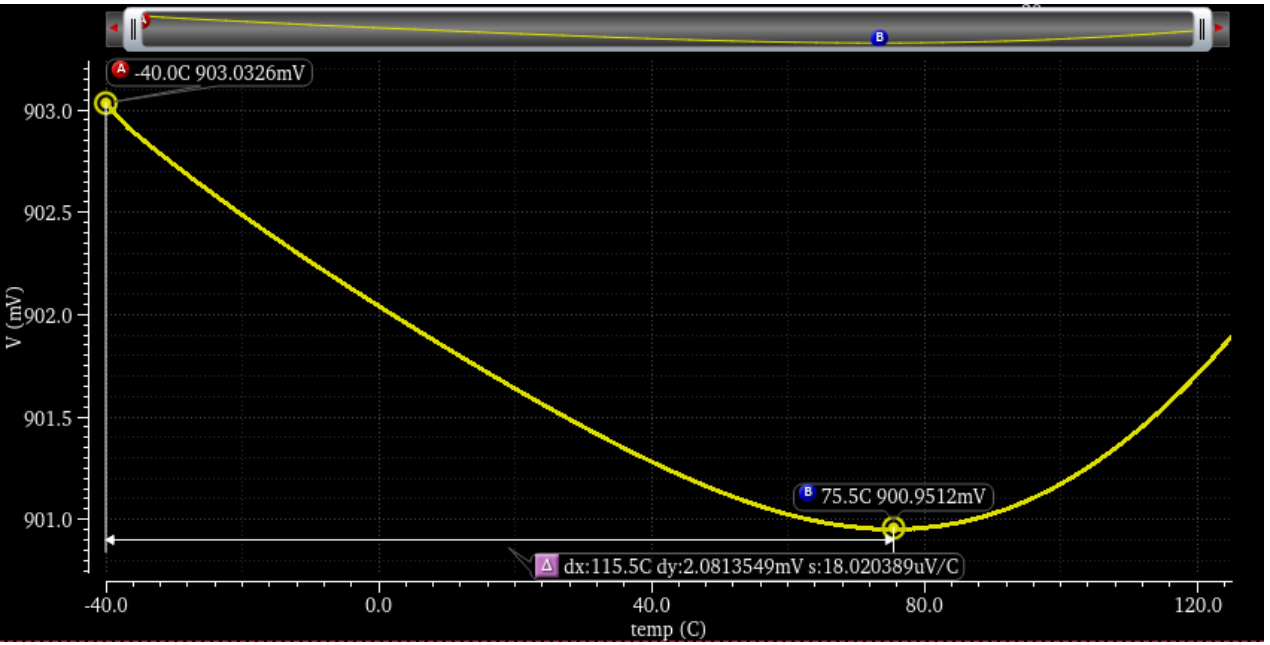
V_{ref} across supply variation



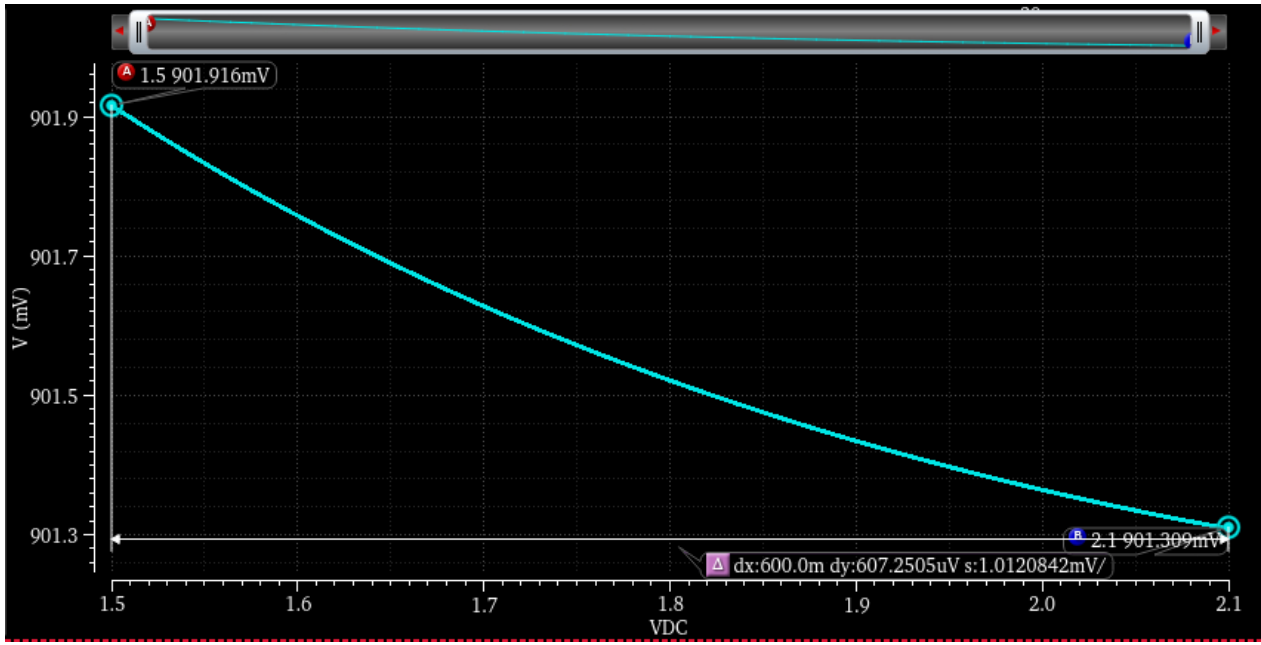
Specification	Goal	Achieved
Line Regulation (dB)	>40	64
Temperature Coefficient ($\frac{ppm}{°C}$)	<60	10
Power (µW)	Minimize	60

Project's Products Achieved So Far - LDO

V_{out} across temperatures



Line Regulation – Vout vs. Vin



Specification	Goal	Achieved
Line Regulation (V/V)	<0.01	0.001
Temperature Coefficient ($\frac{ppm}{°C}$)	<60	13.4
$\frac{\Delta V_{out}}{\Delta I_{Load}}$ =Load Regulation ($\frac{mV}{mA}$)	<0.1	0.036

Updated Schedule

Milestone	Planned Delivery Date	Actual Delivery Date	Notes
Literature review and background study	15/11/24	15/11/24	
Submitting project workplan	24/11/24	24/11/24	
Summary of a digital PLL and the LDO, BGR circuits	08/12/24	08/12/24	Presented during a project meeting
Schematic design of the bandgap reference circuit	15/12/24	Initial – 10/12/24 Final – 15/01/25	Initial – With ideal op-amp Final – With our OTA + topology refinement
Schematic design of the OTA	30/01/25	08/01/25	
Initial Schematic design of the LDO circuit	01/03/25	30/01/25	Moved up to check suitability of OTA + BGR for LDO before starting layouts
Progress Presentation Submission	05/03/25	05/03/25	
Layout design of the OTA	20/03/25		Performed in parallel. Work in progress.
Layout design of the bandgap reference circuit	20/03/25		

Milestone	Planned Date	Actual Date	Notes
Final Schematic design of the LDO circuit	30/03/25		Refining design post layout of OTA + BGR
Layout design of the LDO circuit	20/04/25		
Submitting Mid-Semester Project Update	21/04/25		
Final testing (post layout) and validation	01/05/25 (flexible)		Testing with completed blocks of DPLL by other pairs
Poster Submission and finishing the design	25/05/25		
Writing project book and final presentation preparation	25/06/25		
Tape out	25/07/25		
Final deliverables submission	July-August 2025		