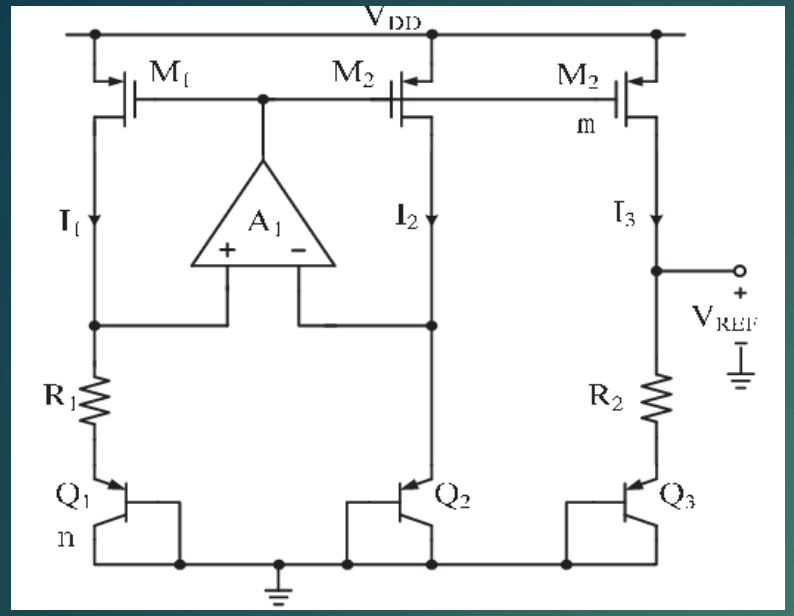
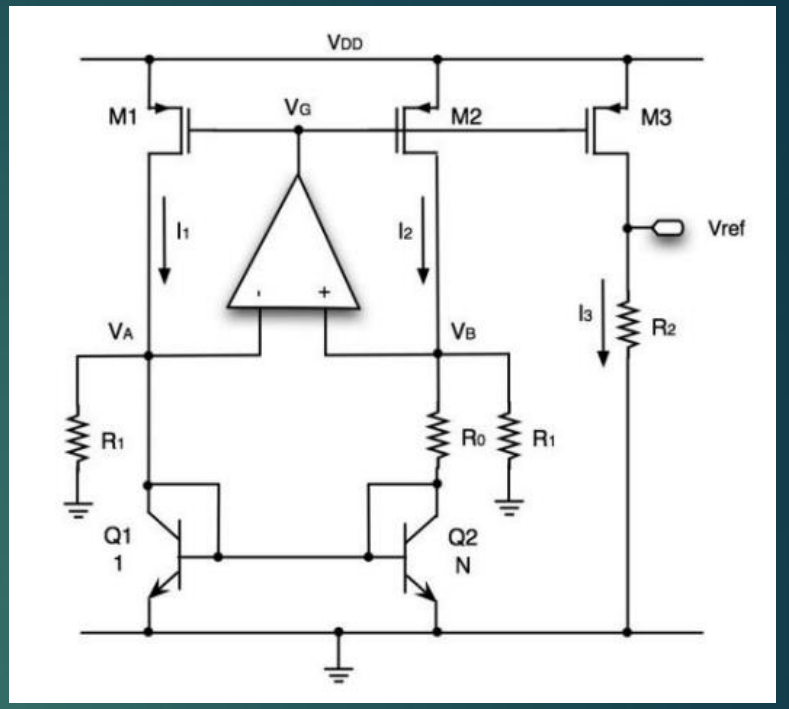
BGR



$$I_1 = I_2 = I_3 = \frac{ln(n)V_T}{R_1}$$

$$V_{ref} = V_{BE} + \frac{R_2 ln(n)V_T}{R_1}$$

- Pick R_1 to set current in the branches
- Pick R_2 to cancel the PTAT with CTAT ($\frac{dV_{ref}}{dT} = 0$)
- V_{ref} set and no control over it, usually around 1.2V



$$I_1 = I_2 = I_3 = \frac{ln(n)V_T}{R_0} + \frac{V_A}{R_1}$$

$$V_{ref} = R_2(\frac{ln(n)V_T}{R_0} + \frac{V_A}{R_1})$$

- Pick R_o or R_1 to get desired current range
- Pick precise R_1 or R_0 to cancel the PTAT with CTAT
- Pick R_2 to get desired V_{ref}
- We wanted a V_{ref} of 713mV

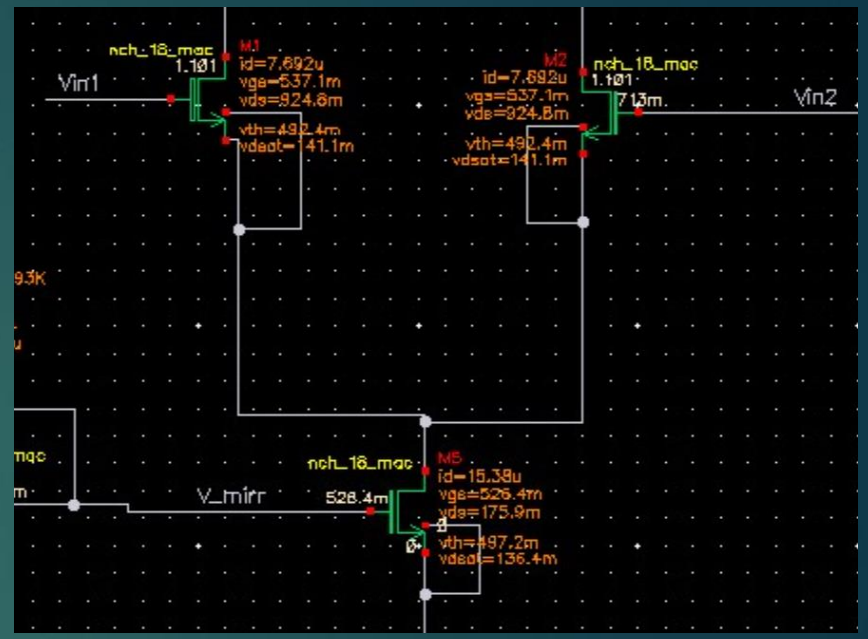
BGR

- Why $V_{ref} = 0.713V$?

1) The minimal input common mode voltage of the OTA that will be used for both BGR and LDO is lower bounded by:

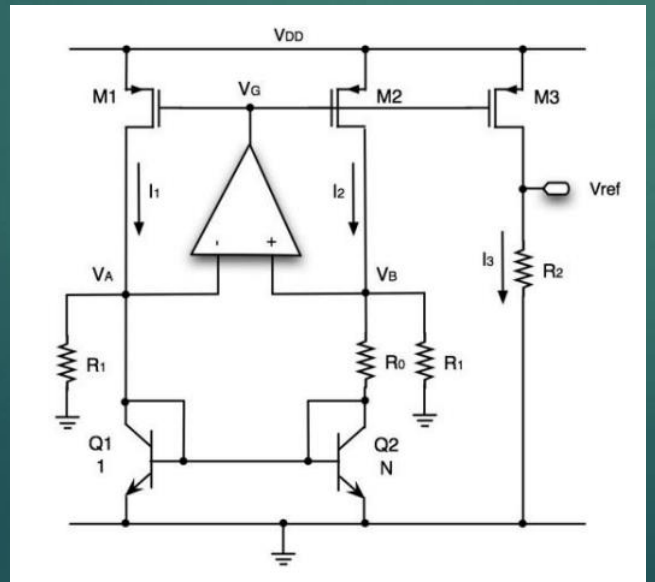
$$V_{in,min} > V_{DSAT_5} + V_{GS1} > 120 + 500 = 620mV$$

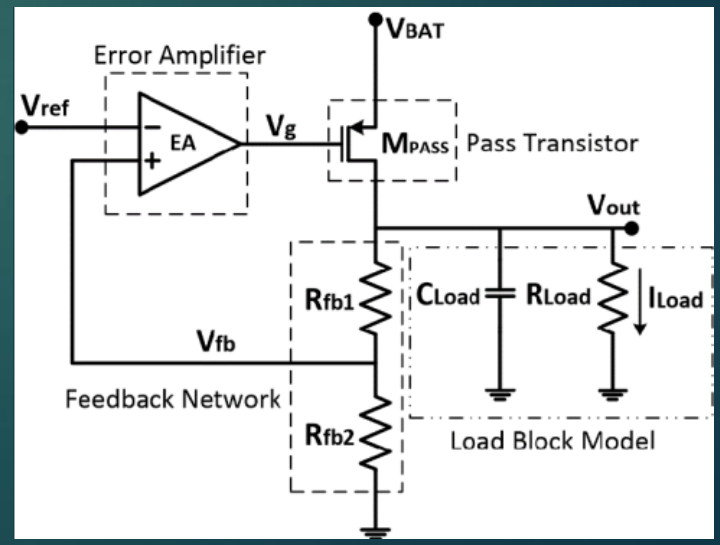
Hence, $V_{ref} > 0.62V$



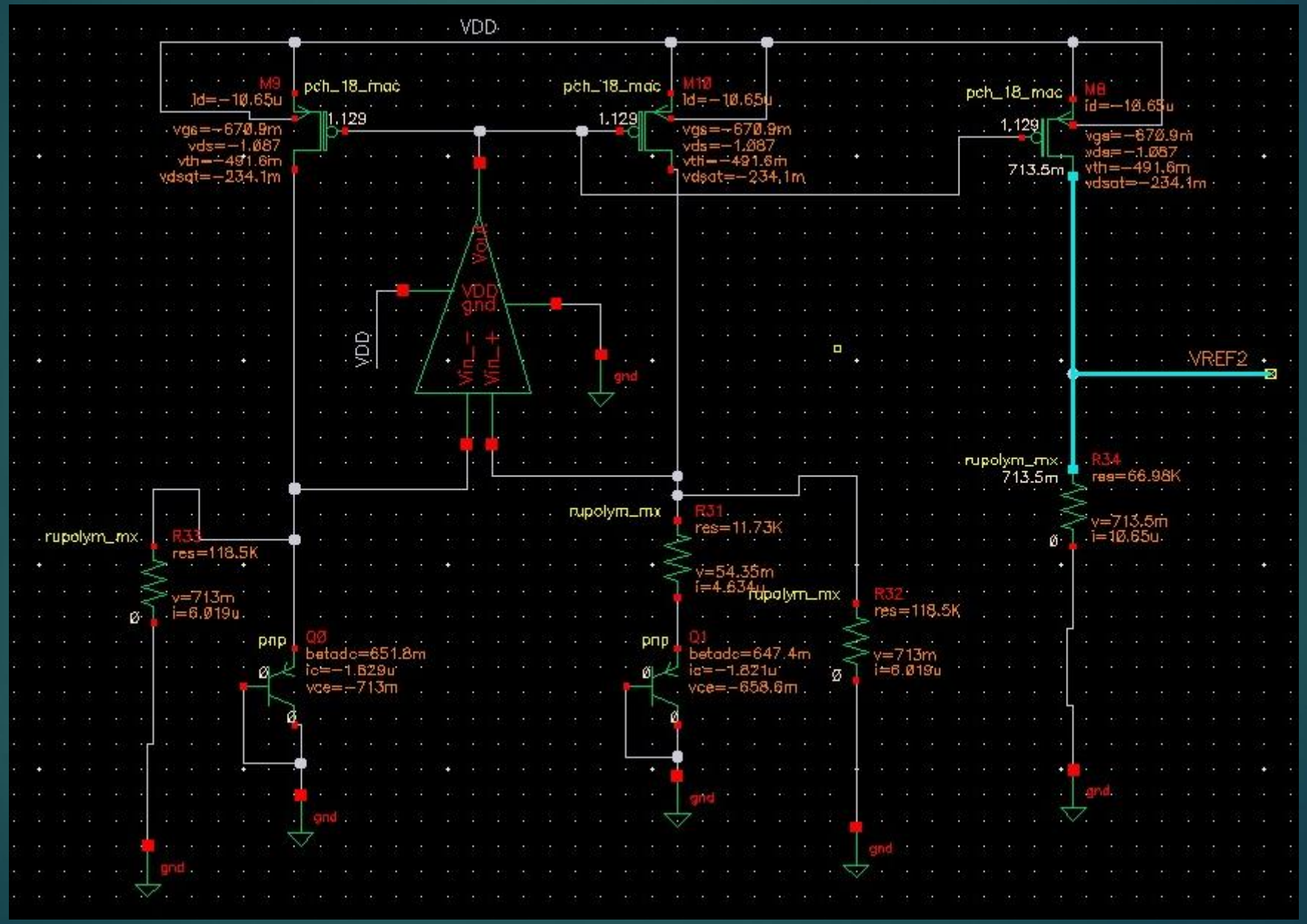
2) In the LDO, nominal V_{out} is 0.9V, hence $V_{fb} < 0.9V$ thus $V_{ref} < 0.9V$

3) $V_A = V_B = 0.713V$, hence V_{DS} will be equal for all current mirror transistors, so current matching is much better, which will improve the PSRR (V_{ref} sensitivity to V_{DD} fluctuations).





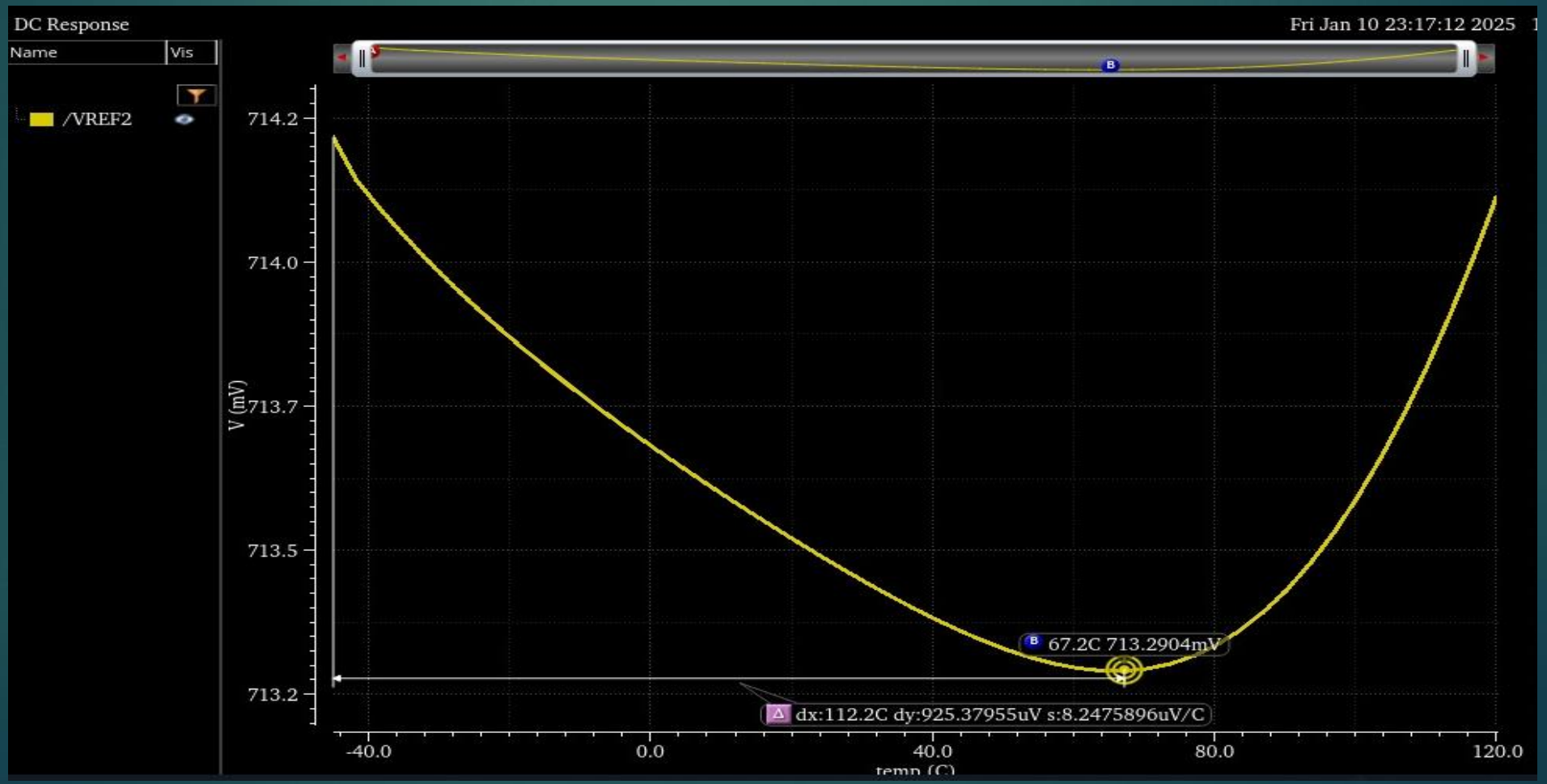
BGR - DC Operating Point



V_{ref} across temperature

Max fluctuation is 0.925mV, approx. $\frac{V_{ref_{max}} - V_{ref_{min}}}{V_{ref_{avg}} * \Delta T} * 10^6 = 7.6 \frac{ppm}{^\circ C}$

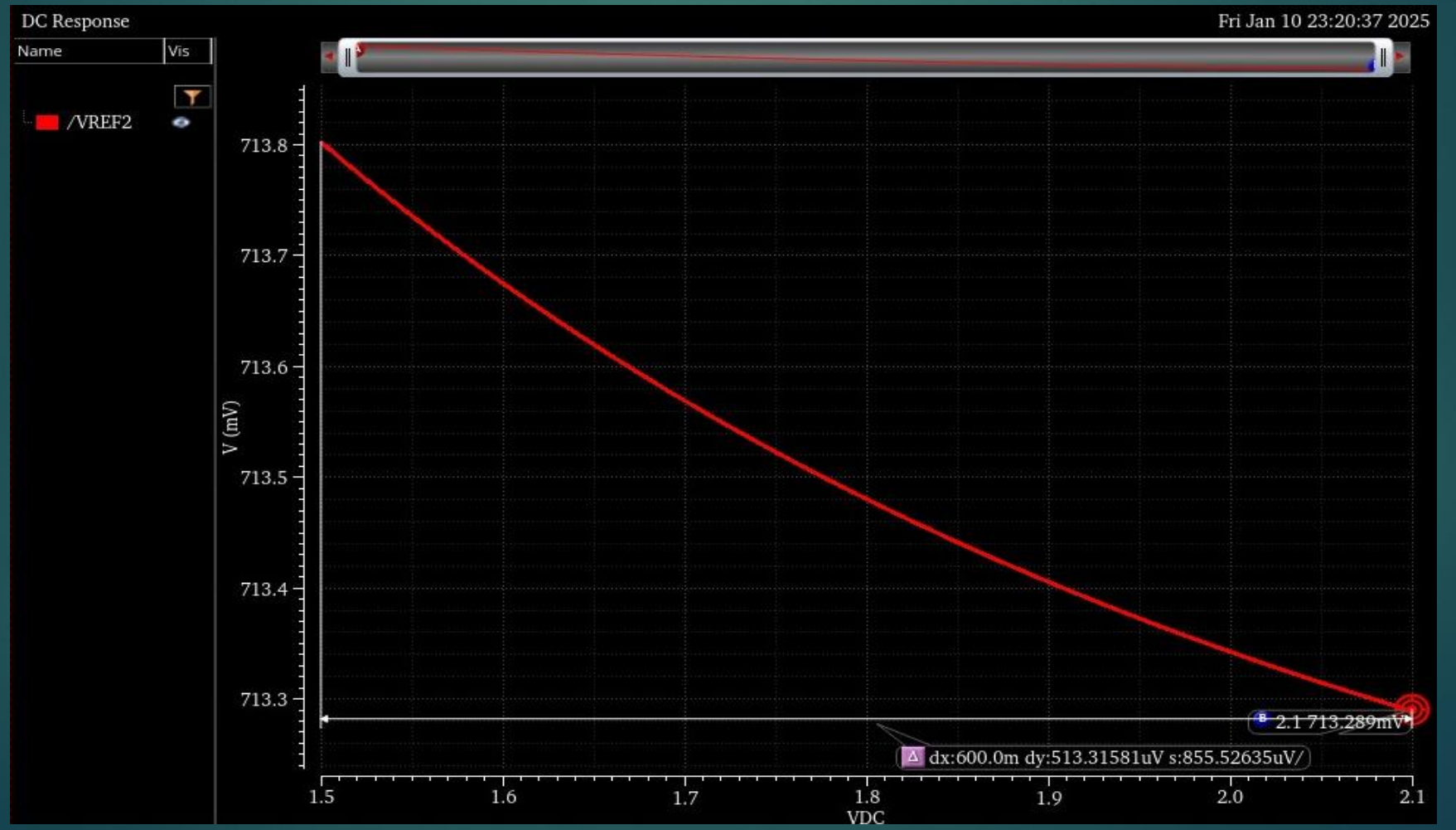
Increasing the OTA gain can improve the result, currently 69dB



V_{ref} across VDD variation

Max variation is 0.513mV, $PSRR = 20log10\left(\frac{\Delta V_{DD}}{\Delta V_{ref}}\right) = 61.3\text{dB}$

As expected, better current matching gave us better PSRR



BGR

Specification	Desired	Reached
PSRR [dB]	>40	61.3
Power (μW)	Minimize	58
Temperature Coefficient	<60 $\frac{ppm}{℃}$	7.6 $\frac{ppm}{℃}$

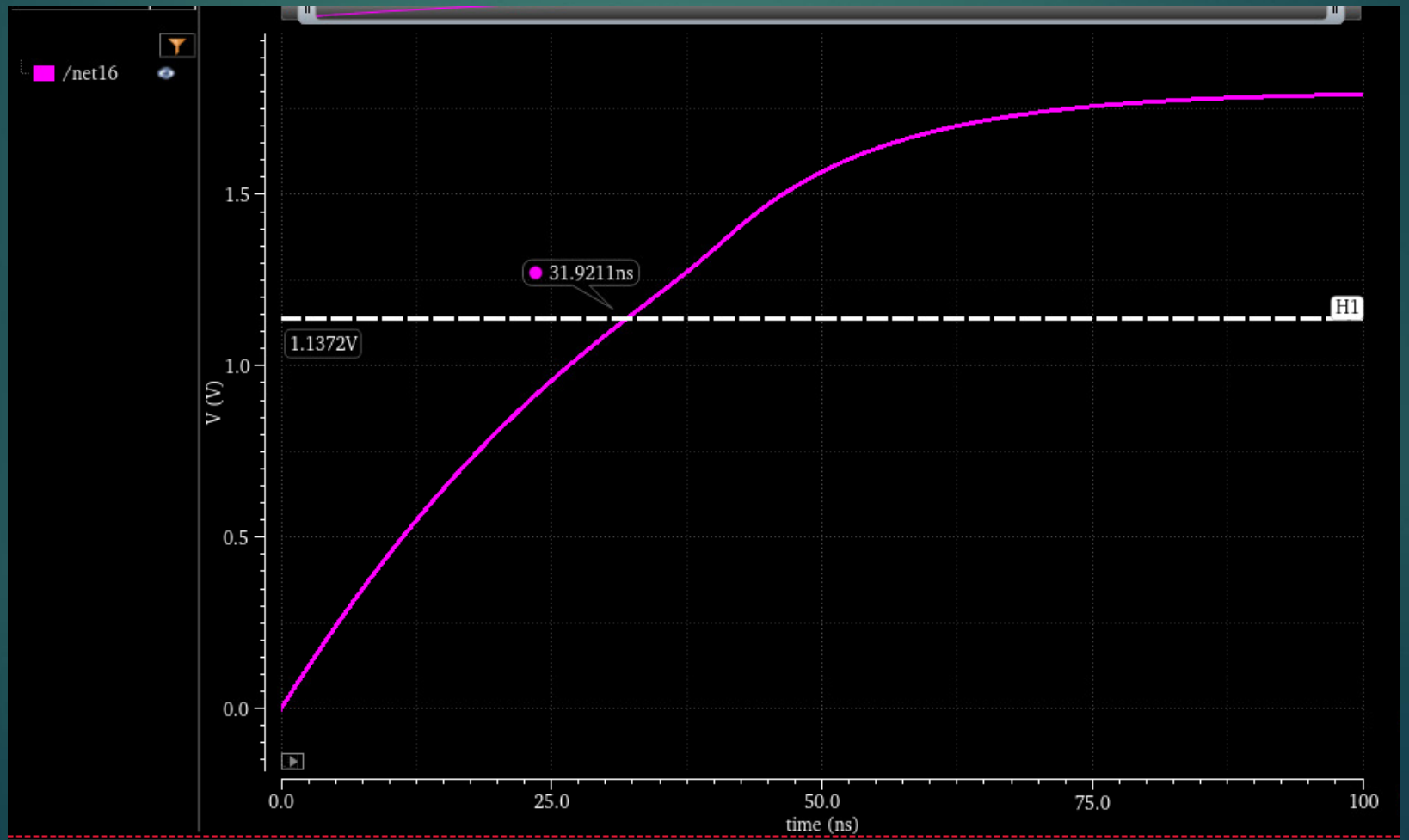
OTA – Design Specs

Specification	Intended	Reached
DC Gain (dB)	>60 (70 if possible)	69.8dB
GBW (MHz)	10-50MHz estimated for LDO	23MHz (tentative)
ICMR (-)	Minimize (Min. 0.62V)	0.67V
V_{out} Dynamic Range	Maximize	0.2V to 1.6V
Phase Margin (°)	60	72
Gain Margin (dB)	15-25	19.3
C_L (pF)	0.1	
C_C (pF)	<1	0.8 (tentative)
Power (μW)	Minimize	120

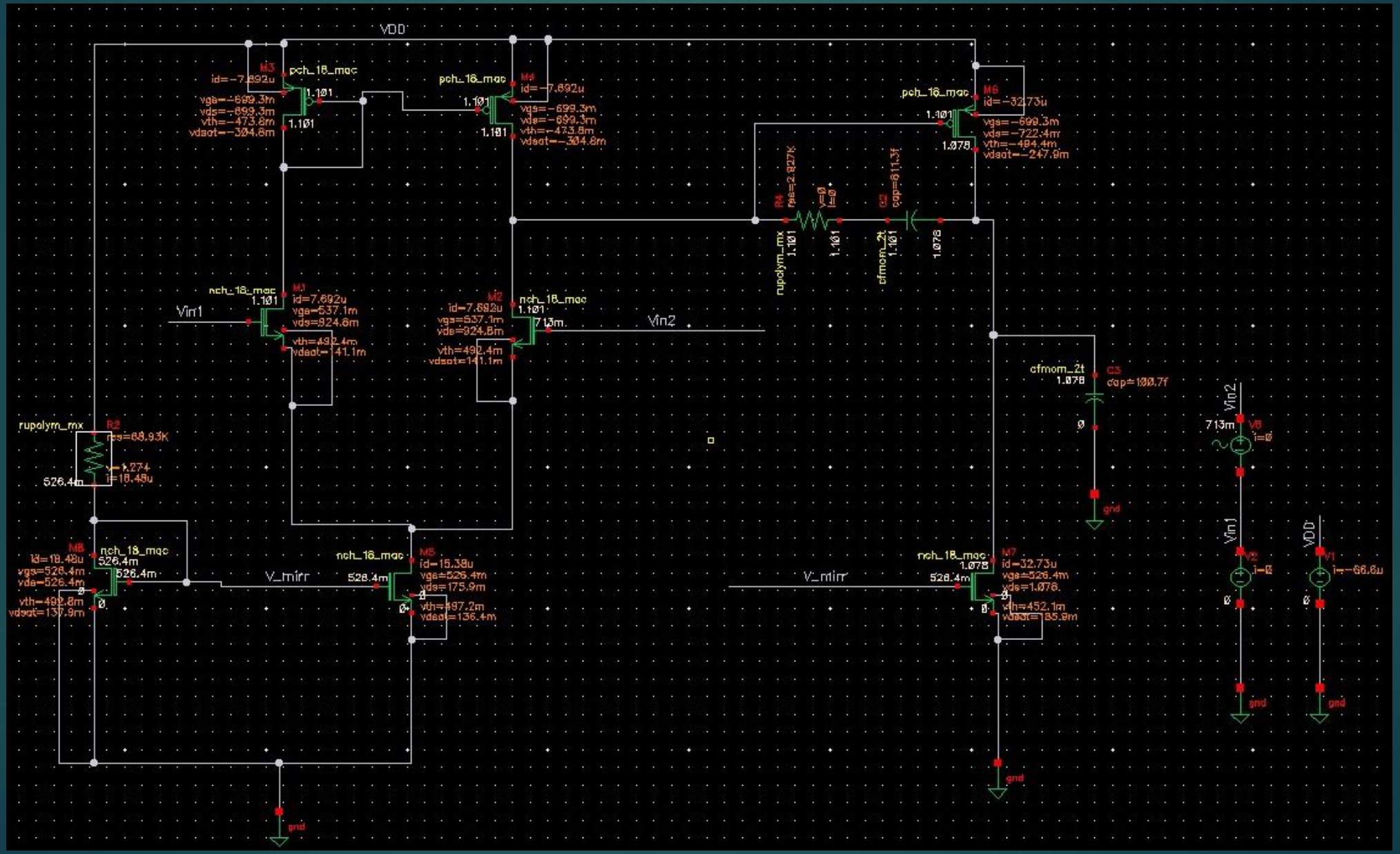
Why $C_L = 0.1pF$

A 0-1.8V pulse voltage source in series with a 500k resistor at the gate of a PMOS with W=60μ, L=150n (LDO pass transistor size)

$$At\ t = \tau = RC\colon\ V = 0.632V_{max} \rightarrow C = \frac{\tau}{R} = 64fF$$

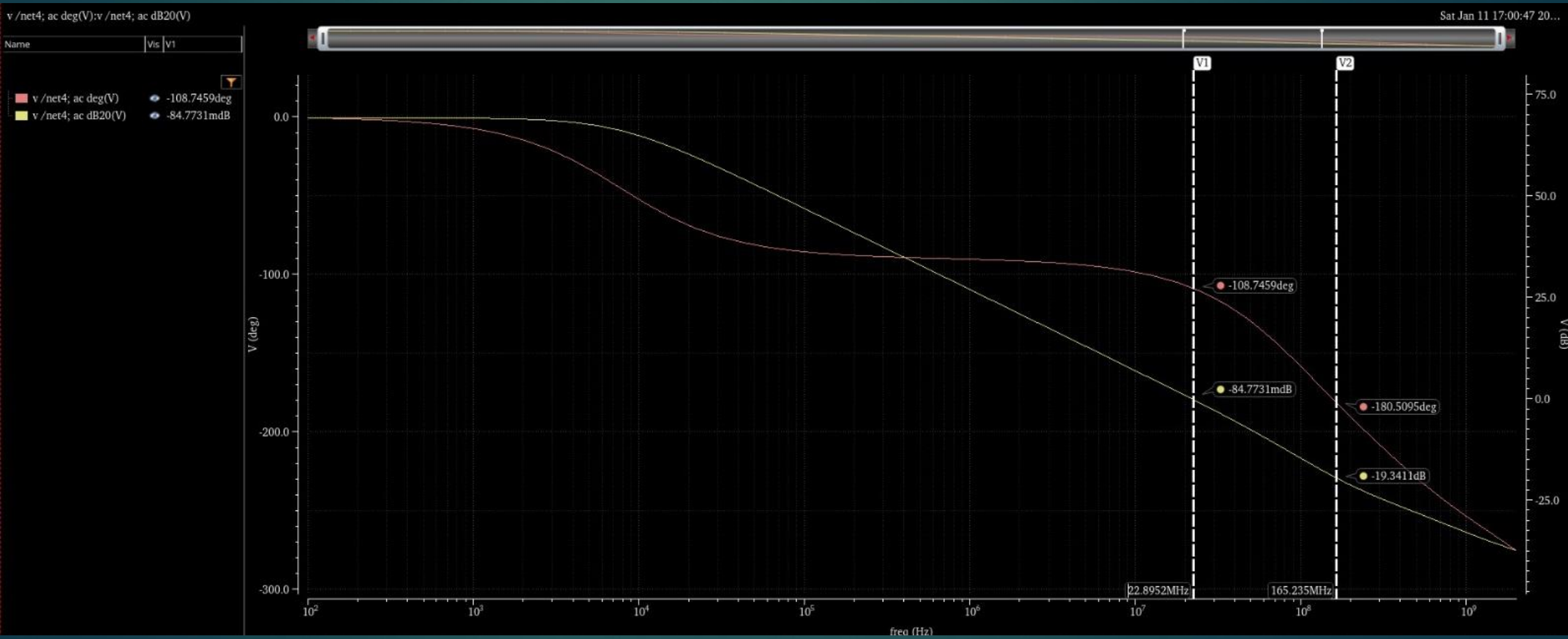


$DC\ Operation\ Point\ for\ V_{CM} = 0.713V$



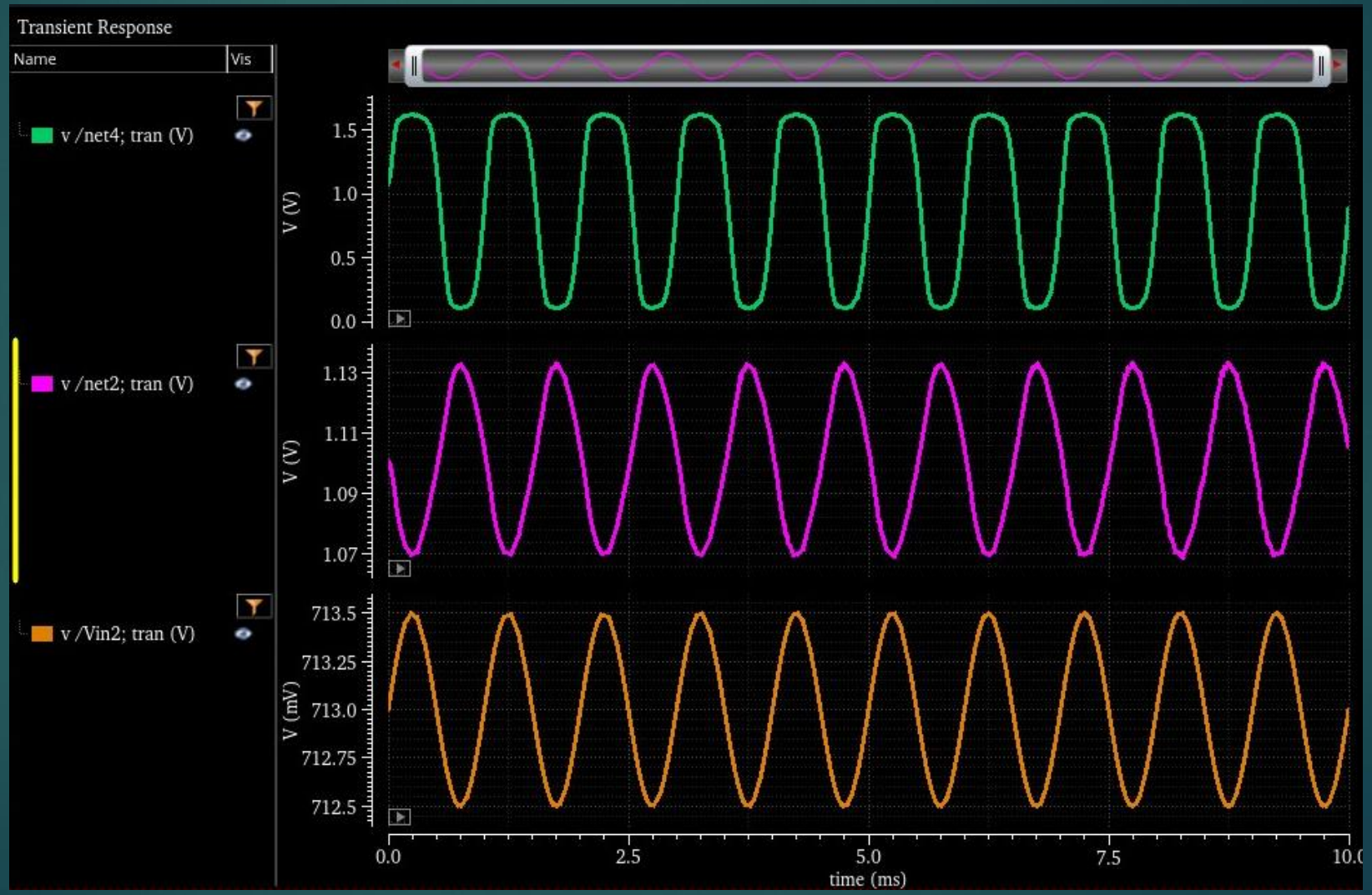
$AC\ Response\ For\ V_{CM} = 0.713V$

PM of 72 degrees
GM of 19.3dB



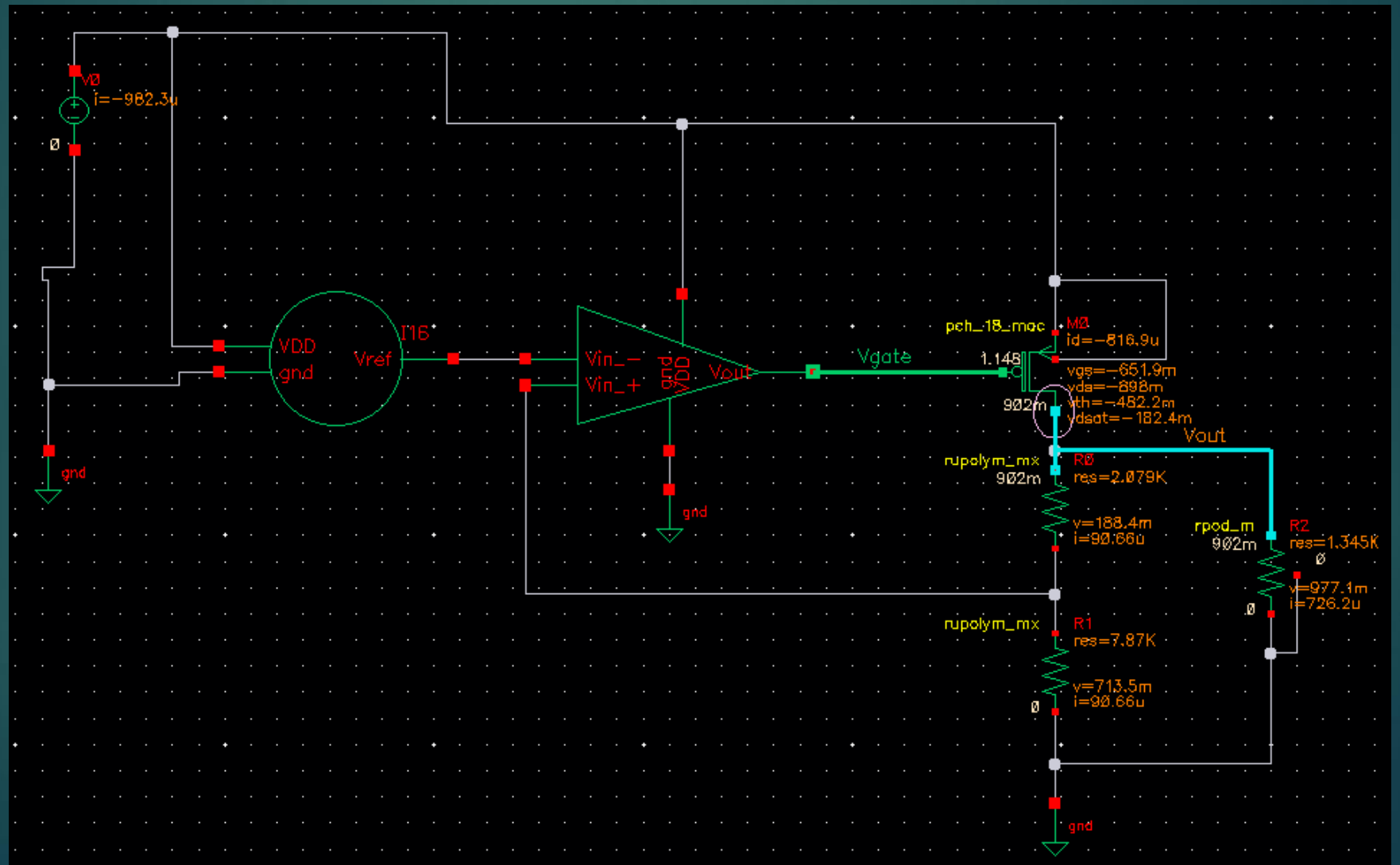
$Transient\ Response\ For\ V_{CM} = 0.713V$

AC input is a 500uV amplitude sin wave at a 1kHz to the non-inverting input

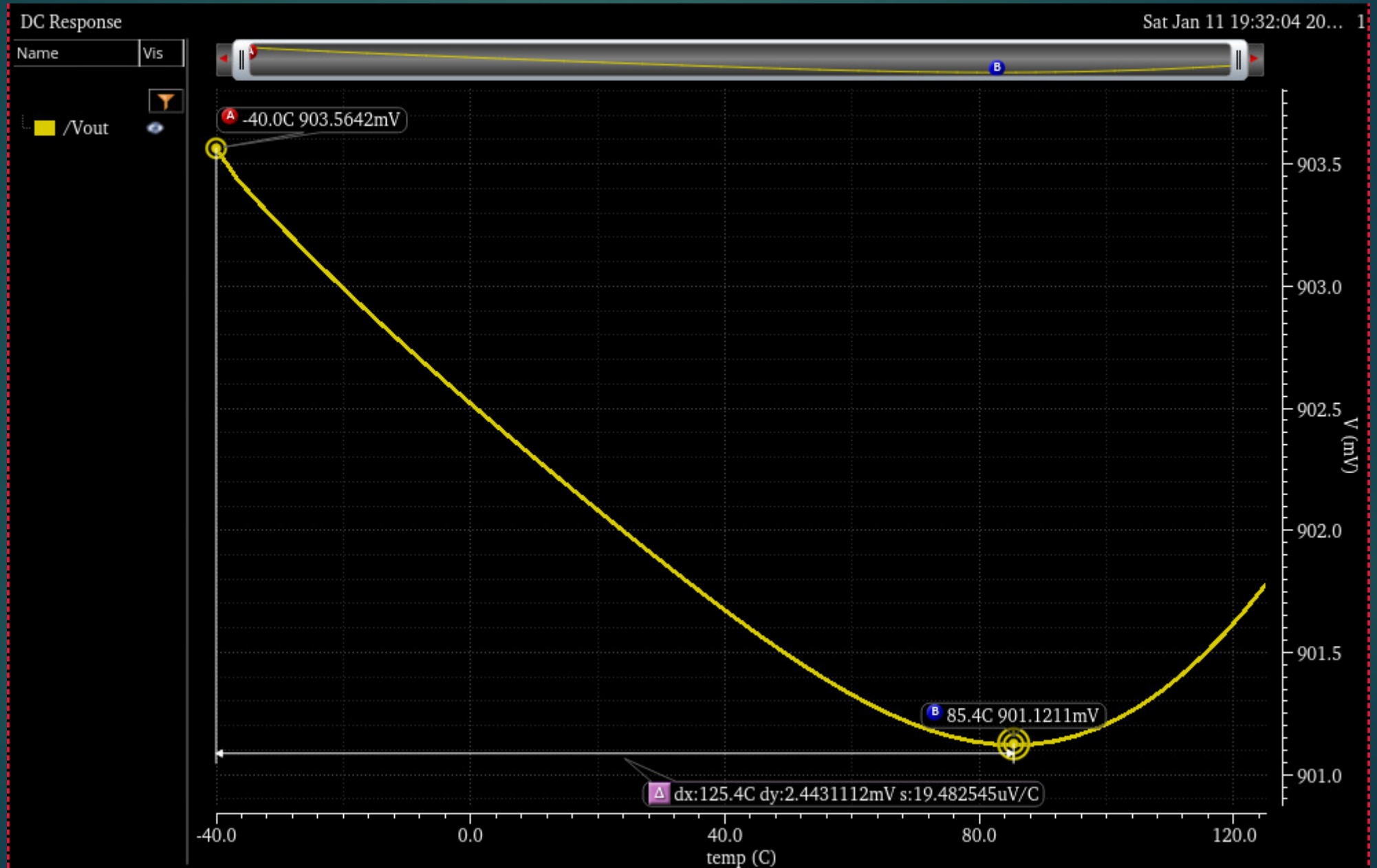


LDO

Initial design of LDO to check the suitability of the BGR and the OTA for the LDO



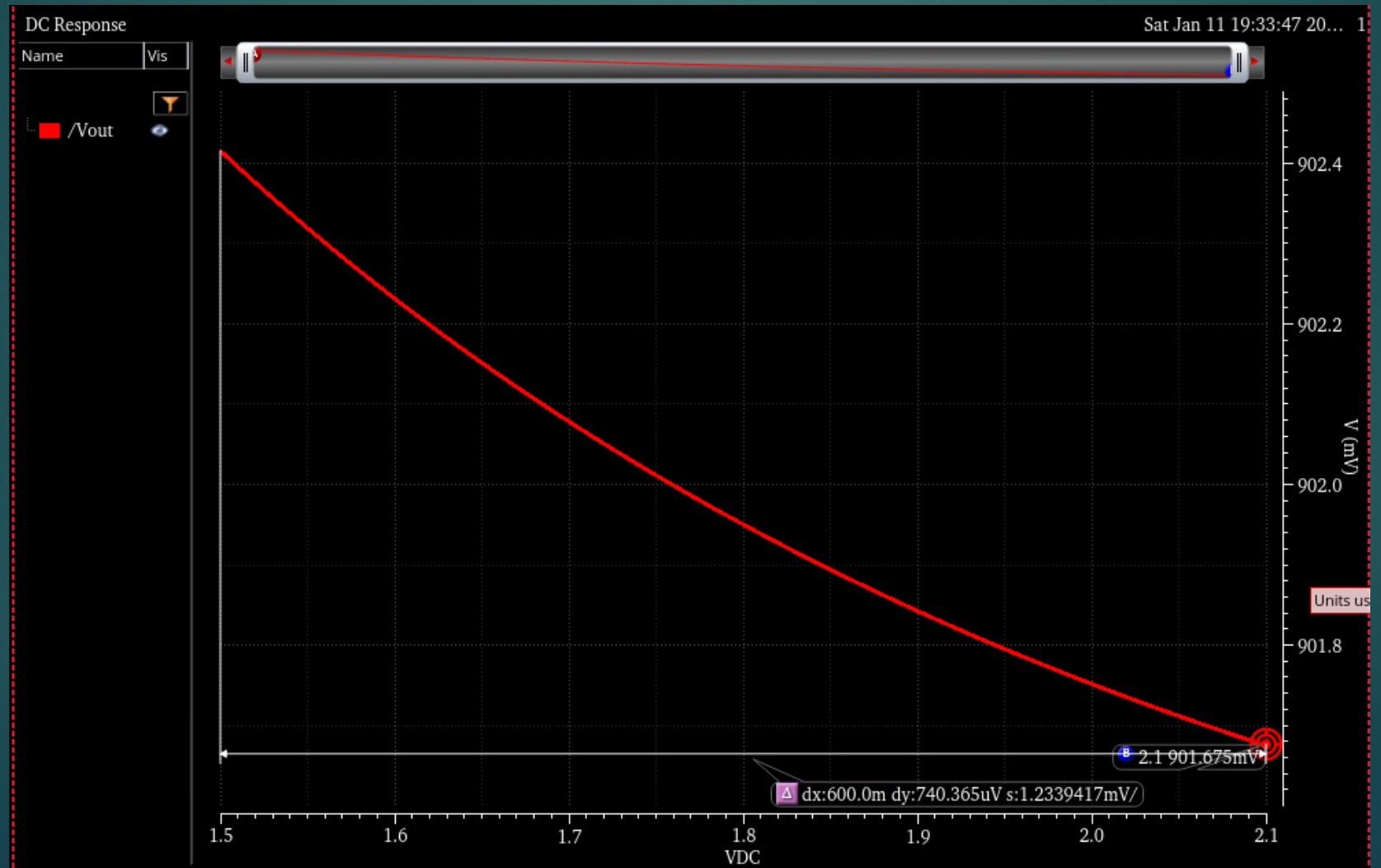
LDO - V_{out} across temperatures



LDO – Line Regulation

How stable V_{out} is despite changes in VDD:

$$\frac{\Delta V_{out}}{\Delta V_{DD}} = \frac{0.74}{600} = 0.00123 \frac{V}{V}$$



LDO – Load Regulation

How stable V_{out} is despite changes in the load current

$$\frac{\Delta V_{out}}{\Delta I_{load}} = \frac{0.429mV}{11.9mA} = 0.036\frac{mV}{mA}$$

The load resistance changed between 70 to 1200 Ohm