Homework 9

Problem 9.1

Solution:

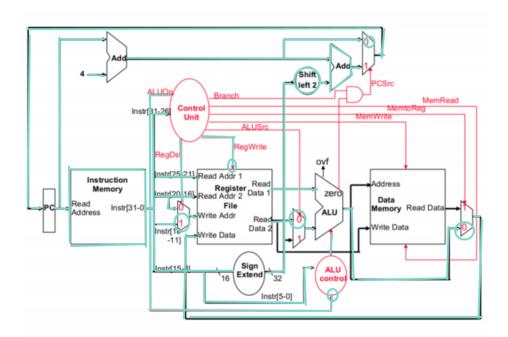
- a) Jump and Branch control signals feed the mutexes at the end of the single cycle data path and output of them goes to PC as input. By default the value would be incremented by 4. These are the only two needed scenarios, therefore the explicit write signal is pointless.
- b) For multi-cycle data path, we need to specify which path to pick in determining the address for next instructions.

https://stackoverflow.com/questions/40835418/why-an-explicit-single-cycle-datapath-i~:targetText=Therefore%20there%20is%20no%20need,address%20of%20the%20next%20instruction

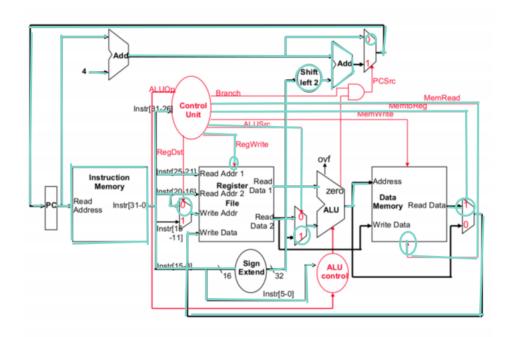
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Problem 9.2 Solution:



a)



Instruction	RegDst	ALUSrc	MemtoReg	Reg Write	Mem Read	Mem Write	Branch	ALUOp
add	1	0	0	1	0	0	1	0
lw	0	1	1	1	1	0	0	0

b) ALU adds when it recieves signal 0010.

That happens for LW and SW instructions. We add to calculate the addresses.

R-type instruction also require ALU to add, if we want to add two registers.