Arsh Singh

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OVERVIEW

Detail-oriented Electronics Engineer with expertise in VLSI design, programming, and cloud/AI technologies, eager to drive innovation by bridging hardware efficiency with intelligent software solutions.

KEY COMPETENCIES

Programming Languages: Python, C/Embedded C, Verilog,TCL

EDA tools: Cadence Virtuoso, Liberate, Mentor Graphics Calibre and other standard tools.

Automation/Build Tools: Makefile, Shell Script

Cloud Platforms: GCP (familiar)

Observability: GCP Monitoring, Prometheus, Cloud Logging

PROJECTS

STD Cell Library Design Intern (SAMSEMI) **Jun 2024 - Jul 2024**

- Designed and implemented a 25-cell standard cell library with logic gates and sequential elements, including transistor-level schematics and layouts ensuring LVS, DRC, and PEX compliance using Calibre.

Early Detection of DR **Oct 2022 - Feb 2025**

- Developed a deep learning model with EfficientNetB0, leveraging transfer learning and data augmentation for automated diabetic retinopathy detection.
- Optimized training using a custom learning rate scheduler and Adam optimizer, validated with K-fold cross-validation and confusion matrices.
- Achieved 94.63% accuracy, outperforming existing models like MobileNet (79%) and VGGNet (78.6%)

SIM Based Tracking using ESP8266 and SIM800L **Jan 2024 - Mar 2024**

- Developed a real-time tracking system with ESP8266/ESP32 and SIM800L GSM/GPRS, enabling remote location monitoring via cellular networks.
- Optimized low-power, battery-operated design with AT command configuration for reliable data transmission and performance across varying network conditions.

EDUCATION & CERTIFICATIONS

Bachelor of Technology, ECE
2022 - Present | **8.67 CGPA**
Jain University, Banglore

Intermediate
2022
Sunbeam Suncity, Varanasi

Google Arcade Legend 2025 (Cohort-I)
Cloud Profile

EXTRACURRICULAR ACTIVITIES

Vice-Organiser
Evalanche Club, Jain University

Red House Captain
School Council

PAPERS

Efficient CNN for DR
NCSEEE 2025
Best Paper Award

MEMBERSHIPS

2024-26
IETE Student Forum (ISF)

INTERNSHIPS

SAMSEMI **Jun 2024 - Jul 2024**
VLSI INTERN (STD CELL LIBRARY)
Helped with design and characterization of a standard cell library for a 45nm process node.
Analyzed delay, power, and area trade-offs for optimized performance.
Tools used: Cadence Virtuoso, Calibre, Liberate