Synthesis Report for 'lab_4'

General Information

Date: Fri May 7 14:27:43 2021
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: lab_4
Solution: solution1
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	8.495 ns	1.25 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
11	12	0.110 us	0.120 us	11	12	none

  - **Detail**
    - **Instance**

N/A

    - **Loop**

Loop Name	Latency (cycles)		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- AC	3	3	3	2	2	1	yes

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	4	0	359	-
FIFO	-	-	-	-	-
Instance	0	-	68	104	-
Memory	2	-	0	0	0

Multiplexer	-	-	-	231	-
Register	-	-	340	-	-
Total	2	4	408	694	0
Available	280	220	106400	53200	0
Utilization (%)	~0	1	~0	1	0

- **Detail**
  - **Instance**

Instance	Module	BRAM_18K	DSP48E	FF	LUT	URAM
lab_4_AXILiteS_s_axi_U	lab_4_AXILiteS_s_axi	0	0	68	104	0
Total	1	0	0	68	104	0

  - **DSP48E**

N/A

  - **Memory**

Memory	Module	BRAM_18K	FF	LUT	URAM	Words	Bits	Banks	W*Bits*Banks
shift_reg_V_U	lab_4_shift_reg_V	2	0	0	0	5	32	1	160
Total	1	2	0	0	0	5	32	1	160

  - **FIFO**

N/A

  - **Expression**

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
mul_ln1148_fu_243_p2	*	4	0	22	32	33
add_ln703_1_fu_224_p2	+	0	0	32	32	32
add_ln703_2_fu_230_p2	+	0	0	39	32	32
add_ln703_3_fu_234_p2	+	0	0	32	32	32
add_ln703_fu_212_p2	+	0	0	39	32	32
sub_ln1148_1_fu_295_p2	-	0	0	39	1	32
sub_ln1148_fu_266_p2	-	0	0	72	1	65
icmp_ln22_fu_201_p2	icmp	0	0	9	3	3
or_ln22_fu_195_p2	or	0	0	3	3	1
acc_V_fu_301_p3	select	0	0	32	1	32
select_ln1148_fu_288_p3	select	0	0	32	1	32
ap_enable_pp0	xor	0	0	2	1	2
ap_enable_reg_pp0_iter1	xor	0	0	2	2	1
xor_ln22_fu_218_p2	xor	0	0	4	3	4
Total	14	4	0	359	176	333

  - **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	53	12	1	12
ap_enable_reg_pp0_iter1	15	3	1	3

ap_phi_mux_i_1_0_phi_fu_153_p4	9	2	3	6
i_1_0_reg_149	9	2	3	6
in_data_TDATA_blk_n	9	2	1	2
out_data_TDATA_blk_n	9	2	1	2
p_Val2_0_reg_161	9	2	32	64
shift_reg_V_address0	38	7	3	21
shift_reg_V_address1	38	7	3	21
shift_reg_V_d0	15	3	32	96
shift_reg_V_d1	27	5	32	160
Total	231	47	112	393

- **Register**

Name	FF	LUT	Bits	Const Bits
acc_V_reg_371	32	0	32	0
add_ln703_reg_338	32	0	32	0
ap_CS_fsm	11	0	11	0
ap_enable_reg_pp0_iter0	1	0	1	0
ap_enable_reg_pp0_iter1	1	0	1	0
i_1_0_reg_149	3	0	3	0
icmp_ln22_reg_329	1	0	1	0
in_data_data_V_tmp_reg_308	32	0	32	0
in_data_last_V_tmp_reg_313	1	0	1	0
mul_ln1148_reg_355	64	0	65	1
p_Val2_0_reg_161	32	0	32	0
reg_172	32	0	32	0
reg_177	32	0	32	0
shift_reg_V_load_1_reg_318	32	0	32	0
tmp_4_reg_360	1	0	1	0
tmp_6_reg_366	30	0	30	0
xor_ln22_reg_345	3	0	3	0
Total	340	0	341	1

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_AXILiteS_AWVALID	in	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_AWREADY	out	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_AWADDR	in	5	s_axi	AXILiteS	scalar
s_axi_AXILiteS_WVALID	in	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_WREADY	out	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_WDATA	in	32	s_axi	AXILiteS	scalar
s_axi_AXILiteS_WSTRB	in	4	s_axi	AXILiteS	scalar
s_axi_AXILiteS_ARVALID	in	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_ARREADY	out	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_ARADDR	in	5	s_axi	AXILiteS	scalar
s_axi_AXILiteS_RVALID	out	1	s_axi	AXILiteS	scalar

s_axi_AXILiteS_RREADY	in	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_RDATA	out	32	s_axi	AXILiteS	scalar
s_axi_AXILiteS_RRESP	out	2	s_axi	AXILiteS	scalar
s_axi_AXILiteS_BVALID	out	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_BREADY	in	1	s_axi	AXILiteS	scalar
s_axi_AXILiteS_BRESP	out	2	s_axi	AXILiteS	scalar
ap_clk	in	1	ap_ctrl_none	lab_4	return value
ap_rst_n	in	1	ap_ctrl_none	lab_4	return value
control	in	1	ap_ctrl_none	lab_4	return value
ap_rst_n_control	in	1	ap_ctrl_none	lab_4	return value
in_data_TDATA	in	32	axis	in_data_data_V	pointer
in_data_TVALID	in	1	axis	in_data_last_V	pointer
in_data_TREADY	out	1	axis	in_data_last_V	pointer
in_data_TLAST	in	1	axis	in_data_last_V	pointer
out_data_TDATA	out	32	axis	out_data_data_V	pointer
out_data_TVALID	out	1	axis	out_data_last_V	pointer
out_data_TREADY	in	1	axis	out_data_last_V	pointer
out_data_TLAST	out	1	axis	out_data_last_V	pointer