Synthesis Report for 'lab_2'

General Information

Date: Thu May 6 09:47:09 2021
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: lab_2
Solution: solution1
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	8.670 ns	1.25 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
77	77	0.770 us	0.770 us	77	77	none

  - **Detail**
    - **Instance**

N/A

    - **Loop**

N/A

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	80	2301	-
FIFO	-	-	-	-	-
Instance	0	15	2551	2761	-

Memory	-	-	-	-	-
Multiplexer	-	-	-	349	-
Register	-	-	722	-	-
Total	0	15	3353	5411	0
Available	280	220	106400	53200	0
Utilization (%)	0	6	3	10	0

- **Detail**
  - **Instance**

Instance	Module	BRAM_18K	DSP48E	FF	LUT	URAM
lab_2_AXILiteS_s_axi_U	lab_2_AXILiteS_s_axi	0	0	182	296	0
lab_2_fadd_32ns_3bkb_U1	lab_2_fadd_32ns_3bkb	0	2	205	390	0
lab_2_flog_32ns_3eOg_U4	lab_2_flog_32ns_3eOg	0	13	485	614	0
lab_2_fpext_32ns_cud_U2	lab_2_fpext_32ns_cud	0	0	100	138	0
lab_2_fsqrt_32ns_dEe_U3	lab_2_fsqrt_32ns_dEe	0	0	405	615	0
lab_2_sdiv_48ns_3fYi_U5	lab_2_sdiv_48ns_3fYi	0	0	587	354	0
lab_2_sdiv_48ns_3fYi_U6	lab_2_sdiv_48ns_3fYi	0	0	587	354	0
Total	7	0	15	2551	2761	0

  - **DSP48E**

    N/A

  - **Memory**

    N/A

  - **FIFO**

    N/A

  - **Expression**

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln581_fu_790_p2	+	0	0	12	6	12
add_ln958_1_fu_611_p2	+	0	0	39	6	32
add_ln958_fu_399_p2	+	0	0	39	6	32
add_ln964_1_fu_676_p2	+	0	0	8	8	8
add_ln964_fu_575_p2	+	0	0	8	8	8
lsb_index_1_fu_454_p2	+	0	0	39	6	32
lsb_index_fu_255_p2	+	0	0	39	6	32
m_3_fu_426_p2	+	0	0	39	32	32
m_8_fu_638_p2	+	0	0	39	32	32
F2_fu_778_p2	-	0	0	12	11	12
man_V_1_fu_758_p2	-	0	0	61	1	54

sub_ln581_fu_796_p2	-	0	0	12	5	12
sub_ln944_1_fu_449_p2	-	0	0	39	6	32
sub_ln944_fu_250_p2	-	0	0	39	6	32
sub_ln947_1_fu_480_p2	-	0	0	15	4	6
sub_ln947_fu_281_p2	-	0	0	15	4	6
sub_ln958_1_fu_621_p2	-	0	0	39	5	32
sub_ln958_fu_409_p2	-	0	0	39	5	32
sub_ln964_1_fu_671_p2	-	0	0	8	5	8
sub_ln964_fu_570_p2	-	0	0	8	5	8
tmp_V_4_fu_366_p2	-	0	0	39	1	32
tmp_V_fu_217_p2	-	0	0	39	1	32
a_1_fu_507_p2	and	0	0	2	1	1
a_fu_308_p2	and	0	0	2	1	1
and_ln581_fu_900_p2	and	0	0	2	1	1
and_ln582_fu_885_p2	and	0	0	2	1	1
and_ln585_1_fu_917_p2	and	0	0	2	1	1
and_ln585_fu_911_p2	and	0	0	2	1	1
and_ln603_fu_934_p2	and	0	0	2	1	1
and_ln949_1_fu_534_p2	and	0	0	2	1	1
and_ln949_fu_335_p2	and	0	0	2	1	1
p_Result_5_fu_496_p2	and	0	0	32	32	32
p_Result_s_fu_297_p2	and	0	0	32	32	32
ashr_ln586_fu_847_p2	ashr	0	0	162	54	54
l_1_fu_387_p3	cttz	0	40	36	32	0
l_fu_238_p3	cttz	0	40	36	32	0
icmp_ln571_fu_772_p2	icmp	0	0	29	63	1
icmp_ln581_fu_784_p2	icmp	0	0	13	12	5
icmp_ln582_fu_810_p2	icmp	0	0	13	12	5
icmp_ln585_fu_833_p2	icmp	0	0	13	12	6
icmp_ln603_fu_838_p2	icmp	0	0	11	7	1
icmp_ln935_1_fu_361_p2	icmp	0	0	18	32	1
icmp_ln935_fu_212_p2	icmp	0	0	18	32	1
icmp_ln947_1_fu_302_p2	icmp	0	0	18	32	1
icmp_ln947_2_fu_470_p2	icmp	0	0	18	31	1
icmp_ln947_3_fu_501_p2	icmp	0	0	18	32	1
icmp_ln947_fu_271_p2	icmp	0	0	18	31	1
icmp_ln958_1_fu_554_p2	icmp	0	0	18	32	1
icmp_ln958_fu_355_p2	icmp	0	0	18	32	1
lshr_ln947_1_fu_490_p2	lshr	0	0	101	2	32
lshr_ln947_fu_291_p2	lshr	0	0	101	2	32
lshr_ln958_1_fu_616_p2	lshr	0	0	101	32	32
lshr_ln958_fu_404_p2	lshr	0	0	101	32	32
or_ln581_fu_923_p2	or	0	0	2	1	1
or_ln582_fu_890_p2	or	0	0	2	1	1

or_ln603_1_fu_961_p2	or	0	0	2	1	1
or_ln603_2_fu_975_p2	or	0	0	2	1	1
or_ln603_fu_948_p2	or	0	0	2	1	1
or_ln949_2_fu_341_p2	or	0	0	2	1	1
or_ln949_fu_540_p2	or	0	0	2	1	1
m_2_fu_419_p3	select	0	0	32	1	32
m_7_fu_631_p3	select	0	0	32	1	32
man_V_2_fu_764_p3	select	0	0	54	1	54
select_ln588_fu_867_p3	select	0	0	2	1	2
select_ln603_1_fu_954_p3	select	0	0	32	1	32
select_ln603_2_fu_967_p3	select	0	0	32	1	32
select_ln603_3_fu_981_p3	select	0	0	32	1	32
select_ln603_fu_940_p3	select	0	0	32	1	32
select_ln935_1_fu_705_p3	select	0	0	32	1	1
select_ln935_fu_604_p3	select	0	0	32	1	1
select_ln964_1_fu_664_p3	select	0	0	7	1	7
select_ln964_fu_563_p3	select	0	0	7	1	7
sh_amt_fu_802_p3	select	0	0	12	1	12
tmp_V_8_fu_222_p3	select	0	0	32	1	32
tmp_V_9_fu_371_p3	select	0	0	32	1	32
shl_ln604_fu_875_p2	shl	0	0	101	32	32
shl_ln958_1_fu_626_p2	shl	0	0	101	32	32
shl_ln958_fu_414_p2	shl	0	0	101	32	32
xor_ln571_fu_880_p2	xor	0	0	2	1	2
xor_ln581_fu_928_p2	xor	0	0	2	1	2
xor_ln582_fu_894_p2	xor	0	0	2	1	2
xor_ln585_fu_905_p2	xor	0	0	2	1	2
xor_ln949_1_fu_521_p2	xor	0	0	2	1	2
xor_ln949_fu_322_p2	xor	0	0	2	1	2
Total		84	0	80	2301	912	1254

- **Multiplexer**

Name	LUT	Input Size	Bits	Total Bits
ap_NS_fsm	349	79	1	79
Total	349	79	1	79

- **Register**

Name	FF	LUT	Bits	Const Bits
ap_CS_fsm	78	0	78	0
icmp_ln571_reg_1160	1	0	1	0
icmp_ln581_reg_1166	1	0	1	0
icmp_ln582_reg_1178	1	0	1	0
icmp_ln935_1_reg_1070	1	0	1	0
icmp_ln935_reg_1031	1	0	1	0
icmp_ln958_1_reg_1114	1	0	1	0

icmp_ln958_reg_1065	1	0	1	0
l_1_reg_1083	32	0	32	0
l_reg_1044	32	0	32	0
m_reg_1093	31	0	31	0
m_s_reg_1124	31	0	31	0
man_V_2_reg_1155	54	0	54	0
or_ln949_1_reg_1109	1	0	32	31
or_ln_reg_1060	1	0	32	31
p_Result_10_reg_1019	1	0	1	0
p_Result_13_reg_1025	1	0	1	0
select_ln603_3_reg_1195	32	0	32	0
select_ln935_1_reg_1134	32	0	32	0
select_ln935_reg_1119	32	0	32	0
sh_amt_reg_1172	12	0	12	0
sub_ln944_1_reg_1103	32	0	32	0
sub_ln944_reg_1054	32	0	32	0
tmp_11_reg_1190	7	0	7	0
tmp_2_reg_1098	1	0	1	0
tmp_9_reg_1129	1	0	1	0
tmp_V_6_reg_1005	32	0	32	0
tmp_V_7_reg_1012	32	0	32	0
tmp_V_8_reg_1036	32	0	32	0
tmp_V_9_reg_1075	32	0	32	0
tmp_i_i_reg_1139	32	0	32	0
tmp_i_reg_1144	32	0	32	0
trunc_ln583_reg_1184	32	0	32	0
trunc_ln943_1_reg_1088	8	0	8	0
trunc_ln943_reg_1049	8	0	8	0
v_assign_reg_1149	32	0	32	0
Total	722	0	784	62

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_AXILiteS_AWVALID	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_AWREADY	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_AWADDR	in	6	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WVALID	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WREADY	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WDATA	in	32	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WSTRB	in	4	s_axi	AXILiteS	pointer
s_axi_AXILiteS_ARVALID	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_ARREADY	out	1	s_axi	AXILiteS	pointer

s_axi_AXILiteS_ARADDR	in	6	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RVALID	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RREADY	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RDATA	out	32	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RRESP	out	2	s_axi	AXILiteS	pointer
s_axi_AXILiteS_BVALID	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_BREADY	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_BRESP	out	2	s_axi	AXILiteS	pointer
ap_clk	in	1	ap_ctrl_none	lab_2	return value
ap_rst_n	in	1	ap_ctrl_none	lab_2	return value