Lab 3

Design a custom IP in Vivado HLS to implement a 5-Point Moving Average Filter using the AXI Stream Interface.

```
def moving_average(x, y):
    for i in range(x):
    # add an if-else to avoid IndexError: list index out of
    # range, for the first 4 values
        y[i] = x[i] + x[i-1] + x[i-2] + x[i-3] + x[i-4]
        y[i] = y[i] / 5
```

The Moving Average Filter operates by averaging a number of points from the input signal to produce each point in the output signal.

Following are some of the possible equations for an M-point moving average filter.
Equation 1:

$$y[i] = \frac{1}{M}\Sigma_{j=0}^{M-1}x[i+j]$$

For example,

$$y[2] = \frac{x[2]+x[3]+x[4]+x[5]+x[6]}{5}$$

Equation 2:

$$y[i] = \frac{1}{M}\Sigma_{j=\frac{-(M-1)}{2}}^{\frac{M-1}{2}}x[i-j]$$

For example,

$$y[12] = \frac{x[10]+x[11]+x[12]+x[13]+x[14]}{5}$$

This equation (Equation 3) is more suitable for a moving average filter IP using the AXI Stream Interface. Because for both of these previous filter equations to work, we need to know the values of the future samples which is not directly possible with the AXI Stream Interface.

$$y[i] = \frac{1}{M}\Sigma_{j=-(M-1)}^{0}x[i-j]$$

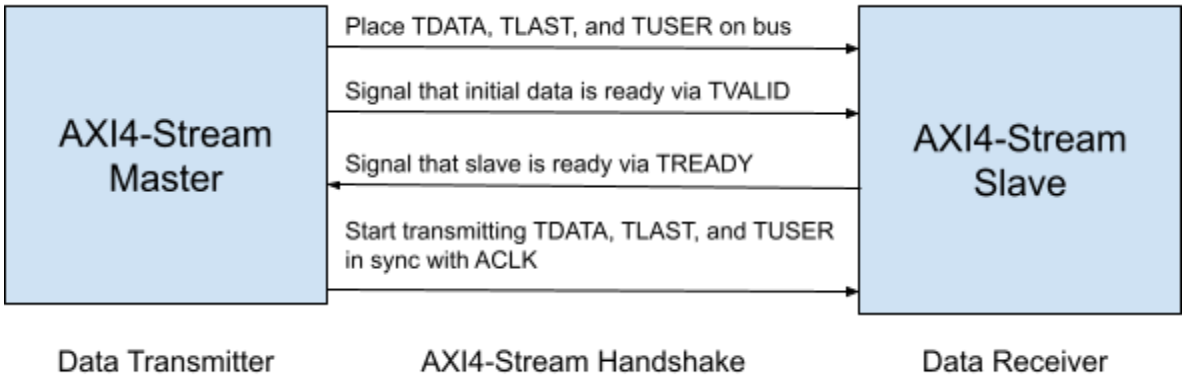
For example,

$$y[11] = \frac{x[7] + x[8] + x[9] + x[10] + x[11]}{5}$$

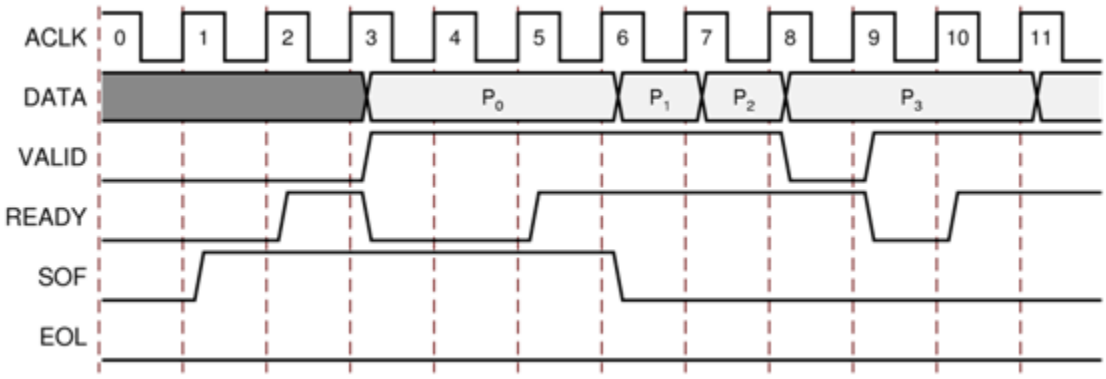
What is the AXI Stream Interface?

AXI4-Stream is one of many AMBA protocols designed to transport data streams of arbitrary width in hardware. Most usually 32-bit bus width is used, which means that 4 bytes get transferred during one cycle. At 100MHz of programmable logic frequency on FPGA-s this yields throughput of magnitude of hundreds of megabytes per second depending on memory management unit capabilities and configuration.

AXI4-Stream is a protocol designed to transport arbitrary unidirectional data streams. It uses a single AXI channel.



In AXI4-Stream TDATA width of bits is transferred per clock cycle. The transfer is started once the sender sends the signal TVALID and the receiver responds with TREADY. TLAST signals the last byte of the stream.



Example of READY/VALID Handshake, Start of a New Frame

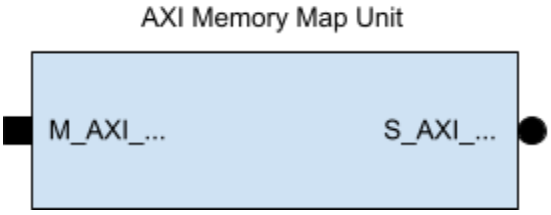
Since the AXI4-Stream does not have a write/read address channel, it cannot interact with the memory subsystem (eg. DRAM). Therefore, we need an AXI Data Mover Module to connect the stream interface to the memory map interface. The AXI DMA is an example of AXI Data Mover Module.

AXI DMA

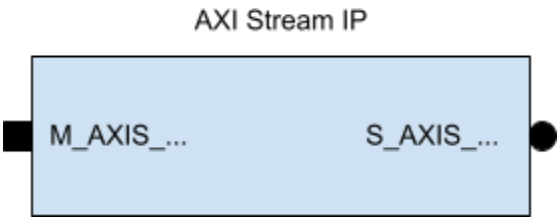
AXI DMA refers to traditional FPGA direct memory access which roughly corresponds to transferring arbitrary streams of bytes from FPGA to a slice of DDR memory and vice versa.

AXI DMA distinguishes two channels: MM2S (memory-mapped to stream) transports data from DDR memory to FPGA and S2MM (stream to memory-mapped) transports arbitrary data streams to DDR memory.

AXI Port Naming Style



In the port name, **M_AXI_…**
M denotes the MASTER
AXI is the name of the Interface
… is the actual name of the signal



In the port name, **M_AXIS_…**
M denotes the MASTER
AXIS is the name of the Interface
… is the actual name of the signal