Synthesis Report for 'lab_1'

General Information

Date: Thu May 6 09:08:34 2021
Version: 2019.2 (Build 2704478 on Wed Nov 06 22:10:23 MST 2019)
Project: lab_1
Solution: solution1
Product family: zynq
Target device: xc7z020-clg400-1

Performance Estimates

- **Timing**
  - **Summary**

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	6.371 ns	1.25 ns

- **Latency**
  - **Summary**

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
0	0	0 ns	0 ns	0	0	none

  - **Detail**
    - **Instance**

N/A

    - **Loop**

N/A

Utilization Estimates

- **Summary**

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	64	-
FIFO	-	-	-	-	-
Instance	0	-	182	296	-

Memory	-	-	-	-	-
Multiplexer	-	-	-	-	-
Register	-	-	-	-	-
Total	0	0	182	360	0
Available	280	220	106400	53200	0
Utilization (%)	0	0	~0	~0	0

- **Detail**
  - **Instance**

Instance	Module	BRAM_18K	DSP48E	FF	LUT	URAM
lab_1_AXILiteS_s_axi_U	lab_1_AXILiteS_s_axi	0	0	182	296	0
Total	1	0	0	182	296	0

  - **DSP48E**

N/A

  - **Memory**

N/A

  - **FIFO**

N/A

  - **Expression**

Variable Name	Operation	DSP48E	FF	LUT	Bitwidth P0	Bitwidth P1
add_ln68_fu_61_p2	+	0	0	32	32	32
Y_V	-	0	0	32	32	32
Total	2	0	0	64	64	64

  - **Multiplexer**

N/A

  - **Register**

N/A

Interface

- **Summary**

RTL Ports	Dir	Bits	Protocol	Source Object	C Type
s_axi_AXILiteS_AWVALID	in	1	s_axi	AXILiteS	pointer

s_axi_AXILiteS_AWREADY	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_AWADDR	in	6	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WVALID	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WREADY	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WDATA	in	32	s_axi	AXILiteS	pointer
s_axi_AXILiteS_WSTRB	in	4	s_axi	AXILiteS	pointer
s_axi_AXILiteS_ARVALID	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_ARREADY	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_ARADDR	in	6	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RVALID	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RREADY	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RDATA	out	32	s_axi	AXILiteS	pointer
s_axi_AXILiteS_RRESP	out	2	s_axi	AXILiteS	pointer
s_axi_AXILiteS_BVALID	out	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_BREADY	in	1	s_axi	AXILiteS	pointer
s_axi_AXILiteS_BRESP	out	2	s_axi	AXILiteS	pointer
ap_clk	in	1	ap_ctrl_none	lab_1	return value
ap_rst_n	in	1	ap_ctrl_none	lab_1	return value