

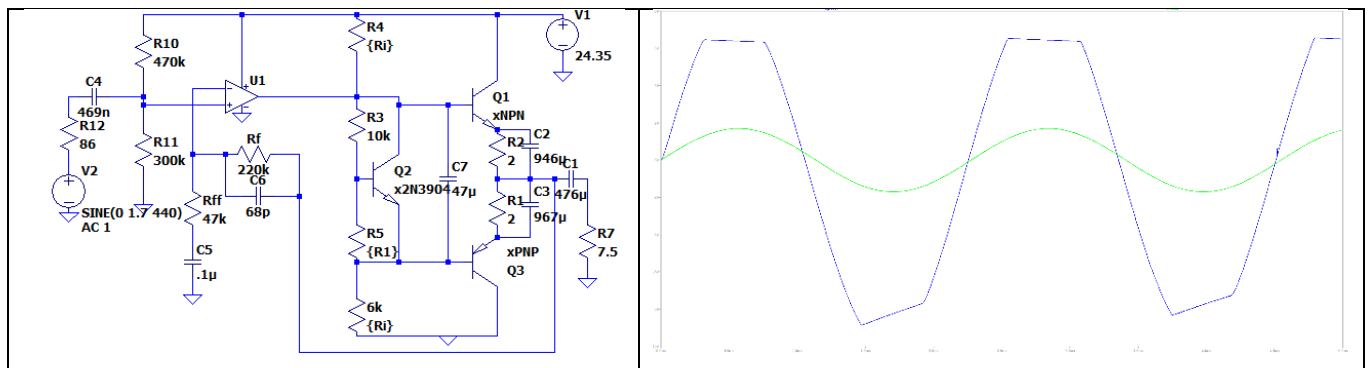
Artem Kulakevich – ECE521 Final Project – Audio Amplifier

1. What you needed to learn in order to start the [1]
2. design sketches and simulations
3. What you discovered that requires more work [3]
4. Preliminary results, which may include simulations, hardware, photographs

My original proposition was a complimentary symmetry amplifier driven by an NE5532 with TIP29/30 outputs. I thought it would be fun to see how much power output I could get with the a few power bricks and the dual transistors. Also this was the sort of project I could do with my “homelab”, which include a PC output audio jack, 2 12v power bricks, a 16\$ DMM, and a component value reader since I didn’t have much time to be at school this term. The original proposition would be that I would try to run as much DC current through the TIPs as I could, this was one of the first things I need to learn before I started. [1] That more DC current doesn’t mean I could get more power on the output.

I measured my TIP29/30s BJTs, and got about beta of 122 for the NPN, and 183 for the PNP, measured a 2N3904 with beta = 208, build the complimentary stage using those transistors, and some biasing for the resistors. I ended up building my circuit with nearly 600mA DC Q current, got hot transistors but very poor power output. At that point I started redesigning the whole thing, because I really wasn’t too happy about it [3]. The good news from this experiment was that my DC values where very close to my simulations, and I was happy with relying on my simulations for the future. I don’t have too much room for the DC values, but they were close to LTSpice, so I’m going to focus on my AC results.

At this point I decided to redesign something like what was on the website, and at this point I decided to solder the non-inverting op-amp (NE5532) gain stage all at once since I was confident in my simulation. This is what I consider my first major design:



I first started with a 4.7k value for R5, and then messed around with different values for R3 based on standards I already had on hand. I tried using a step simulation through R3 values and found that the benefit for using 10k or anything else around that change was pretty much negligible, the same stood true for R4. So I kept all of those at 10k for simplicity. The voltage divider circuit at the input of the op-amp

I had to adjust until my output was approximately centered. That meant the top resistor had to be large while the bottom one was much smaller. This I figure is likely because of the huge difference in beta between the NPN and the PNP. My measured values were a 4.55Vrms at 440Hz, some minor distortion was audible, but my DC values were close to my simulations.

At this point I was happy with my design but wanted a little more. I talked with Ignacio and he recommended using a Darlington Pair and/or putting more transistors in parallel. First, I tried adding 2 transistors in parallel, this design sounded like crap, and had much lower output power. (This might have been because of a mistake I made in my design, but I can't confirm that.)[3]

Next, I decided to try the Darlington pair configuration, by simply rotating those transistors around and resoldering them. This was essentially the same design as before, but with two more transistors hooked up in a Darlington pair. This time I got a worse output than before, but not too terrible. I had 3.7Vrms at 75Hz, but overall much better output at very low frequencies like 5hz. I also measured about 60mA Q-current at DC. I saw potential in this design, and decided to make another big adjusted, by replacing my 220k/47k feedback circuit with an adjustable potentiometer. I had a 10k pot and decided to place that in series with the feedback, and a 1k resistor to ground in series with the capacitor, that meant I had to readjust the capacitor for lower frequencies. I went with a 5uF cap, which would give a $1/(2*3.14*1k*5uF) = 31\text{Hz}$ LP cutoff, and as I write this I noticed that something like 10uF would give me much better low frequencies, but that will have to be used in future versions of the design [3]. With the addition of the pot, I could get my output to be higher, but it was incredibly distorted.

That's when I decided to modify my offset resistors for the op-amp, I believe that with the addition of the Darlington pair, the 470k/300k voltage drop was not necessary, so I retried my simulation with 300k/300k, and that was much better centered. I soldered in the 300k, and my design stopped working completely. The speaker would make loud popping sounds if I touched the circuit and produced noise. After almost an hour of troubleshooting I noticed that I somehow soldered my feedback wire to the wrong terminal while I was trying to clean things up, so I fixed that mistake and the speaker sounded better than ever before. The final design is here:

The image shows a breadboard circuit and its oscilloscope waveform. The breadboard contains a green PCB with various electronic components, including three black electrolytic capacitors labeled 'Toshiba 100µF 50V', several resistors, and integrated circuits. Wires connect the components to a power source. The oscilloscope displays a yellow sine wave. The top status bar shows 'Run' and 'Fig 9'. The top right corner displays three data points: 1) 2.99kHz, 7.40 V; 2) 3.29kHz, 6.00 V; 3) 3.57kHz, 13.4 V. The bottom left shows a table of statistics for the selected trace (1). The bottom right shows settings for 5.00 V, 1.00ms, and 800mV. The date and time '4 Dec 2010 18:10:10' are in the bottom right corner.

	Value	Mean	Min	Max	Std Dev
1 Frequency	439.3 Hz	533.5k	219.8	5.455M	1.029M
2 Max	22.9mV	19.5m	18.0m	26.6m	2.01m
3 Max	22.0mV	19.9m	18.0m	26.6m	2.01m
4 Peak-Peak	18.6 V	12.3	1.00	22.0	5.52

The left screenshot displays a green square wave on a black background. A cursor measurement window is open, showing the following data:

Cursor 1		Cursor 2	
Horz	10.424547ms	Horz	9.259557ms
Vert	-10.389179V	Vert	9.8496921V
Diff (Cursor2 - Cursor1)		Slope	
Horz	-1.1649899ms	Vert	20.238872V
Freq	858.37651kHz	Slope	-17372.6

The right screenshot displays a yellow square wave on a black background. A measurement table is visible, showing the following data:

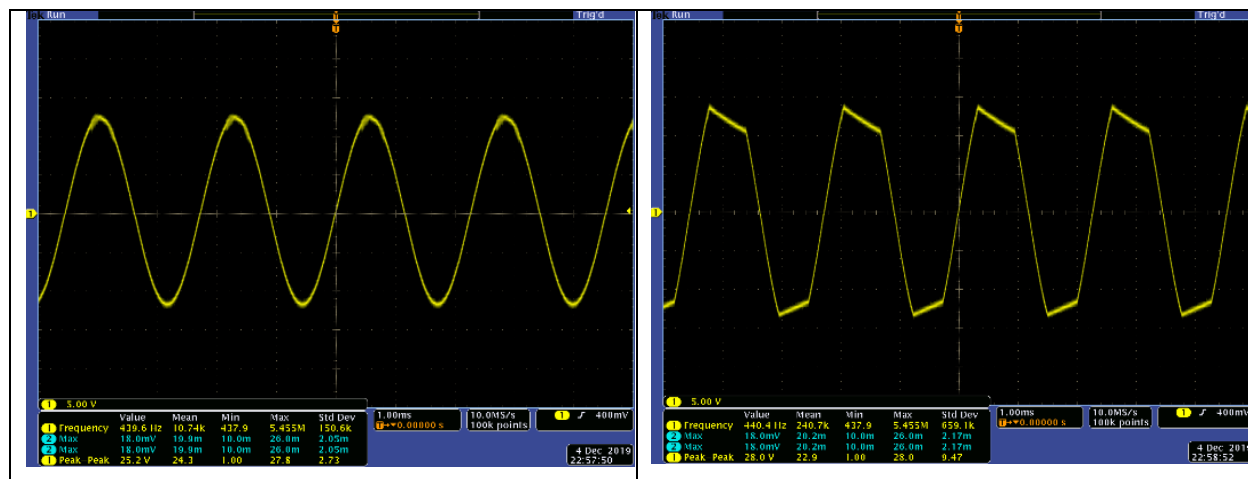
	Value	Mean	Min	Max	Std Dev
1 Frequency	489.7 Hz	1.012M	219.3	5.455M	1.140M
2 Max	22.0mV	20.3m	15.0m	26.0m	1.99m
3 Max	22.0mV	20.3m	15.0m	26.0m	1.99m
4 Peak-Peak	21.8 V	7.14	1.00	22.0	0.06

Additional statistics are shown on the right side of the screen:

- 1 2.98kHz 10.6 V
- 2 3.29kHz 8.66 V
- 3 1.57kHz 18.6 V

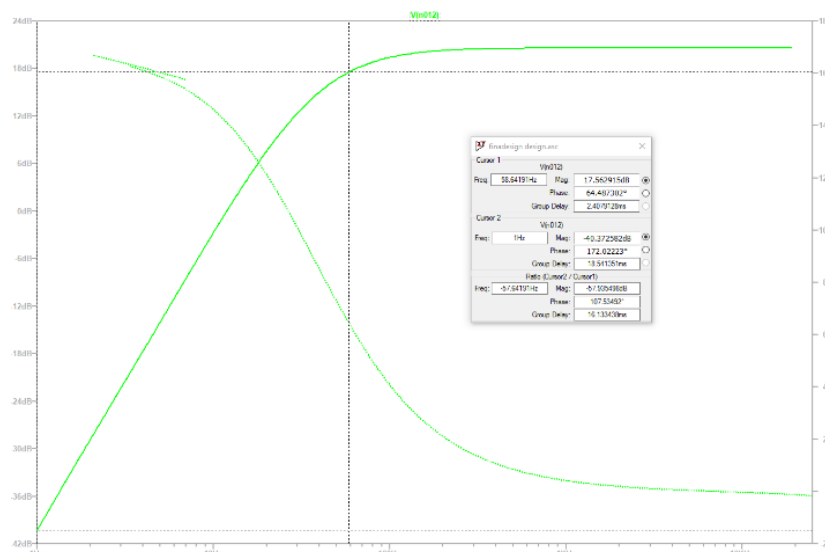
The bottom status bar shows the date and time: 4 Dec 2010 15:05:53.

With around 10.5Vpk on both about outputs. Finally, I wanted to see the limit of this system, so I upped the supply voltage to the max supply voltage of 31.9V, and made some more measurements:



The left is the maximum output I could reach before I got distortion with a 12.6Vpk output, at about 7.94W, and the right image is the has an output of 28.0Vpk which would result in ~9.8W output, which is the rated limit of my resistor. I know the pot had a bit more room for more output, but I was getting nervous because the resistor was getting hot. My simulated and my measured AC output values were within about 1 V of each other.

Simulating the frequency response gave me a ~60Hz LP cutoff frequency with about 20.5dB gain using the 10k/1k resistors for gain, which essentially means the op-amp is doing its job:



I test about 4-5 different integrations of my design for this project, so there is even more room for improvements in the future. The project has motivated me to try and build a full functional amplifier that I could use at home. The first step would be to build a better homelab though...