ECE 527

Getting started guide for DC (Design compiler) and PT (Prime Time)

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1. Synopsys Design Compiler:

The Design Compiler tool is the core of the Synopsys synthesis products. Design Compiler optimizes designs to provide the smallest and fastest logical representation of a given function. It comprises tools that synthesize our HDL designs into optimized technology-dependent, gate-level designs.

Design Compiler and Design Flow:

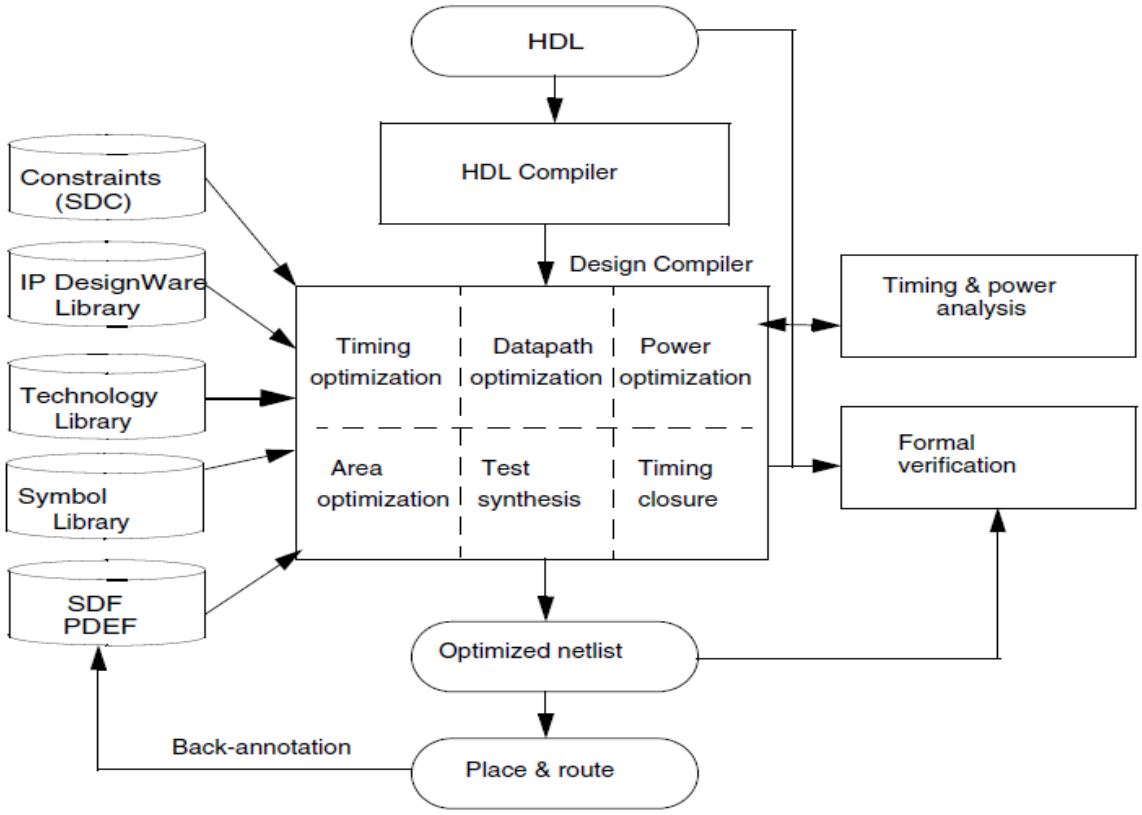

Fig: 1.2 [DC design flow, Synopsys DC user guide]

1. The input to DC is a description of the design using HDLs like SystemVerilog, VHDL etc.

2. DC translates HDL description to components extracted from the technology library (there are various libraries that DC uses along with HDL file to generate and display synthesis results)

3. After translating the HDL description to gates, Design Compiler optimizes and maps the design to a specific technology library, known as the target library.

4. After the design synthesis it is optimized and the design is ready for Place and Route

2. Libraries used by DC:

Synopsys uses the following libraries:

(Refer DC user guide to learn to specify these libraries in your design)

- Technology libraries
- Design ware libraries
- Symbol libraries

Technology libraries:

Technology libraries contain information about the characteristics and functions of each cell provided in a semiconductor vendor's library. It also contains information about Design Rule Constraints, also, it contains operating conditions and wire load models.

Various technology libraries are –

1. Target Library: Design Compiler uses the target library to build a circuit

2. Link Library: Design Compiler uses the link library to resolve references. For a design to be complete, it must connect to all the library components and designs it references. This process is called linking the design or resolving references. DC uses these libraries, in .db format, for following purpose:

- Implementing the design functions (technology libraries used for this are called Target library)
- Resolving Cell references (technology libraries used for this are called Link library)
- Calculating Timing values and Power consumed

Symbol libraries:

Symbol libraries contain definitions of the graphic symbols that represent library cells in the design schematics. Design Compiler uses symbol libraries to generate the design schematic. When you generate the design schematic, Design Compiler performs a one-to-one mapping of cells in the netlist to cells in the symbol library

Design Ware libraries:

A Design Ware library is a collection of reusable circuit-design building blocks (components) that are tightly integrated into the Synopsys synthesis environment.

3. Setting up DC

Step1 - Log on to VLSI Lab's computer. Open terminal: Right click to open a terminal

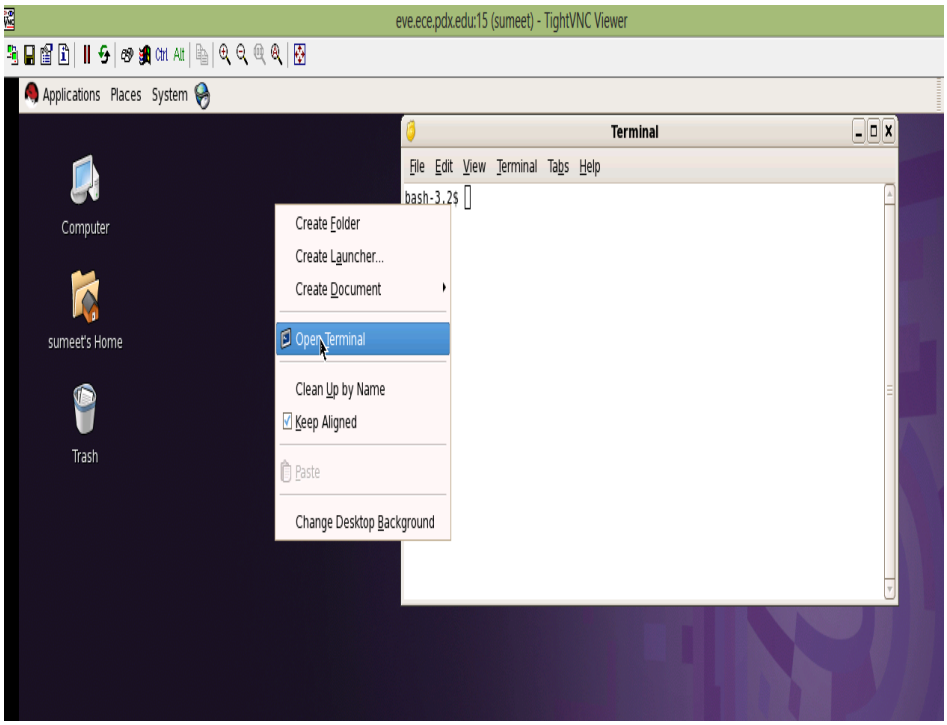

Fig 1.3

Step1.1 - Type "addpkg" (This is a onetime thing….) a blue window, full of tools available, will pop up. Select Synopsys DC and press ok

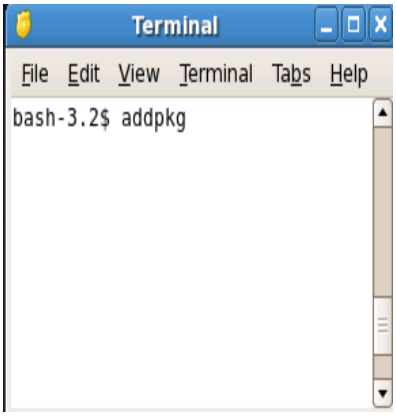

Fig 1.4

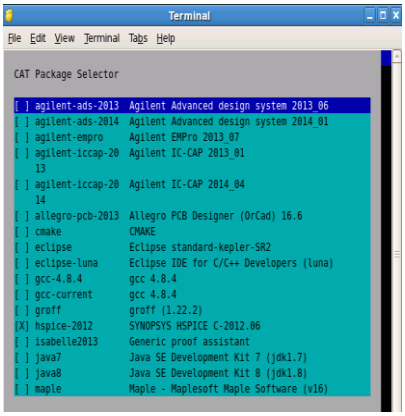

Fig 1.5

Step2 - Invoke Design compiler by typing "**dc_shell**" (Invoke dc from address space where all files are located)[Design Vision is the Graphical version of DC]

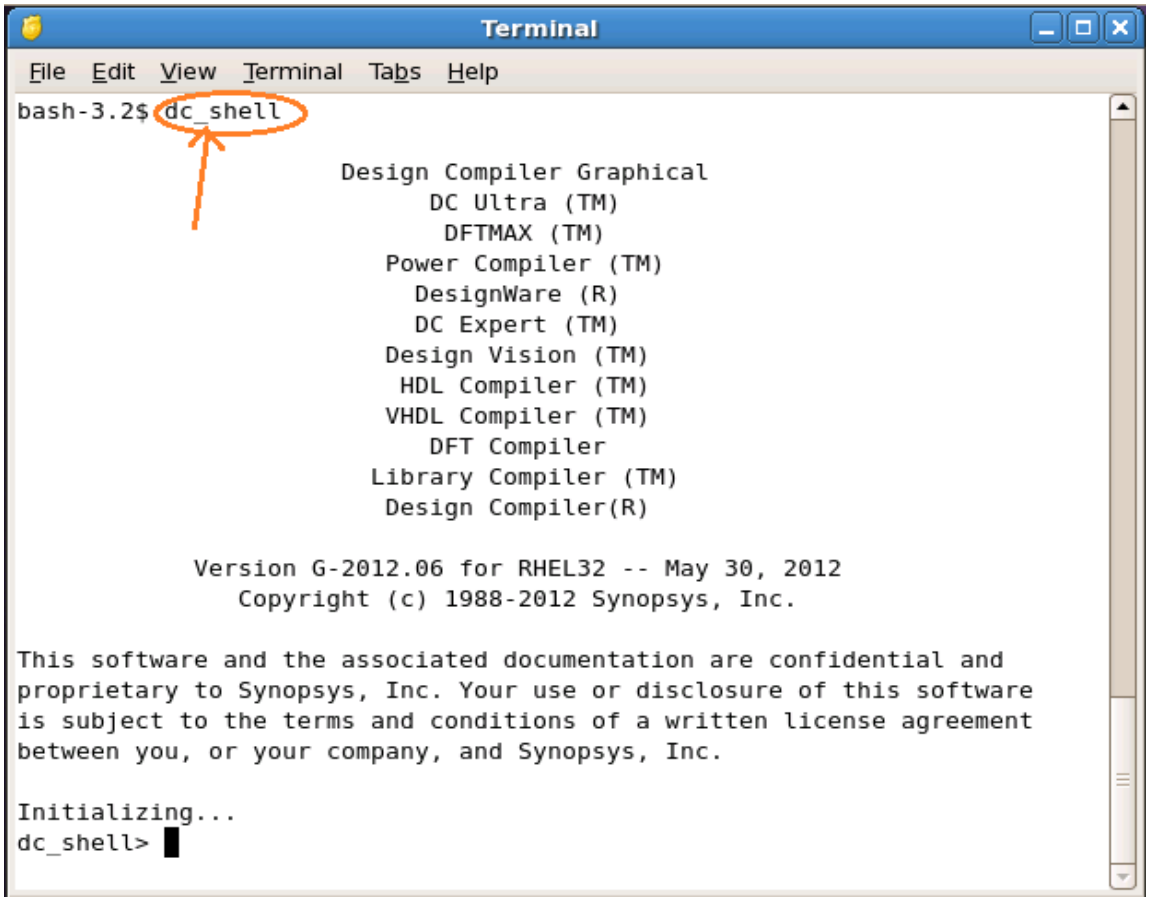

Fig 1.6

After this we can invoke script files with command *source* to run all the commands at once or type every command individually which help you to understand what the meaning of each command is.

4. Using DC for synthesis of the design:

The following steps were followed to synthesize the design to a gate-level netlist

1. Develop the HDL files – In this stage, we generate the HDL code for the FIFO.

2. Specifying the libraries – In this stage, we specify target, link, symbol library etc.

3. Read the design – The FIFO design, verified by simulation, is fed to DC

4. Define design environment – Various design environment constraints are set in this stage Ex- setting operating-conditions, setting wireload-model, setting drive, set driving-cell, setting load, setting fanout-load

5. Set design constraints – This stage has two different constraints to be set up.
1. Design rule constraints like max capacitance, max fan-out are set in this stage
2. Design Optimization constraints like – creating clock, setting clock-latency, and clock –transition time, setting clock-uncertainty, setting input and output delay

6. Selecting compiling strategy – Either top down or bottom up (usually important for large designs)

7. Optimizing the design- At this stage, we have all the input files and library available for tool. All we need to do is compile the design

8. Analyzing and resolving the design- Once the design is compiled without any error, we generate various reports like timing report, area report, check-design etc.

9. Saving the design in required format – The final output file, synthesized netlist, is written in appropriate format

6. Example Design Dual Port FIFO:

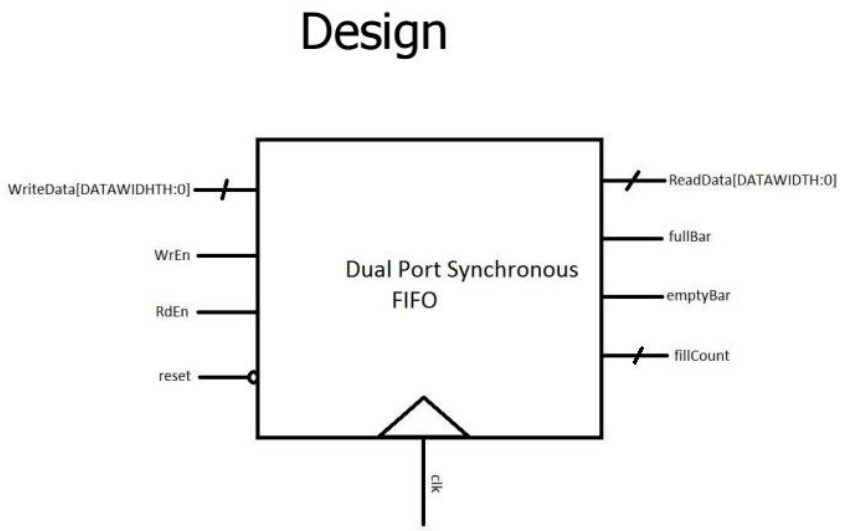

Fig: 1.1 FIFO design

Description:

•**WriteData [DATAWIDTH: 0]**: - Writes data on FIFO

•**Write Enable (WrEn)**: - Active high signal, allows data to be written in FIFO memory

•**Read Enable (RdEn)**: - Allows data to be read from FIFO memory on ReadDatabus

•**ReadData [DATAWIDTH: 0]**: - Data from FIFO memory read on this bus

•**fullBar**: - Active high signal, shows that FIFO is full

•**emptyBar**: - Active high signal, shows FIFO is empty

•**fillCount**: - Counter, shows how much FIFO is filled

•Consist of write and read pointers

•fillCount = WPtr –RPtr

•Producer is only allowed to write when FIFO is not Full.

We provide the design and the tcl script to synthesis it, for more synthesis options please refer to the DC user manual.

Synopsys Primetime

1. Introduction to Synopsys Primetime: [1] PrimeTime is the Synopsys stand-alone, full-chip, gate-level static timing analyzer. PrimeTime performs timing analysis at the gate level and provides a comprehensive set of modeling technologies for representing non-synthesized blocks for analysis

Useful timing checks by Primetime

- Setup and hold requirements of sequential devices and gated clocks
- Minimum period and minimum pulse width for clock signals
- User defined minimum and maximum delay constraints
- Required input and output delays
- Clock Skew

[Please refer to the Primetime User guide for checking all the functions provided by primetime]

2. Primetime User design flow:

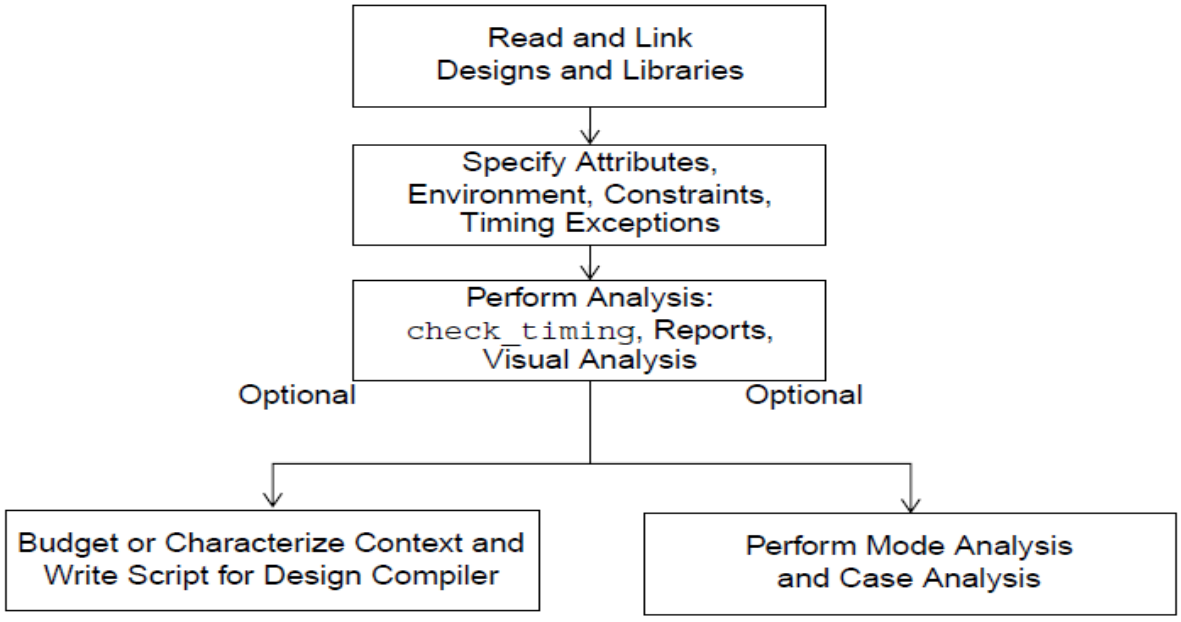

Fig 1 User design flow [primetime user guide]

1. Read and link the designs and libraries. Set the search path and the link path, then run read_db and link_design.

2. Specify the attributes, environment, constraints, and timing exceptions, including wire load models or annotated delays or parasitics; port drive and capacitance; clocks; latches; uncertainty; input and output delay; and false and multicycle paths.

3. Perform analysis.

4. Optionally, budget the design or characterize the context and write a script for Design Compiler, and perform mode analysis and case analysis.

3. Setting up Primetime:

Step1 –Open terminal: Right click to open a terminal

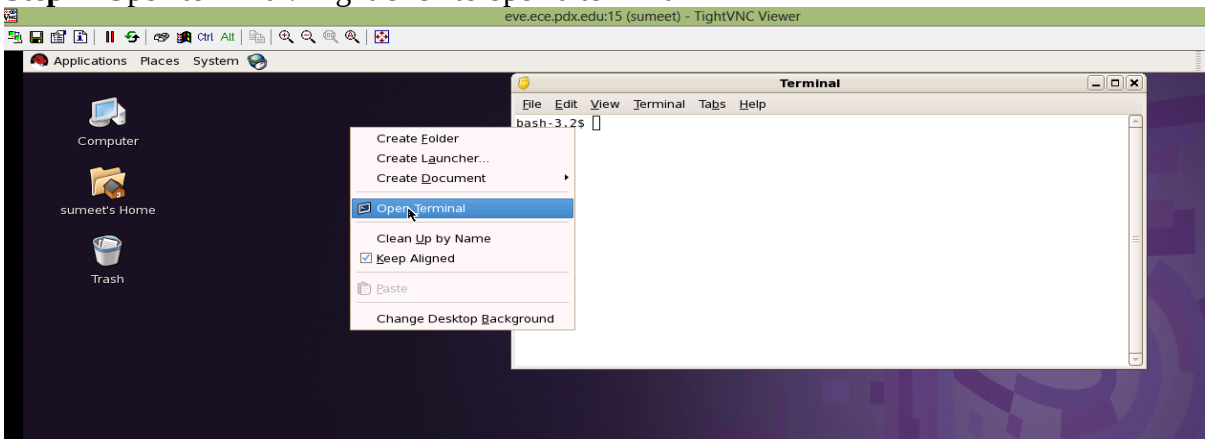

Fig 2

Step1.1 - Type "addpkg" (This is a onetime thing….) a blue window, full of tools available, will pop up. Select Synopsys Primetime and press ok

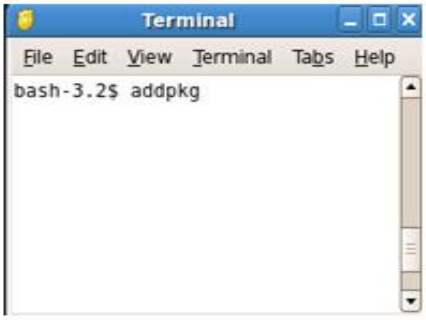

Fig 3

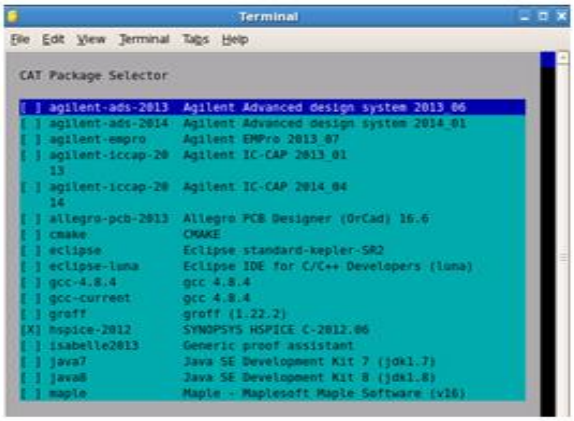

Fig 4

Step2 - Invoke Design compiler by typing "**pt_shell**" (Invoke primetime from address space where all files are located) [To start primetime in GUI type start_gui after you invoke primetime]

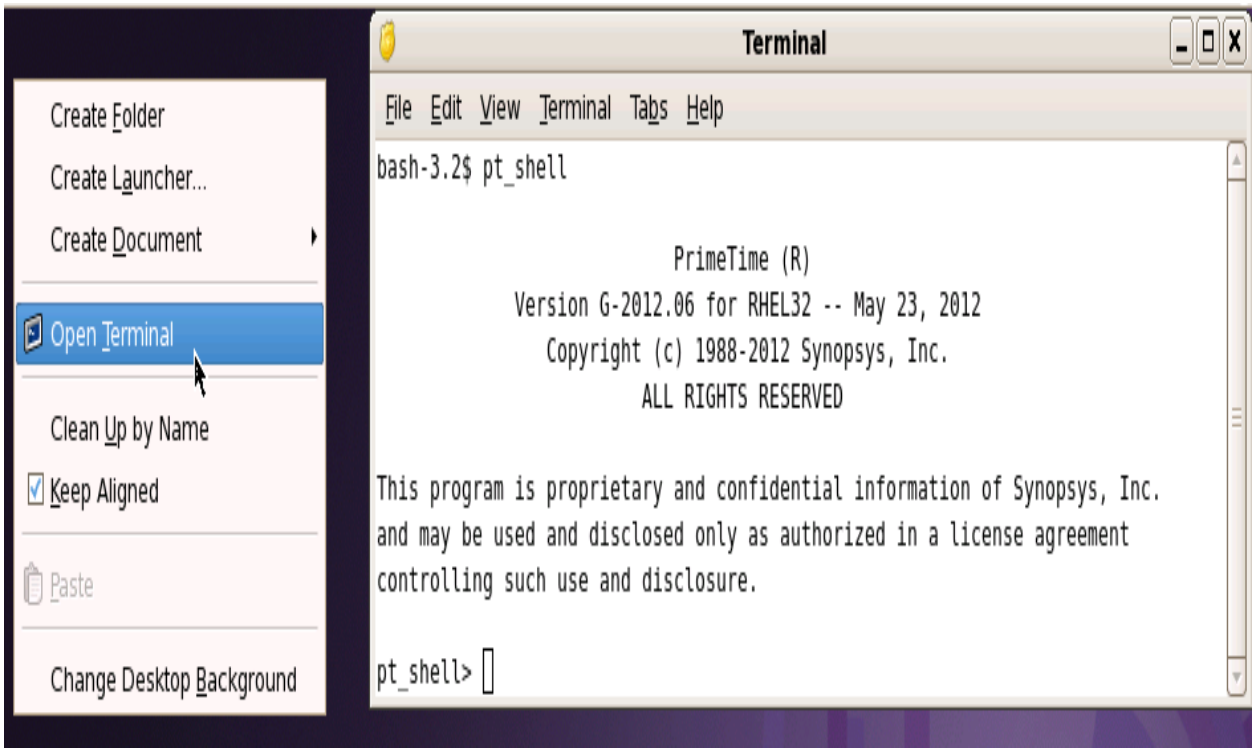

Fig 5

4. Using Primetime for Static timing analysis:

1. Set the link path to specify where PrimeTime searches for designs and library cells when linking the design

2. Read the technology library .db format file into memory

3. Read the design .db format files into memory

4. Link the design to resolve all references in the design

5. Set timing constraints

6. Display the timing reports (set up and hold time etc.)

For the actual commands we used, check the PT script.

7. Script File (source this file after reading the design and libraries)

1. Change the search path to your own path
2. Put the gscl45nm.db in wherever you ran PT or you can modify the link library to the full path.

```
#!/bin/bash

#*************************************************/
#* 16th Aug 2016                                 */
#* Author: Sumeet Jain                           */
#*                                               */
#*Script for Primetime - Synopsys          */
#*                                               */
#* Make changes to this script acc to your design */
#*************************************************/

#set path to search for design files and design libraries
#(In this case both are same otherwise use'/' to go to next line)
set search_path "/u/sumeet/pt"

#linling library .db
set link_library gscl45nm.db

#reading the verilog RTL netlist
read_verilog  SVFIFO_netlist.v

#selecting the current design
current_design SVFIFO
list_libs

#link the design and library
link_design SVFIFO

#setting timing constraints
create_clock -name clk -period 10  [get_ports clk ]
set_clock_uncertainty 0.5 [all_clocks]
set_clock_latency 0.5 [get_ports clk]

#set timing_report_unconstrained_paths "true"
#diaplay the timing report
report_timing -from fifo_reg[7][5]/CLK -delay_type max
report_timing -from fifo_reg[7][5]/CLK -delay_type min
```

This guide is by no means comprehensive. You should find yourself wanting to refer to more authoritative sources for more information on Design Compiler, Design Vision, and Prime time as follows which you can find in the D2L.

Design Compiler User Guide

PrimeTime and PrimeTime SI User Guide