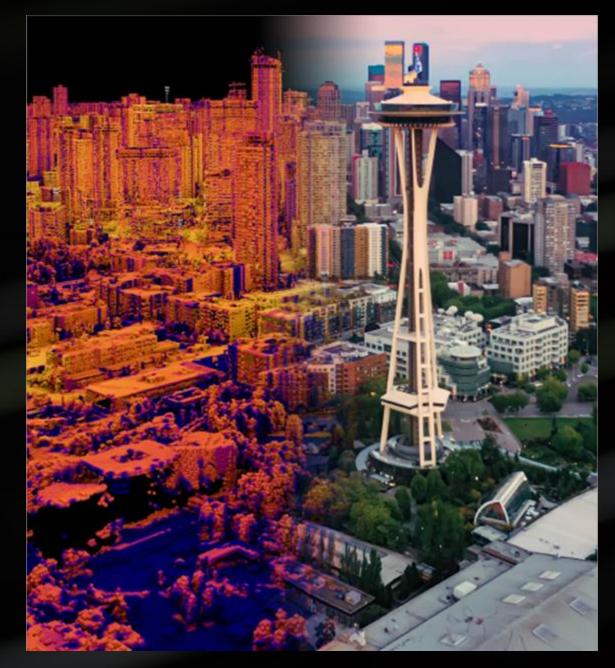


Next Wave of Applications

Transformative technologies opening new frontiers for thousands of new companies





Generative Al
Create new novel and exciting content

Data Science
Turn massive data sets into actionable insights

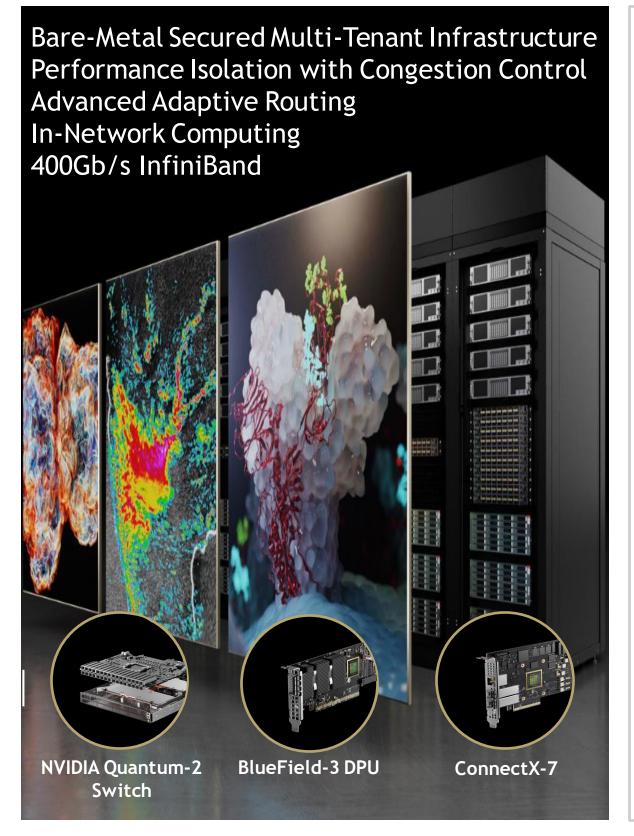
The Metaverse

Design, build, and operate virtual worlds and digital twins



Quantum-2 InfiniBand Platform

Unprecedented Performance, Scalability, and Security for HPC-Al



Most Advanced Networking High High Extremely Message Rate Throughput Low Latency **GPUDirect GPUDirect**

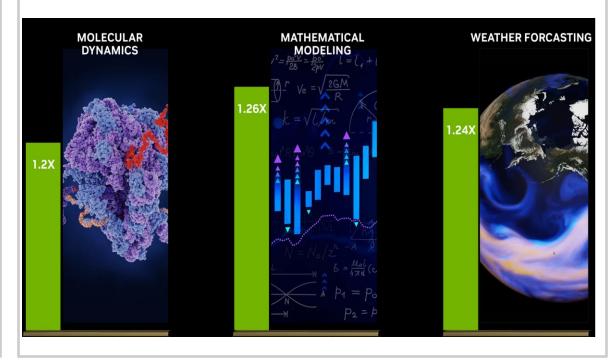
End-to-End RDMA RDMA Storage Smart Adaptive Congestion Routing Control Topologies

In-Network Computing

nd-to-End Adapter	Programmable Datapath Accelerator	Data Processing Units (Arm Cores) ecurity/ Tenant	Self Healing Network	End-to-End Sw
Adapter or/ DPU	All-to-All	MPI Tag Matching	Data Reductions (SHARP)	Switch



1.2x Higher Application Performance with BlueField DPU and Quantum InfiniBand **In-Network Computing**

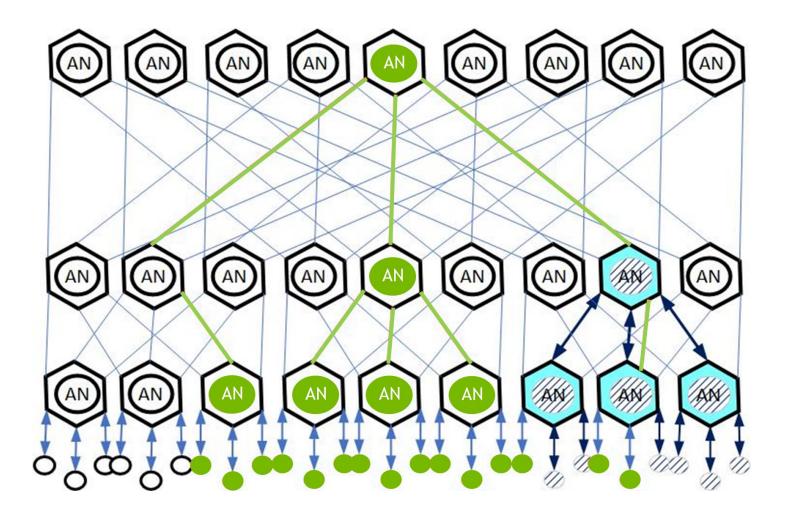




Scalable Hierarchical Aggregation and Reduction Protocol (SHARP)

Offloads collective operations from the host to the network switch

- In-network Tree based aggregation mechanism
- Multiple simultaneous outstanding operations
- Small message and large message reduction
- Barrier, Reduce, All-Reduce, Broadcast and more
- Sum, Min, Max, Min-loc, max-loc, OR, XOR, AND
- Integer and Floating-Point, 16/32/64 bits



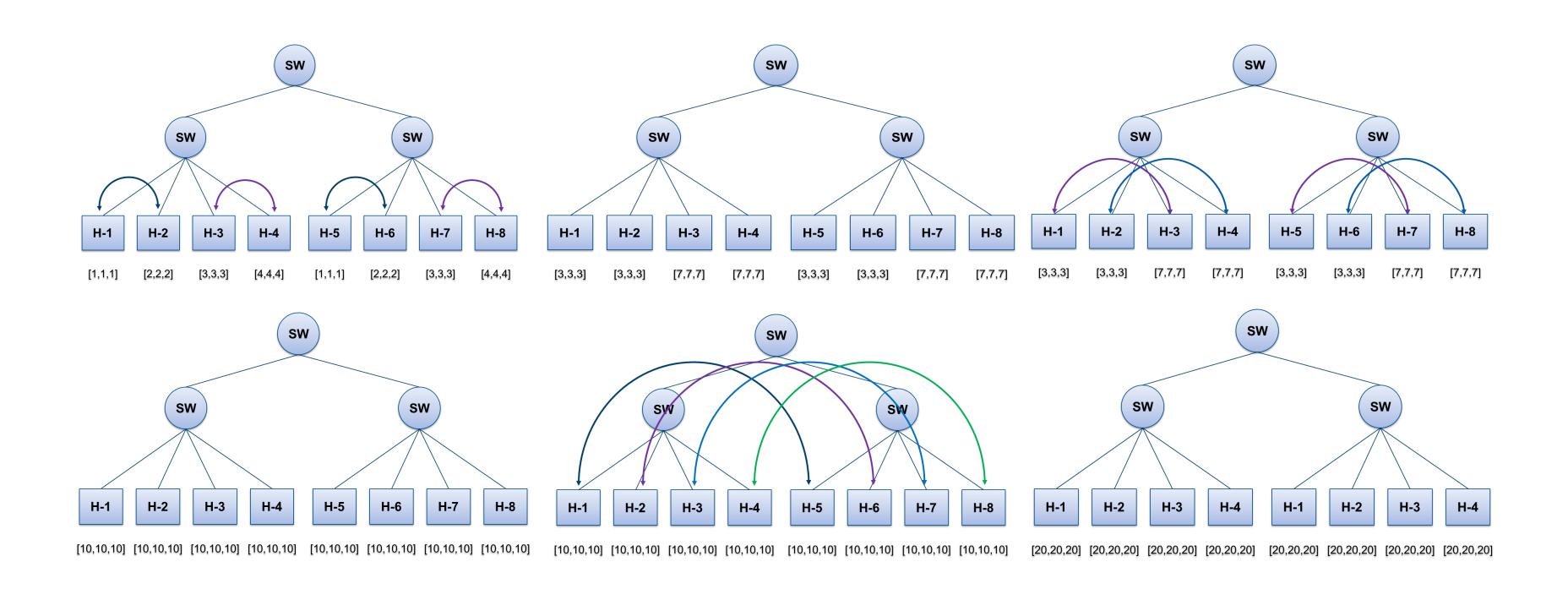


O Host: Data source and Destination



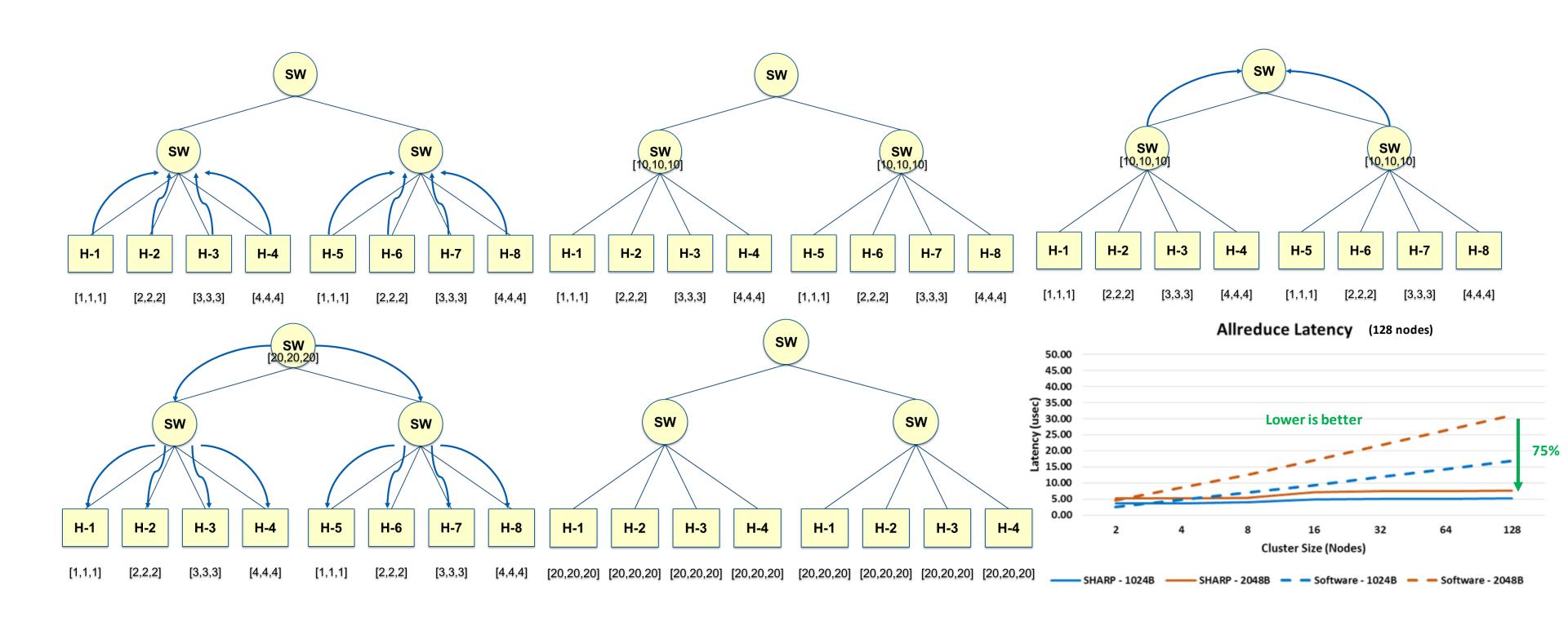
Scalable Hierarchical Aggregation and Reduction Protocol

Recursive doubling Algorithm for AllReduce Operation



Scalable Hierarchical Aggregation and Reduction Protocol

SHARP for AllReduce Operation





Comparison

Discussion

Decoupling latency from node count*

Without the capabilities of SHARP, Allreduce requires at least O(log(N)) phases.

SHARP operates level-by-level in the topology, proportional to the tree height.

\cap	ff	load
W		wau

Standard algorithms require the compute nodes to perform the reduction's compute.

SHARP boosts the effective utilization of the endpoints.

Network performance and consistency

SHARP is data-movement optimal.

Consistent, predictable network performance.

Algorithm	Latency	Bandwidth Req.
Recursive doubling	log2(N)·α	$log2(N) \cdot m\beta$
SHARP	2·α	$m \cdot \beta$

Description of parameters

 α – latency; cost of sending a single message

 β – Inverse bandwidth (1/200 Gbps)

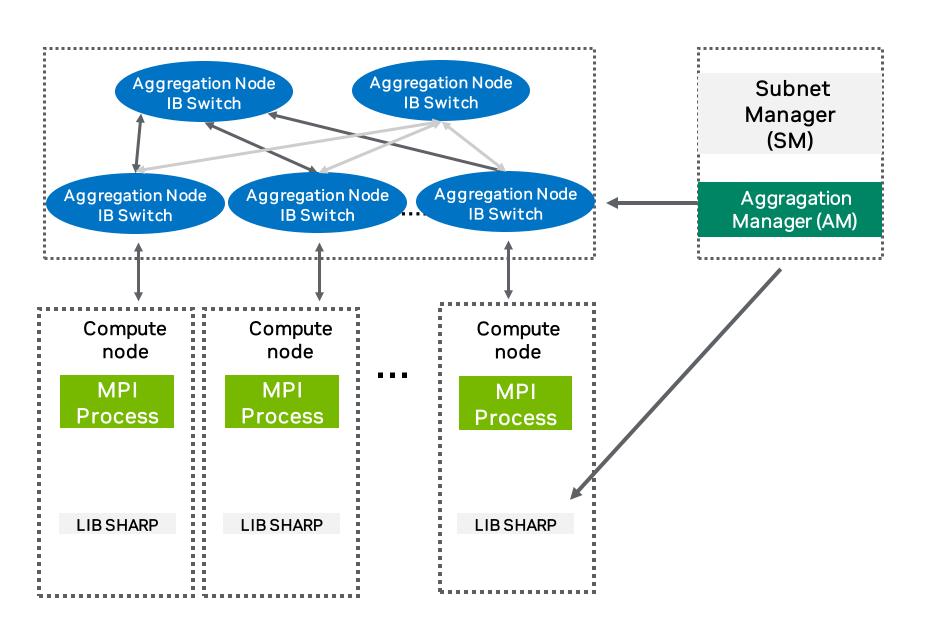
N - number of endpoints/GPUs

m – memory size of a single GPU's data (total memory: Nm)



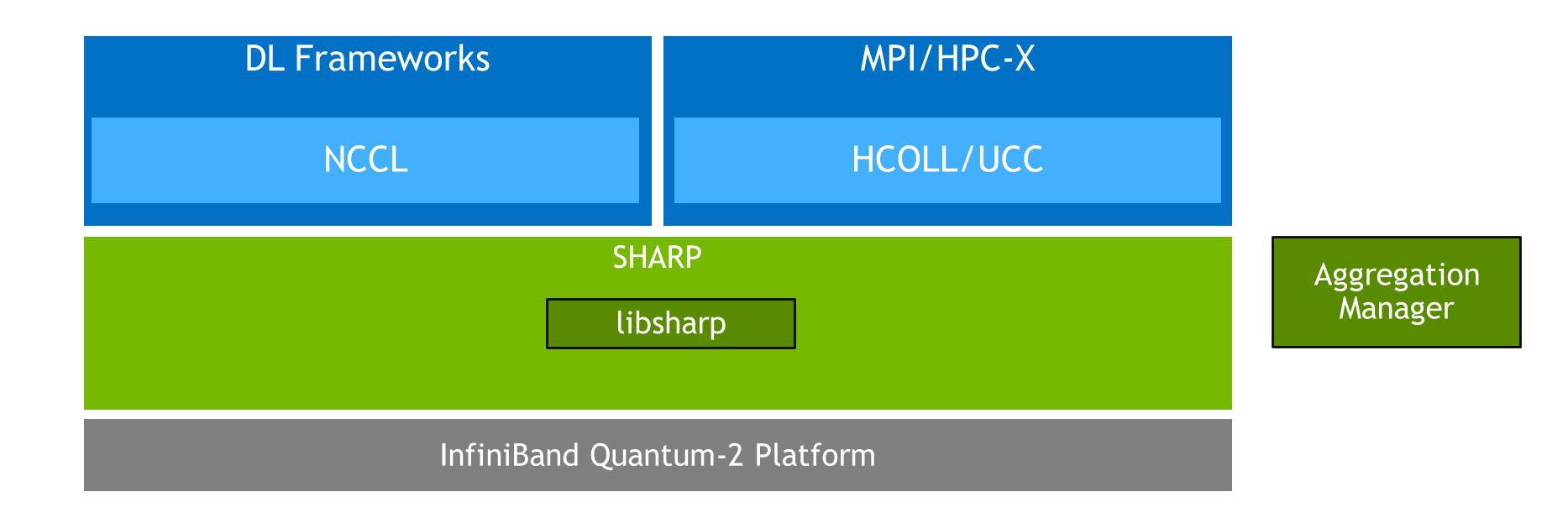
SHARP Implementation Details

- InfiniBand networks have a Subnet Manager ("SM") entity, which is independent of SHARP.
 - The SM populates the SMDB which contains network topology data used by SHARP.
- SHARP is managed by the Aggregation Manager ("AM"), a global software entity.
 - The AM is responsible for all SHARP resources construction of trees, allocations, locks, and so forth.
- Once a SHARP tree has been allocated to a user process, its compute nodes can push data into the corresponding Aggregation Nodes, addressable as virtual nodes.





SHARP Software Architecture

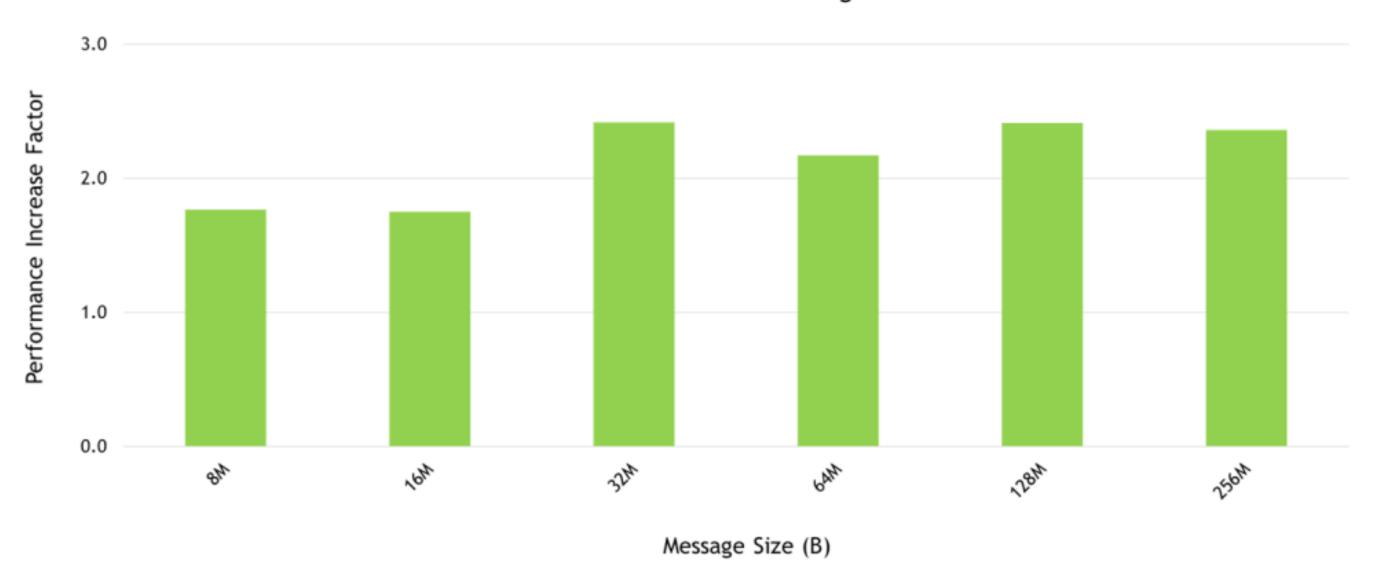




SHARP AI Performance Advantages

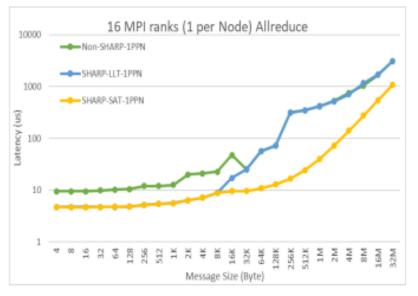
2.5X Higher Performance

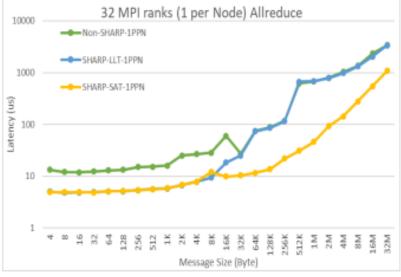
128 NVIDIA DGX A100 (1024 GPUs, 1024 InfiniBand Adapters) NCCL AllReduce Performance Advantage with SHARP

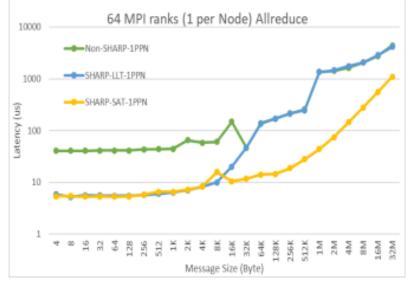


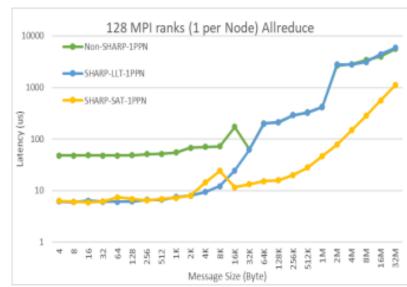
InfiniBand NDR SHARP Performance

NDR: SHARP Performance









- Randomly selected nodes from cluster
- Run MPI AllReduce with 16, 32, 64, 128 nodes with PPN=1
- Significant performance improvement with both LLT and SAT protocols































AI APPLICATION FRAMEWORK





NVIDIA HPC

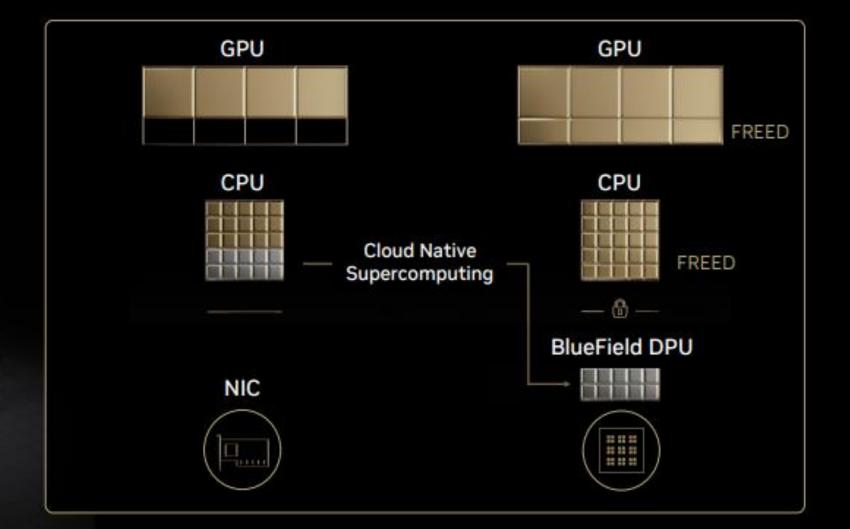


NVIDIA AI



NVIDIA Omniverse

ACCELERATION LIBRARIES

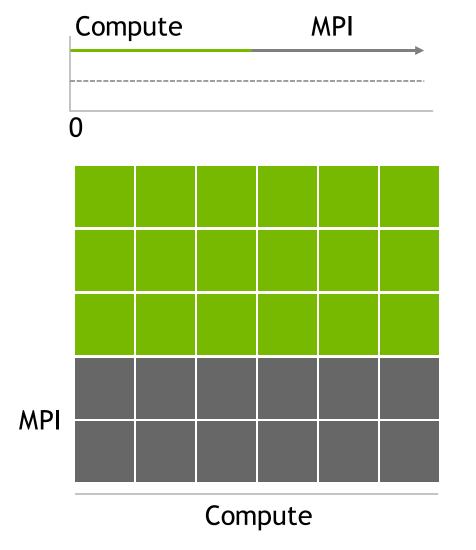


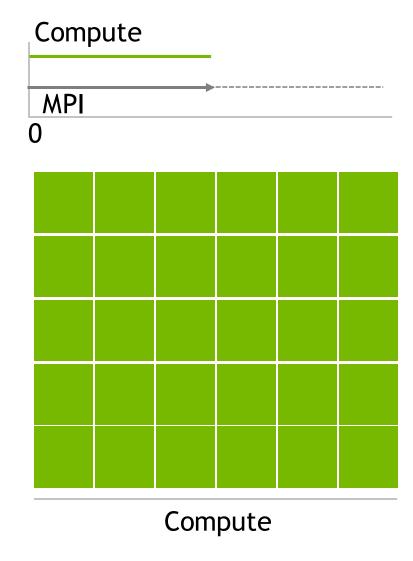


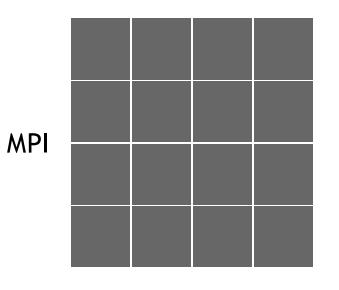
DPU for Scientific Computing

1.2x Higher Application Performance with MPI Acceleration

- Parallel communications impose large overhead on CPU centric platform
- Offloading and accelerating these operations maximize performance
- Enabling computations and communications to be performed in parallel







DPU BlueField-3





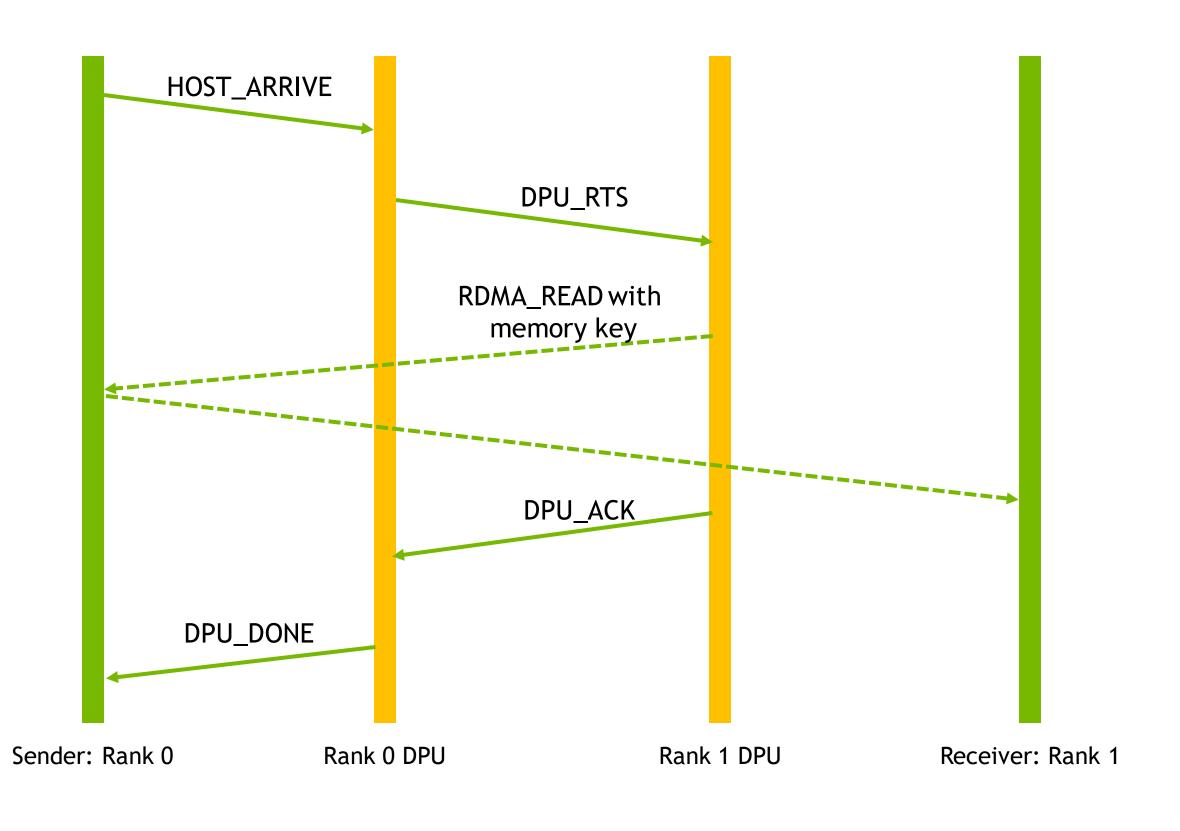






Offloading and Accelerating Data Exchange Example

An Element of Collective Algorithm



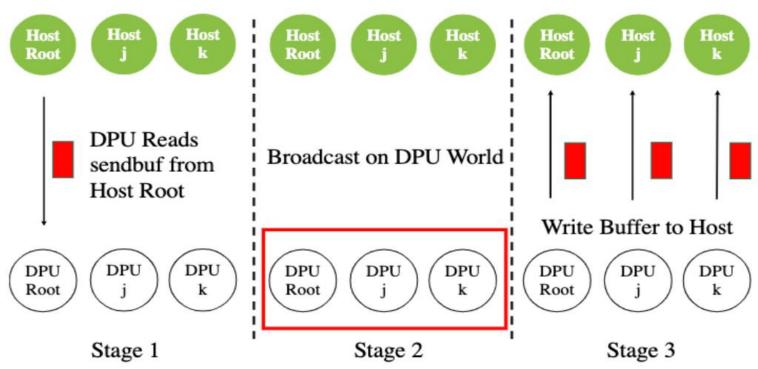
Offload Framework

MVAPICH2

- Non-blocking collective operations are offloaded to a set of Worker processes
- BlueField is set to separated host mode
- Worker processes are spawned to the ARM cores of BlueField
- Once the application calls a collective, host processes prepare a set of metadata and provide it to the Worker processes
- Using these metadata, worker processes can access host memory through RDMA
- Worker processes progress the collective on behalf of the host processes

Once message exchanges are completed, worker processes notify the host processes about the completion of the

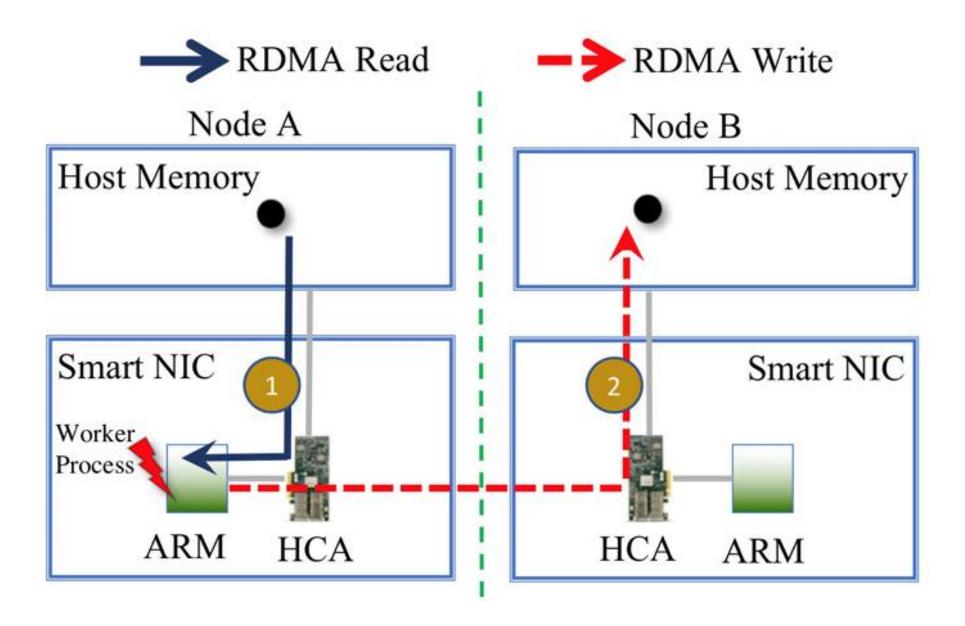
non-blocking operation



Proposed Non-Blocking Alltoall Desgin

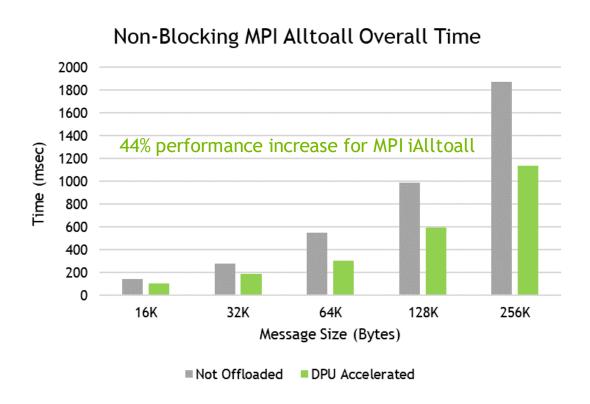
MVAPICH2

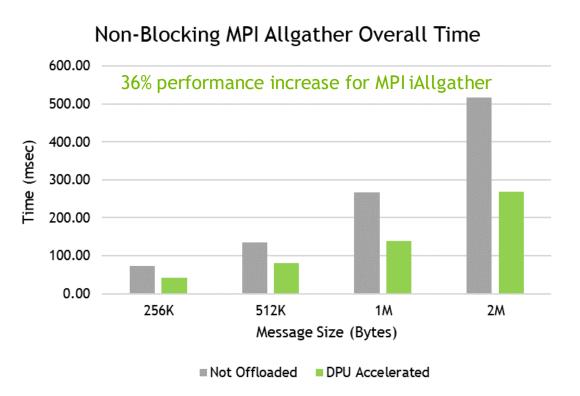
- Worker process performs RDMA Read to receive the data chunk from host main memory
- Once data is available in the ARM memory, worker process performs RDMA Write to the remote host memory

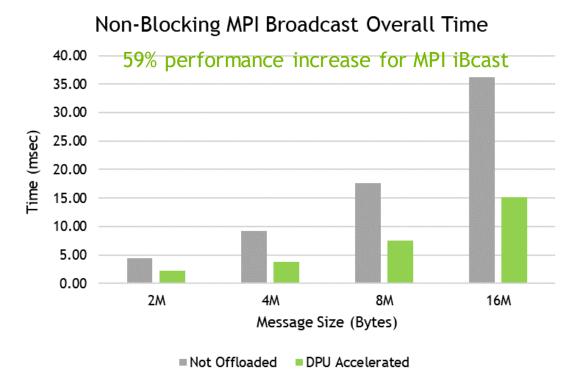


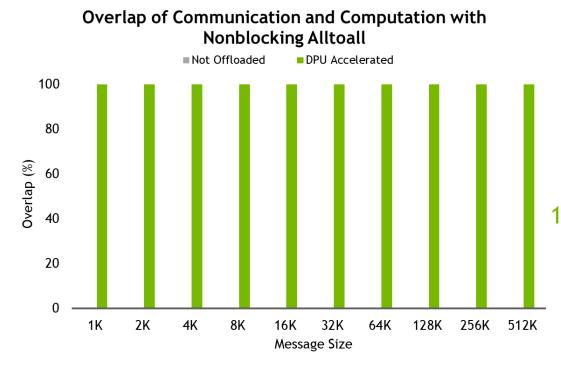


Non-Blocking MPI Performance





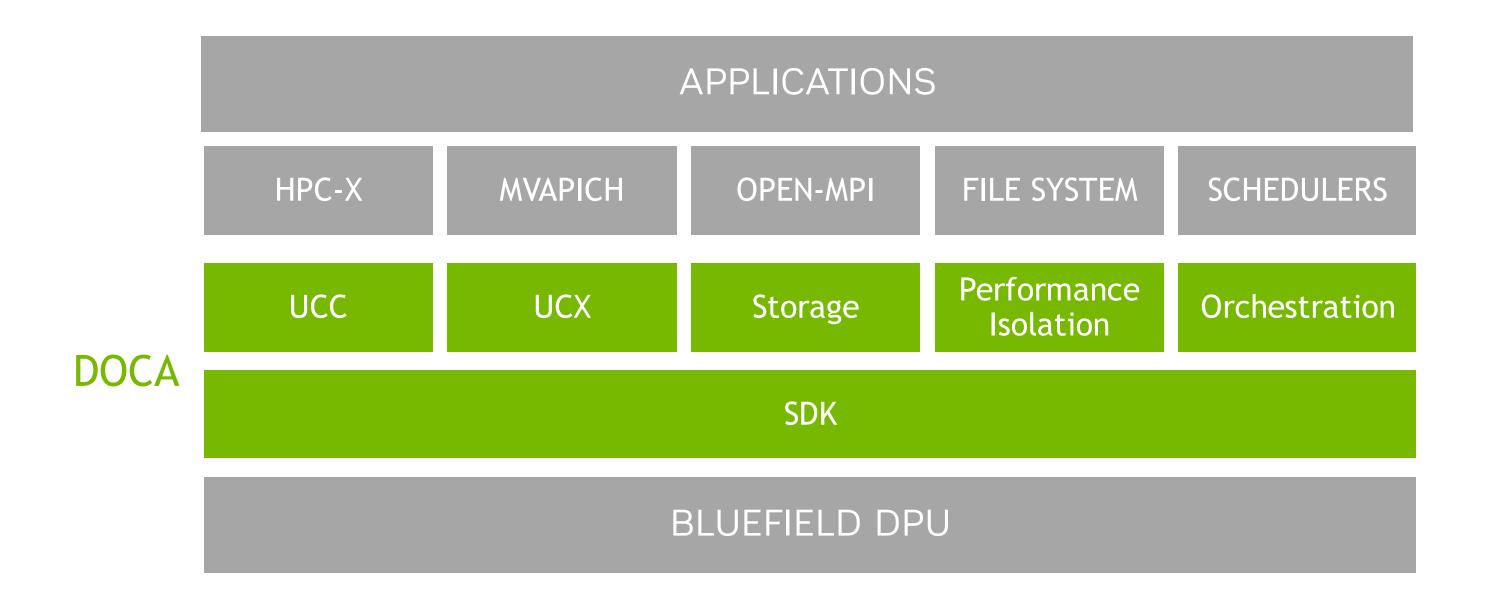




100% Communication - Computation Overlap



Accelerating HPC Applications with DOCA Services

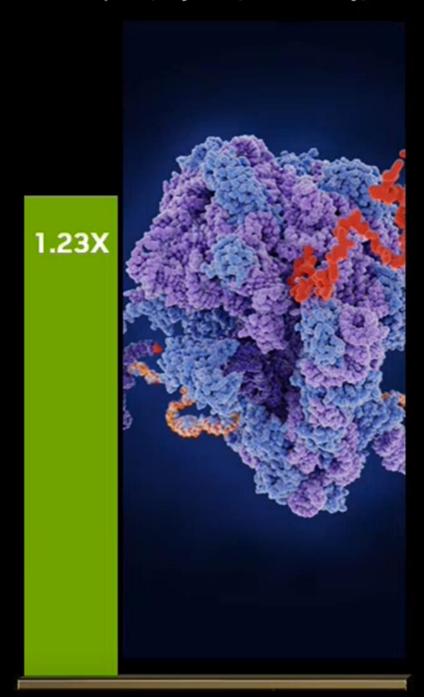




Higher Performance and Cost Saving

With BlueField DPU and Quantum InfiniBand In-Network Computing

Octopus (Physics / Chemistry)



1.23 Higher Performance1.17 Higher Performance / TCO\$1.19 Higher Performance/Watt



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