8-bit FPGA SoftProcessor

VHDL-MCU-8 Series

Technical Reference Manual

High-performance 8-bit RISC Architecture	Integrated 16-bit GPIO Port
Harvard Architecture	Direct/Indirect Addressing Modes
16-bit Fixed Instruction Word	Comprehensive Status Flags (Z, C, N, V, S, H, T, I)
8 × 8-bit General Purpose Registers	Up to 256 Instructions Program Memory
Fully Static Operation	Separate Data RAM (256 bytes)
Single Clock Cycle Execution	Simple 2-stage Pipeline

1 ARCHITECTURAL OVERVIEW

The VHDL-MCU-8 is a simple 8-bit microcontroller implemented in synthesizable VHDL for FPGA targets. Maybe it has a 1970s vibe, but at least it's also unoptimized and sluggish.

The processor follows a strict **Harvard Architecture** with separate Program ROM and Data RAM. The simple 2-stage pipeline allows simultaneous instruction fetch and execution.

2 BLOCK DIAGRAM

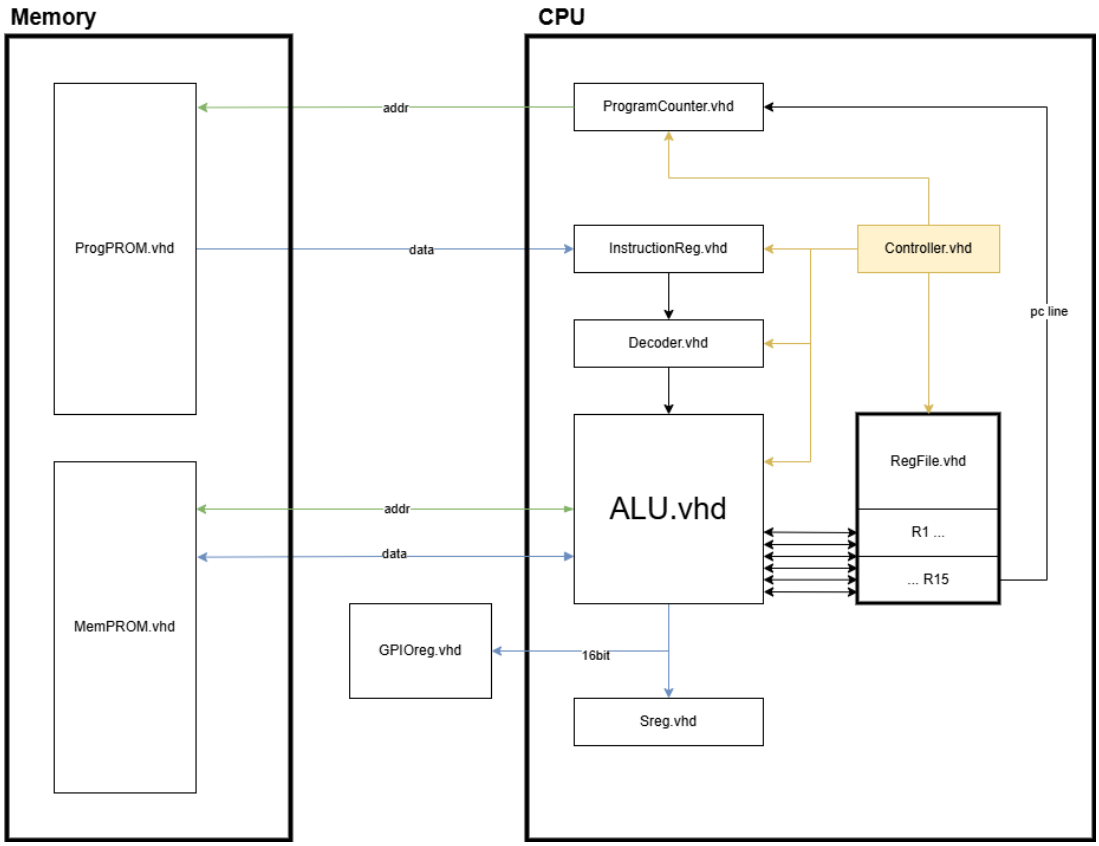

Figure 1: Core Architecture Block Diagram showing the complete data path, control unit, and memory interfaces.

3 REGISTER FILE

The Register File contains 8 general-purpose 8-bit registers, optimized for the instruction set architecture.

Table 1: Register File Organization

Register	Description
R0	General Purpose / Accumulator
R1	General Purpose
R2	General Purpose
R3	General Purpose
R4	General Purpose
R5	General Purpose
R6	General Purpose
R7	General Purpose

4 STATUS REGISTER (SREG)

The Status Register contains flags set by arithmetic and logic operations, used for conditional branching.

Table 2: Status Register Bits

Bit	Symbol	Description
7	I	Global Interrupt Enable
6	T	Bit Copy Storage
5	H	Half Carry Flag
4	S	Sign Bit (S = N V)
3	V	Two's Complement Overflow
2	N	Negative Flag
1	Z	Zero Flag
0	C	Carry Flag

5 INSTRUCTION FORMATS

The instruction set uses fixed 16-bit encoding for all instructions.

5.1 R-Type (Register-Register)

15:11	10:8	7:5	4:0
Opcode	Rd (Dest)	Rs (Src)	Reserved

Used for: `ADD`, `SUB`, `AND`, `OR`

5.2 I-Type (Immediate)

15:11	10:8	7:0
Opcode	Rd (Dest)	8-bit Constant

Used for: `LDI`, `CPI`, `SUBI`

6 CORE MODULES

6.1 Program Counter (PC)

8-bit counter addressing up to 256 instruction locations.

- **Normal:** PC ← PC + 1
- **Jump:** PC ← target address
- **Branch:** PC ← PC + k + 1
- **Reset:** PC ← 0x00

6.2 Instruction Register (IR)

Latches 16-bit instruction during fetch cycle.

- **High Byte:** Opcode + Destination register
- **Low Byte:** Source register or immediate

6.3 Arithmetic Logic Unit (ALU)

Single-cycle execution between registers or register and immediate.

- **Operations:** ADD, ADC, SUB, SBC, AND, OR, XOR
- **Comparison:** CP, CPI (flags only)
- **Flags:** Updates Z, C, N, V, H

6.4 Control Unit

2-state Moore finite state machine:

1. **FETCH:** PC → ROM, ROM → IR
2. **EXECUTE:** Decode, control signals, write back

7 ORDERING INFORMATION

Table 3: Available Configurations

Method	Class	Price / Time
Github Download	Basic	Free / Instant
Contact me on email	Standard	Free / 1h
Get pendrive from me	Premium	1x Coffe / 1 day

DOCUMENT INFORMATION

Document: TRM-VHDL-MCU8-001
Revision: 1.0
Status: Preliminary
Release Date: December 11, 2025
Contact: 263663@student.pwr.edu.pl

8 INSTRUCTION SET SUMMARY

Table 4: Complete Instruction Set Reference

Mnemonic	Operands	Cycles	Description
Arithmetic & Logic			
ADD	Rd, Rs	1	Rd ← Rd + Rs
ADC	Rd, Rs	1	Rd ← Rd + Rs + C
SUB	Rd, Rs	1	Rd ← Rd - Rs
SBC	Rd, Rs	1	Rd ← Rd - Rs - C
AND	Rd, Rs	1	Rd ← Rd Rs
OR	Rd, Rs	1	Rd ← Rd Rs
XOR	Rd, Rs	1	Rd ← Rd Rs
COM	Rd	1	Rd ← 0xFF - Rd
NEG	Rd	1	Rd ← 0x00 - Rd
Data Transfer			
LDI	Rd, k	1	Rd ← k
MOV	Rd, Rs	1	Rd ← Rs
LD	Rd, X	2	Rd ← (X)
ST	X, Rs	2	(X) ← Rs
LDS	Rd, a	2	Rd ← (a)
STS	a, Rd	2	(a) ← Rd
Branch Instructions			
RJMP	k	2	PC ← PC + k + 1
RCALL	k	3	Push PC+1, PC ← PC + k + 1
RET		4	PC ← Stack
BRBS	s, k	1/2	Branch if SREG(s) = 1
BRBC	s, k	1/2	Branch if SREG(s) = 0
Bit Operations			
SBI	P, b	1	Set bit in I/O Register
CBI	P, b	1	Clear bit in I/O Register
BST	Rd, b	1	T ← Rd(b)
BLD	Rd, b	1	Rd(b) ← T