ECE M116C - CS M151B Computer Architecture Systems - UCLA

Homework 2

Deadline: Thursday, Oct. 17, 11:59 PM

Fall 2024

(Upload it to Gradescope.)

Q1. Consider the following latencies for different units in the (single-cycle) datapath described in the class:

Mem (I and D) (read)	**Reg. File (read)**	**Reg. File (write)**	**Mux (any size)**	**ALU**	**Gate (any)**
310 ps	170 ps	12 ps	20 ps	240 ps	3 ps

Imm Gen	**PC (read)**	**Adder**	**PC (write)**	**Mem (D) (write)**	**Control (ALU Control included)**	**Buffer Reg (read/write) (for Q2)**
40 ps	20 ps	140 ps	10 ps	20 ps	75 ps	10 ps

Answer the following questions:

a) What is the latency for ORI instruction?
(i.e., how long does it take to complete this instruction? Assume that the beginning of the instruction is reading the PC. Note that there might be multiple parallel paths, so you need to report the MAX). Show your work.

b) What is the latency for LW instruction (single cycle)?

c) What is the latency for BEQ instruction?

d) What is the minimum clock cycle for this processor?

Q2- Now consider changing the above design into a multi-cycle design where we add buffer registers as explained in Lecture 5. Answer the following questions:

a) What is the new minimum clock cycle for this design?

b) What is the latency for ORI instruction (consider that we cannot bypass stages, for example, memory, even if they are not used)?

c) Repeat the same question, now consider that we can bypass unused stages for ORI?

d) What is the latency for LW?

Q2. We want to add three new instructions to our datapath+controller design discussed in class (single cycle design). Redraw the datapath+controller with the changes needed to support these instructions (show the control signals in a different color). Draw a different plot for each instruction.

a) SRAI

b) SB

c) LUI