ECE M116C - CS M151B Computer Architecture Systems - UCLA

Homework 3

Deadline: Sunday, Nov. 10, 11:59 PM

Fall 2024

(Upload it to Gradescope.)

Q1. Consider the following code:

```
ADDI x1, x0, 36
ADDI x3, x0, 3
ADD x4, x0, x0
JAL x2, 36
ADDI x1, x0, 0x204
ADDI x1, x0, 0x204
ADDI x1, x0, 0x204
ADDI x1, x0, 0x204
ADDI x1, x0, 0x204

BEGIN:
BEQ x0, x3, END
ADDI x3, x3, -1
ADDI x4, x4, 2
JAL x0, -12

END:
XOR x0, x0, x0
```

Complete the following two tables for all JAL/BEQ in the code above. Using the following assumptions:

- Assume that the PC starts at 0.
- BTB has four entries we use lower bits of PC to index it (bits 2 and 3 since the first two bits are always zero).
- BHT is a 2-bit bimodal where 11 is a strong taken. If you need to initilize the BHT for a new branch, do 10 if it was taken and 01 if it was not taken the first time.
- If the tag is not in BTB, we predict Not Taken.
- Misprediction is resolved in DE and BTB is also updated during that stage.

a) Show the BTB after each control-flow instruction. (BTB is initialized with values shown below.)

Tag	BHT	Target
0x00	11	0x34
0x20	10	0x34
0x00	00	0x00
0x00	10	0x24

b) Complete this table. (From left to right is the *execution order*. Add more columns if needed.)

PC	..	…	…			
Prediction	?	?	..			
Actual Outcome	?	?	…			

c) Draw the timeline (by putting f,d,e,m,w) for each instruction. You don't need to show the forwarding. If the instructions need to be flushed and replaced by bubbles show it with b (e.g., eb, mb, and wb for bubbles in each stage). What is the total number of cycles?

	1	2	3	4	5	6
addi						
addi						

Q2. We have the following set of instructions. Assume LW takes four cycles and SRA takes two cycles.

```
0x100: lw x1, 4, x1
0x104: xor x3, x0, x1
0x108: sra x1, x3, x2
0x10c: sub x1, x1, x0
0x110: addi x2, x0, 2
0x114: xor x2, x3, x0
```

We have a 2-issue out-of-order processor (you can access the template below).

HW3-copy.pptx

Start from cycle 2, with Rename, and fill all the tables. In the green table (the one above the reservation station on the left), you should put R, Di (for dispatch), I (for issue), C, and Rt (for retire). If an instruction stays in one stage for multiple cycles, repeat the same character for it (e.g., F, D, R, Di, Di, I, C, C, Rt). `Comp` in ROB shows whether the instruction is completed or not. (Assume that you can retire a maximum of two instructions per cycle.)

Note: You can either show one slide per cycle (i.e., all stages in one slide) or one slide per stage.