1.

a. $\log_2(\text{sets}) + \log_2(\text{bytes per block}) = \log_2(\text{page size})$
Sets = cache size / line size * associativity = cache size / 8 * 16 ways
Bytes per block = 64
Page size = 2 kb
$\log_2(\text{cache size} / 8 * 16) = \log_2(2\text{kb}) - \log_2(64)$ => cache size = 8KB

b. Virtual address space = 2^{34} bytes
Page size = 2^{11} bytes
# of virtual pages = $2^{34}/2^{11} = 2^{23}$

c. Physical address space = 1GB
Page size = 2^{11} bytes
# of physical pages = $2^{30}/2^{11} = 2^{19}$

d. PTE size = 4 bytes
Flat page table size = virtual pages * PTE size = 2^{25} bytes

e. Virtual address space = 2^{34} bytes
Page size = 2^{11} bytes
First level = 10 bits
Remaining bits = 23 - 10 = 13
PTE size = 4 bytes
First-level page table: 2^{10}
Second-level page table (per first-level entry): 2^{13}

First level page table size: $2^{10} * 4 = 2^{12}$
Second level page table size: $2^{10} * 2^{13} * 4 = 2^{25}$

Total = First size + second size = approx. 2^{25} bytes

f. Second level would only be $2^{10} * 2^5 * 4 = 2^{17}$ bytes and since the first one is 2^{12} it is less and 2^{17} masks it

2.

a. TLB entries: 4
Virtual address space = 2^{32} bytes
Page size = 2^{12} bytes
Physical address space = 2^{29} bytes
# of virtual pages = $2^{32}/2^{12} = 2^{20}$ = 20 bits rat problem

# of physical pages = $2^{29}/2^{12} = 2^{17}$ = 17 bits rat problem
8 bits of flag

One TLB entry = 20 + 17 + 8 = 45 bits
TLB size = # entries * 45 bits = 180 bits = 22.5 bytes

b. Avg access time = hit rate * hit time + miss rate * miss penalty = (1 - 0.0001) * 1 + (0.0001) * 150 = 1.015 cycles

c. TLB access time should be the same…

3.

a. Thread 1 x1 = 4, Thread 2 x1 = 3:
Thread1:
T1.1, T1.2, T1.3, T1.4, T1.5, T1.6

Thread2:
T1.1, T3.1, T3.2, T3.3, T2.1, T2.2

b. No because fence rw and the acquiring and releasing of the locks ensure that both thread1 and thread2 run in the exact order I just mentioned with the same values of x1 for each thread. The memory accessed within both threads also independent of each other.