ELEC 402

Standard Cell Layout
Lecture 10

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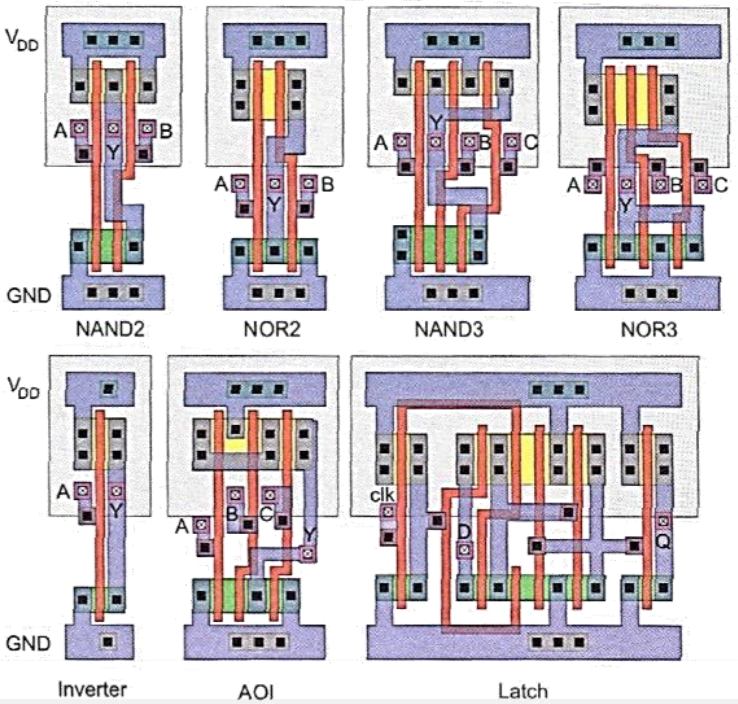
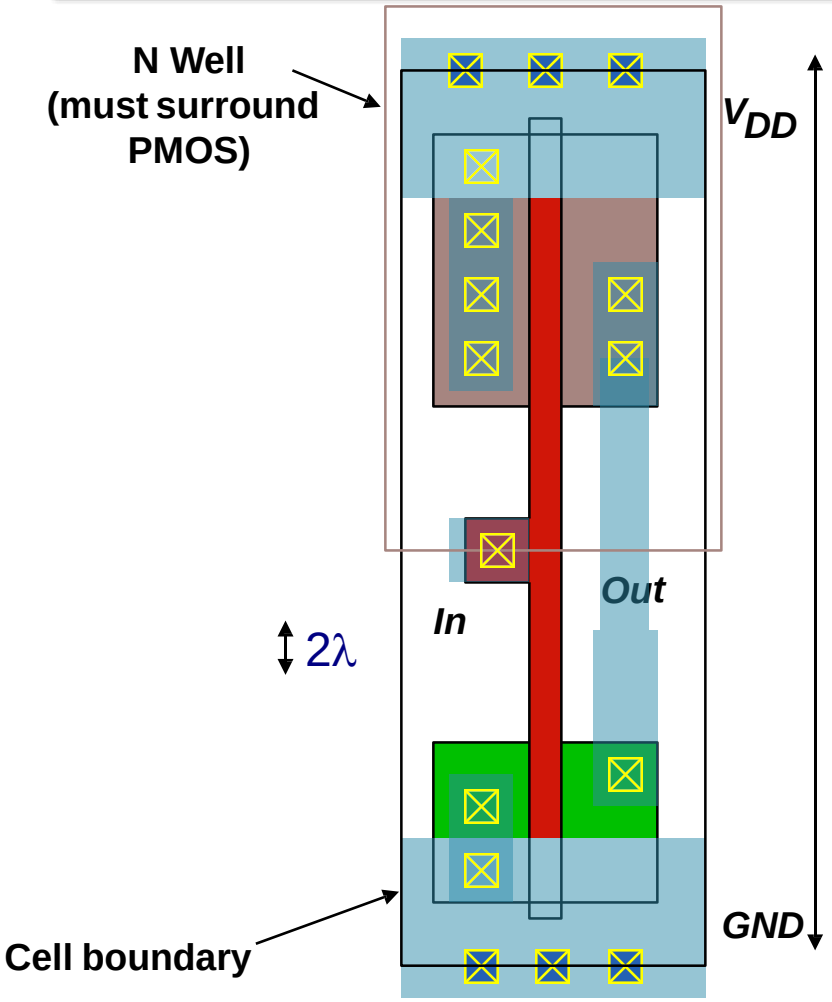
Slides Courtesy : Dr. Sudip Shekhar (UBC)

Gate Layout

- **Layout can be very time consuming**
  - Design gates to fit together nicely
  - Build a library of standard cells
  - Use PNR (placement & routing) tools for synthesis
- **Standard cell design methodology**
  - V_{DD} and GND should abut (standard height)
  - Adjacent gates should satisfy design rules so as to "snap together"
  - NMOS at bottom and PMOS at top
  - All gates include well and substrate contacts
  - Use poly and M1 to route the standard cells and leave upper metal layers (M2, M3…) as routing channels to interconnect cells
  - Upper metal layers often follow HVH or VHV track direction to ease PNR

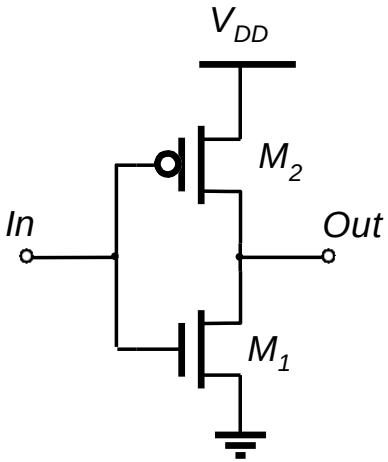


Standard Cells – Inverter



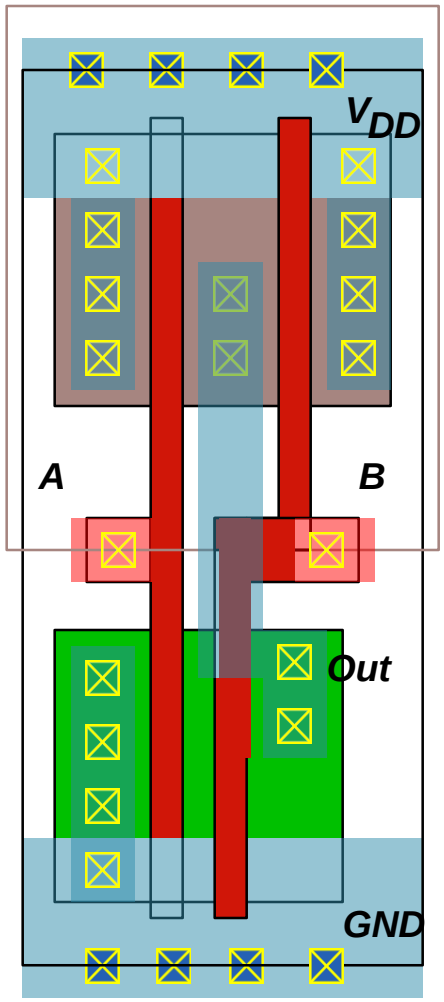
Pitch = repetitive distance between objects
Metal track is ~ 6λ pitch (3λ width + 3λ space)
Cell height 12 metal tracks (integer # tracks)
Cell height is "12 pitch“ or higher

Rails ~10λ

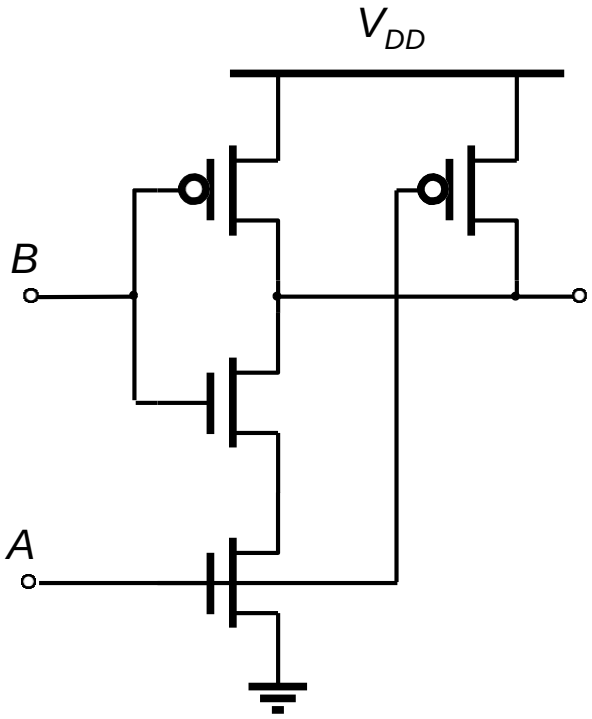


- **Horizontal N-diffusion and P-diffusion strips, Vertical polysilicon gates**
- **Metal1 V_{DD} and GND rails at top and bottom respectively**
- **λ = 0.125 μm in 0.25 μm process → not that useful in newer technologies**

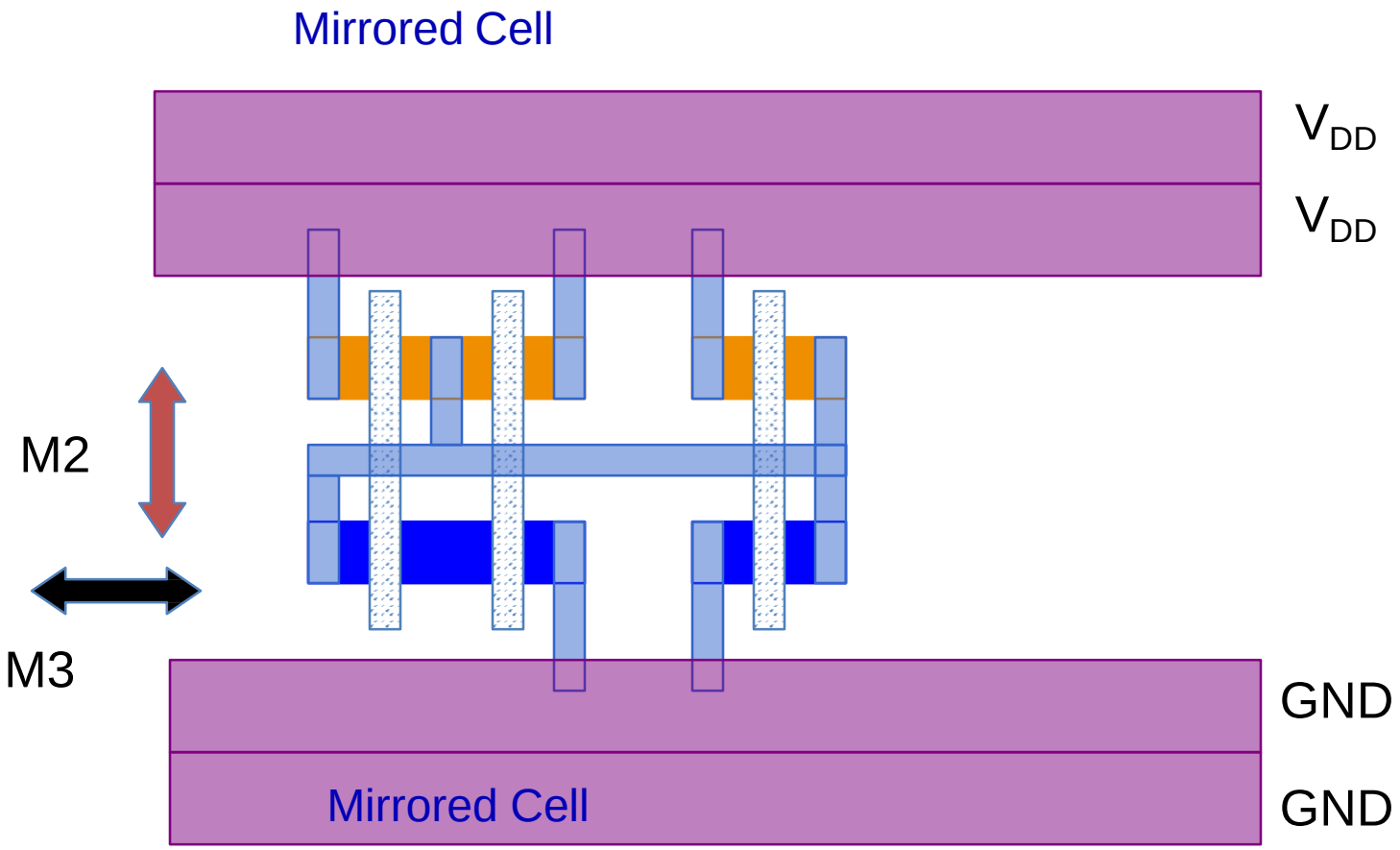
Standard Cells – NAND2



2-input NAND gate



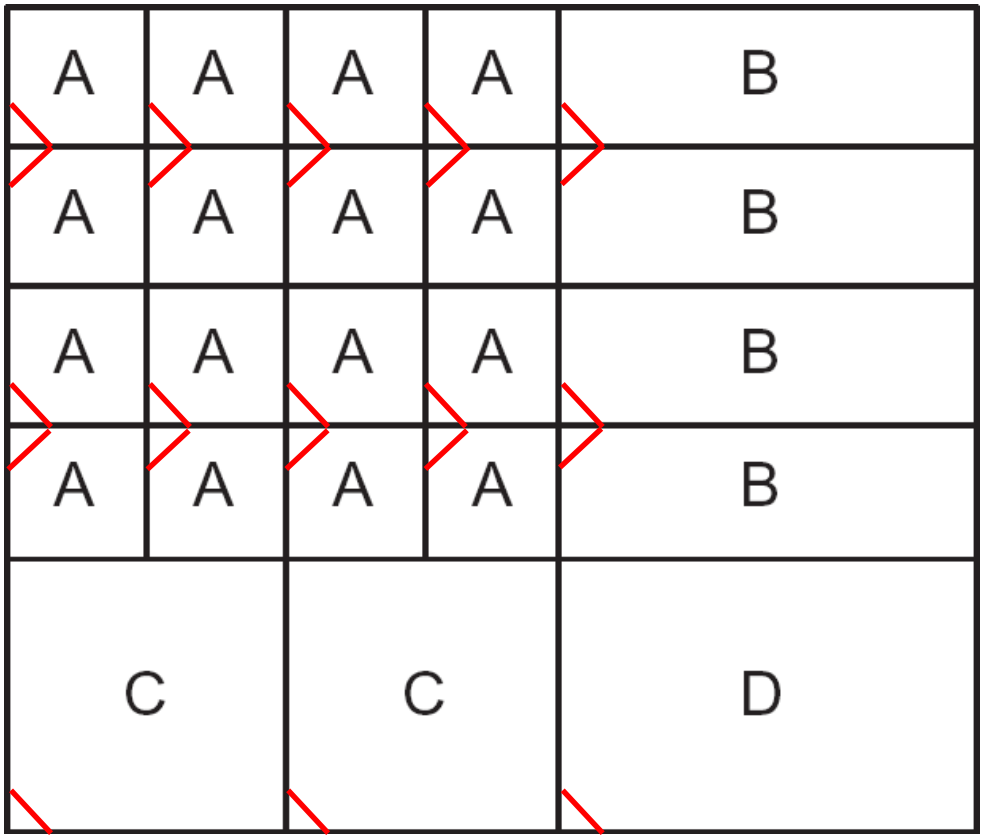
Standard Cell Layout Methodology



- **Contacts & Wells not shown**

Pitch Matching of Snap-Together Cells

The two technique allowing to repeat structures and abut them together

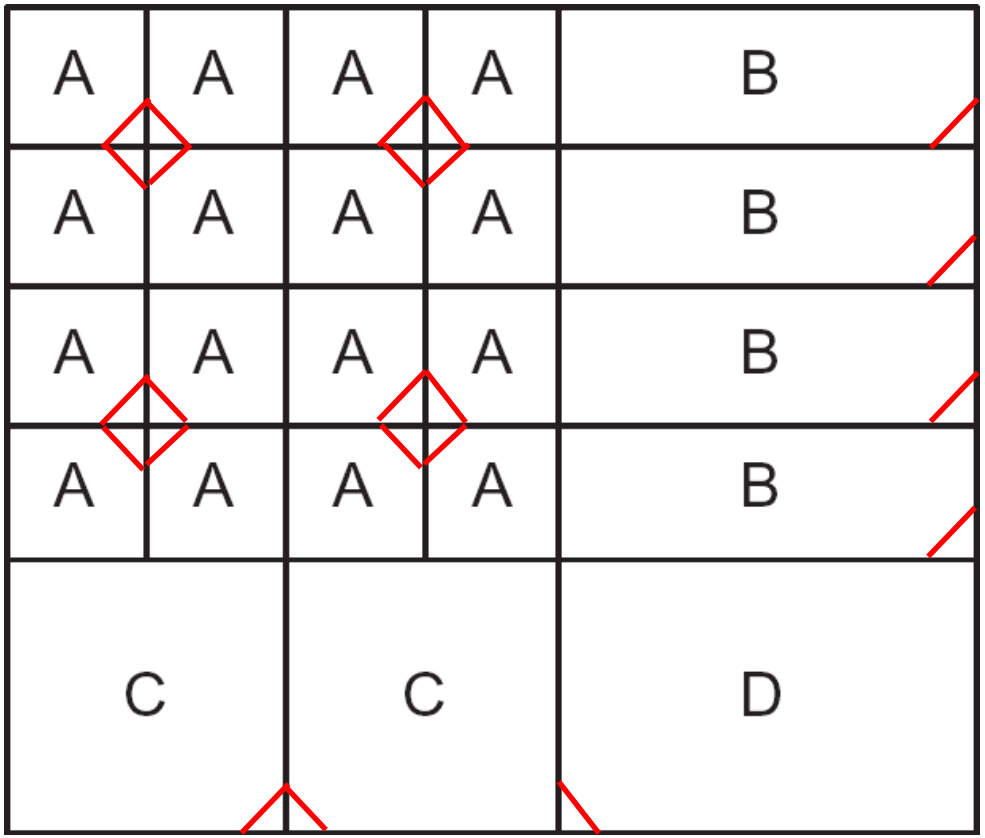


- **Stepping**

Pitch matching is a necessity

Pitch Matching of Snap-Together Cells

The two technique allowing to repeat structures and abut them together

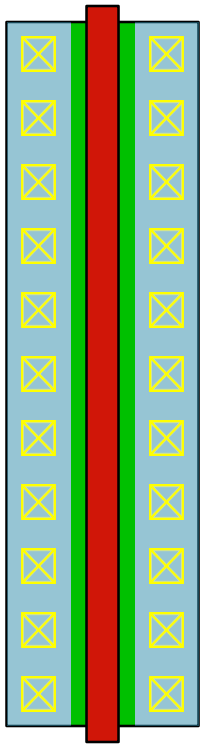


- **Flipping**

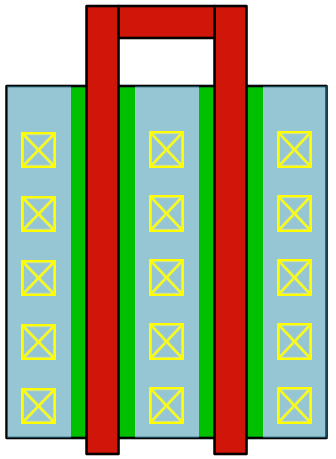
Pitch matching is a necessity

Multi-Fingered Transistors

One finger



Two fingers (folded)

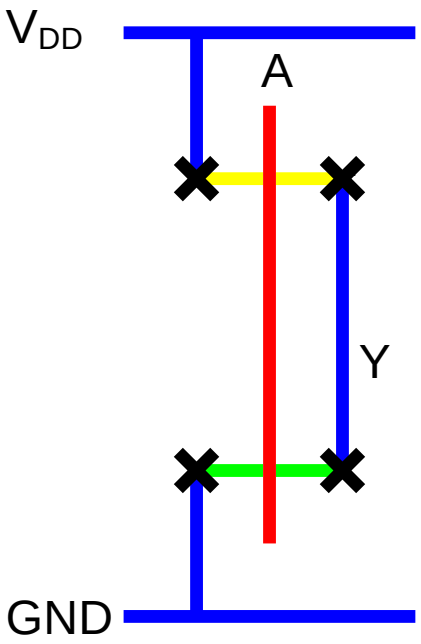


Less diffusion capacitance

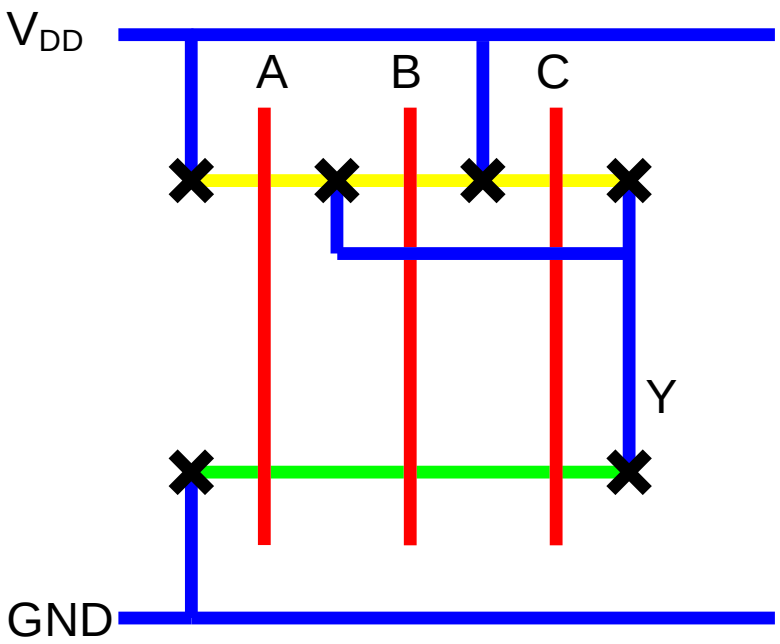
- **For a very wide transistor that does not fit in the standard cell height, break the transistor into multiple fingers → wide layout**

Stick Diagrams

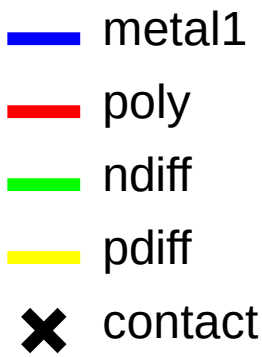
- Contains no dimensions
- Represents relative positions of transistors
- Help plan layout quickly



INV



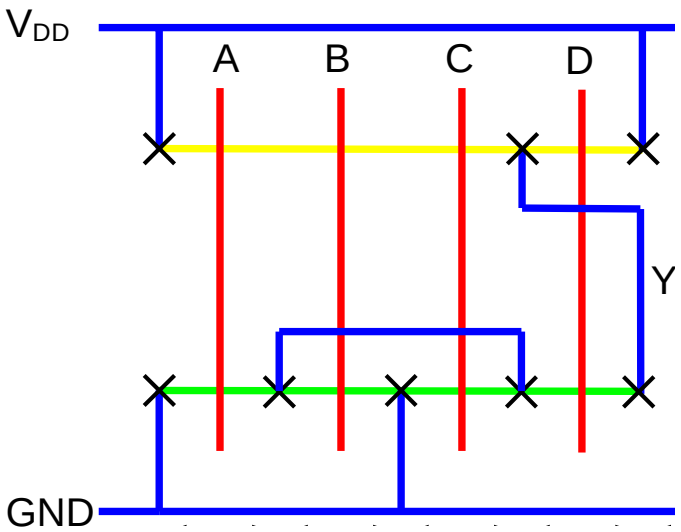
NAND3



Stick Diagrams Example: O3AI

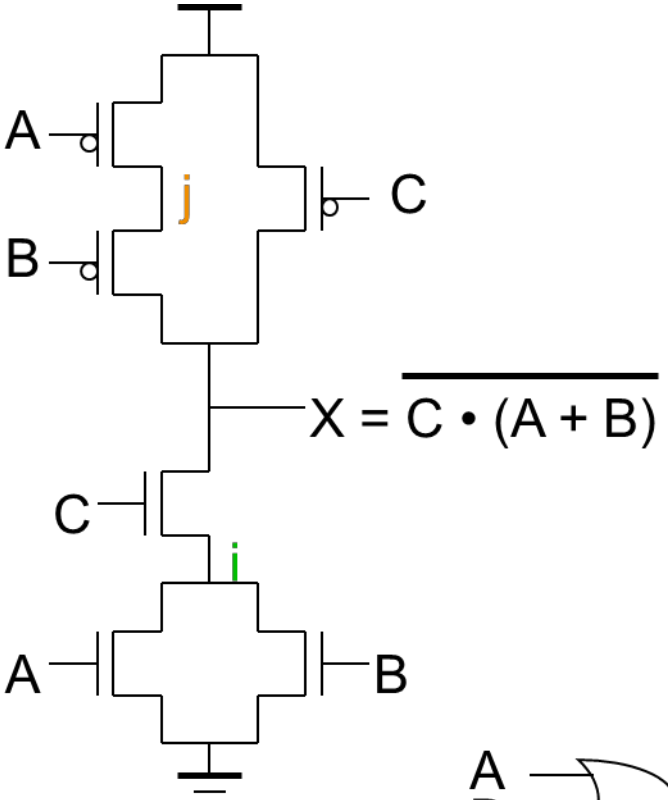
The goal is to draw the layout such that

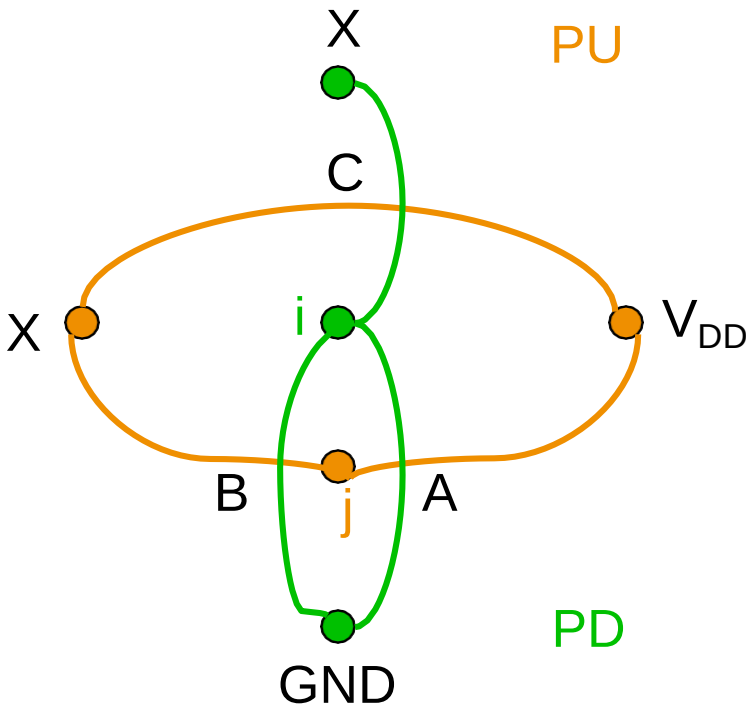
1. there is no discontinuity in diffusion areas
2. gates (polysilicon in red) run vertically
3. No need for crossovers

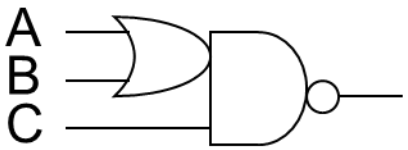


M1 (first metal layer) is drawn in blue to make necessary connections

Stick Diagrams & Logic Graph

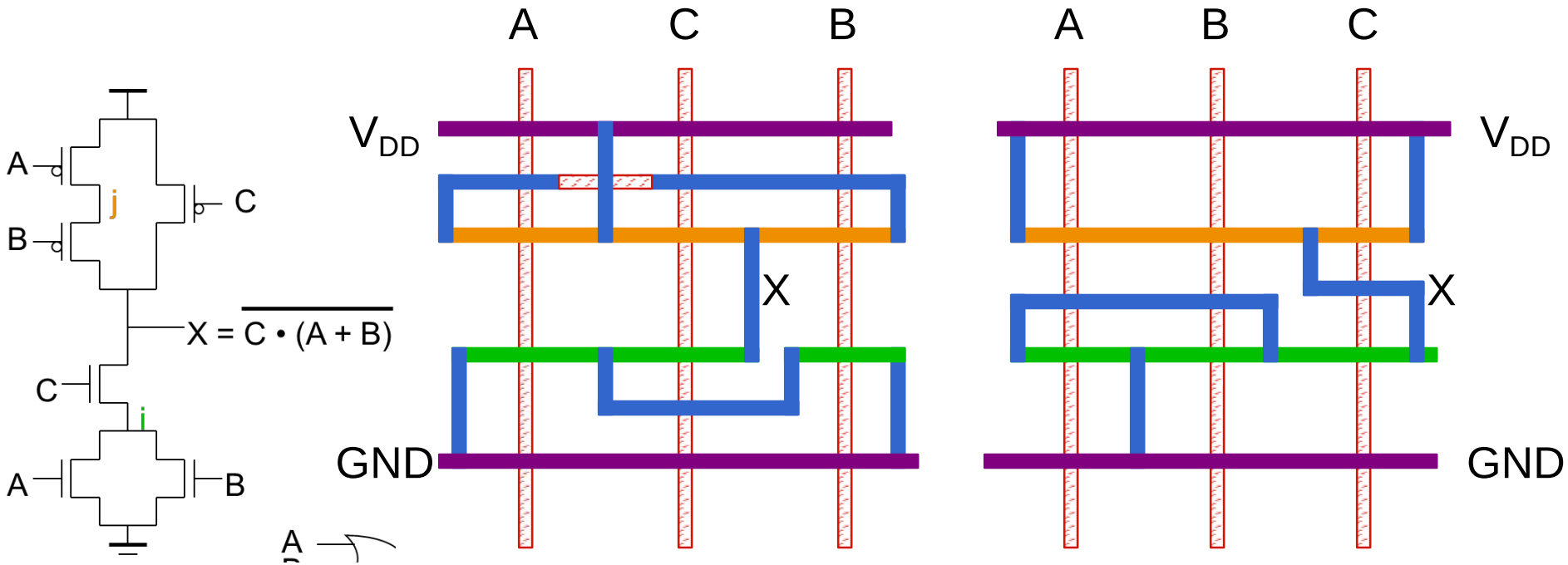






- **Systematic approach to derive order of input signal wires so gate can be laid out to minimize area**
- **PU and PD are duals (parallel ←→ series)**
- **Vertices are nodes (signals) of circuit, VDD, X, GND; Edges are transistors**

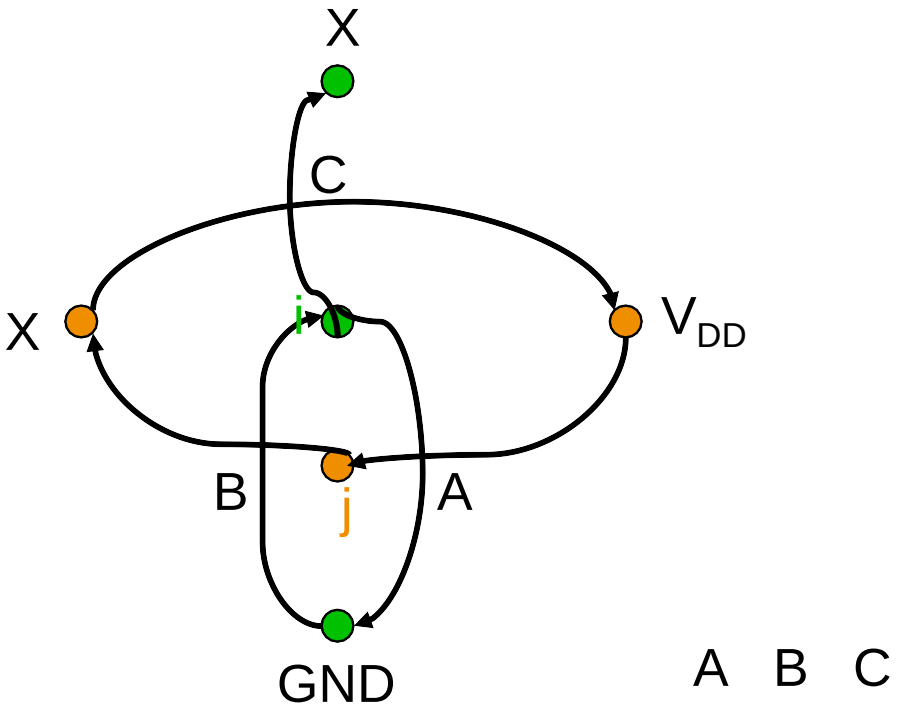
Two Possibilities



- **Line of diffusion layout – abutting source-drain connections**
- **Crossover eliminated by A B C ordering**

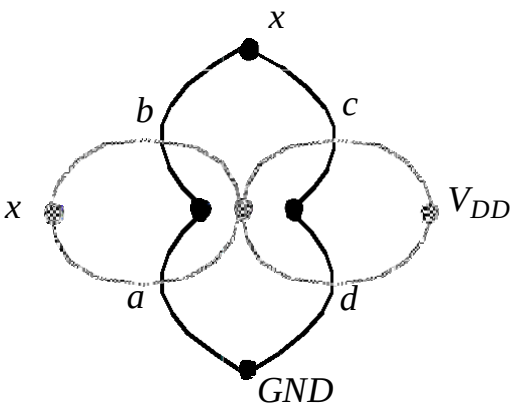
Consistent Euler Trail

- A B C
- C A B
- B C A → no PD
- B A C
- A C B → no PD
- C B A

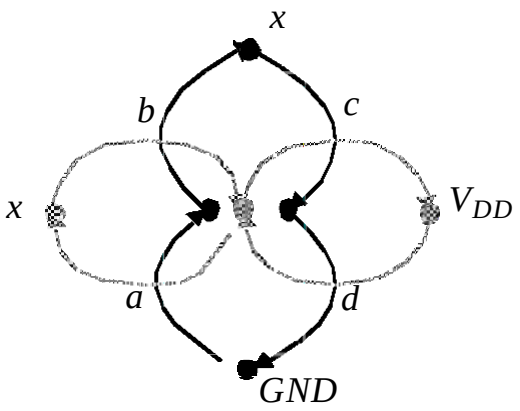


- A path through all nodes in the graph such that each edge is visited once and only once.
- The sequence of signals on the path is the signal ordering for the inputs.
- PU and PD Euler paths are (must be) consistent (same sequence)
- If you can define a Euler path then you can generate a layout with no diffusion breaks

Example 2: AOI22 x = (ab+cd)'

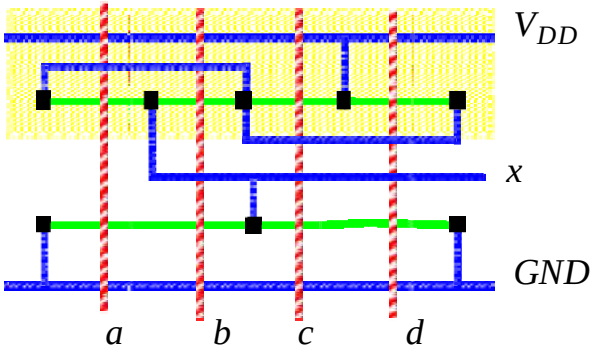


(a) Logic graphs for $\overline{(ab+cd)}$



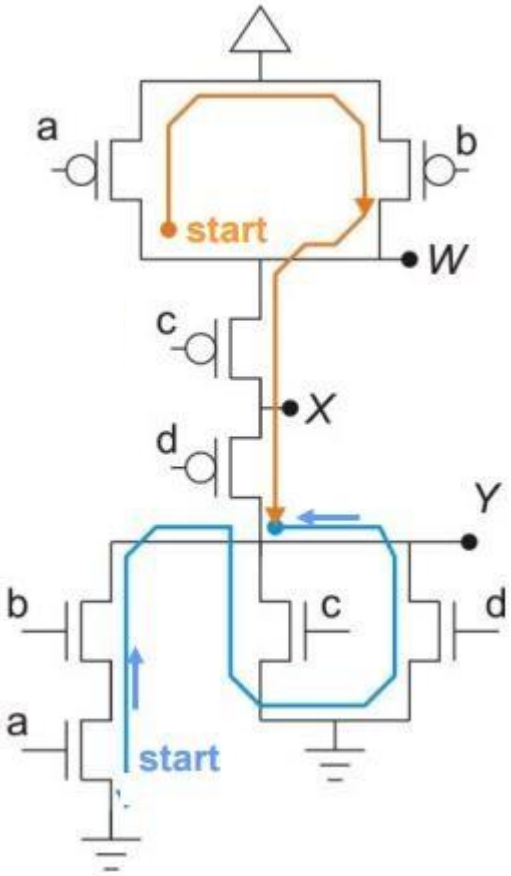
(b) Euler Paths {*a b c d*}

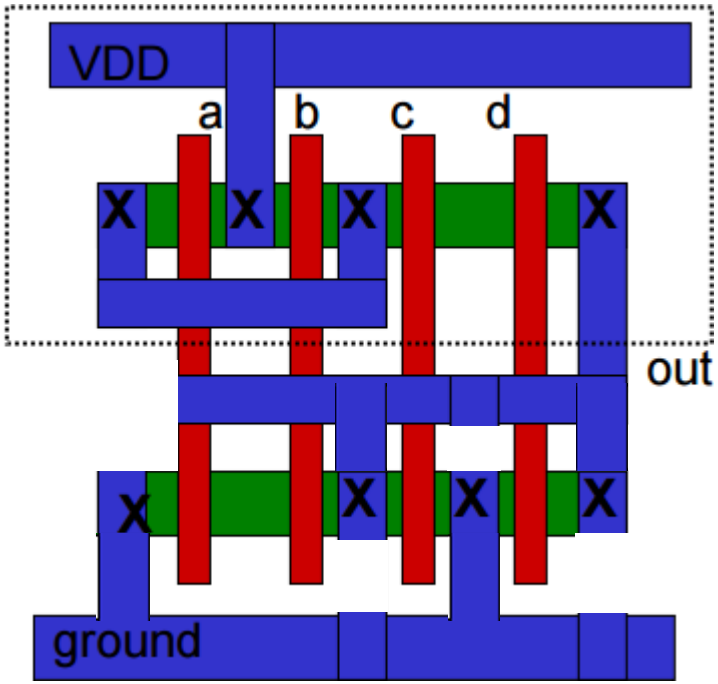
Circuit Diagram



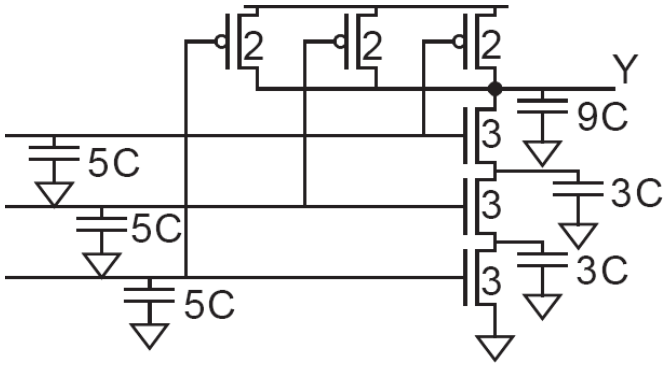
(c) stick diagram for ordering {a *b c d*}

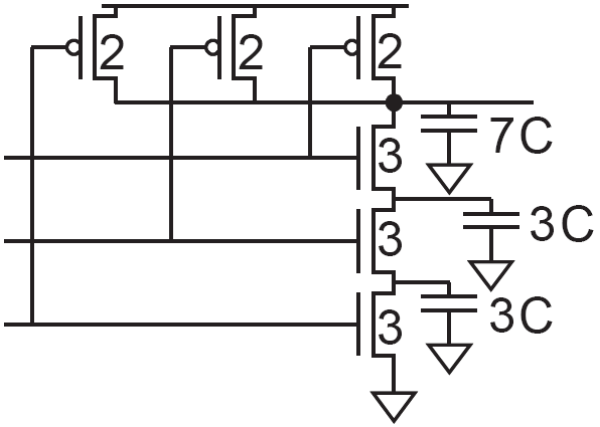
Example 3: Y = (ab+c+d)'

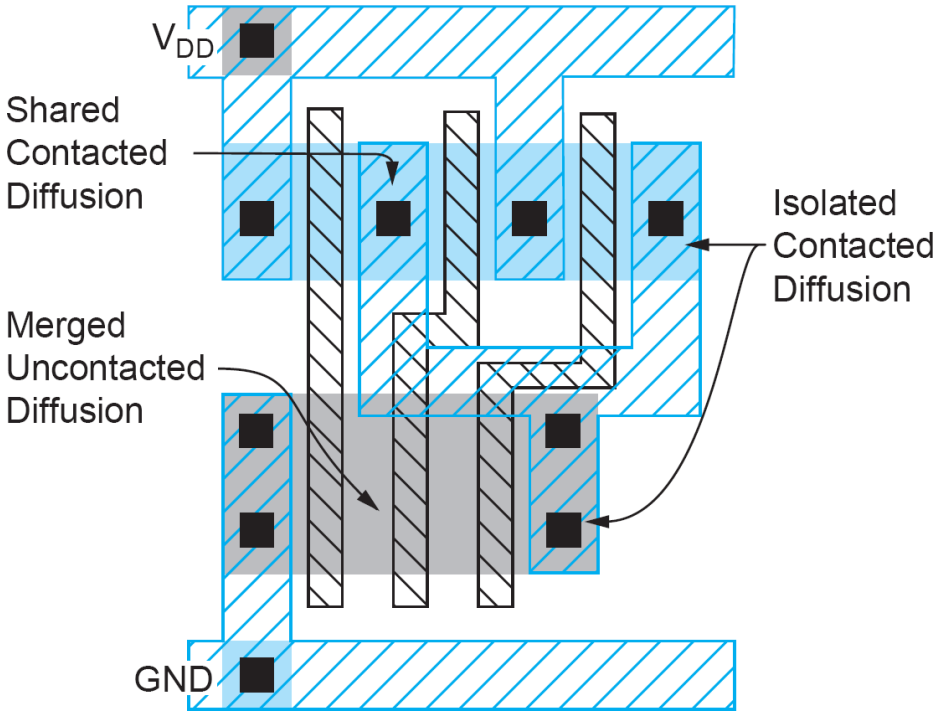




NAND3 with Good Layout







Actual diffusion cap on the output is 7C, instead of 9C

Example 4 and Key Solution

Out' = a(d+e) + bc