Project #2(6)

Due Thursday Oct 3rd, 11:59 PM Email to elec402project@gmail.com - No Exceptions (no late submissions)

Synthesized Verilog Project

Introduction:
For this project, you will use Cadence Encounter RTL Compiler to generate a mapped netlist based on the library of cells which we have provided. After running the Compiler, you will have a better idea of the complexity of your design as well as an exact cell count. This project will also give you a good idea of what cells you will be creating for your own library.

Project Description/Requirements:

- Setup Cadence account and work through the tutorial.
- From the tutorial, you will open your Verilog code and create a netlist based on the library that we have provided.
- Print out the report generated by RTL Compiler showing the total number of cells used for the FSM.
- Using the mapped Verilog and SDF, test the code with ModelSim and obtain graphical waves of the mapped Verilog.
- Compare with your Verilog and verify that both are functioning similarly.

Note: It is a requirement that your design has a minimum of 100 cells. If it is below 100 cells, then at most 20 points will be lost. Only a few points will be deducted if it slightly less than 100 cells.

Report Layout (Single PDF)

1. Name, student number and project title on the first page of your project report
2. Mapped Verilog generated by RTL Compiler. [10]
3. Visual Waveforms showing state transitions from mapped Verilog. [40]
4. Report from RTL Compiler showing total number of cells in the project [50]
5. If you have changed designs completely, you will also need to turn in your Verilog code for the new FSM along with a description and new waveforms.

FAQ:
You will find these resources