Project 4 - NAND3 Simulation & Layout

Width = $0.875\,\mu$m, Length = $2.085\,\mu$m
Area = $1.8244\,\mu\text{m}^2$ Delay = $59.3223\,\text{ps}$
Area * Delay = 108.226

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1 MAIN PORTION: NAND3 Simulation & Layout

1.1 NAND3 Gate Design and Layout

1.1.1 Gate Design

The first thing for the gate design is to make the schematic for the gate. For a NAND gate, the pull down network is a set of 3 series NMOS transistors, and for the pull up network is a set of 3 parallel NMOS transistors. The inputs are labelled simply as A, B and C. Below is the schematic done in Cadence.

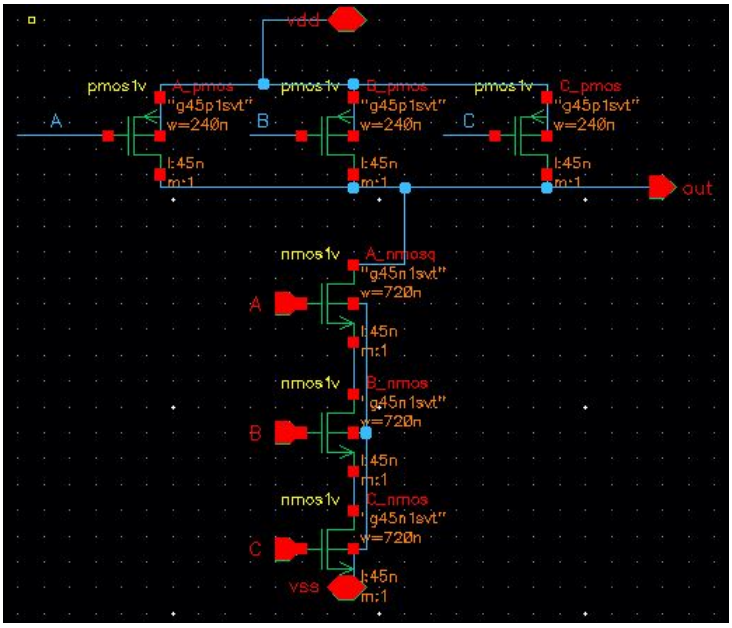

Figure 1: Schematic for the NAND3 Gate

For sizing, we initialy sized to an ideal inverter, with PMOS at 2W and NMOS at 3W. This ratio yielded a t_{pHL} that was too large compared to t_{pLH}, so the NMOS width needed to be adjusted. Eventually the best case was 6W for the NMOS.

1.1.2 Gate Layout

Below is the image of the layout for the NAND3 Gate.

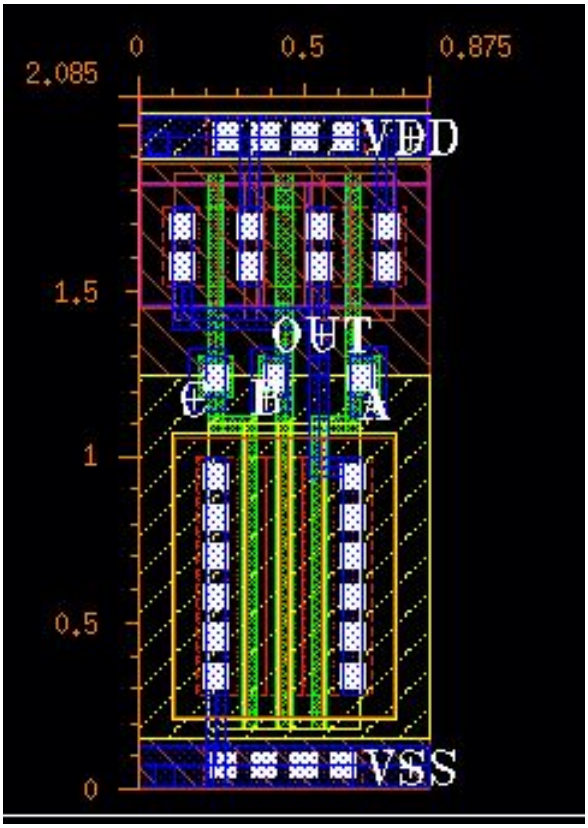

Figure 2: Layout for the NAND3 Gate

The dimensions and area of the layout are thus shown in the table below

Width	Length	Area
$0.875\,\mu$m	$2.085\,\mu$m	$1.8244\,\mu\text{m}^2$

Table 1: Dimensions of the NAND3 Gate

1.2 t_{pHL} and t_{pLH} of the gate

After extracting parasitics of the gate using PVS-QRC, the gate was simulated to find the delay. The result is shown in the figure below.

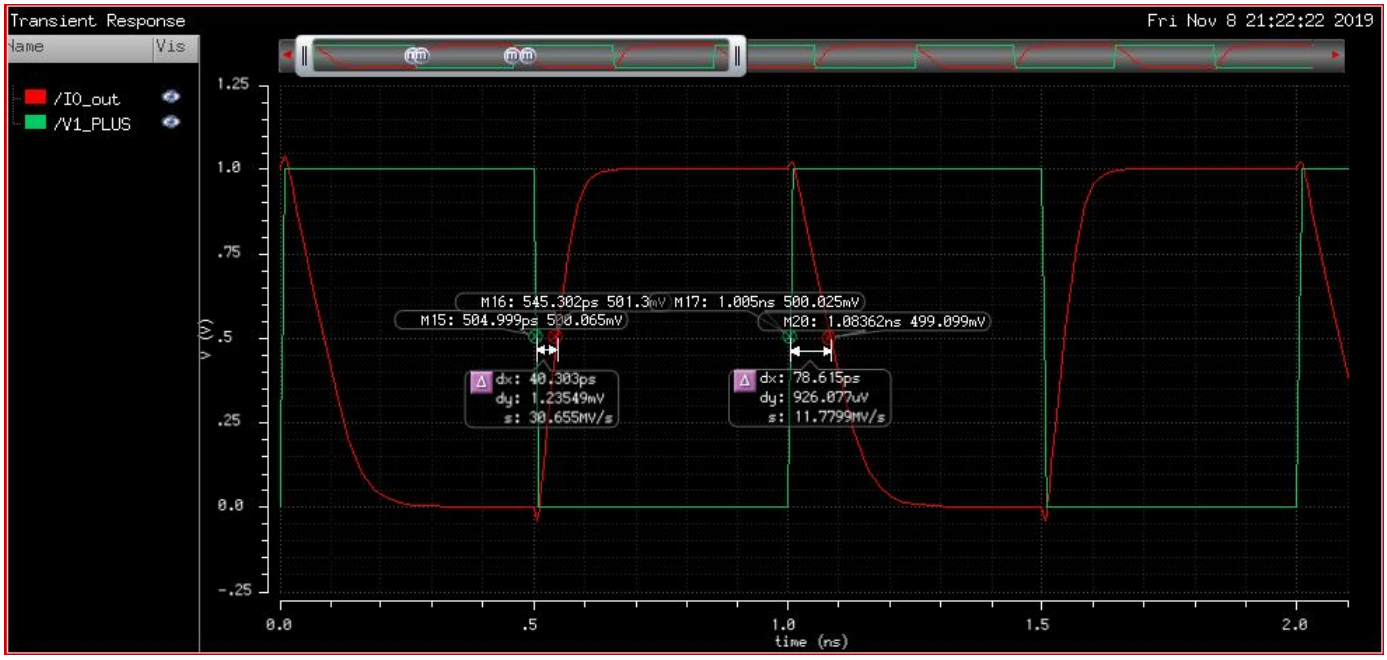

Figure 3: Delay Waveform for the NAND3 Gate

The delay values are thus shown in table below.

t_{pLH}	t_{pHL}	t_{pd}
40.3030 ps	78.615 ps	59.3223 ps

Table 2: Delay values of the NAND3 Gate

I was unable to get the time difference between 5ps, have redone my layout 30-40 times over the course of two weeks.

1.3 Worst-case delay

Analyzing the nature of the circuit, the worst case delay occurs with the following switching pattern.

$$ABC = 110 \rightarrow ABC = 111$$

The worst case occurs when the A and B NMOS are charged, and then C is switched on. This requires the pull down network to fully discharge the stored capacitance in A and B to pull the output fully down to logic 0.

1.4 Parasitics

Below is the original NAN3 schematic with the new parasitics included.

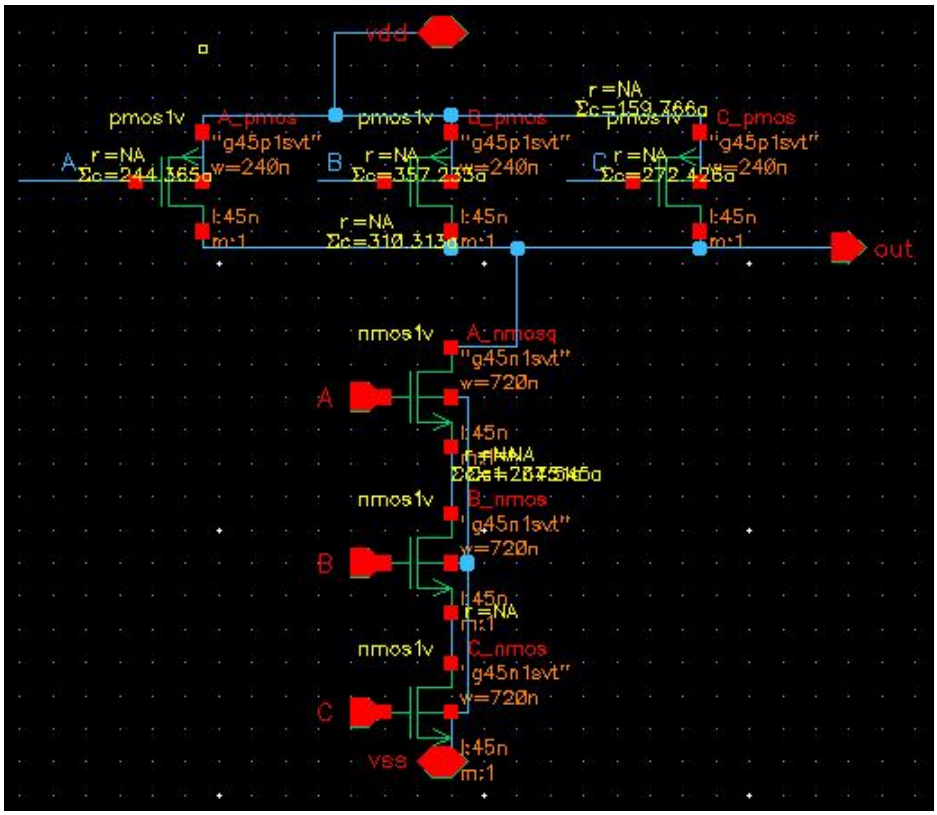

Figure 4: Schematic with parasitics for the NAND3 Gate

For clarity, the list of parasitics of all nets are shown below.

All Parasitics for NAND3_q1_Project4

Report: decoupled C coupled C self C

NetName	R	sum C	sum L
/vss	NA	234.545a	0
/vdd	NA	159.766a	0
/out	NA	310.313a	0
/C_nmos_D	NA	0	0
/C	NA	272.426a	0
/B_nmos_D	NA	1.26751a	0
/B	NA	357.233a	0
/A	NA	244.365a	0

Figure 5: Parasitics of all nets of the NAND3 Gate

1.5 Inclusion of the 10fF load capacitor

Below is the testbench circuit used to simulate the NAND3 Gate. As required in the assignment, the output is connected to a 10 fF capacitor.

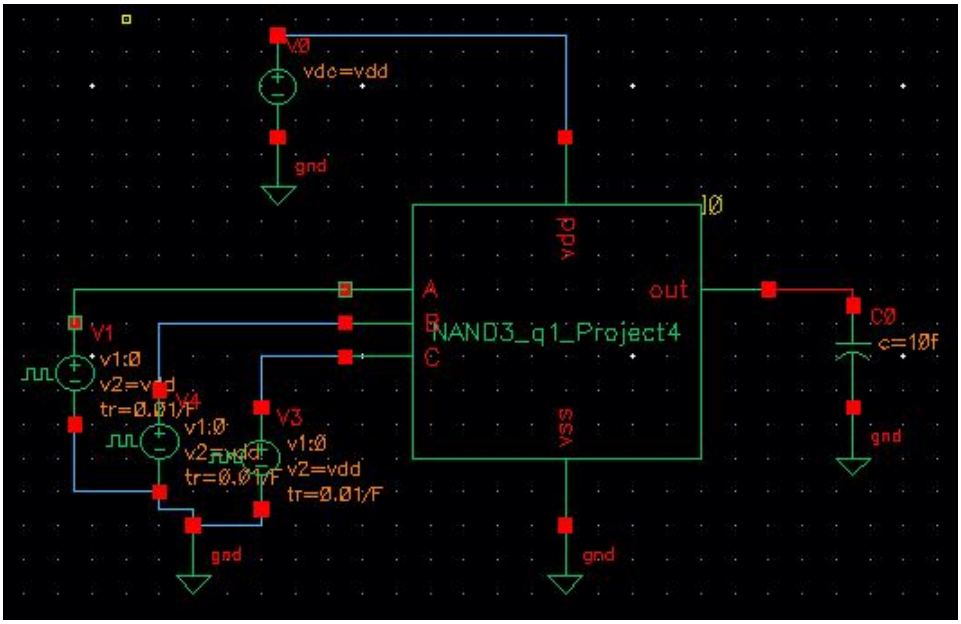

Figure 6: Parasitics of all nets of the NAND3 Gate

2 Examining the Unknown Circuit

2.1 Logic Function of the Block

To obtain the Boolean expression of the circuit, we look at the pull-down NMOS network to get the dual expression. Parallel transistors are OR, and series transistos are AND. To find the original boolean expression we simply take the dual of the dual function

$$\overline{Y} = (A + B)CD$$

$$\overline{\overline{Y}} = \overline{(A + B)CD}$$

$$Y = \overline{A + B} + \overline{C} + \overline{D}$$

$$Y = \overline{AB} + \overline{C} + \overline{D}$$

2.2 Sizing the gates

To size the gates we simply need to examine the branches of both the pull-up and pull-down networks. Parallel connections can apply symmetry properties.

	NMOS W/L	PMOS W/L
A	12λ	16λ
B	12λ	16λ
C	12λ	8λ
D	12λ	8λ

Table 3: Sizings of the Unknown circuits W/L

2.3 Worst case input patterns

For t_{pHL} we want to examine the NMOS network as it is the one that pulls the output from high to low. We want to find the case where it will take the longeset for all NMOS transistors to discharge any capacitance. The input pattern is shown below

$$ABCD = 1110 \rightarrow ABCD = 1111$$

If ABC are all on initially, their capacitance is fully charged and turning on the D NMOS will require the pull-down network to discharge 3 transistors worth of capacitance.

For t_{pLH} we want to examine the PMOS network as it is the one that pulls the output from low to high. We want to find the case where it will take the longest for all PMOS transistors to charge up capacitance. The input pattern is shown below

$$ABCD = 1111 \rightarrow ABCD = 0011$$

C and D must off initially; the only case for a longer charge time would be with the A and B PMOS. If A and B are intially turned off and then turned on, V_{DD} will need to charge up 2 transistors worth of capcaitance.

2.3.1 Cadence Simulation Verification

Below is the schematic for the circuit made in cadence.

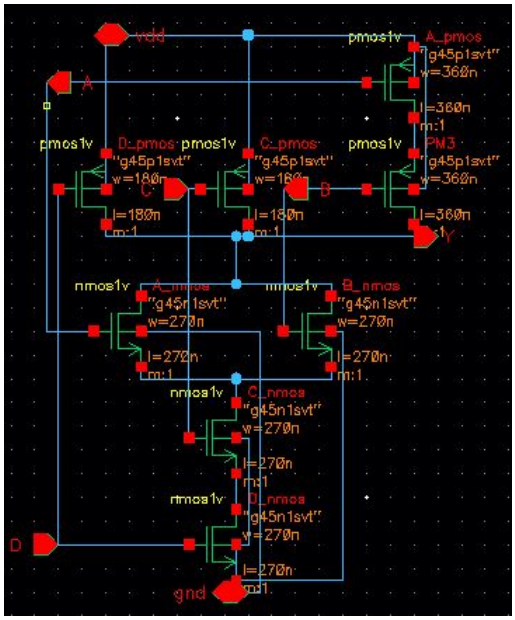

Figure 7: Schematic for the unknown circuit

To simulate the t_{pHL}, the inputs that don't switch use a vdc source as an input, and for the inputs that do switch, we use a vpulse source. The simulation schematic for t_{pHL} is shown below

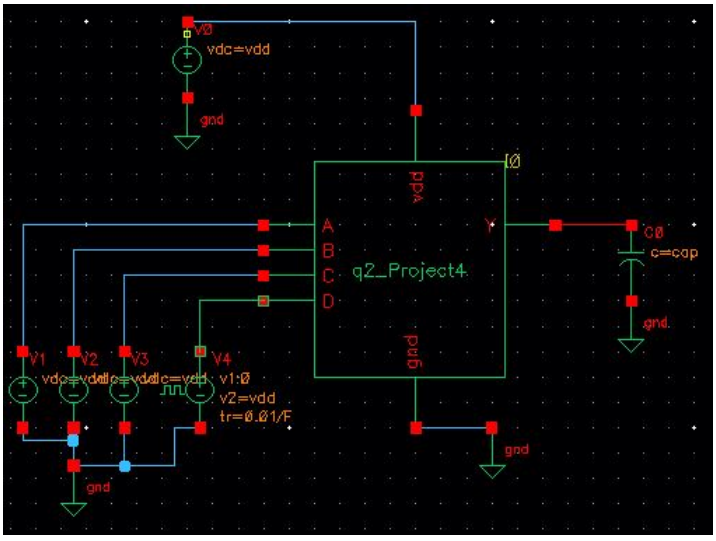

Figure 8: Schematic for t_{pHL} of the unknown circuit

Below is the resulting waveform from simulation.

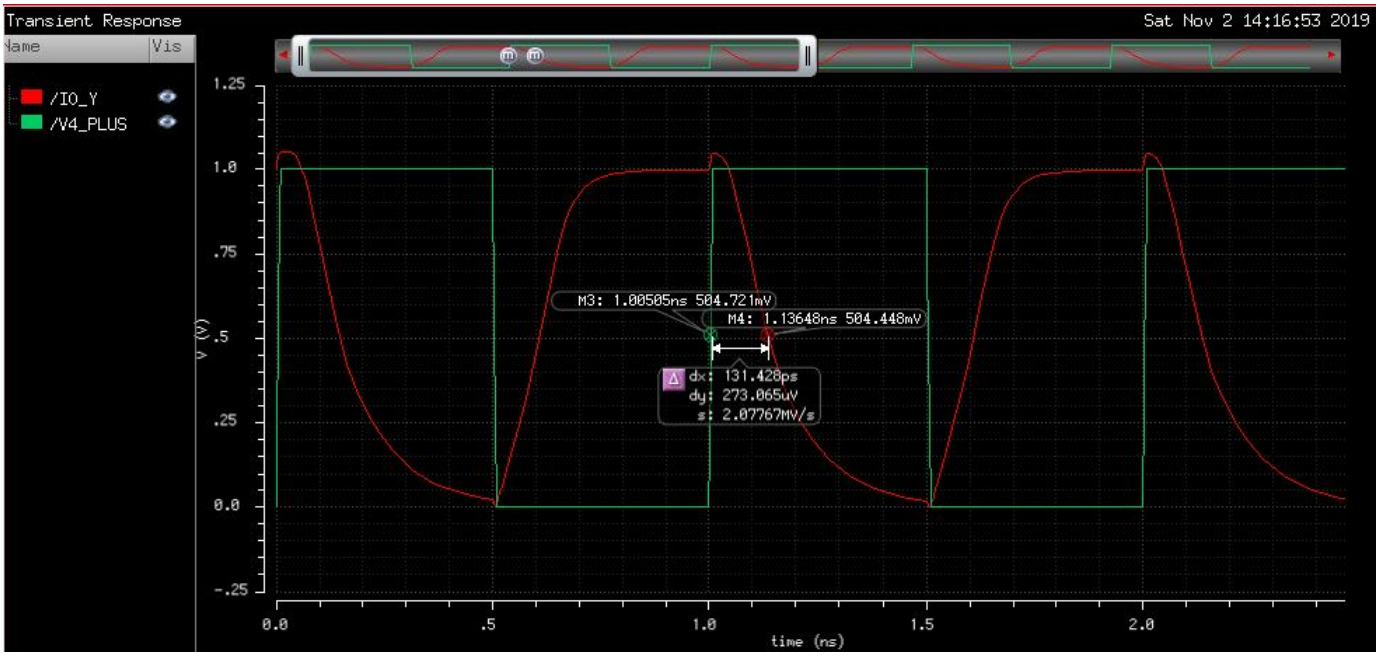

Figure 9: Waveform for t_{pHL} of the unknown circuit

To simulate the t_{pLH}, the inputs that don't switch use a vdc source as an input, and for the inputs that do switch, we use a vpulse source. The simulation schematic for t_{pLH} is shown below

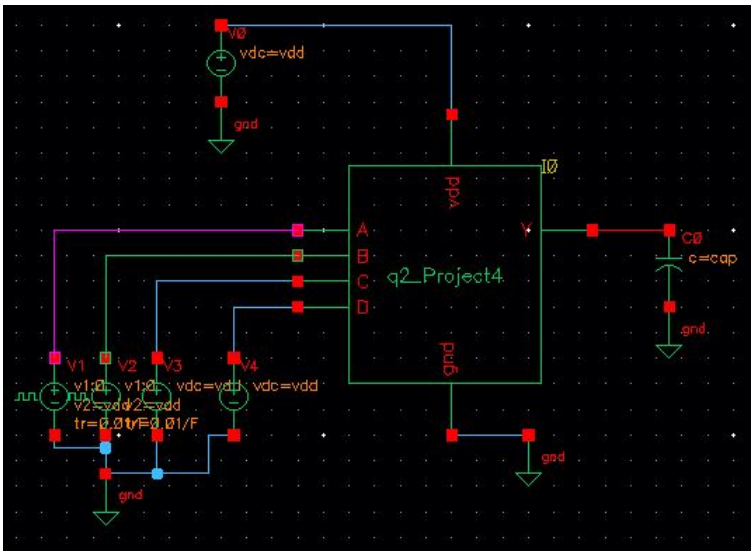

Figure 10: Schematic for t_{pLH} of the unknown circuit

Below is the resulting waveform from simulation.

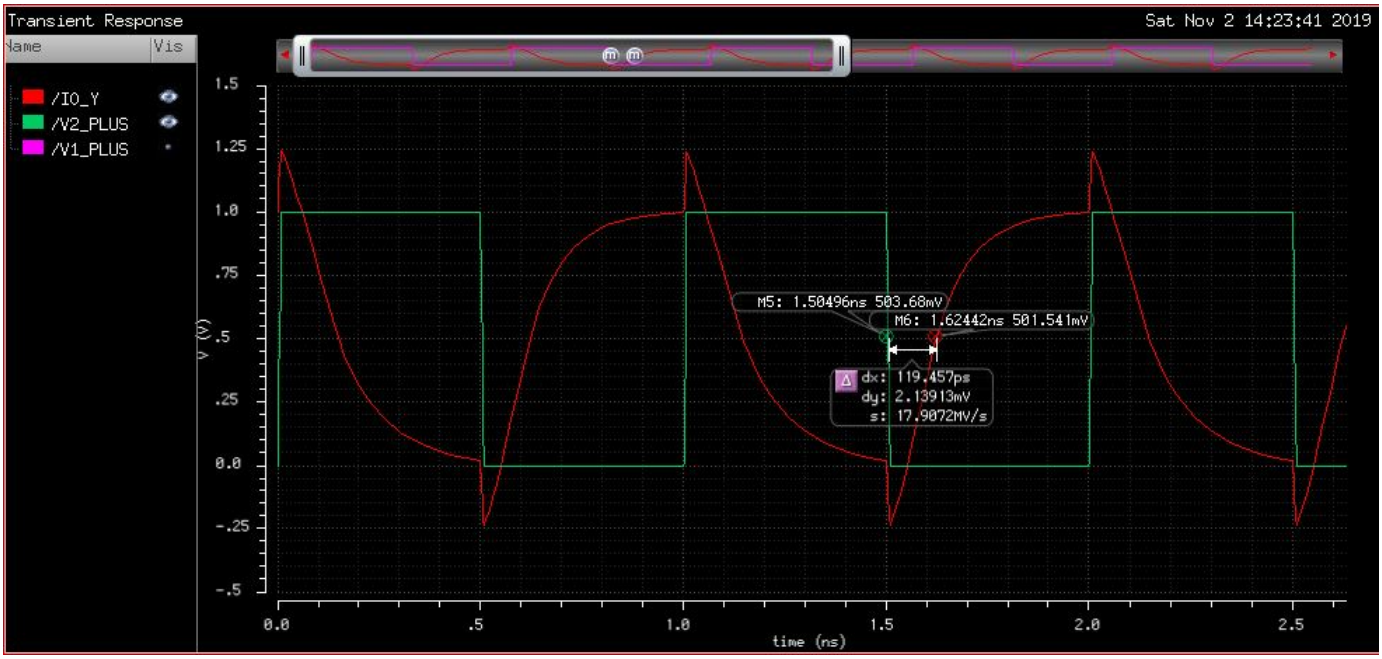

Figure 11: Waveform for t_{pLH} of the unknown circuit

The values of t_{pHL} and t_{pLH} are shown in the table below, based on the measured values from the waveforms.

t_{pHL}	t_{pLH}
131.428ps	119.457ps

Table 4: t_{pHL} and t_{pLH} values of the unknown circuit

3 Examining Figure 1

3.1 Output Function Expression

From the schematic we can see that the transmission gate only passes A when sel is high, and only passes B when selB is high. Thus the output funciton of the schematic is.

$$OUT = Bselb + A\overline{selb}$$

3.2 Equivalent RC circuit model

Below is the image of the equivalent RC circuit model for the path from A to C.

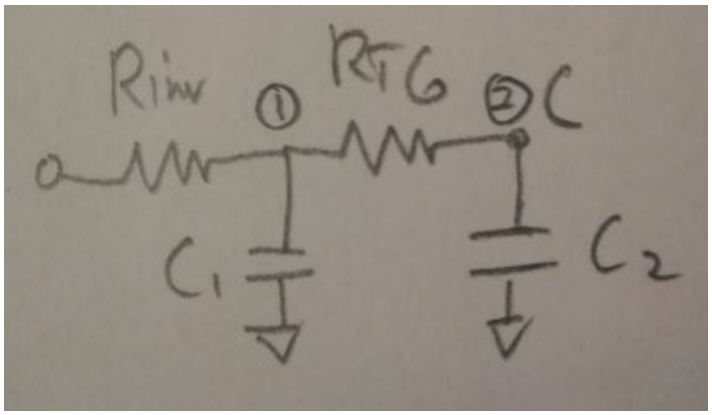

Figure 12: Equivalent RC circuit of Figure 1

There are three main nodes in the circuit path of A to C: the input node(A), the intermediate node between the input inverter and transmission gate(①), and the node between the transmission gate and the output inverter (C or ②). The contributions at each node are given by the table below.

	Node ①	Node ②
Resistance	R_{inv}	$R_{inv} + R_{TG}$
Capaitance	C_1	C_2

Table 5: Resistance and Capacitance contirbutions for the AC path

3.3 Delay expression from A to C

From the theory described in class, we note that we can approximate R_{inv} and R_{TG} to use the value of R_{eqn} for an NMOS. The capcitances C_1 and C_2 have contributions from either input/output devices at the node. They are described in the table below.

	Node ① - C_1	Node ② - C_2
General	$C_{eff-inv} + C_{g-TG} + C_{eff-TG}$	$C_{g-TG} + 2 * C_{eff-TG} + C_{g-inv}$
Numerical Expression	$3C_{eff}W + C_gW + 2C_{eff}W$	$C_gW + 2C_{eff}W + 3C_{eff}W$

Table 6: Capactiance expressions for the RC circuit model of the AC path

Using Elmore delay, the expression for the delay from A to C is given by

$$t_{AC} = R_{inv}C_1 + (R_{inv} + R_{TG})C_2$$

Substituting in the previous declared values and simplifying yields the delay expression

$$t_{AC} = R(13C_{eff}W + 3C_gW + 6C_gfW)$$

where $R = R_{eqn}\frac{L}{W}$

3.4 Delay expression through the output

For the output inverter, we keep the value of R but the capcitance is different. The delay through the output includes C_{eff} of the inverter and the load capacitance $C_{load]}$. This inverter is sized differently, with the multiplier of f. The value f reduces the overall resistance becuase of its effect on the width and increases C_{eff}.

$$R \to \frac{R}{f} \quad and \quad C = 3C_{eff}fW + 50\,\text{fF}$$

Becuase we are taking the RC delay, we take into account that the output inverter expects a step input in the most ideal case, so we need to include the $ln2@$ value in the expression.

$$t_{out} = 0.69\frac{R}{f}(3C_{eff}fW + 50\,\text{fF})$$

3.5 Determining optimal size of the output inverter

The total delay from A to OUT is thus.

$$t_{total} = t_{AC} + t_{OUT}$$

$$t_{total} = R(13C_{eff}W + 3C_gW + 6C_gfW) + 0.69\frac{R}{f}(3C_{eff}fW + 50\,\text{fF})$$

In order to minimize t_{total} with respect to f, we can take the derivative with repsect to f and equate to zero.

$$\frac{dt_{total}}{df} = 6RC_gW - \frac{R * 0.69 * 50\,\text{fF}}{f^2} = 0$$

Solving for f

$$f = \sqrt{\frac{0.69 * 50\,\text{fF}}{6C_gW}}$$

Taking the value of $C_g = 2\,\text{fF}/\mu\text{m}$ and $W = W_n = 0.4\,\mu\text{m}$, the value of f is.

$$f = 2.68 \sim 3$$