# ELEC 402

# Design of CMOS Inverter

## (Noise-margin-centric approach)

## Lecture 7

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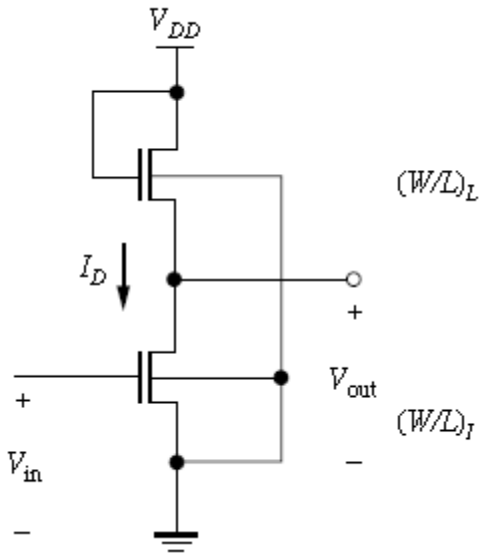
# Saturated-enhancement-load Inverter




To alleviate the area problem we replace the resistor

With a diode-connected transistor (always in saturation)

This performance of this logic gate is affected by the ratio

Of devices, hence called *ratioed* inverter

$$K_R = \frac{k_{\text{invert}}}{k_{\text{load}}} = \frac{k'(W/L)_I}{k'(W/L)_L} = \frac{(W/L)_I}{(W/L)_L}$$

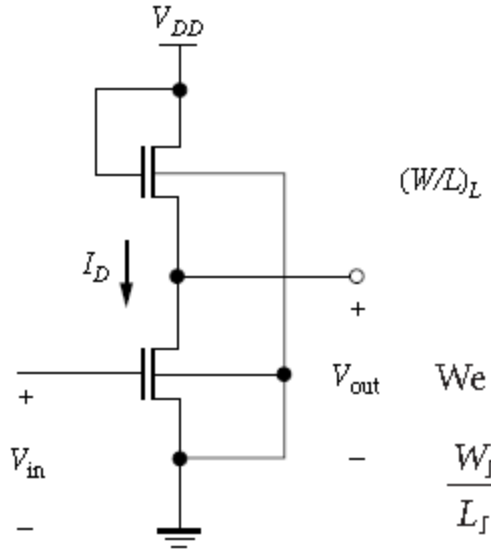
The output voltage does not quite reach $V_{DD}$

(The Load device requires at least VT drop on its $V_{GS}$ )

$$V_{OH} = V_{DD} - V_T(V_{OH})$$

$$= V_{DD} - [V_{T0} + \gamma(\sqrt{V_{OH} + 2|\phi_F|} - \sqrt{2|\phi_F|})]$$

# Saturated-enhancement-load Inverter – cont'd




To derive the $V_{OL}$ again it is important to find the proper region of operation for each transistor

$$I_{DI}(\text{lin}) = I_{DL}(\text{sat})$$

We can substitute in the current equations to obtain

$$\frac{W_I}{L_I}\frac{\mu_n C_{ox}}{\left(1+\dfrac{V_{\text{out}}}{E_{CN}L_I}\right)}\left[(V_{in}-V_{TI})V_{\text{out}}-\frac{V_{\text{out}}^2}{2}\right]=\frac{W_L v_{sat} C_{ox}(V_{DD}-V_{\text{out}}-V_{TL})^2}{(V_{DD}-V_{\text{out}}-V_{TL})+E_{CN}L_L}$$

Note that $V_{in}$ should be the output of previous stage (ideally $V_{DD} – V_T$), however, to keep Things simple we occasionally assume $V_{in} = V_{DD}$

# Example – Why is it a *ratioed* logic gate

**Design of Saturated Load Inverter**

**Problem:**

Design the saturated enhancement load inverter of Figure 4.10a such that it delivers a low output voltage of $V_{OL} = 0.1$ V when the input is $V_{DD}$. Assume a 0.13 $\mu$m technology, with $L = 100$ nm and let the pull-up device be of unit size. Use the parameters

$$\mu_n = 270 \text{ cm}^2/\text{V-s}, \quad C_{ox} = 1.6 \ \mu\text{F/cm}^2, \quad V_{T0} = 0.4 \text{ V}, \quad V_{DD} = 1.2 \text{ V}$$

$$E_{CN}L = 0.6 \text{ V}, \quad v_{sat} = 8 \times 10^6 \text{ cm/s}, \quad \gamma = 0.2 \text{ V}^{1/2}$$

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Use the current equation for the pull-down in the linear region and the pull-up in the saturation region.

$$\frac{W_I}{L_I}\frac{\mu_n C_{ox}}{\left(1+\dfrac{V_{out}}{E_{CN}L_I}\right)}\left[(V_{in}-V_{TI})V_{out}-\frac{V_{out}^2}{2}\right]=\frac{W_L v_{sat}C_{ox}(V_{DD}-V_{out}-V_{TL})^2}{(V_{DD}-V_{out}-V_{TL})+E_{CN}L_L}$$

We can eliminate $C_{ox}$ and then set $V_{in} = V_{DD}$ (we should really set it to $V_{OH}$ but we keep things simple in this problem) and $V_{out} = V_{OL}$:

$$\therefore \frac{W_I}{L_I}\frac{\mu_n}{\left(1+\dfrac{V_{OL}}{E_{CN}L_I}\right)}\left[(V_{DD}-V_{TI})V_{OL}-\frac{V_{OL}^2}{2}\right]=\frac{W_L v_{sat}(V_{DD}-V_{OL}-V_{TL})^2}{(V_{DD}-V_{OL}-V_{TL})+E_{CN}L_L}$$

# Saturated-enhancement-load Inverter – cont'd

Since we know that the output voltage is $V_{OL} = 0.1$ V, we can compute the correct $V_{TL}$:

$$\begin{aligned} V_T &= [V_{TO} + \gamma(\sqrt{V_{SB} + 2|\phi_F|} - \sqrt{2|\phi_F|})] \\ &= [0.4 + 0.2(\sqrt{0.1 + 2|-0.44|} - \sqrt{2|-0.44|})] \\ &= 0.4 + 0.2\left(\sqrt{0.1 + 0.88} - \sqrt{0.88}\right) \\ &= 0.41 \text{ V} \end{aligned}$$

The degree of body effect is small, as one would expect with a body-bias of 0.1 V. We can substitute the known quantities and solve for the transistor sizes:

$$\therefore \frac{W_I}{0.1(10^{-4})\text{cm}} \frac{(270 \text{ cm}^2/\text{V-s})}{\left(1 + (0.1/0.6)\right)} \left[(1.2 - 0.4)0.1 - \frac{0.1^2}{2}\right]$$

$$= \frac{W_L(8 \times 10^6 \text{ cm/s})(1.2 - 0.1 - 0.41)^2}{(1.2 - 0.1 - 0.41) + 0.6}$$

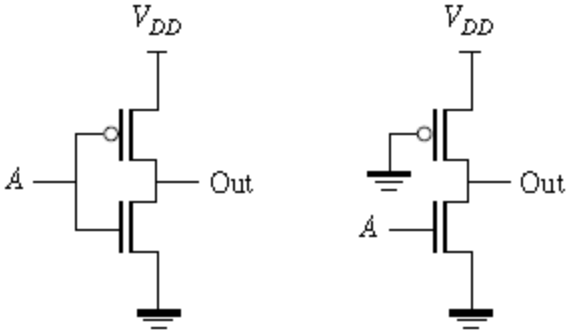
$$\therefore K_R = \frac{W_I}{W_L} = \frac{2.95}{1.75} = 1.7$$

If $W_L = 100$ nm, then $W_I = 170$ nm.

# Pseudo-NMOS Inverter

To address issues with NMOS loads

- Saturated NMOS load, a.k.a diode connected load, has degraded $V_{OH}$
- Linear NMOS load requires two supplies and extra area/interconnects
- CMOS gates require multiple loads for multi fanin inputs (?)




Solves the abovementioned problems, However

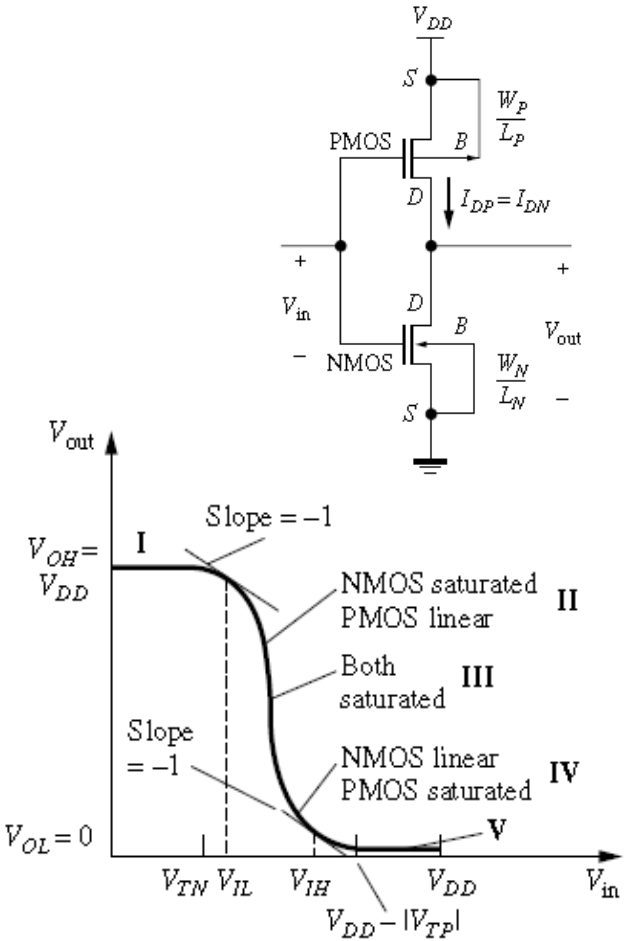
-*Ratioed* inverter, i.e. $V_{OL}$ a function of two device ratios

- Large $T_{PLH}$ (why?)

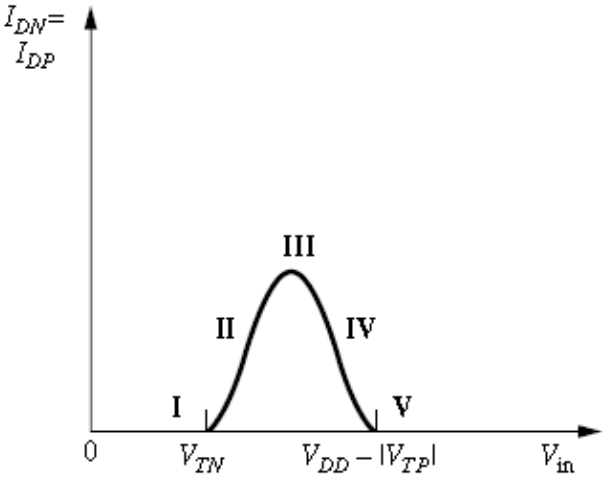
$$I_{DP}(\text{sat}) = I_{DN}(\text{lin})$$

$$\frac{W_P v_{sat} C_{ox}(V_{DD} - |V_{TP}|)^2}{(V_{DD} - |V_{TP}|) + E_{CP}L_P} = \frac{W_N}{L_N}\frac{\mu_n C_{ox}}{\left(1 + \frac{V_{OL}}{E_{CN}L_N}\right)}\left[(V_{DD} - V_{TN})(V_{OL}) - \frac{(V_{OL})^2}{2}\right] \Rightarrow V_{OL} = \frac{I_{DP}(\text{sat})}{k_N(V_{DD} - V_{TN})}$$

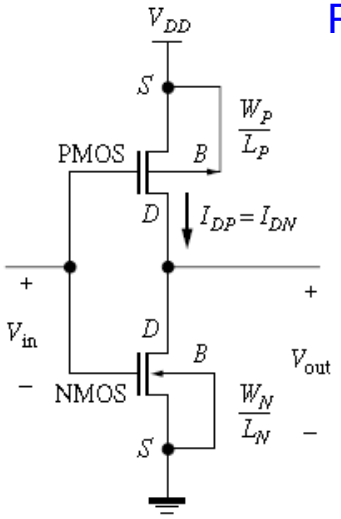
# CMOS Inverter




- Address both issues of area and static power consumption
- Load that is complementary to the inverting device
- 5 distinct regions of operation can be detected



# CMOS Inverter




Region III: NMOS saturation, PMOS saturation

$V_s$ falls in this region (why?)

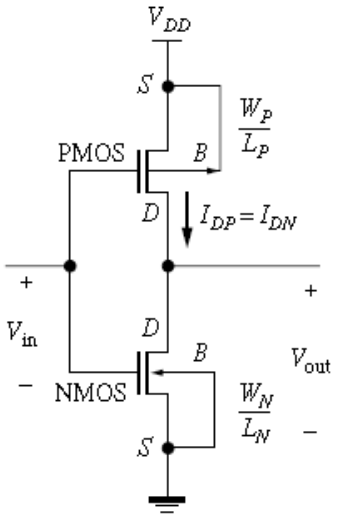
$$\frac{W_N \upsilon_{sat} C_{ox}(V_S - V_{TN})^2}{(V_S - V_{TN}) + E_{CN} L_N} = \frac{W_P \upsilon_{sat} C_{ox}(V_{DD} - V_S - |V_{TP}|)^2}{(V_{DD} - V_S - |V_{TP}|) + E_{CP} L_P}$$

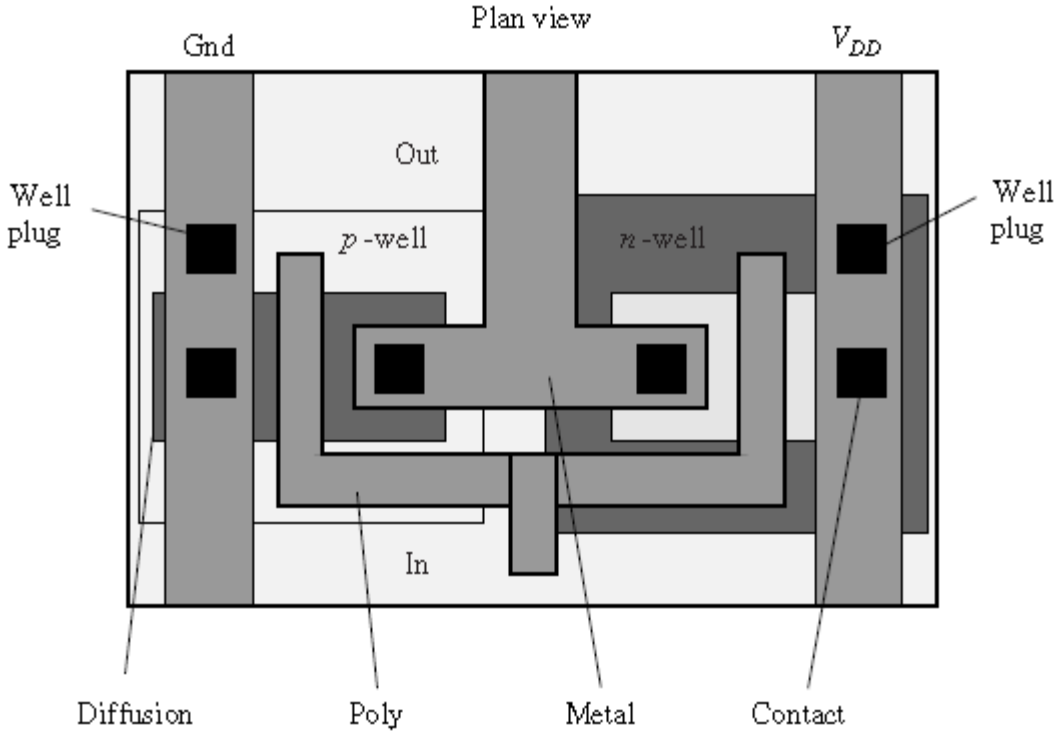
(Board Notes)

$$V_S = \frac{V_{DD} - |V_{TP}| + \chi V_{TN}}{1 + \chi}$$

$$\chi = \sqrt{\frac{\frac{W_N}{E_{CN} L_N}}{\frac{W_P}{E_{CP} L_P}}} = \sqrt{\frac{\mu_n W_N}{\mu_p W_P}}$$

# CMOS Inverter - Layout




Note Minimum size, well-plugs, design rules