ELEC 402

MOS Basics
Lecture 4

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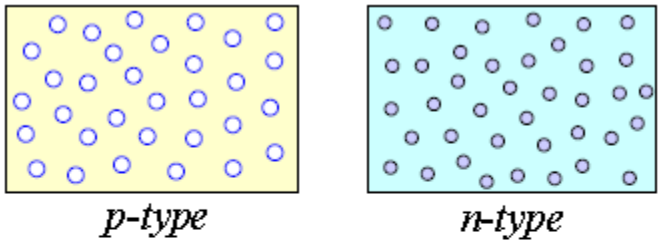
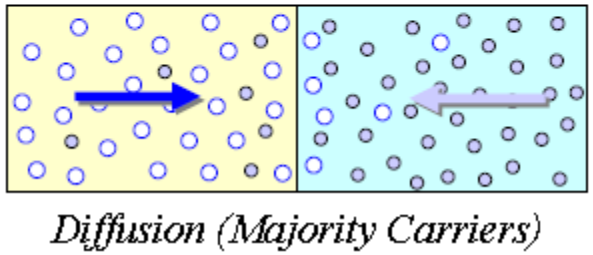
PN Junction and Diodes

p-type semi-conductor heavily doped with acceptor atoms, e.g. boron



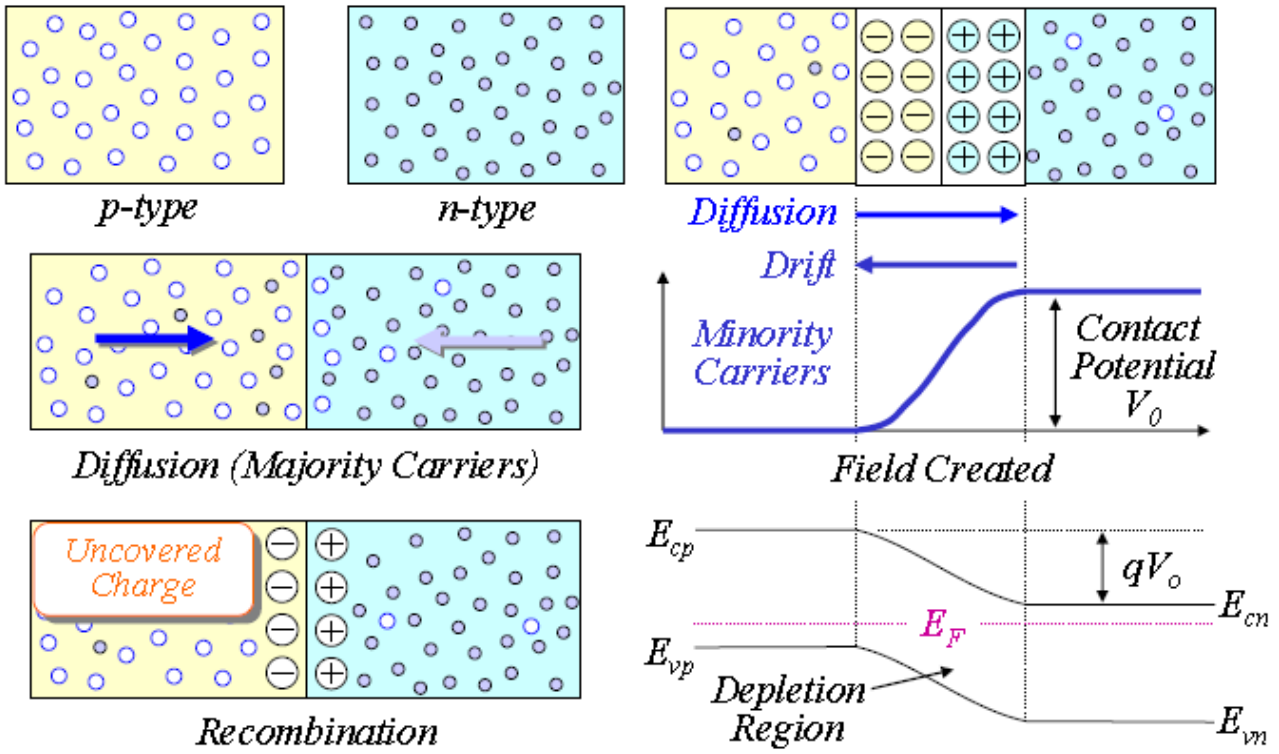
n-type semi-conductor is heavily doped with donor atoms, e.g. arsenic and phosphorus

PN Junction



- The concentration of different carrier in p, and n-type semi-conductors (also called gradient) causes diffusion of electrons from *n* to *p* and holes from *p* to *n* leaving immobile ions behind
- The region at junction where majority carriers are removed, is called the *depletion* or *space-charge region*

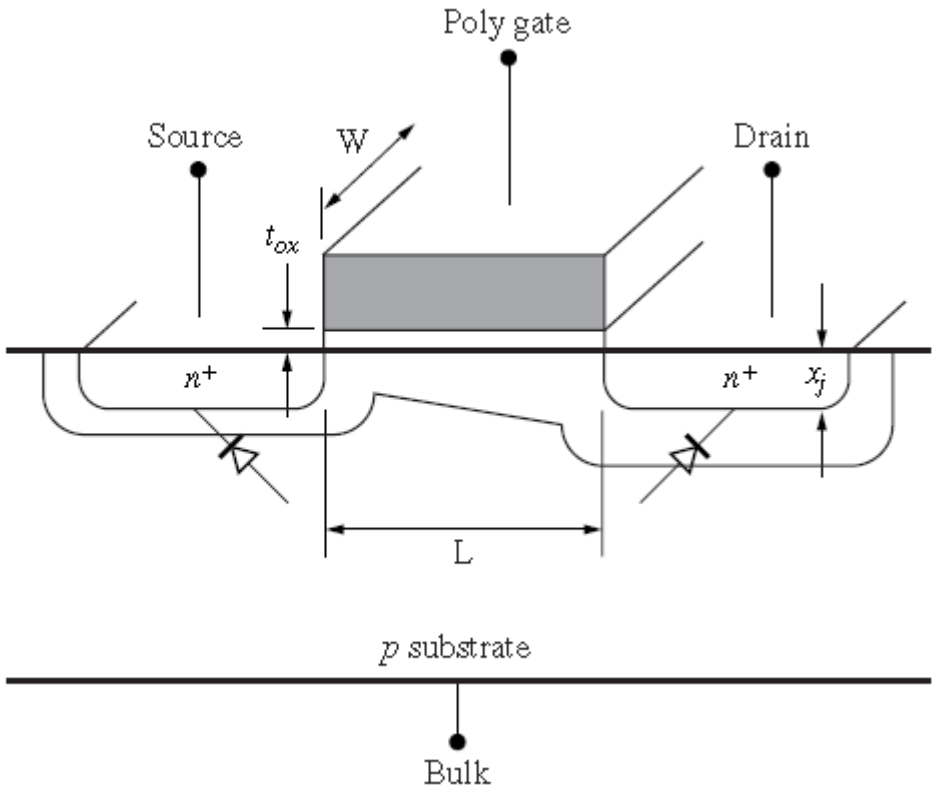
PN Junction Basics

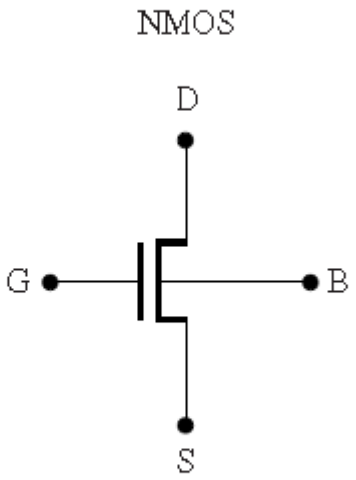


- The charges in each region create an electric field across the boundary of junction to counteract the diffusion of majority carriers

-This electric field creates a potential across the junction called *contact* or *barrier potential*

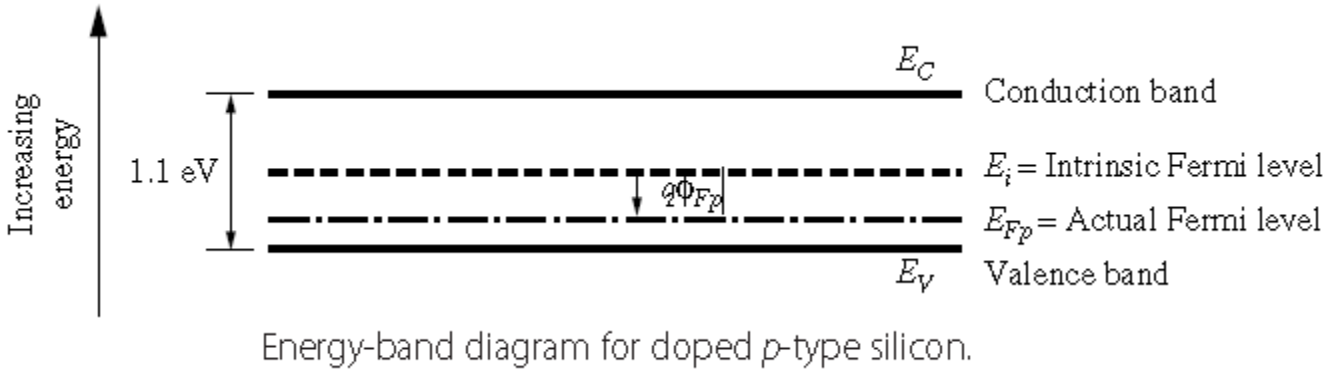
MOS Transistor Basics





The source and drain regions (*n*+) and substrate (*p*) in NMOS transistor create two back-to-back diodes at equilibrium (therefore, requires external stimulus for any conduction)

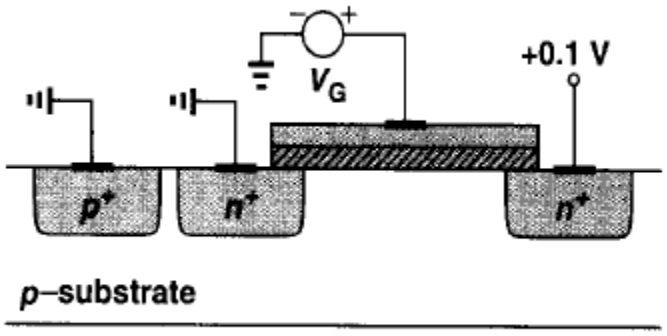
Definition of Threshold Voltage



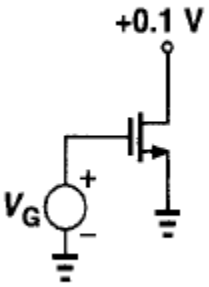
Energy-band diagram for doped *p*-type silicon.

- We need to apply an external voltage to turn the *p*-type substrate into an *n*-type substrate to create a channel for conduction
- As we apply a positive V_{GS} the substrate is first depleted under the gate area (immobile ions)
- Further increase of V_{GS} creates a conducting layer of minority carriers under the gate
- The V_{GS} voltage required to make the surface of the substrate "as much *n*-type as the rest of substrate is *p*" is called Threshold Voltage

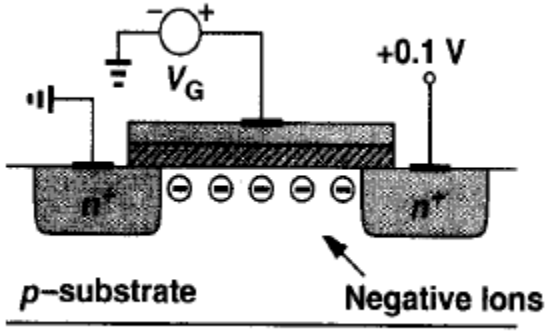
Definition of Threshold Voltage



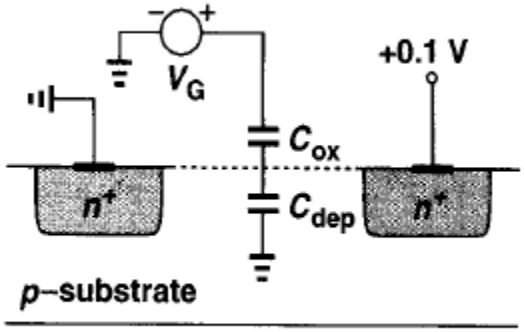
(a)



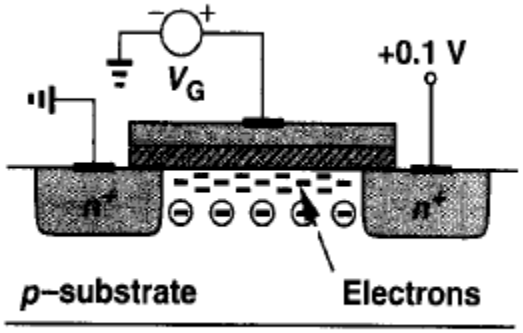
Small V_{GS}, no channel yet!



(b)



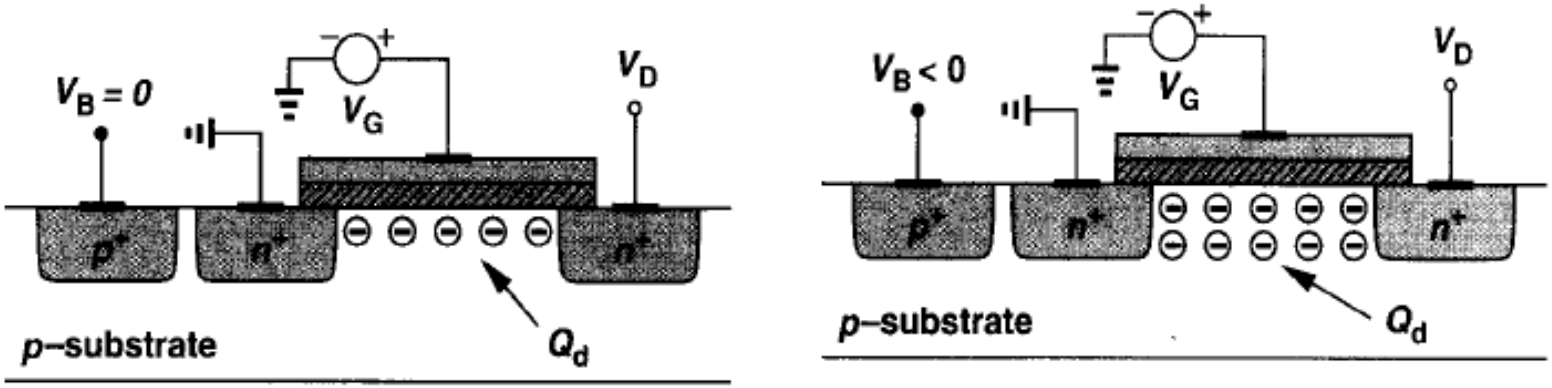
(c)



(d)

The onset of inversion in NMOS transistor (creation of channel under the gate in (d)

Effect of Body bias on Threshold Voltage

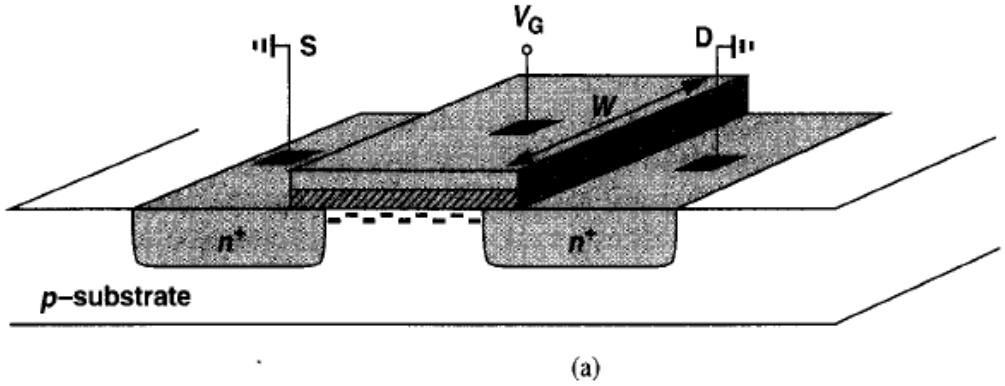


- Application of negative voltage to bulk attracts holes and leaves behind “negatively charged ions”
- As a result, there should be more positive charge on gate plate to mirror the negative ions in the substrate and more positive voltage is required to create the channel, i.e. V_{TH} increases

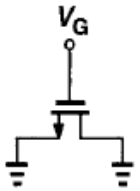
$$V_{T0} + \gamma\left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right)$$

where $\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{si}N_A}$ *body-effect coefficient*

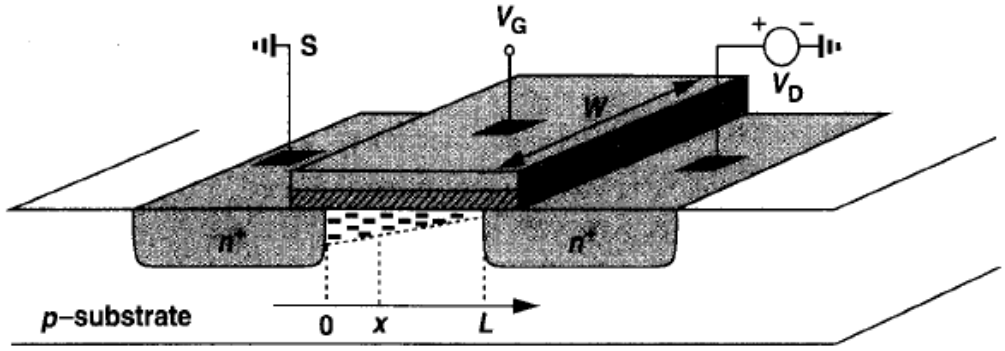
MOS Current Calculation



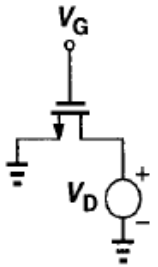
(a)



$V_{GS} > V_{th}$ channel created, no current yet!



(b)



$V_{DS} > 0$ carriers start flowing From source into the drain

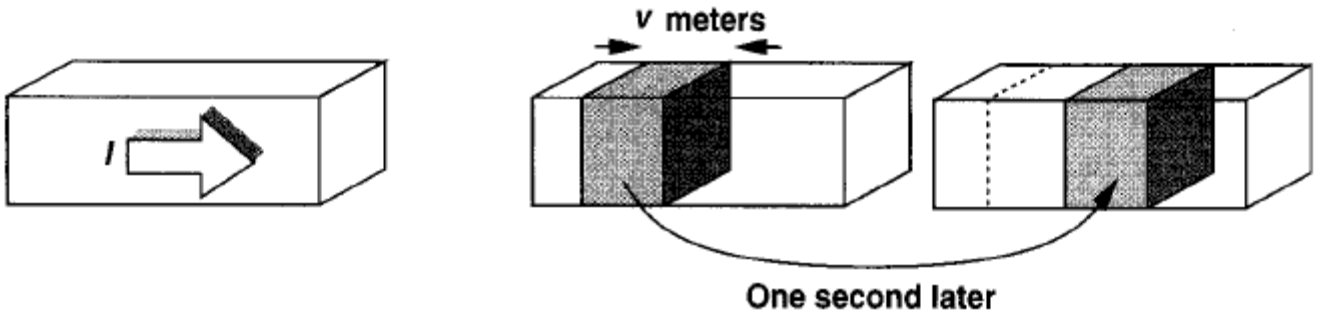
$$Q_n(y) = C_{ox}\left[V_{GS} - V(y) - V_T\right]$$

Charge per unit area

MOS Current Calculation

$$Q_d = W Q_n(y)$$

Charge density along direction of current



$$I = Q_d \cdot v.$$

Total charge in the grey box (amount of charge hat passes through the channel in 1 second)

$$v = \mu E \quad \text{where } E = \frac{dV(y)}{dy}$$

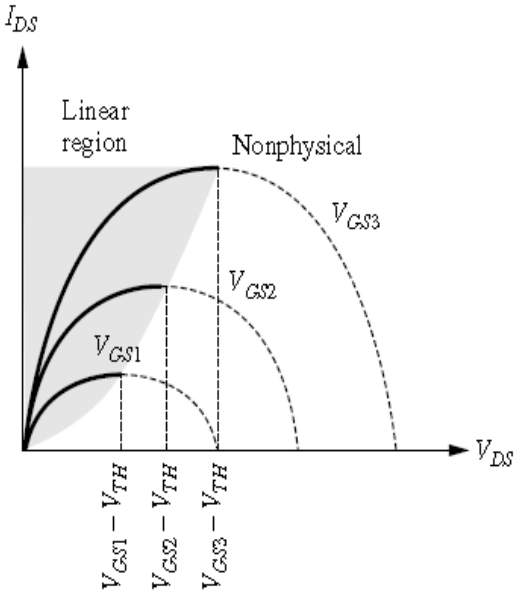
Velocity of carriers is a function of the horizontal electric field

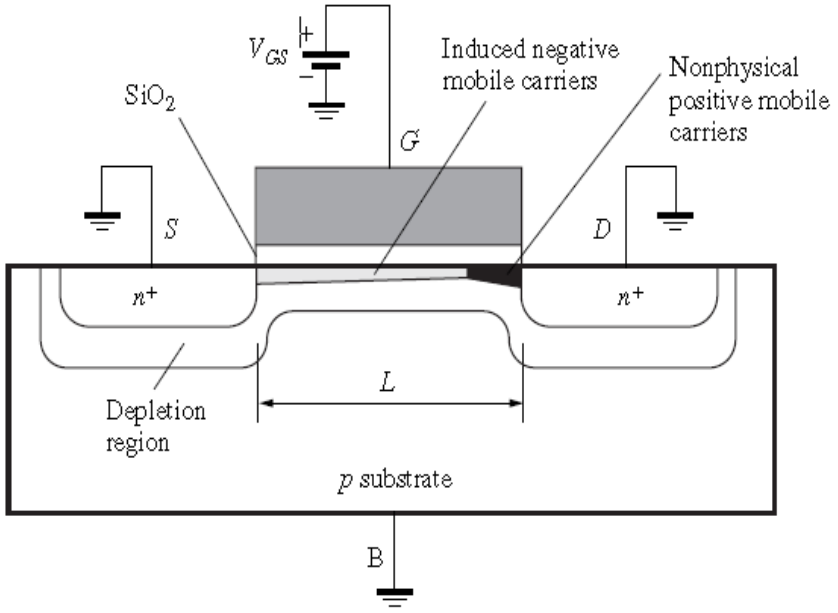
$$I_{DS} = C_{ox}\left[(V_{GS} - V(y)) - V_T\right] \times \mu_n E \times W$$

MOS Current Calculation

$$I_{DS} = k'\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right] \qquad k' = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

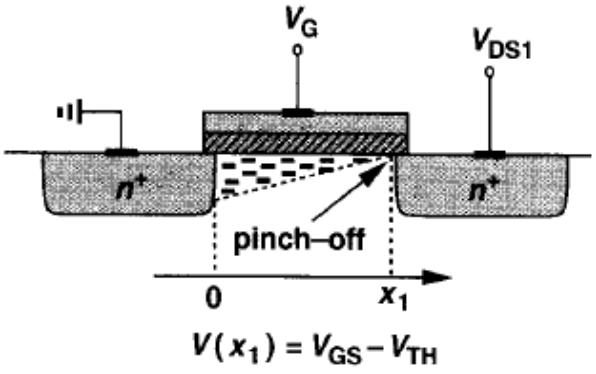
(Board Notes)

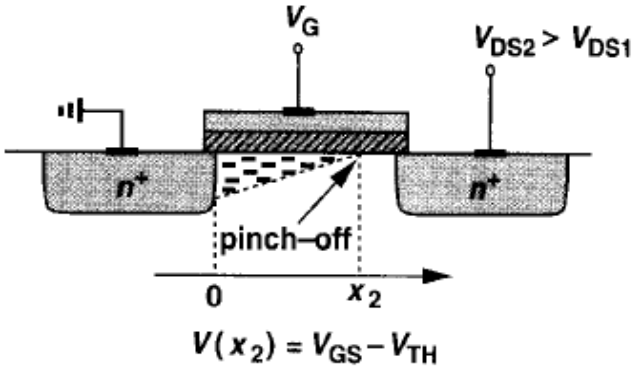


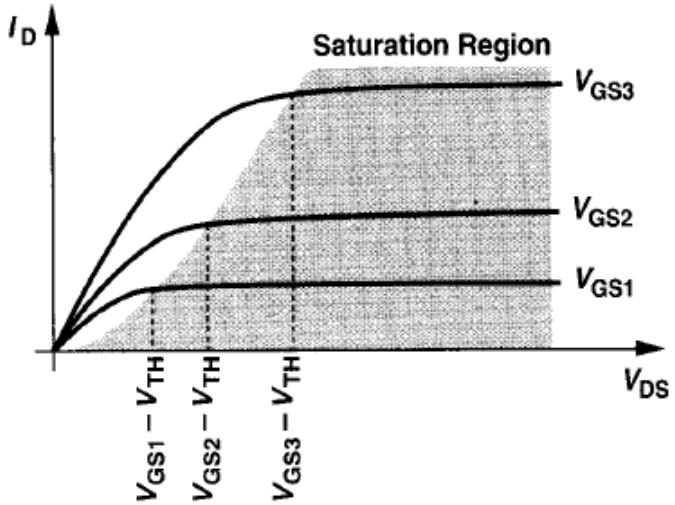


This equation predicts roll-off after reaching a peak due to the existence of non-physical positive carriers. Therefore, the equation must be adjusted after V_{DS} reaches V_{GS}-V_T

MOS Current in Saturation







If we increase V_{DS} beyond V_{GS}-$V_{T,}$ The local potential difference is not enough to sustain the inverted channel. The channel is “pinched-off “

After the pinch-off is reached, the current stays relatively constant!

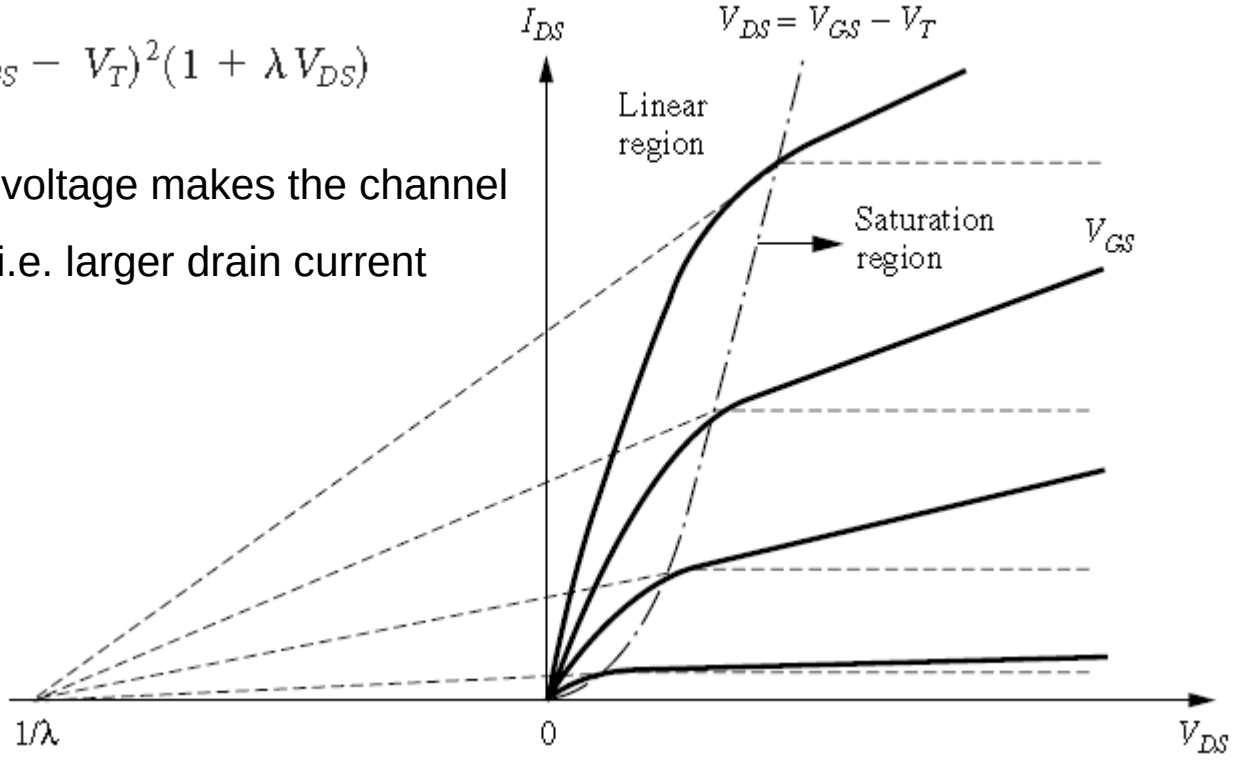
Channel-length Modulation (I_{DS} dependence on V_{DS})

$$I_{DS} = \frac{k}{2}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Large drain-source voltage makes the channel

Effectively smaller, i.e. larger drain current

(Board Notes)



nMOS I-V (65nm)

L = 50nm

W = 100nm

μ_n = 80 cm²/V-s

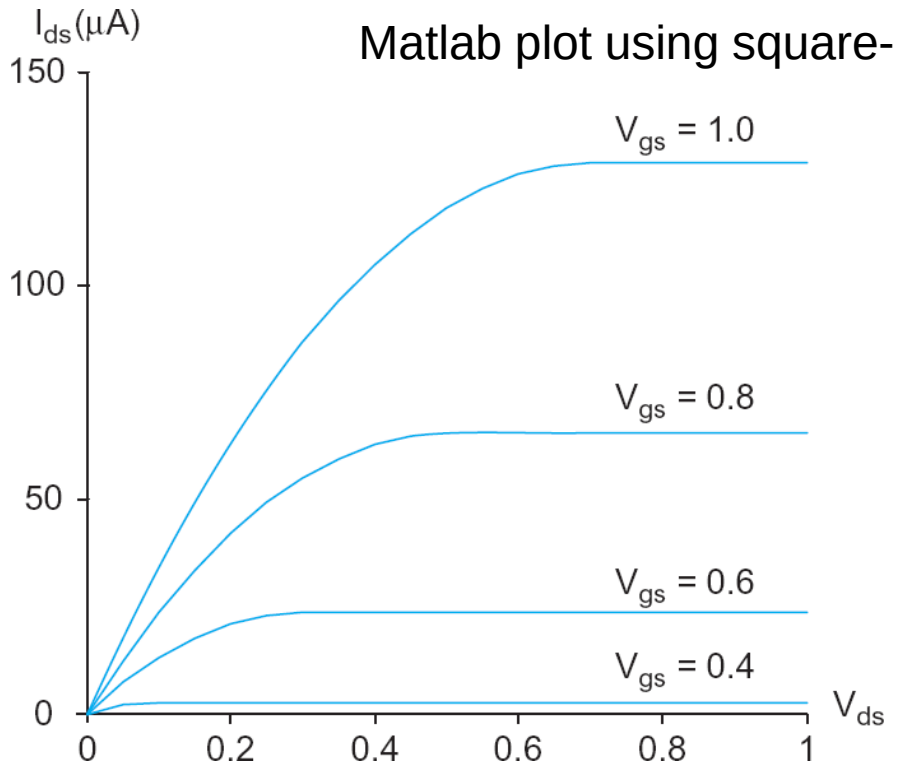
Temp = 70˚C

V_{tn} = 0.3V

t_{ox} = 10.5Å

Calculate β_n

Matlab plot using square-law model



➢ Overestimates current at high voltages

pMOS I-V

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility μ_p is determined by holes
  - Typically 2-3x lower than that of electrons μ_n
  - 40 cm^2/V-s in 65nm process
- Thus pMOS must be wider to provide same current
  - Assume $\mu_n / \mu_p = 2$

Short Channel Effects

(Large *E* Fields in Short Channel Devices)

1980	1995	2001
$E_y = \frac{5V}{5\,\mu m} = 10^4\,V/cm$	$E_y = \frac{3.3V}{0.35\,\mu m} = 9.4 \times 10^4\,V/cm$	$E_y = \frac{1.2V}{0.1\,\mu m} = 1.2 \times 10^5\,V/cm$

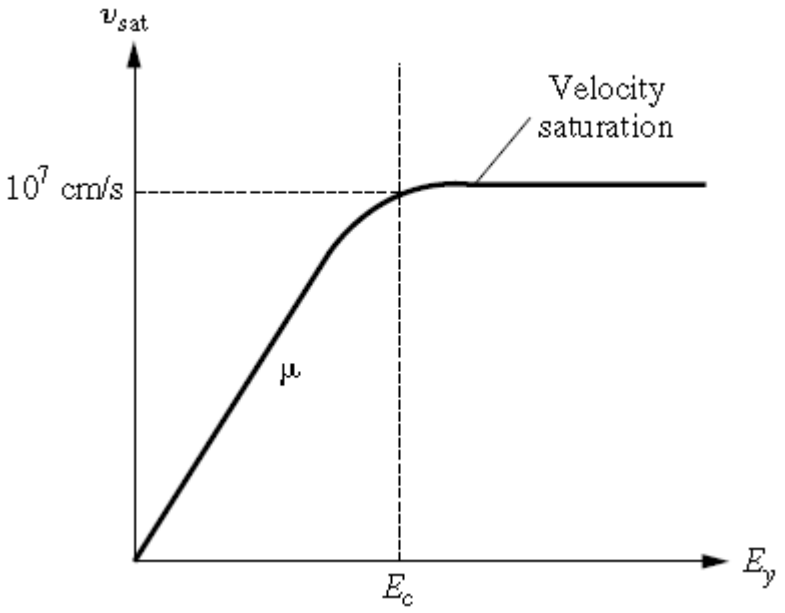
Horizontal Electric field (between the source and drain) = V_{DS} (=V_{dd}) / L

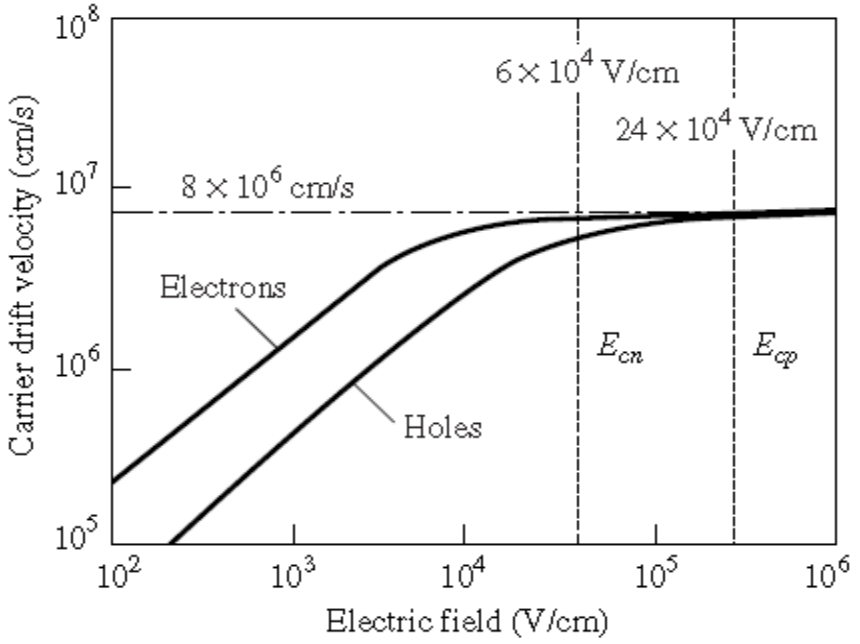
1980	1995	2001
$E_x = \frac{5V}{1000\,Å} = 50 \times 10^4\,V/cm$	$E_x = \frac{3.3V}{75\,Å} = 4.4 \times 10^6\,V/cm$	$E_x = \frac{1.2V}{22\,Å} = 5.5 \times 10^6\,V/cm$

Vertical Electric field (between the gate and channel) = V_{GS} (=V_{dd}) / t_{ox}

Large electrical field causes an early velocity saturation for carriers in short channel devices

Velocity Saturation





- Beyond a certain field limit velocity does not increase!
- NMOS saturates faster than PMOS (due to their larger mobility)

$$v = \mu_e \frac{E_y}{\left(1 + \frac{E_y}{E_c}\right)} \qquad E_y < E_c$$

$$v = v_{sat} \qquad E_y \geq E_c$$

$E_{cn} = 6 \times 10^4 \ \frac{\text{V}}{\text{cm}}$ for electrons

$E_{cp} = 24 \times 10^4 \ \frac{\text{V}}{\text{cm}}$ for holes

Short-Channel MOS Current

$$I_{DS} = W \times Q_n \times v$$

General current of short channel MOS

$$= W \times C_{ox}(V_{GS} - V_T - V(y))\left(\frac{\mu_e E_y}{1 + \frac{E_y}{E_c}}\right)$$

where $E_y = \frac{dV(y)}{dy}$

Plugging in and re-arranging produces

$$I_{DS}dy = W\mu_e\left[C_{ox}(V_{GS} - V_T - V(y)) - \frac{I_{DS}}{W\mu_e E_c}\right]dV(y)$$

After integration, we obtain

$$I_{DS} = \frac{W}{L}\frac{\mu_e C_{ox}}{\left(1 + \frac{V_{DS}}{E_c L}\right)}\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$$

Similar to long channel device except for an extra term in denominator

Cont'd

$$I_{DS} = W \times Q_n \times \upsilon_{sat}$$

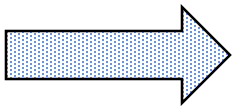
Current of short channel MOS in saturation

Since the current is the same throughout the channel we can set $V(y) = V_{DS}$ and write

$$I_{DS} = W \times C_{ox} (V_{GS} - V_T - V_{DS}) \upsilon_{sat}$$

Equating this current and that of previous slide gives the required V_{DS} for saturation

$$V_{Dsat} = \frac{(V_{GS} - V_T) E_c L}{(V_{GS} - V_T) + E_c L}$$



Always smaller than V_{GS}-V_T

indicates early saturation

(Board Notes)

Example for 0.18 um CMOS Technology

NMOS and PMOS Saturation Voltages for 0.18 μm Technology

Problem:

Consider a 0.18 μm technology. Compute the values of V_{Dsat} for the NMOS and PMOS device assuming $V_{GS} = 1.8$ V, $V_{TN} = 0.5$ V, $V_{TP} = -0.5$ V. Assume the channel length is 200 nm for convenience.

Solution:

Using (2.22), we find that $E_{cn}L_n = 6 \times 10^4\ (0.2\ \mu\text{m}) \approx 1.2$ V and $E_{cp}L_p = 24 \times 10^4\ (0.2\ \mu\text{m}) \approx 4.8$ V. Using (2.28),

NMOS: $$V_{Dsat} = \frac{(1.8 - 0.5)(1.2)}{(1.8 - 0.5 + 1.2)} \approx 0.6 \text{ V}$$

PMOS: $$V_{Dsat} = \frac{(1.8 - 0.5)(4.8)}{(1.8 - 0.5 + 4.8)} \approx 1.0 \text{ V}$$

- Note how fast NMOS saturates (at VDS of 0.6 rather than 1.3 (1.8-0.5)
- Note the difference between NMOS and PMOS

MOS Capacitor: Operating Modes

- Accumulation
  - -ve voltage to G → -ve charge on G
  - Holes attracted to the region beneath G
- Depletion
  - +ve voltage to G → +ve charge on G
  - Holes repelled beneath G, forming a depletion region
- Inversion
  - Even more +ve charge on G
  - Holes repelled further
  - Some free electrons attracted beneath G