UNIVERSITY OF BRITISH COLUMBIA
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

ELEC 402: Introduction to VLSI Design
Fall 2019
Assignment 3: The MOS Transistor / Cadence
Due Date: Thursday, Oct 17th (via Email)

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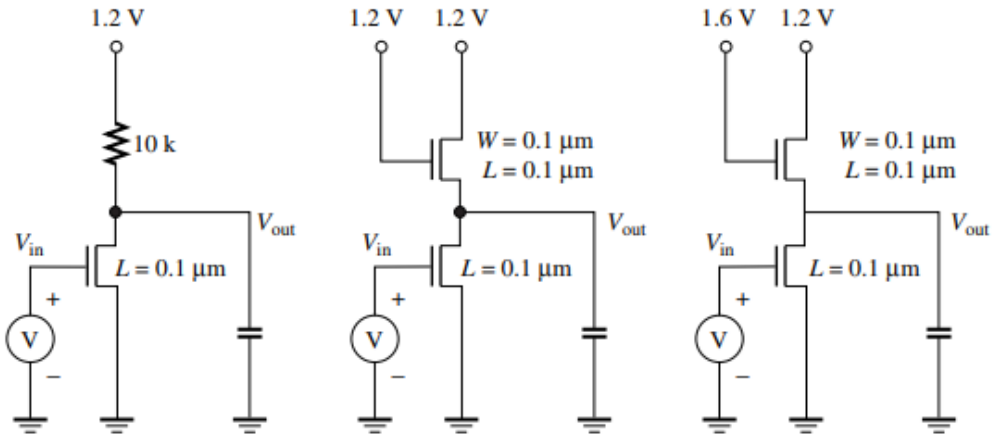
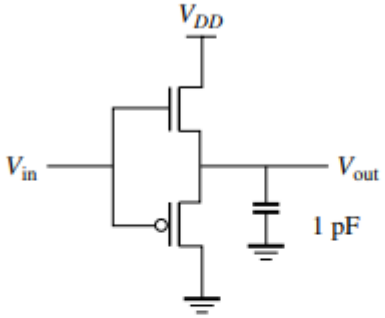
1. In the circuits of Figure , design the widths of the pull-down tran sistors so that $V_{OL} = 0.1$ V. (All transistors are minimum size, $L = 0.1\ \mu$m.) Explain the results. (15 points)



2. (a) What is the intended function of the circuit shown in Figure ? What is the output swing?

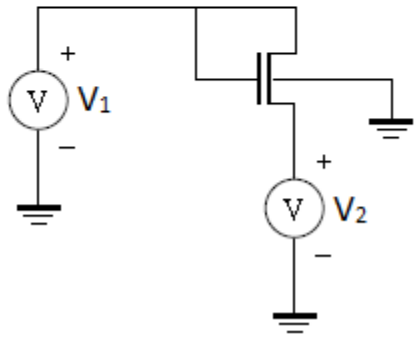


(b) Draw the dc voltage transfer characteristic of the above gate. Label V_{OL} and V_{OH}, and any other interesting values in the VTC. Since the gate has hysteresis, be sure to handle both the rising and falling cases.

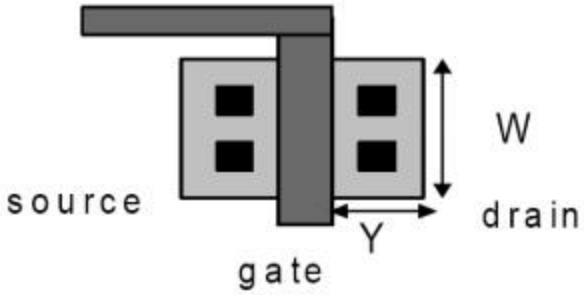
(c) What is the gain of the circuit? Is this a valid gate (i.e., does it have the needed noise rejection properties)?

(d) Use CAD to validate your solution by plotting the VTC (20 points)

3. Figure shows a circuit used to measure the effective value of body effect factor (γ) by measuring V_T at different source voltages. Using the formula of threshold voltage $V_{T0} + \gamma\left(\sqrt{V_{SB} + |2\phi_F|} - \sqrt{|2\phi_F|}\right)$ and assuming $|2\varphi_F| = 0.88V$, find V_{T0} and γ using CAD simulations for a transistor with L = 400nm and W = 800nm (repeat this for L =100nm, what difference do you observe?). Can you revise your approach to confirm $|2\varphi_F|$ value using simulations (and find any assumption errors)? Attach your CAD netlist, graphs and measurement data to your answers. (**20 points**)



4. Consider the layout in the figure below implemented in a 180nm technology. Assume that the transistor has W=900nm, L=180nm and a source/drain dimension Y=800nm and a lateral diffusion of 22nm. Let tox =40 Å (Angstroms). (15 points)



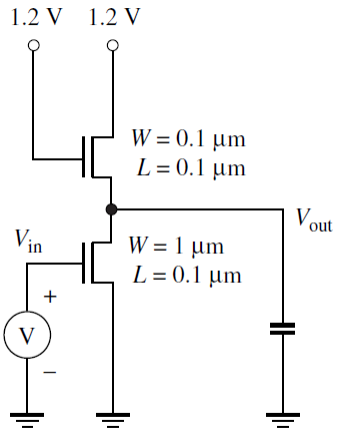
a. Compute the worst case gate capacitance per unit width, C_g, in units of fF/um. Estimate C_{GS}, C_{GD} and C_{GB} in linear, saturation and cutoff, including overlap effects.

b. If $N_A=3x10^{16}/cm^3$ and $N_D=3x10^{19}/cm^3$, x_j=300nm, compute the worst-case capacitance value per unit width, C_j, in units of fF/um.

c. Compute the drain junction capacitance for the following cases (m=0.5):
   i. V_D=1.8V, V_B=0V
   ii. V_D=0V, V_B=0V

5. Calculate Vs of 2-input NOR gates when one input is switching and with both inputs tied together. The device sizes are $W_p = 24\lambda$ and $W_p = 6\lambda$. Use Cadence to find results when switching only input A, AB together. Results for two inputs switched separately vary slightly. Explain the discrepancy between theory and simulation (**15pts**)

6. Using the following schematic and Cadence simulations find NM_H and NM_L (15 points)



(**Bonus**) Does this match the analytical calculations? why? (7 points)