Project/Assignment 5
Due Wednesday November 27th, 11:59 PM to elec402projects@gmail.com – **No Exceptions (no late submissions)**

This assignment has more than 50% bonus point (70/110 would be considered full grade for this assignment). As a second bonus, if you receive more than 70 it will be added to your previous assignments).

1. Cell Library Layout (60 points)

Introduction:
For this project, you will take your Verilog code from project 1 and 2 and lay it out using GPDK45nm standard cells. You will need to download the PnR_files.tar.gz from Canvas, and go through the tutorial "Cadence SoC Encounter" on Canvas

Project Goals:

Auto-route and layout FSM using SoC Encounter.
Test the final layout.

Project Description/Requirements:

Assume a 10fF of load capacitance when simulating for all your outputs.

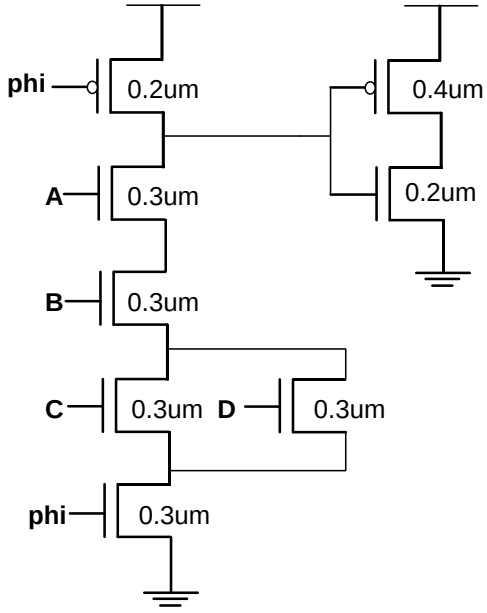
Report Layout

1. Name, student number and project title on the first page of your project report.
2. Your report must include, but not limited to, the following:
    a. Description regarding the function of your FSM design
    b. Description in detail for all the inputs and outputs
    c. Testing procedure
3. Complete layout with rulers (from Cadence) showing the dimensions of the full layout.
4. Output waveforms of the original Verilog code along with the waveforms from simulations of the FSM layout.
5. Test files to show that you tested your layout properly.

2. Domino Logic (11 marks)

1. (a) Determine the logic function OUT (3 marks)

2. (b) Determine the reduction in voltage at the input of the inverter under the worst case charge sharing condition. Consider 0.13 um technology. (8 marks)



3. In the circuit of Figure **4** , determine the capacitance of each node and calculate the minimum and maximum delay. (All transistors are minimum size, $L = 2\lambda$ and $W = 2\lambda$, unless otherwise specified.)

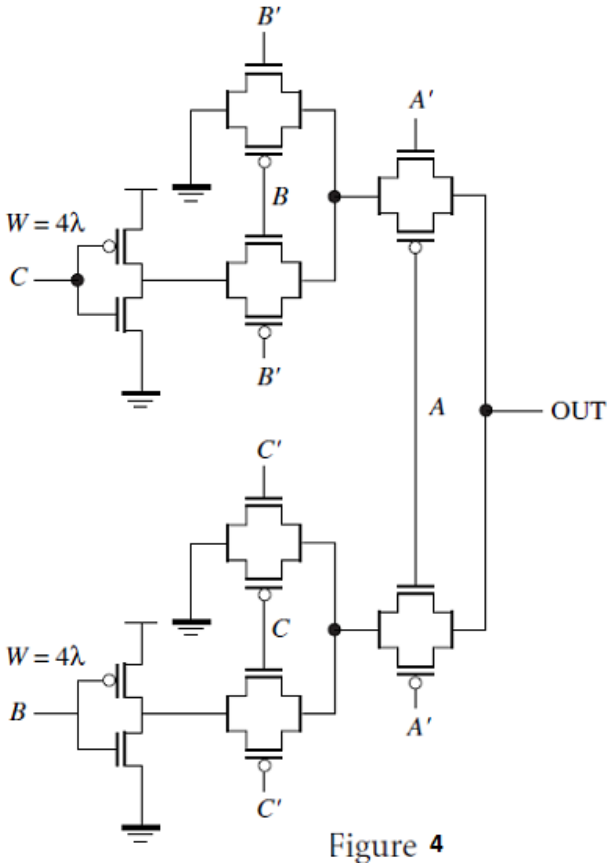


Figure **4**

(13 points)

4. Consider the SRAM cell of Figure 5 with a stored 0 on the left side and a stored 1 on the right side. Design the transistors of the SRAM such that node q does not exceed V_{TN} during a read operation and node $\overline{q}$ drops below V_S during a write operation. The desired cell current during a read operation is 300 μA.

(13 points)

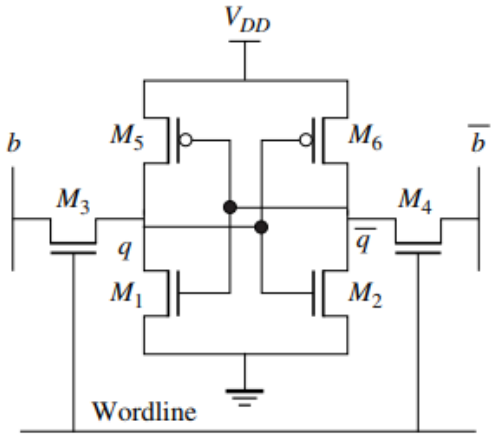


Figure 5

5. How would you implement a 4-input logic function in FPGA with 3-LUTs (hint: note that your function must span more than one PLB). Assume the following arbitrary truth table and work out the details of your PLBs. (13 points)

A_3	A_2	A_1	A_0	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1