ELEC 402
Interconnects
Lecture 15

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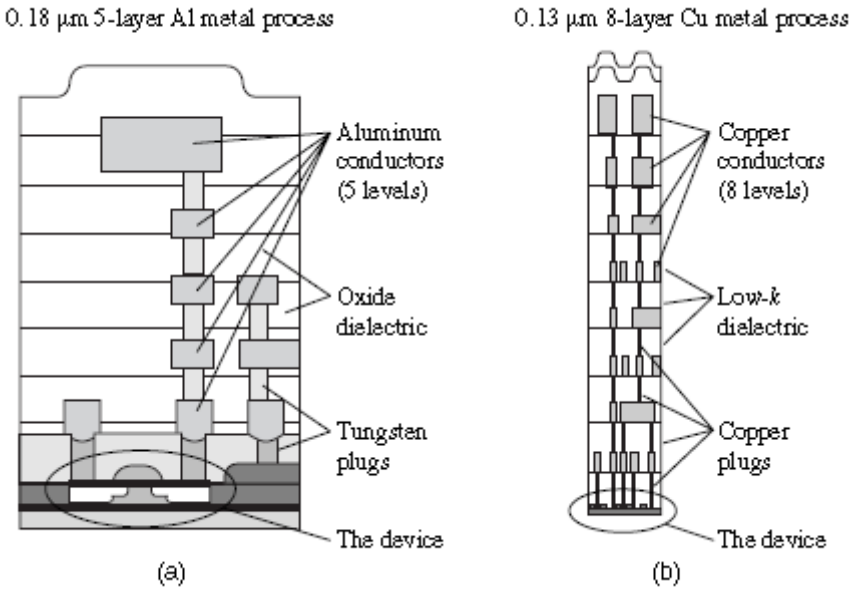
Slides Courtesy : Dr. Res Saleh (UBC), Dr. D. Sengupta (AMD), Dr. B. Razavi (UCLA)

Interconnects



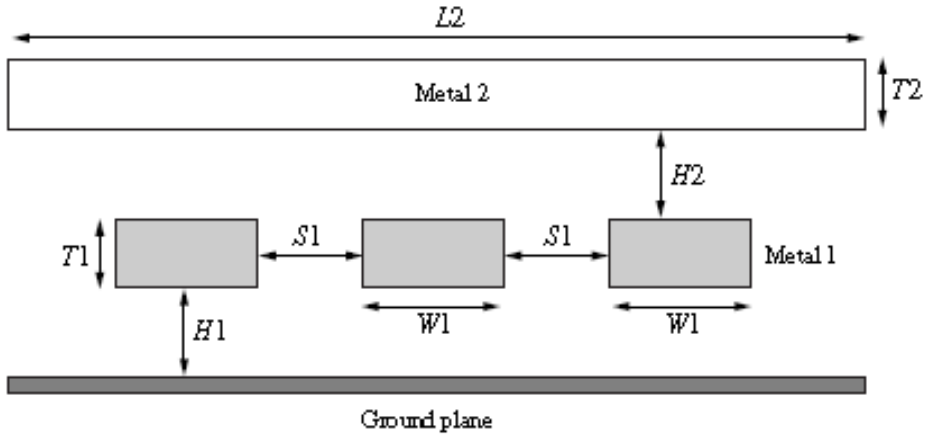
Chip design is a 3D environment creating several parasitics elements

“Interconnect is everything!”

Todays technologies may have up to 13 metal layers such as 16 nm CMOS by TSMC

with different thickness and properties. They control all the important electrical connections on chip

Wire Dimensions



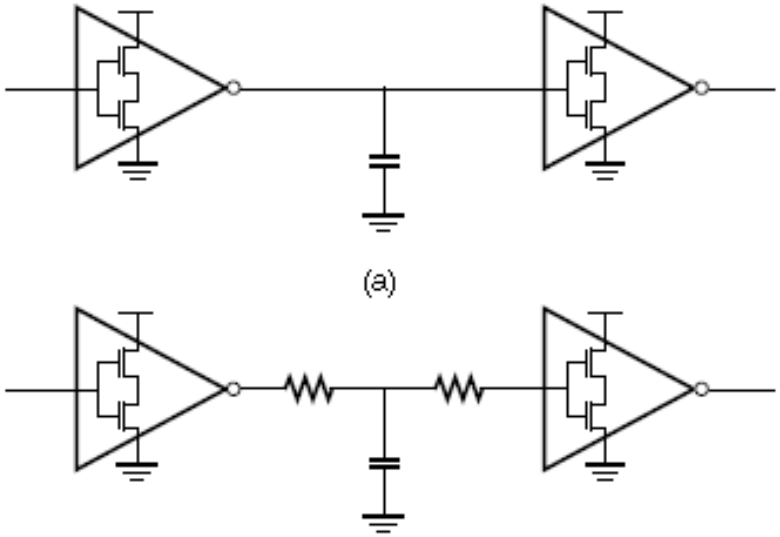
Use has no control over vertical dimensions (metal-metal separation (H), and each Layer thickness (T).

However, proper design of lateral dimensions (S1, and W1) is a full-time job

Sometimes these structures have to run several mm's alongside one another

Signal integrity team in each company plays an important role

Interconnect RC delay



Resistance of an interconnect is given by: $R = \frac{\rho L}{A} = \frac{\rho L}{TW}$

This term (called sheet resistance) is an important one determine $R_{sq} = \frac{\rho}{T}$

The quality of interconnect (note the similarity this term to R_{eqn} and R_{eqp} in transistors)

DSM Sheet Resistance

Resistivity of top metal layers are much smaller due to a couple of reasons

-They normally carry much higher current (tope level connection between blocks, and power Grid)

- Implementation of high-quality passive devices such as inductors

$$R_{sq} = \frac{\rho}{T} = \frac{2.7\ \mu\Omega\text{-cm}}{0.5\ \mu\text{m}} = 54\ \text{m}\Omega/\square \quad \text{Al} \quad \text{metals 1–4}$$

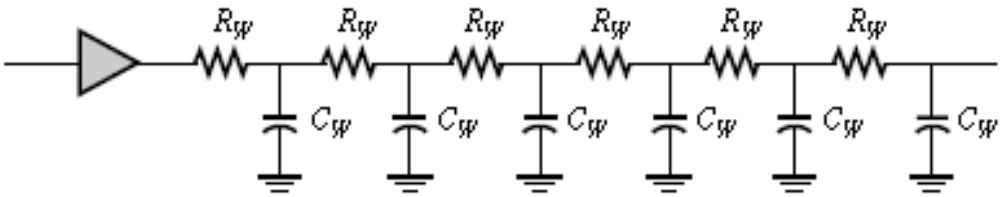
$$R_{sq} = \frac{\rho}{T} = \frac{2.7\ \mu\Omega\text{-cm}}{1.0\ \mu\text{m}} = 27\ \text{m}\Omega/\square \quad \text{Al} \quad \text{metal 5}$$

In DSM technologies copper is introduced to lower the sheet resistance of interconnects

$$R_{sq} = \frac{\rho}{T} = \frac{1.7\ \mu\Omega\text{-cm}}{0.4\ \mu\text{m}} = 42\ \text{m}\Omega/\square \quad \text{Cu} \quad \text{metals 1–6}$$

$$R_{sq} = \frac{\rho}{T} = \frac{1.7\ \mu\Omega\text{-cm}}{0.8\ \mu\text{m}} = 21\ \text{m}\Omega/\square \quad \text{Cu} \quad \text{metals 7–8}$$

RC delay in long wires



Let's say the interconnect is very long length of L and it is divided into N smaller piece of Length ΔL each (n* ΔL= L)

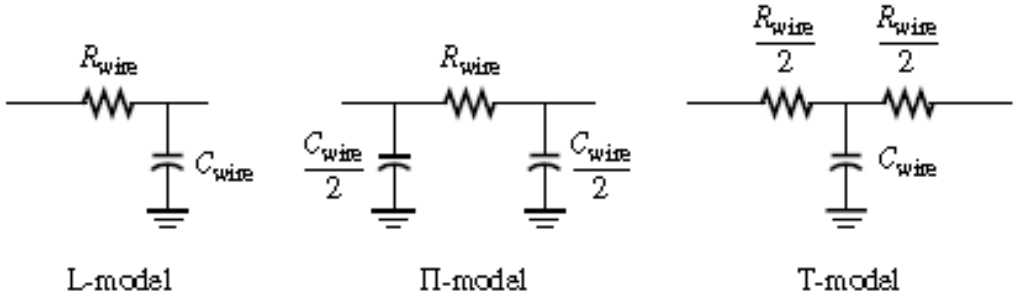
$$\tau_{\text{Elmore}} = (r\Delta L)(c\Delta L) + 2(r\Delta L)(c\Delta L) + \cdots + n(r\Delta L)(c\Delta L)$$

$$= (\Delta L)^2 rc(1 + 2 + \cdots + n)$$

$$= (\Delta L)^2 rc(n)(n+1)/2$$

$$\approx (\Delta L)^2 rcn^2/2 = L^2 rc/2 = R_{\text{wire}} C_{\text{wire}}/2$$

Equivalent Model



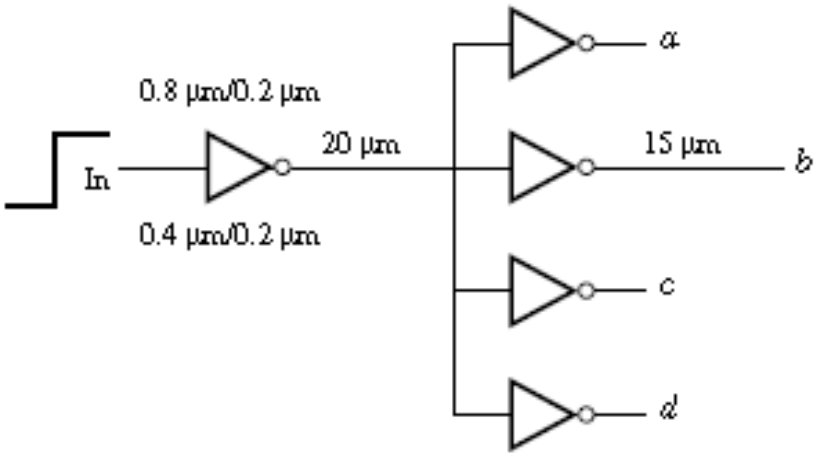
Both T and pi models represent the same delay as the Elmore of long channel

The pi one is less computing-expensive (one less node in the equivalent model)

Short Channel Case Example

What is the propagation delay through the first inverter shown below, ignoring the wire resistance? Assume all inverters are equal in size. Include all capacitances and use 0.18 μm technology parameters. Recompute the delay including interconnect resistance. Assume that the metal is Al and that the width of the wire is 0.2 μm. Is wire resistance significant?

Parameters: $C_{eff} = 1$ fF/μm, $C_{int} = 0.2$ fF/μm, $C_g = 2$ fF/μm.



Long Wire Example

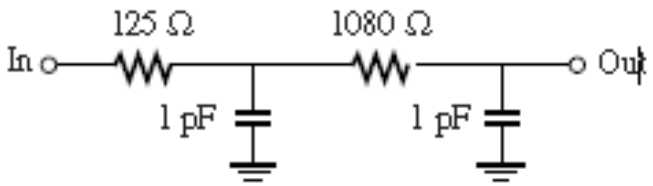
Consider an isolated metal 5 Al wire that is 20 mm long and driven by a 100X inverter (i.e., 100 times larger than the minimum size inverter). Since the wire is isolated, its capacitance is 0.1 fF/μm. Estimate the total line resistance and the total line capacitance assuming that the width of the wire is 0.5 μm. What is the propagation delay as calculated by Elmore for the π-model from the input of the inverter to the end of the wire?

$$R_{wire} = R_{int}L = \left(\frac{0.027\ \Omega/\square}{0.5\ \mu m}\right)(20{,}000\ \mu m) = 1080\ \Omega$$

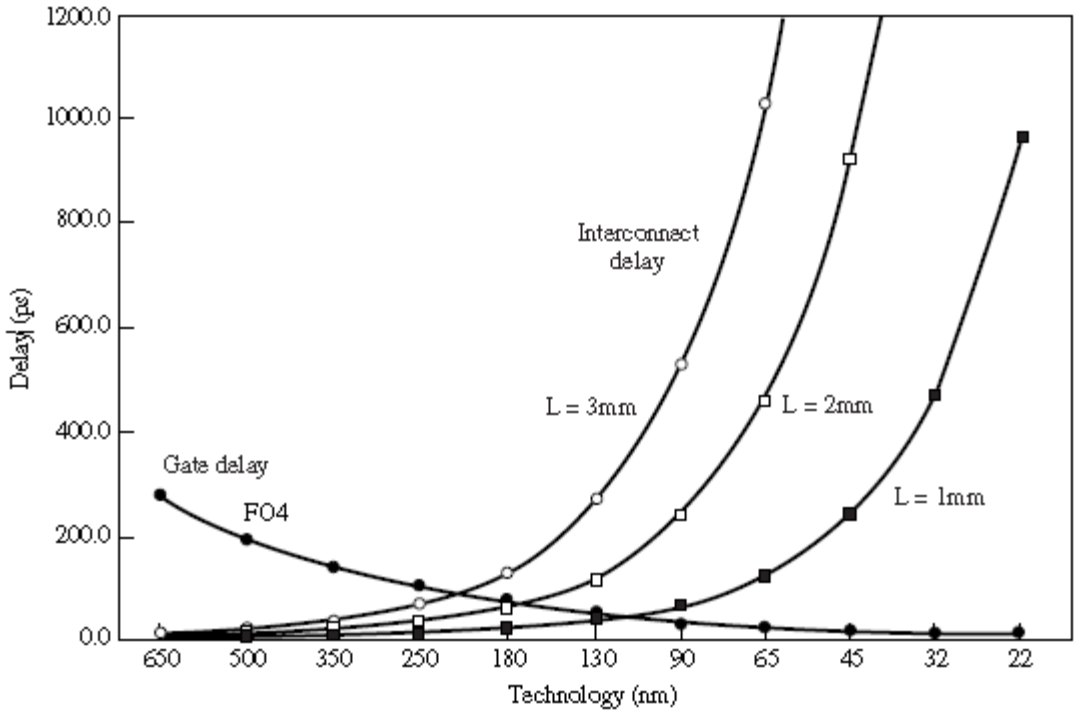
$$C_{wire} = C_{int}L = (0.1\ fF/\mu m)(20{,}000\ \mu m) = 2\ pF$$

$$R_{eff} = R_{equiv}/100 = 12.5\ k\Omega/100 = 125\ \Omega$$

$$C_{self} = C_{eff}(2W + W)100 = (1\ fF/\mu m)(0.6\ \mu m)100 = 60\ fF$$



Interconnect Delays Grows!

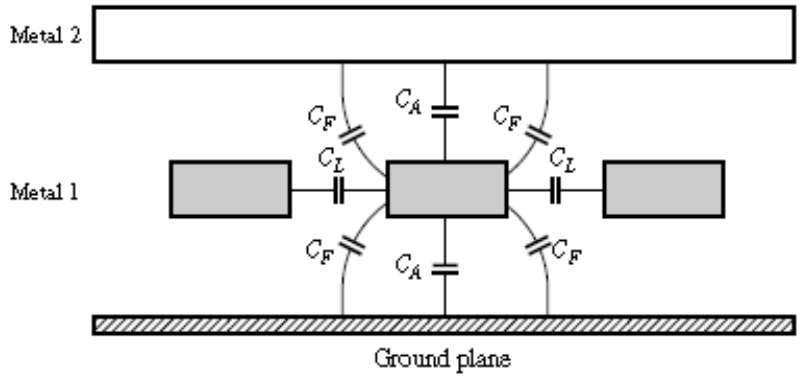


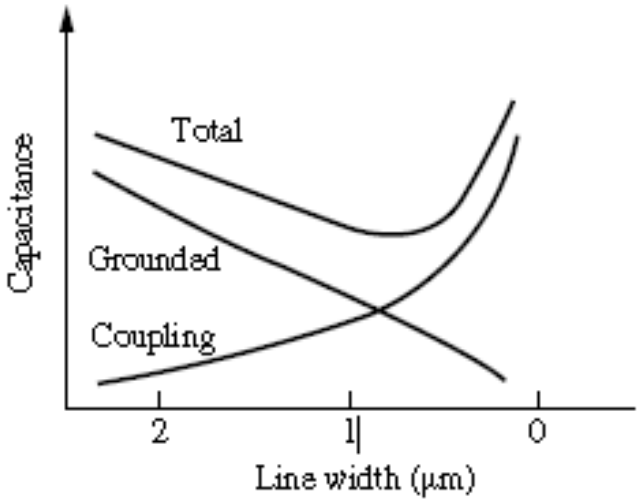
FO4 delay reduces in each technology(?)

Interconnect length is becoming larger, for complex chips, the parasitics are becoming

More visible, hence need to address the problem

Capacitance of interconnects





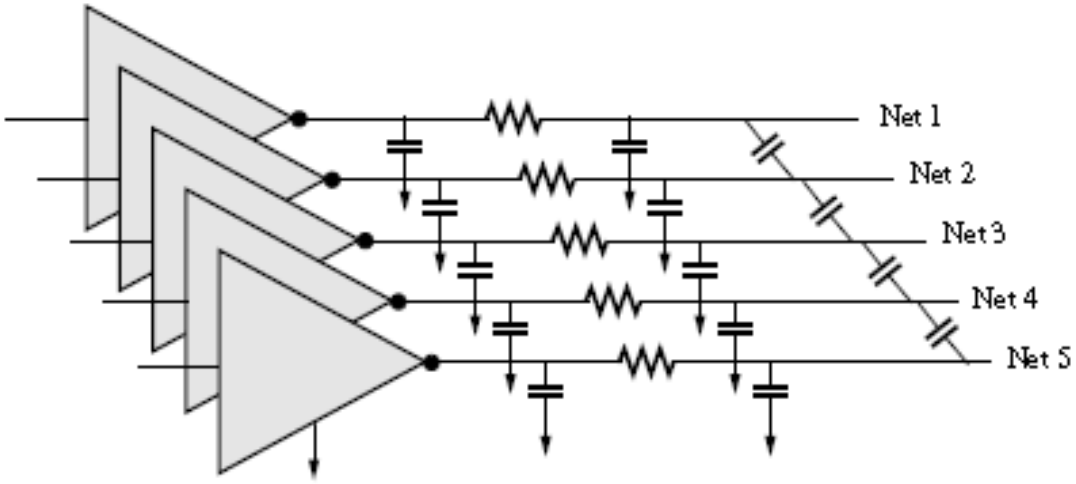
Due to scaling effects the ground capacitance is becoming less important

However, area and fringe capacitance effects are more pronounced in DSM technologies

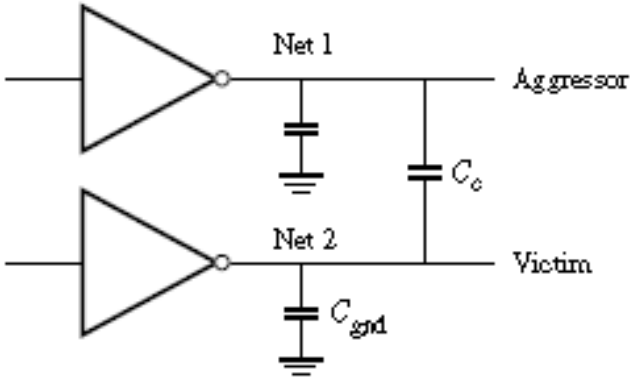
(these days more than 70% of total cap is due to coupling to adjacent nodes)

Capacitance Summary
(optional details in App slides)

For upper layers, when closely spaced the capacitance is maximum and is roughly 0.2fF/um, for other situations we can assume 0.1fF/um (lower metal layers or upper Metal layers when loosely coupled)



Coupling effect on Delay



When a line is switching (victim), the presence of another line (aggressor) in the vicinity

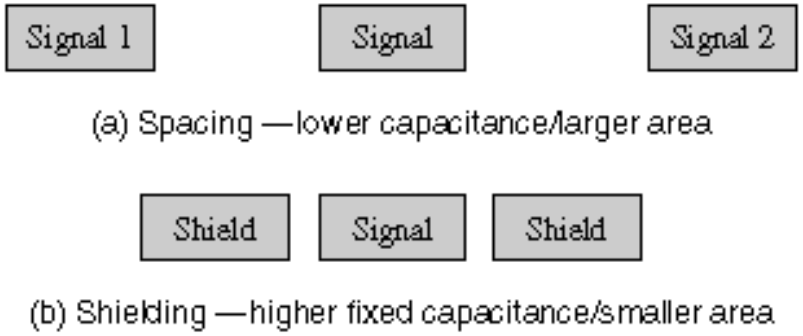
Can cause change to the total capacitance seen by the victim node

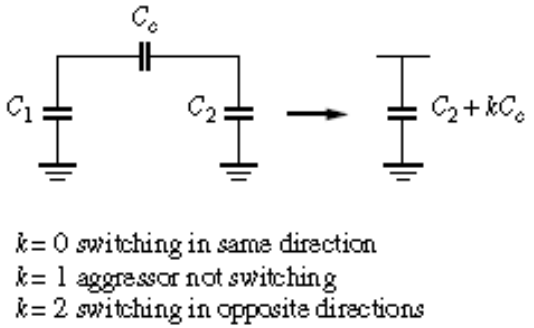
$$C_L = C_{gnd} + C_c \quad \text{aggressor not switching}$$

$$C_L = C_{gnd} \quad \text{both switching together}$$

$$C_L = C_{gnd} + 2C_c \quad \text{both switching opposite}$$

How To Deal with The issue?





Therefore if we have n nodes in the circuit there might be 3^n different scenarios for total cap

- We should space out neighboring signals as much as area allows

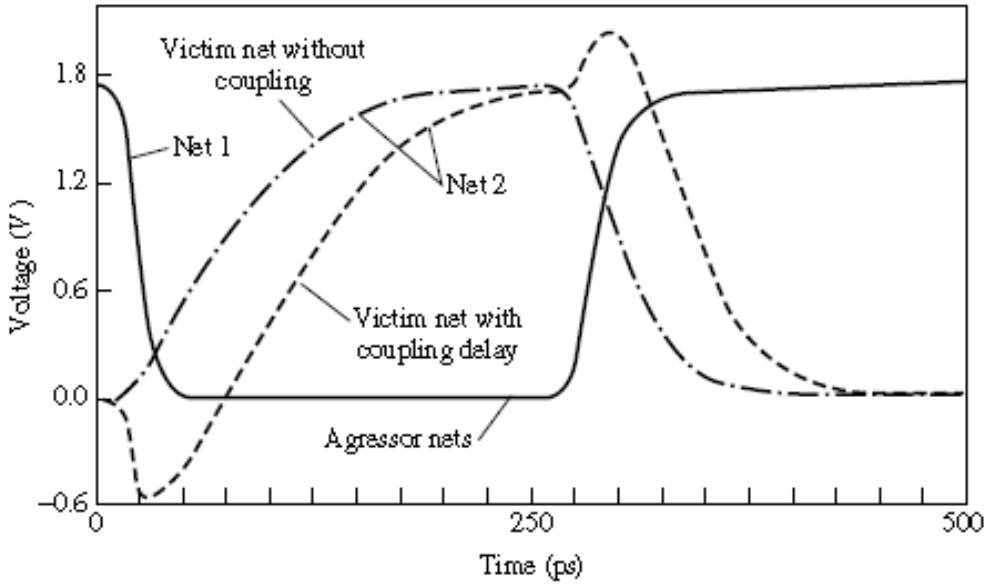
- Using ground shields in between differential signals can potentially reduce the capacitance

By a factor of 2 (increase in total area though)

- Using *low-k* materials

-Using timing tools based on worst-case capacitance (consider worst-case k and ground all nodes

Effect of Signal Feedthrough



An early timing in aggressor can potentially cause wrong direction for initial movement

Of the victim signal

This can be included in worst-case k model (extend k range from -1 to 3 rather than 0 to 2)

Capacitive Noise or Cross-talk

Even when the victim is supposed to be silent, changes in aggressor node my pose transient

Changes in the victim, also called *soft errors* (might be an issue for flip-flops and dynamic logic)

$$\Delta V_2 = \frac{C_c \Delta V_1}{(C_{gnd} + C_c)} \qquad (1$$