

# Working principle

This is an integrating differential pulse-code modulation quantiser inspired by a delta-sigma ADC and based directly on the lecture 'Sigma-Delta Modulation' of the TU Delft EE2S31 course on Signal Processing. See also: https://cas.tudelft.nl/Education/courses/ee2s31/

Together with the firmware, the goal of this circuit is to redistribute the ADC noise (both quantisation and otherwise) away from the low frequencies of interest, and towards higher frequencies. This enables a digital low-pass filter to nearly eliminate ADC noise, so that a much better effective resolution can be achieved (from 10 bits to 20 bits).

## Dimensionina

As a rule of thumb, noise shaping of order p and filtering to  $1/(2^n)$  of the nyquist bandwidth gives:  $\Delta SQNR = n \cdot (3 + 6p) dB$ 

Whereas additional bits of effective resolution give:

 $\Delta$ SQNR = B · 6.02 dB

Assuming a common 10-bit ADC with a conservative 8 bits of effective resolution, using the first order noise-shaping implemented here and

equating for 9 additional bits gives:  $9 \cdot 6.02 \text{ dB} < n \cdot (3 + 6 \cdot 1) \text{ dB}$   $n = 9 \cdot 6.02 / 9 \approx 6.03$ 

Since sample numbers which are a power of two are easier to work with, we Since sample numbers which are a power of two are easier to work with, we round to n=6. Then the sample rate must be at least 276 = 64 times higher than the nyquist frequency. The bandwidth of interest is 10Hz, so the nyquist frequency is 20Hz, and the sample frequency must thus be at least 1.28kHz. However, this is only the sample frequency per channel. Since there are two channels, the system sample rate will be twice as high. or 2.56kHz. We sacrifice a little bandwidth for a nice 16MHz clock division

From measurements, the minimum full scale input current is  $1\mu A$ . The integration capacitor must be charged up to the full scale ADC voltage with a full scale input current within one period time. Then:  $Q = C \cdot V \Rightarrow C = | \cdot T / V = | / (V \cdot f) = 1 \mu A / (2V \cdot 2.5 kHz) = 800 pF$ 

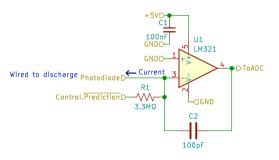
Nonidealities which may mess up measurement:

- Capacitor leakage

- Multiplexer charge injection
- Multiplexer leakage current
   Controller noise (voltage & current)
- Resistor noise (voltage & current)
   Mosfet threshold voltage
- Stability?Bandwidth?
- Aliasing?

### Things to analyse: ! Input noise

- ! Find out difference between input referred noise and ADC noise
  - Find input referred current noise
- ! Find ADC referred noise
- ! MOSFET threshold voltage
- ! Find maximum output voltage from MOSFET threshold voltage
- Find whether MOSFET threshold voltage hinders startup
- ! Find out the effects of aliasing at input ! Find out the effects of aliasing at ADC
- Channel bleeding
- · Linear addition or noise?
- Capacitor leakage
- Linear scaling or additional noise?
- Does parallel capacitor reduce it?
- Multiplexer charge injection
- Where to
- What magnitude
- Does parallel capacitor reduce it?
- Multiplexer leakage current
- Where to
- Output signal sensitvity Does parallel capacitor reduce effect?
- Linearity
- Effect of ADC nonlinearity on overall linearity?
- Stability
- Small-signal model at operating point
- Find bandwidth
- Find gain and phase margin
- Possible stability mitigations



- 2 MOSFETs could be replaced with single JFET
- Look into using 10-bit ADC for lower sample rate
- Check doubling dynamic range by taking into account unipolar

Feedback resistor noise and input referred controller current noise directly impact the input SNR. The resistor noise can be made arbitraily small by using a voltage divider and lower resistor value. The controller voltage noise only adds to the ADC noise since it isn't integrated as the current noise, and is thus noise shaped away.

### # MOSFET threshold voltage

# MOSFEI threshold voltage
Maximum output voltage is Vo = Vcc - (Vth + 2 - Vi). At startup, the capacitors have Vc=0V, so the MOSFETs nicely conduct. When the input clips, the capacitors are charged to the maximum output voltage. As soon as the input current drops within the minimum range, the feedback resistor will discharge them

### # Aliasing

Noise before the integrator is integrated and then sampled at the ADC sample frequency. Noise after the integrator is directly sampled at the ADC sample frequency. Hence, noise will be aliased down at all points in the system by the ADC sample frequency, However, the limited bandwidth of the system by the ADC sample requestly, nowever, the timited below the integrator will act as an anti-aliasing filter for noise before the integrator. In absence of a dedicated anti-aliasing filter after the integrator, the only limit to aliasing will be the bandwidth of the ADC itself.

### # Channel bleeding

# Capacitor leakage According to https://www.murata.com/en-eu/support/fags/products/capacitor/mlcc/char/0039, ceramic capacitors generally have an isolation resistance of  $>10G\Omega$ , so for voltages <3.3V, this gives currents of I = 3.3V / 10 = 0.33nA

# **TU**Delft

Trades bandwidth to increase resolution By Arthur Admiraal & Daan de Groot **POxiM** 

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Size: A4 Date: 2020-05-06 Rev: A KiCad E.D.A. kicad (5.1.0-0) ld: 2/9

