half adder

truth table

A	B	Co	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

K maps

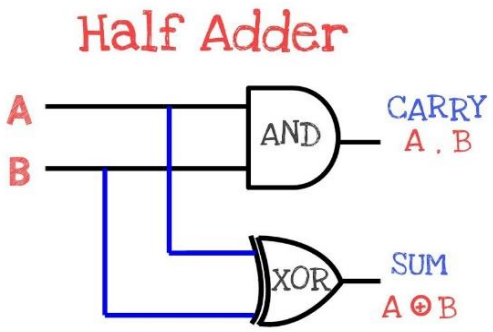
Co	B=0	B=1
A=0	0	0
A=1	0	1

A

logic expression without XORs
Co = AB , S =BA'+AB'
3 AND gates & 1 OR gate & 2 NOT gates

logic expression with XORs
Co = AB, S = A⊕B
1 AND gate & 1 XOR gate

gate level schematic



full adder

truth table

A	B	Ci	Co	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

K maps

Co	Bci 0&0	0&1	1&0	1&1
A=0	0	0	0	0

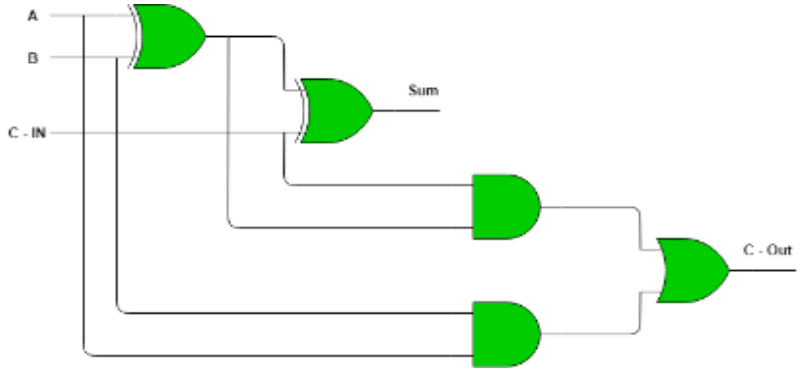
1

		1	0	1	1	1

logic expression without XORs
Co = AB + BC + AC
S = A'B'C + ABC + A'BC' + AB'C' 6 NOT, 11 AND 2 , 5 OR 2

logic expression with XORs
Co = AB + (A⊕B)Ci S = (A⊕B)⊕Ci
2 XOR, 2 AND2, 1 OR2

gate level schematic

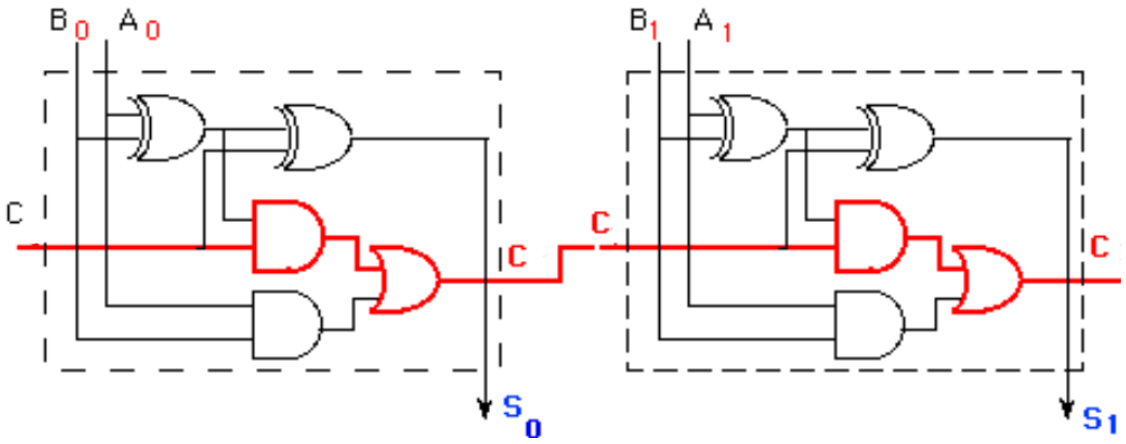


2-bit Ripple Carry Adder
truth table

input					output
A1	A0	B1	B0	Cin	Cout
0	0	0	0	0	0
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0

1	0	1	0	1	0
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

gate-levelschematic



	B	
S	0	1
0	0	1
1	1	0

	Bci			
	S	0&0	0&1	1&0	1&1
A	0	0	1	1	0

1 1 0 0 1

S1	S0	
	0	0
	0	1
	0	1
	1	0
	0	1
	1	0
	1	1
	0	0
	0	1
	1	0
	1	0
	1	1
	1	0
	1	1
	0	0
	0	1
	0	1
	1	0
	1	0
	1	1
	1	0

1	1
0	0
0	1
1	1
0	0
0	0
0	1
0	0
0	1
0	1
1	1