Introduction to Digital Systems Design

ECEN 248 Fall 2019

Instructor:	Dr. Jeyavijayan (JV) Rajendran
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Office Hours:	Open-door policy on Tuesdays and Thursdays (Walk in if the door is open) or make an appointment through e-mail to jv.rajendran@tamu.edu
Class Meets:	Sections 507–512, T Th from 3.55pm–5:10 pm in ZACH Room 341
Course:	Introduction to Digital Systems Design, (3-3), Credit 4: Combinational and sequential digital systems design techniques; Design of practical digital systems.
Textbook:	Frank Vahid, *Digital Design with RTL Design, VHDL, and Verilog, 2nd Edition.* John Wiley & Sons, 2011. The textbook is required. Exams are open book and notes, but no electronics. You will have to print textbook sections for the exam if you have an electronic version of the textbook.
TA's:	TBA
Web Site:	Class notes, online homework, handouts, old exams, and the grade book will be found in the university's learning management system, eCampus. Go to http://ecampus.tamu.edu and login with your NetID/password. The class notes are either developed by the course instructor or derived from the original copyrighted notes of the textbook author.
Prerequisites:	MATH 152 with a grade of C or better; PHYS 204 with a grade of C or better or concurrent enrollment.
Grading:	Homework 30% Laboratory 25% Exam I 15% Exam II 15% Exam III 15%
Grading scale:	A (90-100), B (80-89), C (70-79), D (60-69), F(<60)

Learning Outcomes

Digital Systems are ubiquitous and significantly impact the way we live. A student who successfully fulfills the course requirements will have demonstrated the ability to convert desired system functionality into a digital design. Specific learning outcomes include: (1) ability to analyze and design combinational logic circuits, (2) ability to analyze and design sequential logic circuits, (3) ability to design high-level digital systems using Register-Transfer Level (RTL) design, and (4) utilize the Verilog hardware design language, logic simulation, and Field Programmable Gate Array (FPGA) technology to implement combinational, sequential, and RTL- based digital systems. A class-by-class topic and reading list is at the end of the syllabus.

Exams

The three exams will be open book and open notes. Exams are not cumulative. No electronic devices are allowed in Exam I. The only electronic device allowed during Exam II and Exam III is a calculator. Please put your cell phone, smartphone, smartwatch, laptop, etc. in your backpack during the exam. The first two exams will be in-class. Exam III is at the scheduled time for final exams.

Attendance and Makeup Policy

Attendance to class is optional. Please do your best to be present for the exams. If you miss an exam and have a *university excused absence*, you will need to schedule a makeup exam. If you do not have an excused absence, you will receive a zero unless there are extenuating circumstances. Please see me at least a week before the scheduled time for the exam if possible. I will expect written confirmation of a visit to a health care professional, affirming the date and time of the visit, for an injury or illness that requires you to be absent from an exam or the final. Please review the Student Rule on attendance http://student-rules.tamu.edu/rule07.

Homework

Homework will be assigned weekly, and it will all be online in eCampus. I will accept late homework for up to one class period after the original due date (e.g., for homework due on Tuesday, you can submit late homework through Thursday at 11:59 pm), but there will be a 10-point penalty (i.e., one letter grade).

Academic Integrity

"An Aggie does not lie, cheat, or steal or tolerate those who do." Students are expected to be aware of the Aggie Honor Code and the Honor Council rules and procedures (see http://aggiehonor.tamu.edu).

It is acceptable to discuss homework problems with your classmates but the work you submit in eCampus should be your own and not a team effort.

ADA Statement

The Americans with Disabilities Act (ADA) is a federal anti-discrimination statue that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for a reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact Disability Services, currently located in the Disabil- ity Services building at the Student Services at White Creek complex on west campus or call 979-845-1637. For additional information, visit http://disability.tamu.edu.

Texas A&M University
Department of Electrical and Computer Engineering

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DATE (Tentative)	READ VAHID	TOPICS
T 8-27	1.1, 1.2	Intro to Digital Design; Digital vs Analog; Binary Numbers
Th 8-29	1.3, 2.1–2.4	Implement Dig. Systems; Switches; CMOS Transistors; Logic Gates
T 9-3	2.4–2.6, App A	Using Gates; Boolean Algebra; Representing Boolean Functions
Th 9-5	2.6–2.9	Combinational Logic Design; More Gates; Decoders and Muxes
T 9-10	2.10, 6.2	Propagation Delay; Minimization
Th 9-12	6.2, 4.1, 4.3	Minimization (cont); Data path; Adders
T 9-17	4.3, 6.4, 4.4–4.5	Incrementer; Carry-Lookahead Adder; Comparator; Multiplier
Th 9-19	4.6	Subtractors and Signed Numbers
T 9-24	4.7–4.8, 7.4	Arithmetic Logic Unit (ALU); Comb. Shifter; 7400 SSI; PLD's
Th 9-26	Exam I	1/15–2/7 (Ch 1, Ch 2, App A, 6.2, 4.1, 4.3-4.6, 6.4)
T 10-1	3.1, 3.2, 4.2	Flip-Flops (FF) and Registers
Th 10-3	4.2, 9.2, Notes	Registers (cont); Verilog – Combinational
T 10-8	9.3, Notes	Verilog – Simulation (Testbenches) and Sequential
Th 10-10	9.4, Notes, 3.3	Verilog – Datapath; Finite State Machines (FSM)
T 10-15	3.4, 3.5	Controller Design; Metastability
Th 10-17	3.5, 6.3, 3.8	FF Set-Reset; Glitches; Seq. Logic Opt; Mealy & Moore FSM's
T 10-22	4.2, Notes, 4.9	Shift Reg.; Serial Trans; Multifunction Reg.; Counters
Th 10-24	4.9–4.10, 6.4, 5.1–5.2	Counters (cont); Timers; Reg. Files; Datapath Tradeoffs; RTL Intro
T 10-29	5.2, 5.3, 5.4	RTL Design; High-Level State Machines; RTL Desgin Process
Th 10-31	Exam II	2/12–3/21(4.7–4.8, 7.4, Ch 3, 6.3, 4.2, 4.9–4.10, 6.4, 5.1, 5.2, Verilog)
T 11-5	5.4, 5.5, 5.6	RTL Design (cont); RTL Max Clock Freq; RTL Behav. Design
Th 11-7	5.7	RAM; ROM; Flash
T 11-12	5.8, 5.9, 5.10, 5.13	FIFO's; Multiple Processors; Hierarchical Design
Th 11-14	6.5, 6.6, 7.1, 7.2	RTL Design Optimization and Tradeoffs; Intro Manf. IC Types
T 11-19	7.2, 7.3	Manufactured IC Types (cont); FPGAs
Th 11-21	7.5, 8.1–8.5	IC Tradeoffs; Prog. Processors-Basics, Three and Six Inst. Proc
T 11-26	8.6, Notes	Processor Extensions; Error Detection and Correction in Digital Design
Th 11-28		Thanksgiving Holiday; No class
Th 12-03	Notes	Redefined Day (Virtual Thursday); ECC (cont); Intro to Testing; Intro to Hardware Security
T 12-10	Exam III	Sections 507–512, TBA