Digital Design
with RTL, VHDL, and Verilog
2nd edition

Errata and Clarifications

Although we exerted tremendous effort to ensure the book
would not contain errors, a few errors may still manage
to slip by. Below are mistakes found. Many thanks to the students and
teachers who found them. Report errors to vahid@cs.ucr.edu.

Chapter 2

* Pg 45, Ex 2.1, number 3: Problem statement should be "Both a and b are 0"
  Currently says "not 0".
  (Thanks to Prof. Alper Sen, Bogazici University, Turkey, 3/8/13)
* Pg 61: "(a + b + c)' = (abc)'" should be "(a + b + c)' = a'b'c'"
  (Thanks to Prof. Mahamed G.H. Omran, Gulf Univ of Science and Tech, 3/3/11)

Chapter 3

* Figure 3.47: Input is b, output is x (declarations are reversed). 2/24/11
* Figure 3.80: The value of "u" should be the inverse of "D".
  The error does not affect the main point of the diagram.
  (Thanks to Aswin Krishna, M.S. graduate student at Case Western, 3/25/10).

EXERCISES

* Exercise 3.23: Do not assign this exercise. It refers to
  a figure from the book's first edition, and thus the exercise
  description no longer matches the figure.
  (3/25/10)
* Exercise 3.52: The delay of an XOR gate should have been included
  in the exercise description. Assume it is the same as for an AND gate.
  (3/25/10)

Chapter 4

* Pg 212, first full paragraph: -6 divided by 2 if done correctly
  should be -3, or 1101, not -1 as currently appears.
  Likewise, -6 multiplied by two should be -12, not -4 as currently
  appears. The point of the paragraph is still correct: normal shifts
  do not work for multiplying/dividing signed numbers by powers of 2.
  (Thanks to Prof. Mahamed Omran, Gulf Univ, Kuwait, 12/5/10)
* Pg 214: "the maximum data value could be 18,137, which would
  require 15 bits" -- the max value is actually 26,010 (which would
  still require 15 bits). (Thanks to Felix Dujmenovic, 2/25/11)
* Pg 220, Fig 4.72: the (a) and (b) are swapped.
  (Thanks to Jiang Hu, Texas A&M, 7/6/11).

Chapter 5

* Figure 5.3: The transition from Wait to Disp should have its second term complemented, i.e.: c'*(tot<s)' (the ' at the end is missing)

* Fig. 5.28(c) (page 266), because state "Out1" reads A[1], then the following actions should be added to that state:

A_Ra1 = 0
A_Ra0 = 1
A_Re = 1

(Thank you to Prof. Mahamed G. H. Omran of Gulf University for Science & Technology, 5/2011).

Also Fig. 5.28(c), in state Init1 the second A_Wa1=0 should be A_Wa0=0 [Cantrell]

* Fig 5.33: The bottom-left arrow, from R in state A to Q in state B, should be deleted, because the assignment Q=R was moved to state B. The main point of the figure is still correct, but the extra arrow suggests a transfer that does not occur. (Thank you to Prof. Mahamed G. H. Omran of Gulf University for Science & Technology, 5/2010).

* Page 279: A fifth path from "b" through "+" to "c" can also be considered (path delay = 2 ns). (Thank you to Prof. Mahamed G. H. Omran of Gulf University for Science & Technology, 12/2010).

* Page 280: References to 5.43 should be to 5.44. (Thank you to Prof. Mahamed G. H. Omran of Gulf University for Science & Technology, 12/2010).

Fig 5.44 – Should be an inverter bubble (o) on tot_lt_s input to AND gate to Implement soda machine correctly. [Cantrell]

* Page 290: The sentence "how to write a 9 and a 13 into locations 500 and 999" should be "how to write a 500 and a 999 into locations 9 and 13". (Thank you to Prof. Mahamed G. H. Omran of Gulf University for Science & Technology, 5/2010).

* Fig 5.98: The "(sum<5099)" on the bottom-right should be
"(sum<5099)'" (add the ').
(Thank you to Dr. Anil Celebi, Kocaeli University, Turkey, 1/12/12).

Chapter 6

* Page 344 (Fig 6.31): The first "X" in column z should be in row 1 rather than row 0. x'y' is still determined essential, but because it is the only prime implicant that covers minterm (0) x'y'z', rather than (1) x'y'z. The solution thus remains the same.
(Thank you to Dr. Anil Celebi, Kocaeli University, Turkey, 1/4/11).

Example 6.17 (p.363) – The assumption that b remains asserted for only one clock Cycle implies that the Moore Machine should not have “b” on the transition to states S2, S4, and S6. The way the Moore machine is shown currently would require two button presses to move between the four modes. [Cantrell]

Sequential Multiplier (pp. 375-376) - You need to add carry-out from the adder and store the carry-out in a one-bit register (or alternatively use a 9-bit register). The example only works because there is no carry from the adder. [Cantrell]

* Page 408 (Fig 6.99): The second column of gates should have two inputs each, not three. (Thank you to Mark Brehob, Univ. of Michigan, 5/29/12).