Chiplet Technologies for an Emerging Ecosystem

David C. Kehlet, Research Scientist

11/25/2020

intel®

Legal Information

This presentation contains the general insights and opinions of Intel Corporation ("Intel"). The information in this presentation is provided for information only and is not to be relied upon for any other purpose than educational. Statements in this document that refer to Intel's plans and expectations for the quarter, the year, and the future, are forward-looking statements that involve a number of risks and uncertainties. A detailed discussion of the factors that could affect Intel's results and plans is included in Intel's SEC filings, including the annual report on Form 10-K.

Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No computer system can be absolutely secure. Check with your system manufacturer or retailer or learn more at www.intel.com.

Results have been estimated or simulated using internal Intel analysis or architecture simulation or modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

Overview

- 2013-2020: Chiplets on the Rise
- State-of-the-art Heterogeneous Integrated Packaging (SHIP) Project & Second Generation Chiplet Concepts
- Conclusion

Chiplets on the Rise:
Early Days and the Mother of Invention

Chiplets on the Rise: Early Days

Intel to make 14-nm FPGAs for Altera

By Rick Merritt 02.26.2013

SAN JOSE, Calif. – Intel Corp. will build FPGAs for Altera Corp. using its 14-nm FinFET process technology in a deal that turns up the heat on in foundry and Xilinx in high-end FPGAs.

Source: EE Times

Digital focused PDK

& Intel EMIB

Altera and Intel Extend Manufacturing Partnership to Include Development of Multi-Die Devices

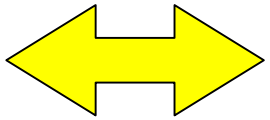
Collaboration Will Optimize Integration of 14 nm Tri-Gate Stratix 10 FPGAs with Heterogeneous Technologies into a Single System-in-a-Package

San Jose and Santa Clara, Calif., March 26, 2014 – Altera Corporation (Nasdaq: ALTR) and Intel Corporation today announced their collaboration on the development of multi-die devices that leverage Intel's world-class package and assembly capabilities and Altera's leading-edge programmable logic technology.

Source: Intel

Intel® Arria 10® Legacy

- Arria 10 on TSMC 20nm, the generation preceding Intel® Stratix 10® on Intel 14nm



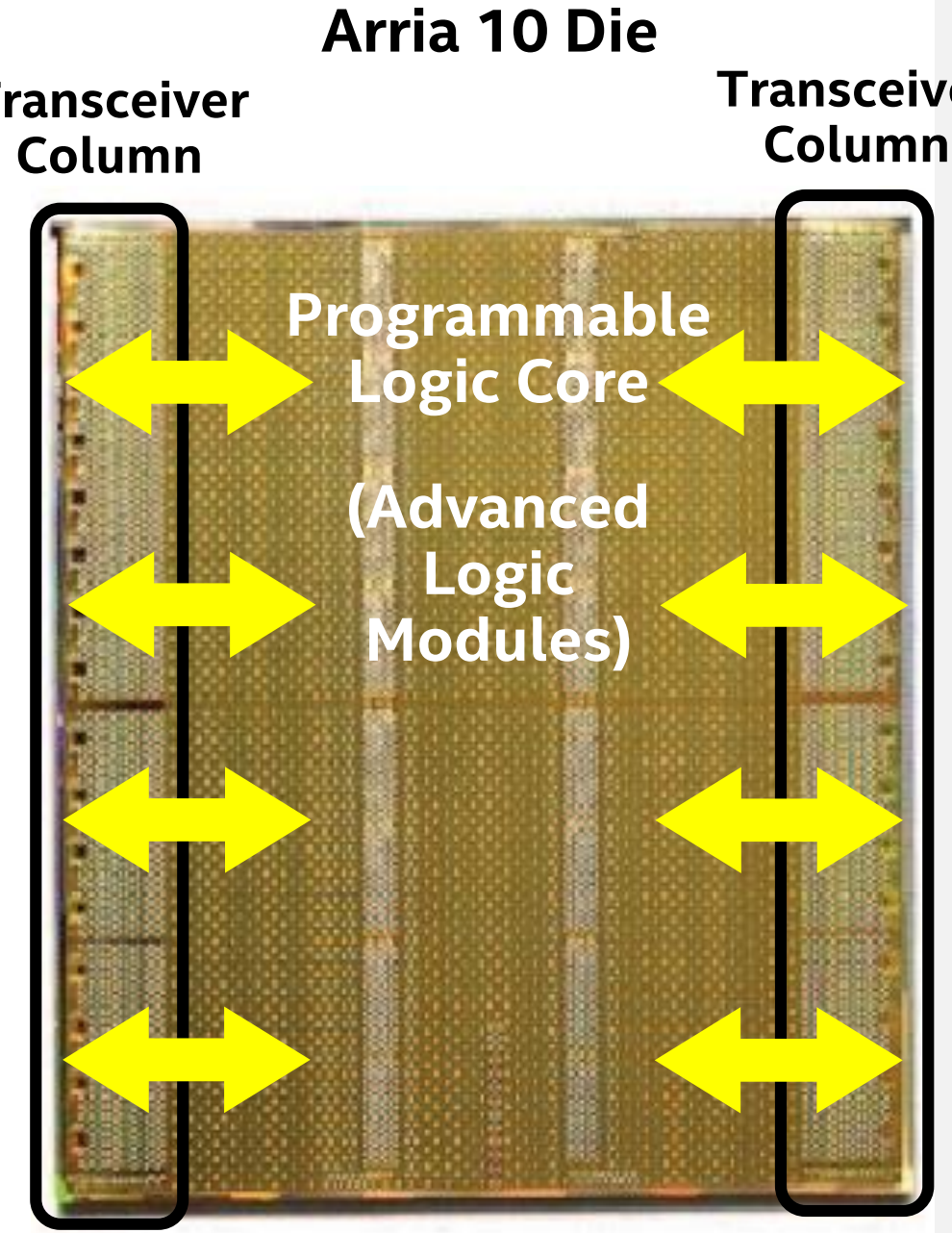
= Thousands of wires between Core & Transceiver Columns:

Data Tx, Rx

Clocks

Configuration

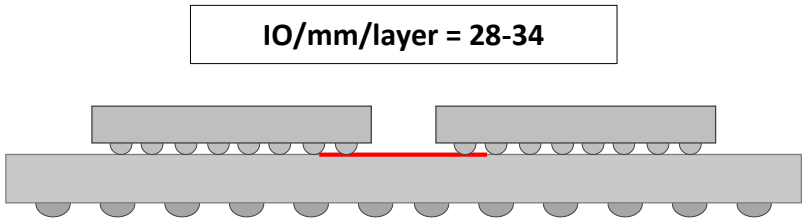
Control



Arria 10 die image source: IEEE CICC, "Arria 10 Device Architecture," Tyhach et al

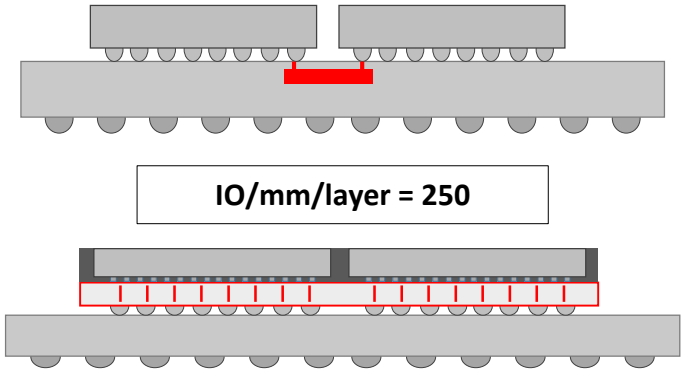
High-Density Packaging

Standard Flip-Chip Packaging Technology



FCXGA, FCCSP

High-Density Packaging Technology



EMIB

Silicon Interposer

High-density packaging technology provides 7-8x IO density increase

Early Days and the Mother of Invention Takeaways

- Advanced packaging technology enabled new thinking about SoC microarchitecture
  - Die disaggregation
  - Heterogeneous integration
  - Die-to-die interface with high bandwidth and low latency gives near-monolithic performance

Chiplets on the Rise:
DARPA CHIPS and Standardization

"In CHIPS, we're working with Intel on some of their integration strategies … so that you can do that composable design."

DARPA's ERI director Bill Chappell

Source: IEEE Spectrum 7/2018

What is CHIPS?

Common Heterogeneous Integration and IP Reuse Strategies

CHIPS will develop the **design tools and integration standards** required to demonstrate **modular electronic systems** that can leverage **the best of DoD and commercial** designs and technology.

Today – Monolithic

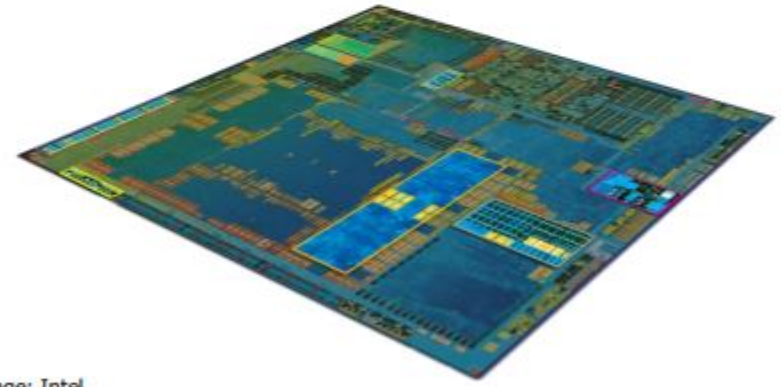
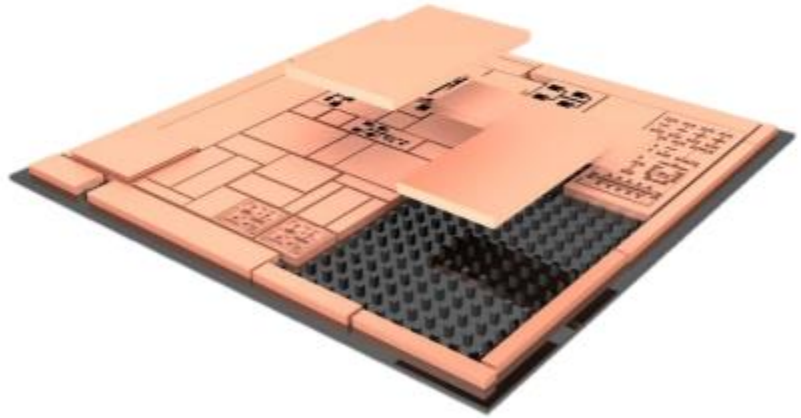


Image: Intel

Tomorrow – Modular



CHIPS is focused on creating modular IP – not new IP!

Chiplet Technology: AIB Interface

- AIB: CHIPS Alliance standard and Industry de facto die-to-die standard
- From Intel/DARPA roots to a central technology of the State-of-the-art Heterogeneous Integrated Packaging (SHIP) project

Device with AIB	Process	Status
Intel® Stratix® 10 FPGA	Intel 14	Production
L-tile 17G SERDES	TSMC 20	Production
H-tile 28G SERDES	TSMC 20	Production
E-tile 56G SERDES	TSMC 16	Production
Intel® Agilex™ FPGA	Intel 10	Sampling
P-tile PCIe Gen4/UPI	TSMC 16	Production
University offload ASIC	TSMC 16	Powered up
Jariet ADC/DAC	GF 14	Powered up
Ayar Labs Photonics I	GF 45RFSOI	Powered up
University & IP Test Chip (University, Blue Cheetah*)	Intel 22	Powered up
Intel® High Performance Computing	TSMC x	In progress
Customer I	Intel 22	In progress
Ayar Labs Photonics II	GF x	In progress
Ayar Labs Photonics III	GF x	In progress
Customer II	Intel 22	In progress
Customer III	Intel 22	In progress
R-tile PCIe Gen5/CXL	Intel x	In progress
F-tile 116G SERDES	Intel x	In progress
Commercial	TSMC x	In progress
University	Intel 22	In progress
Intel® next generation FPGA and eASIC™ devices	Intel x	In progress

Today

* Settaluri, K., Kehlet D., "Automated Mixed-Signal PHY Generation of the AIB Die-to-Die Interface," Design Automation Conference (DAC) 2020, Chiplet Integration Tutorial, July 2020

DARPA CHIPS and Standardization Takeaway

- Government stepped in when industry could not make a standard on its own
- Chiplet architecture allowed us to add powerful new capability to an existing SoC, ahead of cycle for the next generation

State of the art Heterogeneous Integrated Packaging (SHIP) Project & Second Generation Chiplet Concepts

Chiplet Design Technologies

- First Generation Chiplet Accomplishments
  - Chiplets are extending Moore's Law
  - Chiplets are commercially viable from multiple silicon suppliers
  - Standardization with the AIB interface is enabling an emerging ecosystem
- Starting on Second Generation Chiplets
  - Scale up to die-to-die bandwidth requirements of new wireless and optical systems with AIB 2.0
  - Flow down SoC concepts like security to chiplets
  - Provide a more complete framework of hardware for chiplet developers

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1]."

Gordon E. Moore

1: 3rd Page of Moore's 1965 paper, "Cramming more components onto integrated circuits"

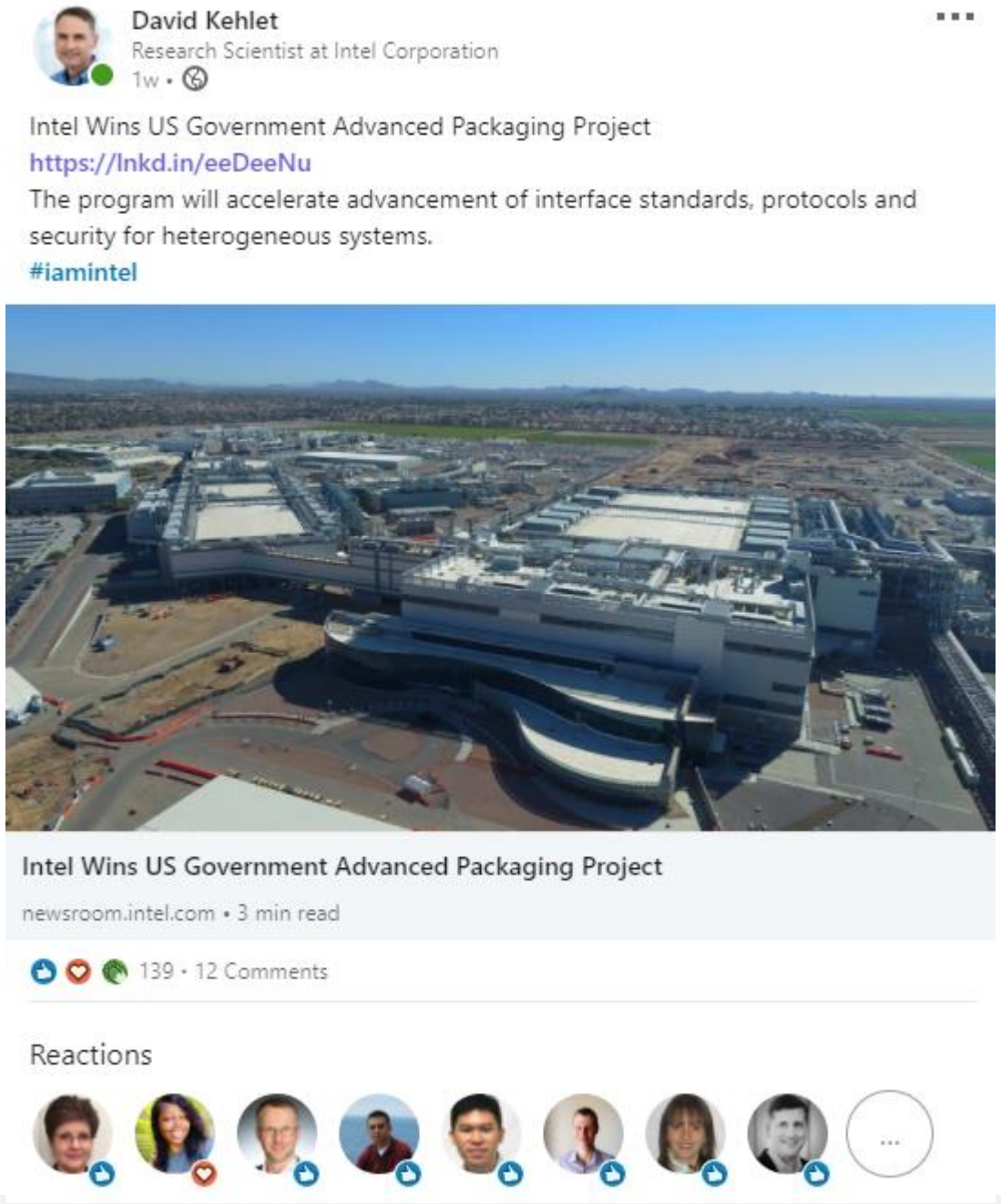
Chiplet AIB Interface Standards

SHIP

intel newsroom October 2, 2020

What's New: The U.S. Department of Defense has awarded Intel Federal LLC the second phase of its State-of-the-Art Heterogeneous Integration Prototype (SHIP) program. The SHIP program enables the U.S. government to access Intel's state-of-the-art semiconductor packaging capabilities.

- SHIP is about packaging and manufacturing, right?
- Also about chiplet interface standards, protocols and security!



Chiplet Design Technologies

- Ecosystem development to enable partners to develop and use chiplets
  - Chiplet interface standards
  - Protocols for chiplet communications
  - Security on a chiplet scale
- Builds on Intel's chiplet ecosystem development and heterogeneous integration experience

Applications Need More Bandwidth

Case	Tx+Rx Gigabits per Second
AIB 1.0 on Stratix 10 FPGA (24 channels of 20Tx, 20Rx)	1920
Jariet Baldwin ADC/DAC (4 channels) [1]	5120 !
Ayar Labs TeraPHY (10 TX/RX macros) [2]	5120 !

Image: Ayar Labs, Inc.

- Advanced Interface Bus (AIB) 2.0 is being developed to meet the demands of high performance applications

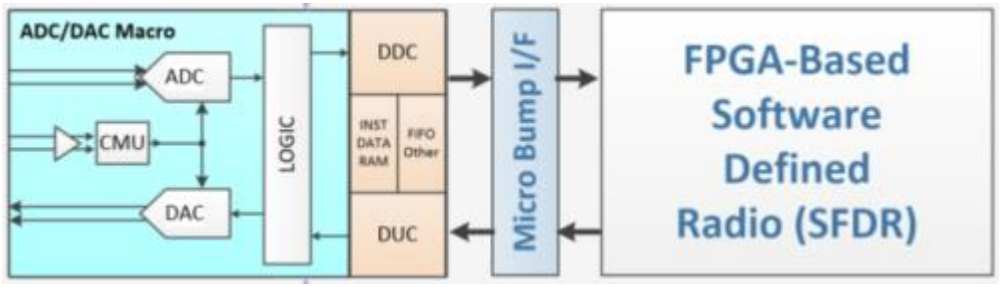


Image: Jariet Technologies, Inc.

[1] Hornbuckle, C., "Ultra-High Speed Direct RF Sampling ADCs and DACs for Heterogeneous 2.5D Integration," ERI, DARPA Microsystems Technology Office, July 2018

[2] Wade, Mark, et al., "TeraPHY: A Chiplet Technology for LowPower, High-Bandwidth In-Package Optical I/O", IEEE Micro, March/April 2020

Chiplet Design Technologies

- New Chiplet Interface Standard Version
  - AIB 2.0 for advanced packaging
- Externally facing standards
  - See https://github.com/chipsalliance/AIB-specification
- Continues to support an unmatched portfolio of chiplets!

Chiplet AIB Interface Standard

Intel and CHIPS Alliance

- Standard setting organization home of the AIB specification
- The CHIPS Alliance AIB specification and CHIPS Alliance AIB hardware open source project align with the CHIPS Alliance objectives[1]:

  "The mission of the CHIPS Alliance is to develop high-quality, open source hardware designs relevant to silicon devices and FPGAs."

  "By creating an open and collaborative environment, CHIPS Alliance shares resources to lower the cost of development."

- CHIPS Alliance Members[1]:

Mentor A Siemens Business, QuickLogic, Yale University, intel, Alibaba Group, Google, SiFive, Western Digital, antmicro, codasip, FUTUREWEI, SAMSUNG, Esperanto TECHNOLOGIES, imperas, qamcom, Hochschule für angewandte Wissenschaften München, 24h OpenROAD, UC San Diego, Berkeley University of California, MERL, Universidad Nebrija

1. Source: chipsalliance.org

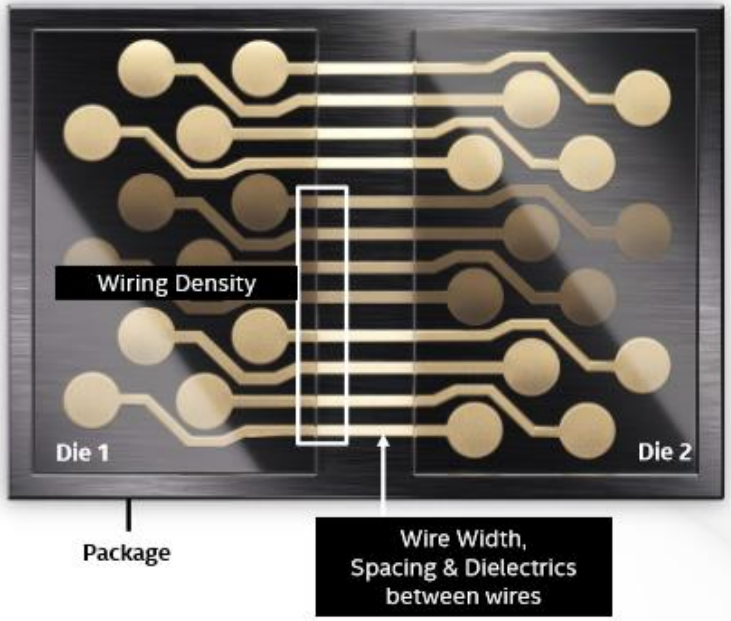
AIB 2.0: A Second Generation Die-to-Die Interconnect

- https://github.com/chipsalliance/AIB-specification

At 4Gbps/wire, 7.68Tbps (Rx+Tx) bandwidth per interface

Enabling an Ecosystem

High density die-to-die interconnects



Feature	AIB 1.0	AIB 2.0
Bandwidth/wire (Gbps)	2	Up to 6.4
Bump density (um)	55	55/45/36
Bandwidth/mm shoreline (Gbps/mm)	256	1638
IO Voltage (V)	0.90	0.90/0.40
Energy/bit (pJ/bit)	0.85	0.50
Backward Compatibility	n/a	1.0

AIB Generator available at: **github.com/chipsalliance**

intel | TECHNOLOGY PILLARS

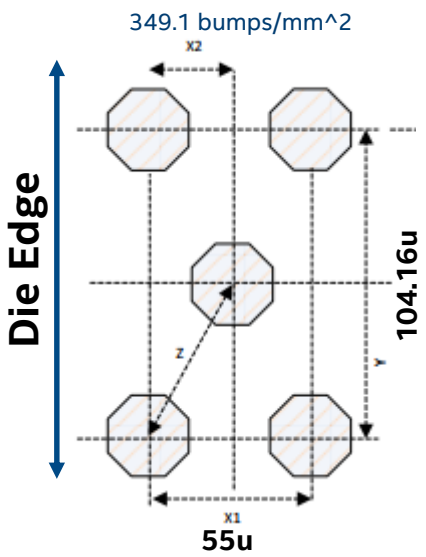
Architecture Day 2020

Images: Intel

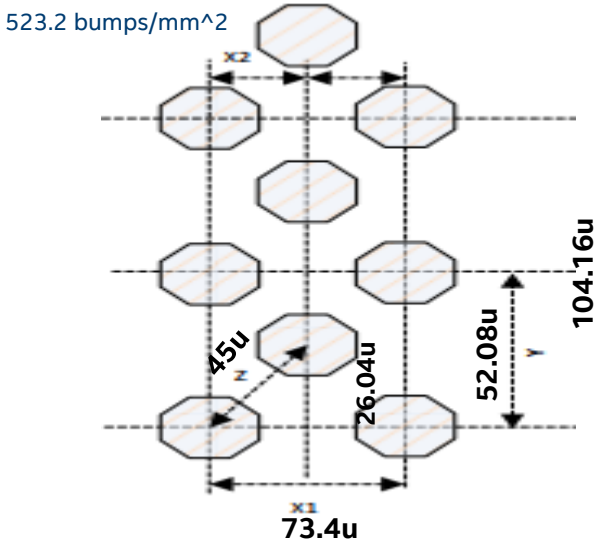
Chiplet Technology: Fine Pitch Microbumps

AIB 1.0

AIB 2.0

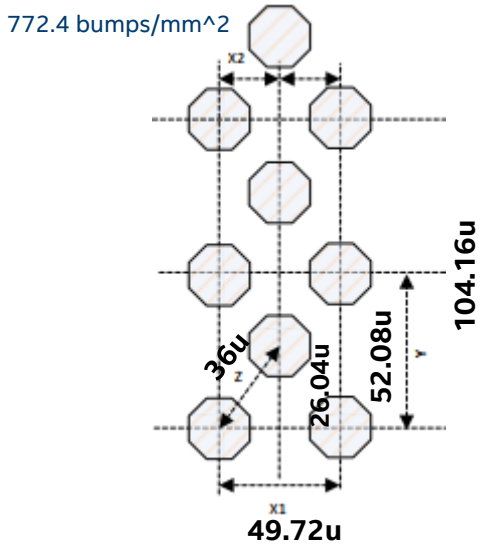


55u Spacing



45u Spacing

Same Die Edge spacing as 55u to maintain physical compatibility



36u Spacing

Same Die Edge spacing as 55u to maintain physical compatibility

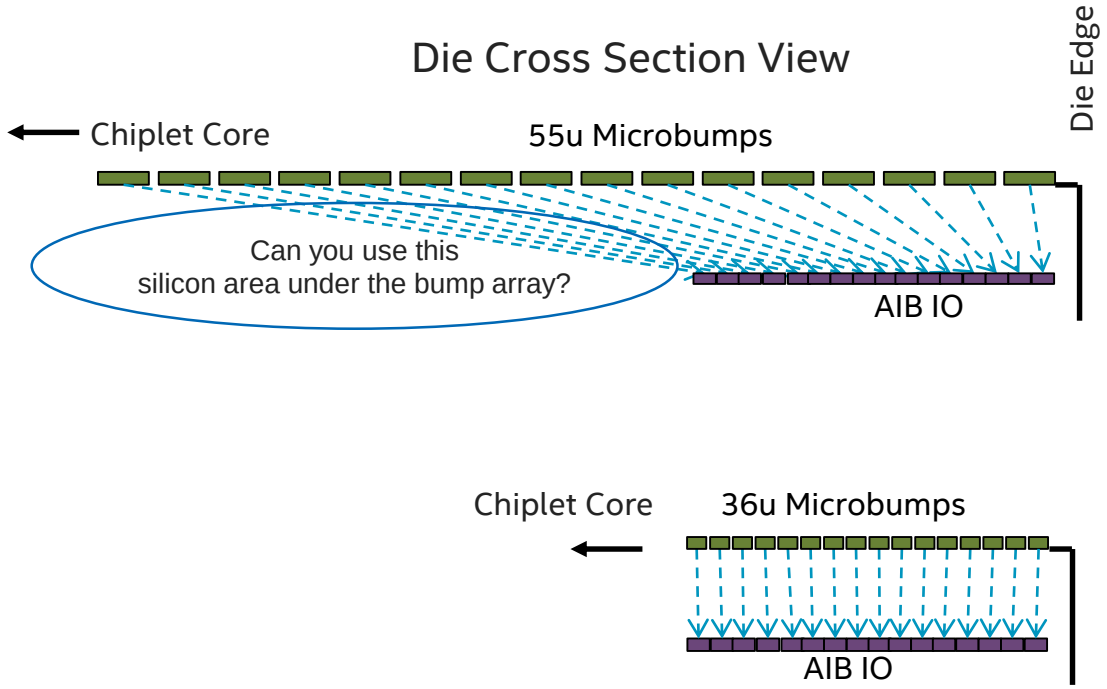
Any of 55u, 45u, 36u can be combined compatibly

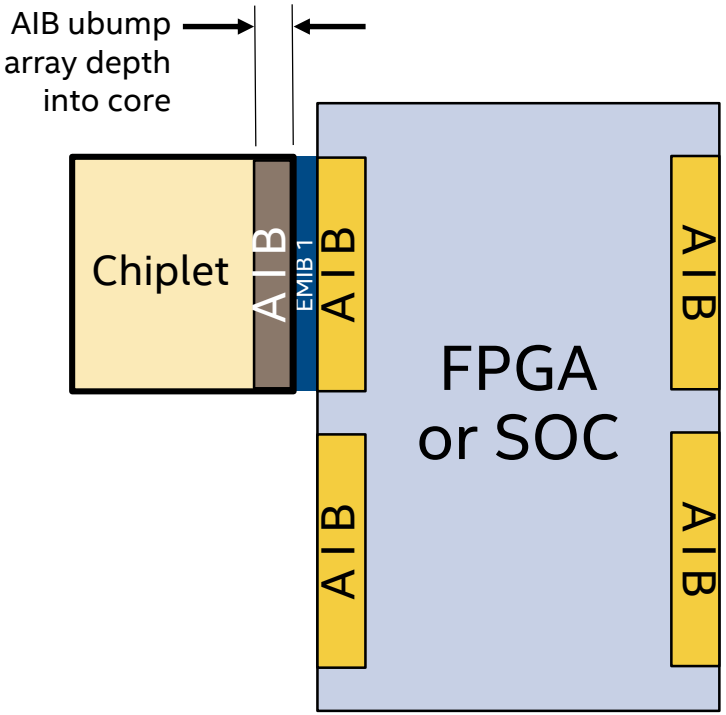
Interposer, bridge, or substrate provides “straight-line” gasketing

Chiplet Technology: Reducing Interface Area

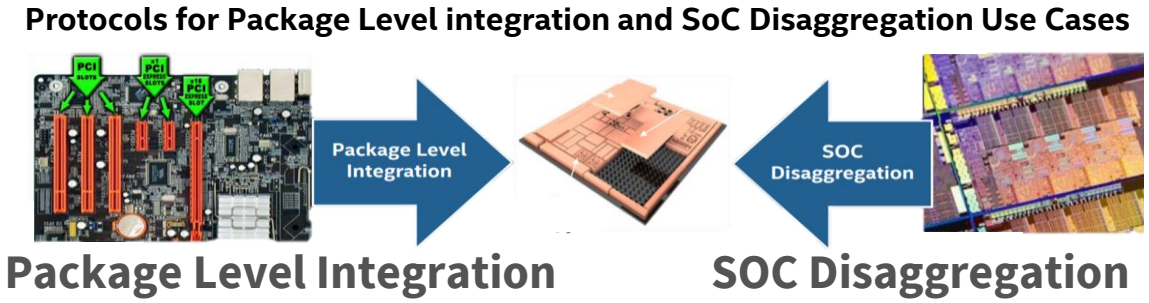
- Smaller bump pitch → smaller bump array depth into core → less Si area needed for AIB

Microbump Pitch	AIB ubump array depth into core
55u	1.27mm
45u	0.881mm
36u	0.596mm





Chiplet Protocols for Two Broad Use Cases

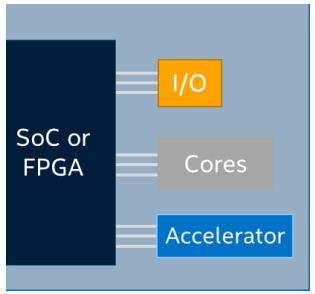


Package Level Integration

- Commonly attached to CPU
- Currently PCIe boards
- Developers want a coherent memory model
- Example: CXL

SoC Die Disaggregation

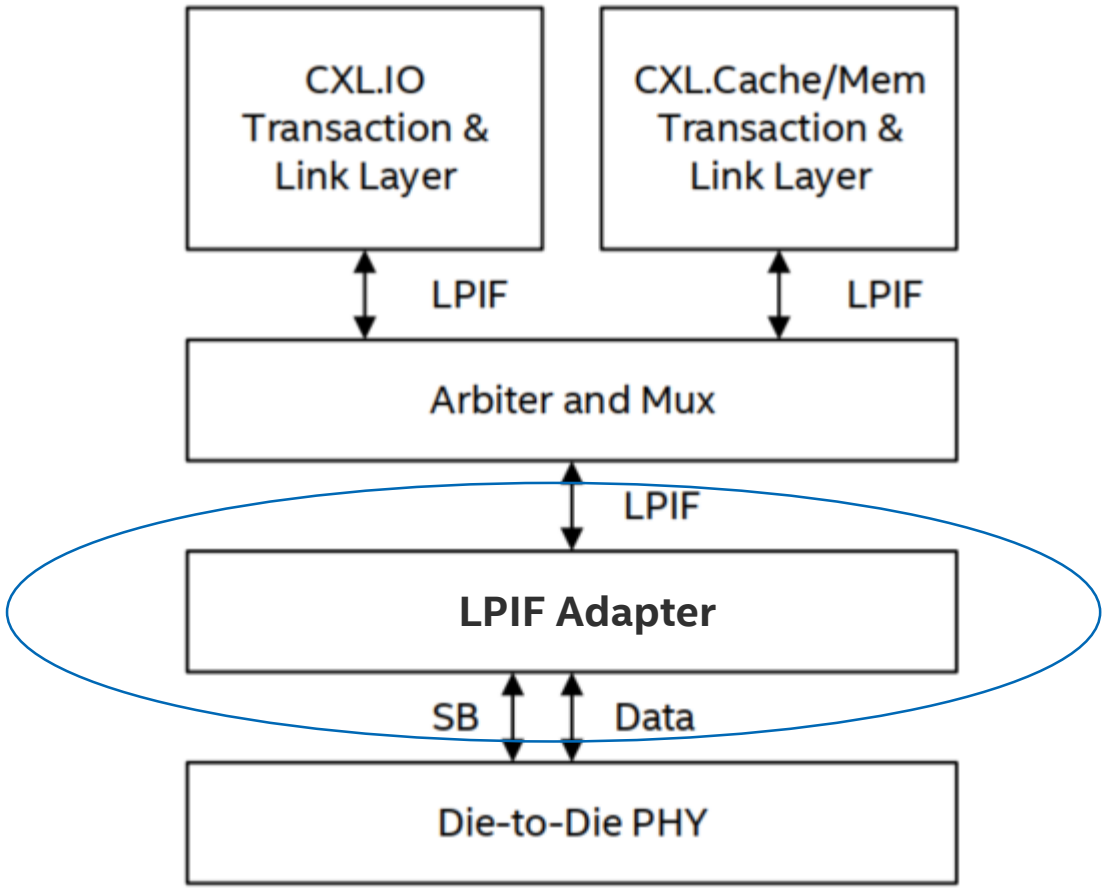
- Currently on die module-to-module
- ASIC developers like their AXI-style existing lightweight protocols
- Examples: AXI Streaming, AXI4 (Memory Mapped)



Package Level Integration Protocols

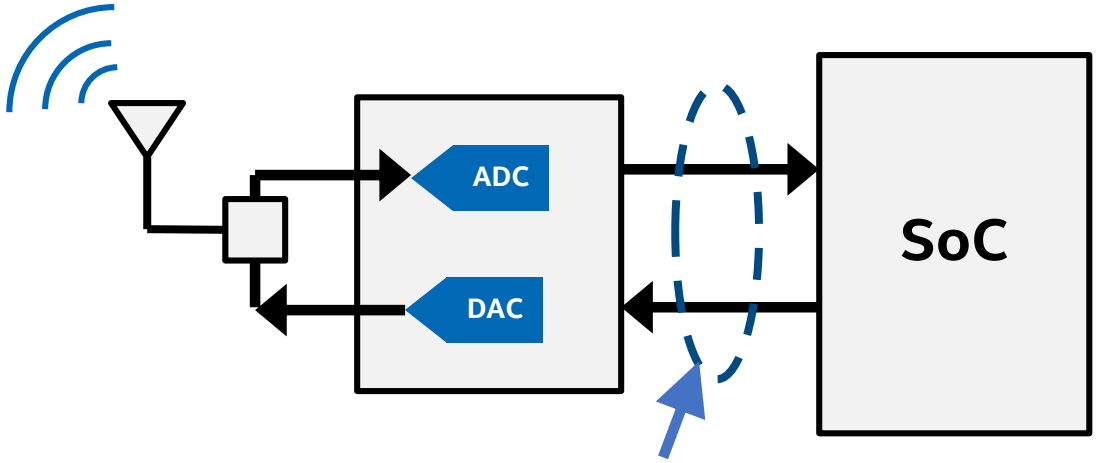
- Package level integration protocols: PCIe, CXL
  - Create LPIF AIB PHY adapter to support Compute Express Link (CXL for shared and distributed memory) and PCI Express controllers
  - CXL and PCIe controllers can be stacked on top of LPIF

Figure 1 LPIF Adapter instantiation with ARB/MUX

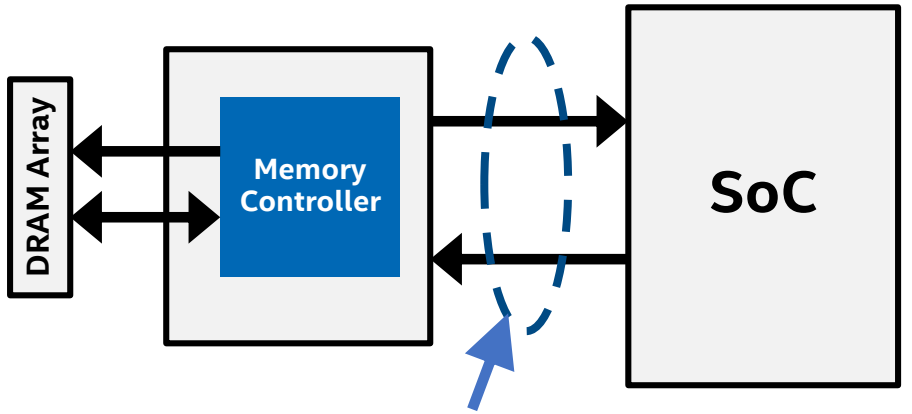


LPIF: Logical PHY Interface
"LPIF Adapter for Die-to-Die Interconnect," Revision 0.5, Intel Corporation, 2020, https://www.intel.com/content/www/us/en/io/pci-express/lpif-adapter-die-to-die-interconnect.html

SoC Die Disaggregation Protocols



- Ideal protocol characteristics:
  - Looks like AXI Stream to the SoC
  - Transfer rate linked to the sample rate (common clock reference)
  - Data arrives every clock
  - Low latency
  - Simple convention on sample packing

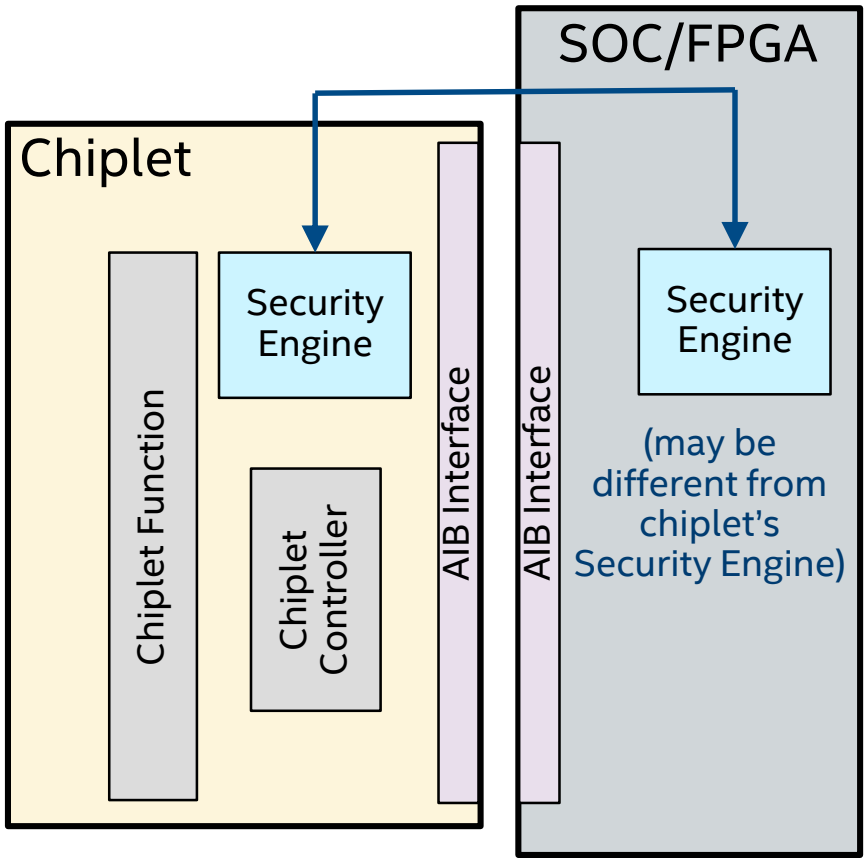


- Ideal protocol characteristics:
  - Looks like AXI-4 (Read/Write) to the SoC
  - Efficiently transports my SoC's reads & writes
  - Low latency
  - Memory clock asynchronous to the transfer clock

Chiplet Design Technologies

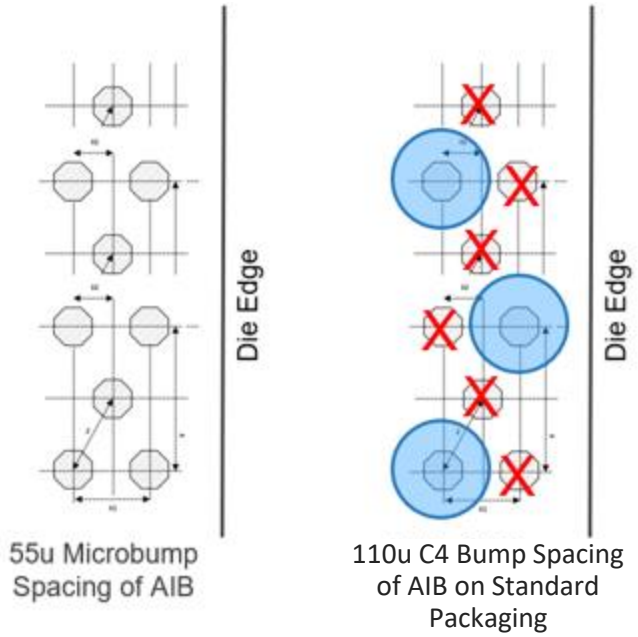
- **Chiplet Security IP**
  - ECDSA, SHA & AES-256 algorithms in a chiplet framework
  - Counters threat models of Firmware IP theft, Unauthorized firmware, Counterfeit or malicious chiplets
  - Chiplet scale: 1mm^2 or less area, fuses for keys, scan/JTAG disable (no PUF)

Chiplet Security brings SoC security concepts to chiplet scale



Concept for Lower Cost

- AIB on standard packaging
- 10Tx+10Rx per channel, vs. AIB 2.0 40Tx+40Rx
  - AIB 2.0 interface: 7.68Tbps
  - AIB on standard packaging: 1.92Tbps
  - 3 layers std vs. 2 layer EMIB, at ¼ bandwidth: advanced packaging wire density advantage reduced to 6x
- Cost vs. bandwidth tradeoff is better for some applications
  - < 1Tbps (today)
  - Cost pressure on wireless



55u Microbump Spacing of AIB

110u C4 Bump Spacing of AIB on Standard Packaging

Conceptual, not actual bump placement

Conclusion: Chiplet Technology for an Emerging Ecosystem

- Chiplet idea is very popular, but chiplets are a lot of work to build!
  - AIB die-to-die interface standard and IP are helping
  - Protocol and utility IP will reduce chiplet effort
- Cost of advanced packaging is driving alternatives
- Investment in chiplet design technologies gives us muscle to continue chiplet leadership


intel