A SiP Standard for Reusable Chiplet Enabled Platforms

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Abstract—A new ecosystem of System in Package (SiP) integration of reusable chiplets (physical IP) is on the horizon. The innovations enabled by this ecosystem benefit a broad range of applications including Government microelectronics use cases.

Today's ecosystem of IP supply is changing from solely enabling a monolithic SoC design capability to now provide SiP IP in the form of fabricated chiplets. This change enables faster development and lower integration costs of dissimilar technology nodes into a single package for higher performance. The emerging SiP chiplet ecosystem requires high density, monolithic-like scalable packaging technologies and multi-vendor interoperability. Intel, as a member of the DARPA CHIPS program, enables the industry to meet these requirements by providing the industry with an open SiP chiplet die-to-die interface standard and assists in developing EDA support required for an ecosystem of reusable chiplets.

This paper reviews SiP enabling technologies including the Intel royalty-free AIB (Advanced Interface Bus) chiplet-to-chiplet interconnect standard as adopted by the DARPA CHIPS program. Using Stratix® 10 FPGAs, which currently supports AIB compliant interfaces, Intel, demonstrates how DARPA CHIPS program is helping the industry to realize an interoperable chiplet based ecosystem for SiP solutions. The paper includes the status of available high density multi-chip packaging solutions. It also includes a roadmap to even higher density interconnectivity and the growth in availability of AIB-enabled IP and how these new developments enable faster innovation in a broad range of applications. Special focus is also placed on the CHIPs demonstration platform incorporating high speed data converter chiplets.

Keywords—SiP; DARPA CHIPS; AIB; ERI; HBM; chiplet; platform; Direct RF; eco-system

I. INTRODUCTION

Rapidly changing and increasing computing workloads and emerging applications require an ever-increasing pace of innovation for system designers. The semiconductor industry as a result is faced with increased device development cycles, longer TTM (time to market) and increased NRE (non-recurring expense). In high performance compute, wireless and EW (electronic warfare) the required pace of innovation might require a TTM on the order of 9 months, yet the development of state of the art monolithic SoC is customary on the order of 2+ years with NREs often in the $100s millions. Industry is at inflection point where required pace of innovation is much shorter than that achievable through monolithic SoC development.

A. Cost and Performance Disparity in Scaling:

As shown in Figure 1 feature size scaling has been far more aggressive for silicon technologies than for board or package technologies. As feature size disparity between silicon and package/board technologies grew the need for serialization of data transfer is necessitated. Moreover, the data requirements also increased enabled by faster semiconductor technologies further compounding the need to serialize data transfers. As a result, more complex serializer/deserializer (SERDES) use prevails, this means the industry endures long analog design optimizationas part of device development. SERDES use increases interface latency and power. Furthermore, as the serial data rate increases, a non-linear power penalty is often traded-off against the SoC need to be in the latest and emerging digitally optimized semiconductor node which results in overall:

1. Increased complexity, system latency and power
2. Long coupled development cycles for analog and digital on same monolithic die

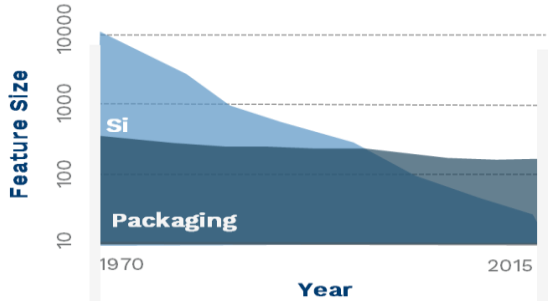

Figure 1: *Technology Si vs. Package/Board Feature Scaling*

In a current designs of high end SoC devices, a SERDES at full chip level can consume approximately 30% of the die area and often in excess of 30% of the power budget. It is instrumental to examine (Bandwidth density)/(Energy) Figure of Merit (FoM), as illustrated in Figure 2 for two cases, On-Board as in PCB traces and intra SoC as in on-die communication. For On-Board communication PCI-E SERDES is taken by way of example, which consumes ~0.3mm of die edge shoreline and ~20pJ/bit (PMA+PCS) energy at a 16Gbps line rate; it can drive 1000mm.

FoM=(16Gbps/0.3mm)/(20pJ/bit)=2.7

Point "1" in Figure 2 shows this FoM region. As specific SERDES implementations can vary in performance from the one selected, the circled region generalizes the overall On-Board solution space. Latency of 100ns is rather common for PCI-E. Point "2" in Figure 2 is SoC on-die communication FoM region for a 14nm technology node. Within a SoC, to communicate ~1mm of distance, it requires approximately 12 inverters, 2 D-type flip-flops and 2 multiplexers. Circuitry would occupy roughly 1um of the shoreline operating at 2Gbps at 0.1pJ/bit for 1.5ns of latency.

FoM=(2Gbps/0.001mm)/(0.1pJ/bit)=20,000

Similarly, to On-Board communication, the SoC solution circle accounts for process and implementation variations. Examining both solution circles, a significant disparity is observed as:

1. ~10,000x Bandwidth Density/Energy FoM
2. ~100x Latency

SERDES-based communication is prohibitory expensive especially if short intra package distances are considered.

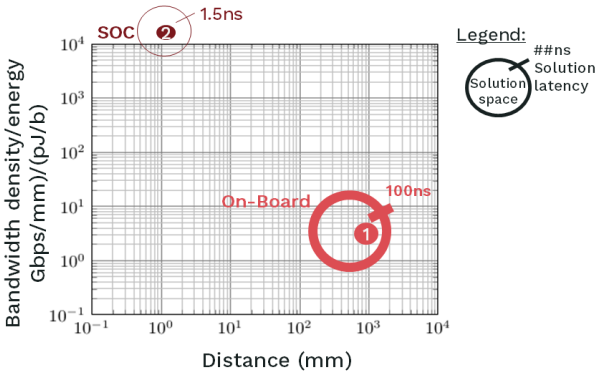

***Figure 2**: Interconnect Figure Of Merit (FoM)*

At SERDES data rates beyond 56Gbps, PAM encoding is used and necessitates a forward error checking(FEC) requirement which, in turn, further increases power and latency. As data rates increase beyond 112 Gbps per differential pin pair, electrical input/output (I/O), performance fast approaches critical limitations of signal integrity inherently imposed by a pin-count-constrained package. Furthermore, the demand for higher data rates increases the challenge and compounds other issues of importance such as physical reach, electromagnetic interference (EMI) immunity and the power consumed for the link. Meanwhile, SoC technology scaling improves the on-die communication FoM and as a result, Points 1 and 2 in Figure 2 are expected to further diverge over time.

B. DARPA CHIPS and 3rd Page of Moore's Law paper

"Is this the end of Moore's Law?" some may ask …. In 1965, at the end of the 3rd page of his now seminal paper [5], Gordon Moore writes *"…It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected"* which he argues *" … should allow the manufacturer of large system to design and construct a considerable variety of equipment both rapidly and economically."* As pointed out in Figure 1, it is a disparity in package scaling to that of Moore's law silicon scaling that is responsible for significant system level performance degradation. It is natural to ask at this point if packaging technology could allow rapid scaling?

Intel in conjunction with other CHIPS collaborators, worked with the Defense Advanced Research Projects Agency (DARPA) to enable an industry-wide CHIPS vision of an ecosystem of discrete modular, reusable IP blocks, which can be assembled into a system using existing and emerging Multi-Chip Package (MCP) integration technologies. The program goal is to enhance overall system flexibility and reduce design time for next-generation products. The foundational assumptions are that:

- the system can be sub-divided into chiplets
- a high-performance system can be created via the heterogeneous integration of chiplets
- a high-density packaging technology is available to support integration.

If the above assumptions hold true, then 53 years past the publication of Gordon Moore's seminal paper, heterogeneous integration would now become feasible to allow to increase the pace of device developments thereby TTM at a significantly reduced NRE to extend Moore's law beyond just lithographic scaling of silicon.

C. High Density Packaging Technology enables Heterogeneous Integration at SoC-like FoM

Embedded Multi-die Interconnect Bridge (EMIB) [6] is cost-effective approach to in-package high density interconnect of heterogeneous chiplets. This MCP approach is often referred to as 2.5D package integration. Figure 3 shows more detail on this physical technology approach.

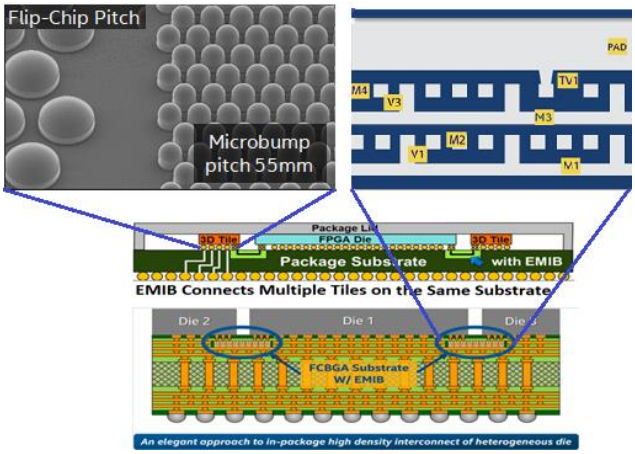

***Figure 3**: Intel EMIB for Heterogeneous Die Integration. Top left: coplanar mixed bump pitches; Bottom EMIB-based high density package cross-section; Top right: EMIB cross-section.*

EMIB allows for mixed bump pitches between those used in conventional flip-chip packaging and tighter micro-bump pitch needed to support high density routing. In initial EMIB deployments, two routing layers for signals at 2um signal width and spacing were utilized. At 2Gbps per signal, that gave a maximum bandwidth density across two layers of 1Tbps/mm of shore line. The remaining two layers are used for power and

ground. A plan view of the heterogeneous assembly of chiplets, such as Intel® Stratix® 10 programmable MCP platform shown in Figure 4. In this example, one Stratix® 10 FPGA chiplet connects to six SERDES chiplets using six EMIB interconnects. Advance Interface Bus (AIB) [2] is the electrical signaling layer used to connect the chiplets. While this MCP platform leverages Intel's EMIB technology, AIB interfaces are defined to work equally well with alternative MCA technologies, such as a Standard 2.5D Silicon Interposer as shown in Figure 5.

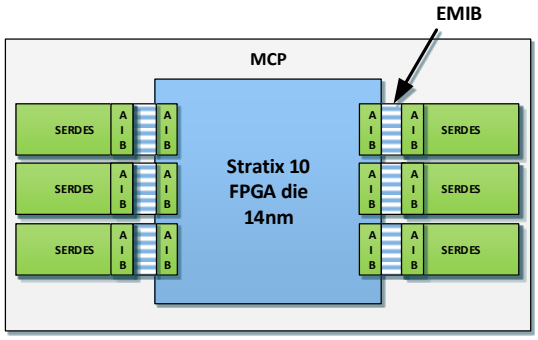

***Figure 4**: Intel® Stratix® 10 MCP Platform*

The silicon interposer in a typical 2.5D package shown as a dark shaded area in Figure 5 is normally a silicon die larger than any one of the interconnecting dies. In contrast, the silicon bridge die used in EMIB can be much smaller than the connected chiplets as it is only used under the edges of the two interconnecting chiplets.

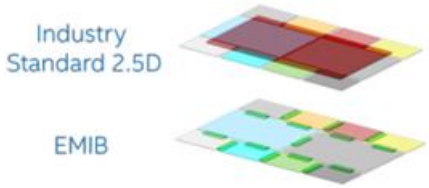

***Figure 5**: Intel® EMIB and Industry Standard 2.5D Technologies (top);*

EMIB allows for most size die to be attached in multiple directions thus eliminating most additional physical constraints on the heterogeneously used chiplets. With just a localized high-density Si-base interconnect region of the chiplet used only for die-to-die connectivity, the rest of the package and chiplets are unaffected. This allows for I/O (input output pads/pins) such as, power and RF routing flexibility. Use of multiple EMIB bridges are possible. In the case of a typical standard 2.5D package, all signals travel through the Si interposer to the active die, including sensitive signals such as RF which can unduly impair performance. EMIB does not pose such constraints. A first generation AIB/EMIB interconnect FoM is calculated and plotted on the Figure 6. A 55um microbump pitch is used, AIB I/O design supports drive for an average EMIB length of a few millimeters resulting in 0.8pJ/bit (1100 transition density) at 2.5ns of latency:

FoM=(1Tbps/mm)/(0.85pJ/bit) = 1,250

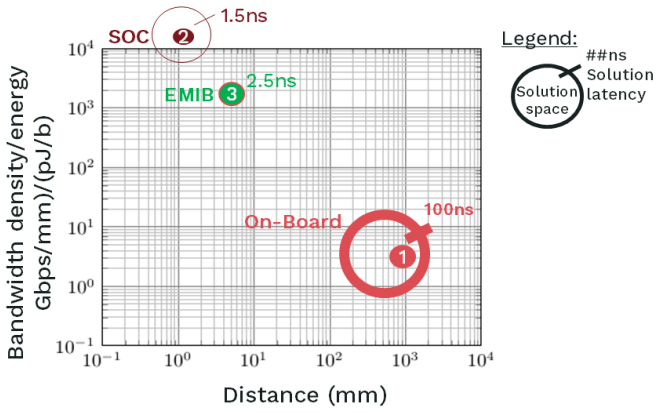

***Figure 6**: High density interconnect FoM*

Nearly three orders of magnitude improvement in the bandwidth density/energy FoM vs. current state-of-the-art designs using on-package wireline transceiver interconnect solutions is shown. There is also nearly two orders of magnitude reduction in latency. AIB and EMIB are key enablers for Intel's PSG commercial programmable heterogeneous integration chiplet platform. AIB is offered royalty to CHIPS adopters as a common interface to create ecosystem of chiplets with plug and play capability [2].

II. AIB, CHOICE OF SIGNALLING

Differential NRZ (Non-Return to Zero) signaling has been the long-term mainstay for data transmission using SERDES links. But as data rates keep increasing, differential NRZ is proving inadequate to cope with the increasing channel losses necessitating the use of new advanced signaling schemes like PAM-4. In this section, the signaling scheme used by AIB is compared against the more conventional schemes that are in use.

In AIB, data bits are transmitted over a parallel bus using single-ended, full-swing signaling. AIB uses a clock-forwarded architecture where the clock is transmitted along with and in the same direction as the data. Shown in Figure 7 is a simple I/O buffer that transmits, and a corresponding I/O buffer that receives the data and clock on the other chiplet. This scheme is suitable for USR (ultra-short reach) and XSR (extra-short reach) channels, see Figure 10 for definition of reach.

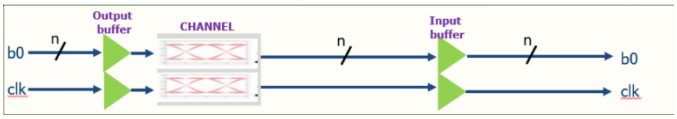

***Figure 7**: AIB Signaling Scheme - Single-ended, Parallel*

In a differential NRZ scheme, a SERDES IP transmits one bit at a time over two wires differentially. Since the clock is not forwarded with the data, a clock and data recovery (CDR) circuit is needed on the receiver as shown in Figure 8. This is a complex I/O design often comprising of equalization schemes like TX pre-emphasis, linear equalization and DFE to transmit and receive the data effectively.

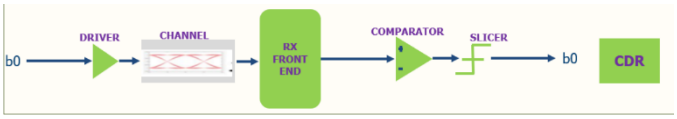

***Figure 8**: Differential NRZ Signaling Scheme*

This scheme is applicable to SR (short reach) and LR (long reach) channels.

PAM4 doubles the data rate by transmitting two bits at a time over the two differential wires without doubling the analog bandwidth. The two bits are encoded as four signal levels, resulting in a signal-to-noise ratio that is worse than NRZ which has only two signal levels. This scheme, shown in Figure 9, is more complex than the differential NRZ scheme because multiple comparators are needed to decode the multi-level signal.

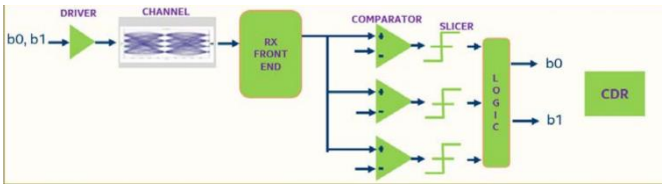

***Figure 9**: PAM4 Signaling Scheme*

As the complexity of the signaling scheme increases, (single-ended, differential, in the ascending order) correspondingly the area, power, and latency also increase. To effectively compare various signaling schemes, a FoM is used. The FoM is a ratio of the area efficiency (Gbps/mm^2) to the energy per bit (pJ/bit). This FoM is plotted against the maximum channel loss (dB) the design can support. A set of designs employing various signaling schemes from published literature is used for the comparison. All these comprise state-of-the-art designs and are representative of the best-case performance achievable, see Figure 10.

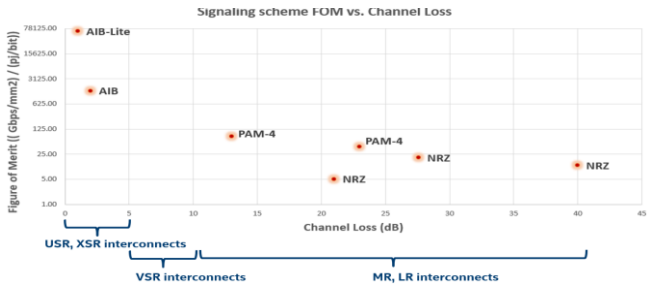

***Figure 10**: Comparison of the Various Signaling Schemes*

PAM-4 signaling based designs are used in the high interconnect loss regions. Because of the high channel loss through the Medium Reach (MR) and Long Reach (LR) interconnects, I/O designs for these tend to be complex with large area and high power. Thus, they have a lower FoM. Single-ended parallel signaling, that is used in AIB has a high FoM and is concluded best for USR channels. AIB-Lite, the short reach version of AIB is discussed later in Roadmap section of this paper.

III. High Performance Use Case

As noted earlier, it can take $100s millions to develop an advanced monolithic SoC therefore could it be possible to combine a sensitive analog IP, such as ultra-high speed Direct RF sampling ADC's (analog to digital converter) and DAC's (digital to analog converter) [7] with a high-performance FPGA [4] using heterogeneous 2.5D integration?

A. Programmable Platform to Reduce Portfolio Cost

In order to comprehensively validate the approach, Intel proposed a heterogeneous MCP platform that includes an FPGA with AIB interfaces. An Intel® MCP based platform with five chiplet options are shown in Figure 11.*Figure 11:* Intel provides the FPGA, wireline transceivers, EMIB interconnects and AIB interface designs to enable heterogeneous integration of third party chiplets. The MCP proposed includes an Intel® commercially available 14nm Stratix® 10 FPGA (Opt1). Two types of wireline transceiver chiplets (Opt2) are made available to support either PCIe and/or Ethernet connectivity. HBM (Opt3) is also made available for integration. Jariet Technologies developed as part of the CHIPS program a Direct RF transceiver (Opt4) as an example of re-usable chiplet for a most challenging massive MIMO application use case. Opt5 is offered as flexible university research platform jointly developed with University of Michigan. In general, chiplets can be any size where subset of AIB interface is instantiated. The platform goal is to reduce barriers to innovation and speed-up time-to-market..

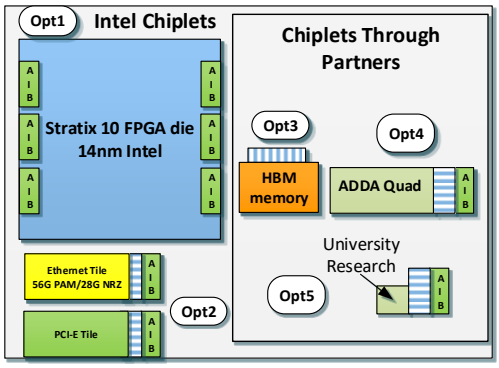

***Figure 11:** Heterogeneous MCP Platform.*

B. Direct RF Sampling

Direct RF sampling is a technique of digitally sampling the radio frequency signals and using digital signal processing techniques to select bands of interest within the RF spectrum. As shown in Figure 12, conventional analog RF mixing typically down converts the desired RF signal band of interest to an intermediate or baseband frequency, which is then converted to the digital domain through ADCs. Direct RF sampling by contrast is a new architecture for radio transceivers enabled by very high sample rate data converters. Applications for wideband Direct RF sampling converters at these sample rates include emerging 5G wireless, radar, electronic warfare, broadband cable and test and measurement equipment.

Direct RF sampling allows for a first Nyquist band of up to half the sample rate of the data converter. The product of the sample rate and the sample bit width of the data converter necessitates a high bandwidth interface requirement especially if four data converters are operating concurrently sharing a common AIB interface. For this reason, DSP to perform digital–up conversion (DUC) and digital down conversion (DDC) is

facilitated on the data converter chiplet as is the case for the CHIPS program.

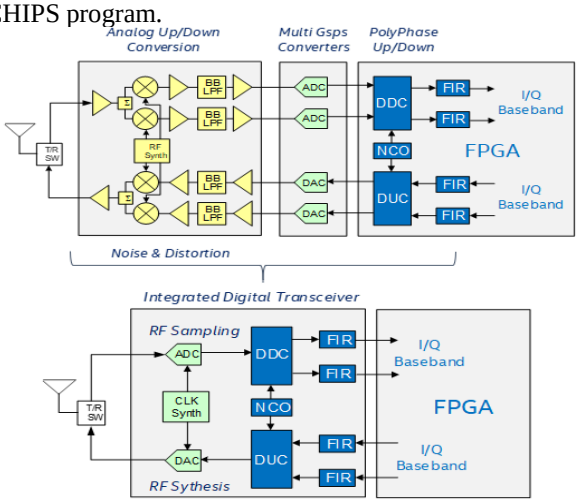

***Figure 12**: I/Q Sampling vs. Direct RF Sampling*

The data converter chiplet comprises four duplex paths of ADC/DAC pairs running at sample rates above 40 Gsps. Each data converter path is accompanied by the requisite digital signal processing of DUC/DDC stages and the appropriate filtering.

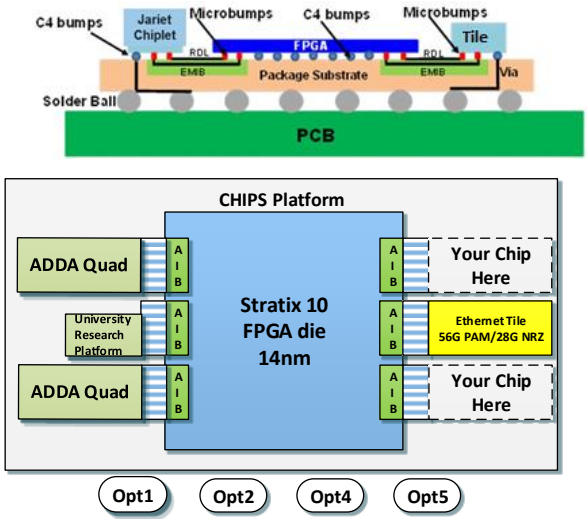

***Figure 13:** DARPA CHIPs MCP Platform with Direct RF data converter chiplets, Ethernet wireline transceiver and University research chiplets.*

Figure 13 includes a cross-sectional view and a plan view of the CHIPS platform. All the RF traces are routed directly from the chiplet through an organic package substrate FCBGA (Flip-chip ball grid array) balls. This allows for routing to be optimized without the constraints of an interposer die. Even so, management of signal integrity is still required. These include maintaining signal impedance continuity from the host PCB to the C4 bumps on the chiplet. Isolation between RF signals and signal which could give rise to EMI interference such as digital I/O, digital power rails and SERDES I/O still must be carefully managed. Advantageously, the AIB interface using EMIB interconnect is sufficient to minimize coupling to the RF signal ports of the data converters. The signal is constrained to be within the die interconnect. The interface used is low power and floor-planned such that the interface is routed to the opposite side of the chiplet from the critical RF ports. The stackup of the organic laminates in the package substrate also allows for the routing of signals of different types to be routed on different layers. RF signals can be isolated from each other and from other signal types as a result. Furthermore, the use of via type stitching structures can also be used to provide further isolation.

The use of an organic substrate has been shown to be sufficient to meet performance goals. The performance goals set out over such an extremely wide RF bandwidth can be met. State-of-the-art packaging technology to date often uses more expensive packaging technology such as LTCC (low temperature co-fired ceramic), and this is now not seen as a critical requirement for such integration.

RF performance of an MCP solution can compare better than monolithic performance or that of more conventional state-of-the-art platform solutions whereby the data converter and RF chips are on a different package to the DSP processing device.

Modular systems will require MCP ability to accommodate a variation of chiplet shapes. Furthermore, chiplets that only partially use an available AIB interface could also be accommodated. This concept is best illustrated by the University Research Platform chiplet included in Figure 13 as part of the CHIPS platform.

IV. Conclusions/Future

Rapidly emerging application specific computing work-loads demand step function improvements in executing integrated system designs over conventional monolithic SoC development to curtail escalating TTM and NRE overheads. Breakthroughs in packaging technologies is shown to approach on-die connectivity capabilities. Programmable commercial platforms with flexible high bandwidth AIB interfaces implemented using high density packaging technology, such as EMIB offers innovation paths not previously realizable for system integrators. An ecosystem of chiplet IP providers can ensure "best of breed" IPs from any foundry and technology node can be combined at fraction of the monolithic SoC cost while at the same time creating breakthrough system performance capabilities.

A. Differentiated Access & National Security Impact

Options for sourcing domestically fabricated advanced process node semiconductors is dwindling. Heterogeneous integration has risen to prominence by now offering a broad range of high-performance plug and play eco-system of chiplets. The US Government contractor base access to domestically produced MCPs complete with DoD application specific chiplets is attainable. Such chiplets can be heterogeneously integrated with a high performance SoC FPGAs and other commercially available chiplets. This leads to a resurgence in performance improvements in electronics system over time, similar, to that achieved through Moore's law geometric scaling achieved by the semiconductor industry over the past 50 years. Furthermore, heterogeneous platform allows mitigation of

supply chain security risks as those outlined in publications such as [7]. While commercial markets will likely adopt these technologies, defense customers will have the opportunity to become first adopters for this emerging high-performance heterogeneous technologies.

B. The Roadmap

Further research on MCPs will likely focus on some key areas, one of which is to improve interconnect FoMs to be ever closer to monolithic performance. As MCP packaging scaling is considered over next few generation, the microbumps are expected to shrink from 55um bump pitches productized today to a 10um bump pitch. It is also expected that there would be a corresponding scaling in the density of package level silicon interconnect from the 2um/2um line width/pitches commercialized today.

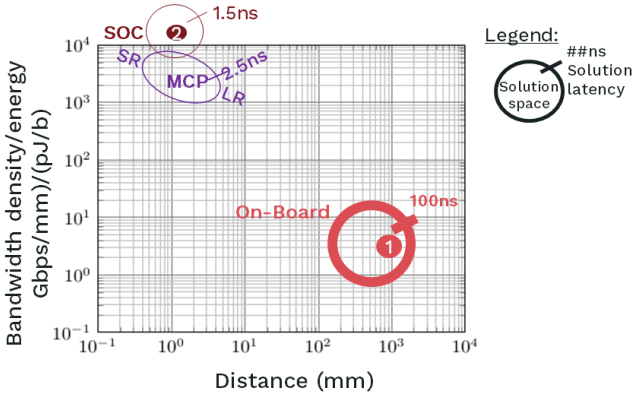

Figure 14: *MCP Interconnect Roadmap FoM*

The projected MCP roadmap interconnect FoM is shown in Figure 14 and when considering two use cases, Short Reach (SR) and Long Reach (LR) covering the range from 0.1 to 10mm to CHIPS connectivity distance. With a modest I/O density assumption of 500IO/mm shoreline used today, a projected energy of SR to LR use cases will range between 0.1 to 1.0pJ/bit.

$FOM_{LongReach}$=(1Tb/mm)/(1pJ/b)=1,000

$FOM_{ShortReach}$=(1Tb/mm)/(0.1pJ/bit)=10,000

This overall MCP performance is plotted in the elliptical region of Figure 14, it approaches an SOC-like FoM.

C. Domain Specific Future

In [9] a detailed case study of FPGAs vs. ASICs and a heterogeneously integrated version of both is shown. This case study concludes that the flexibility expected of an FPGA and efficiency of ASIC is adequately achieved through the heterogeneous integration of a Stratix® 10 FPGA with an ASIC chiplet. This approach can be more effective than developing stand-alone monolithic ASICs. A mix-and-match of domain-specific ASIC chiplets combined with commercial programmable platforms establishes how a low NRE and fast TTM path available for DoD primes to differentiate their application specific solutions. Application specific chiplets can be implemented on any foundry and any technology node to supplement a system solution. Our Vision is to leverage a broad portfolio of commercial chiplet offerings that can be incorporated in solutions for the most demanding DoD systems. The DARPA CHIPS program creates an innovative chiplet ecosystem of industry and academia partners where new business models and partnerships are developed.

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