AIB 2.0 Usage Note

4/28/2022

Legal Information

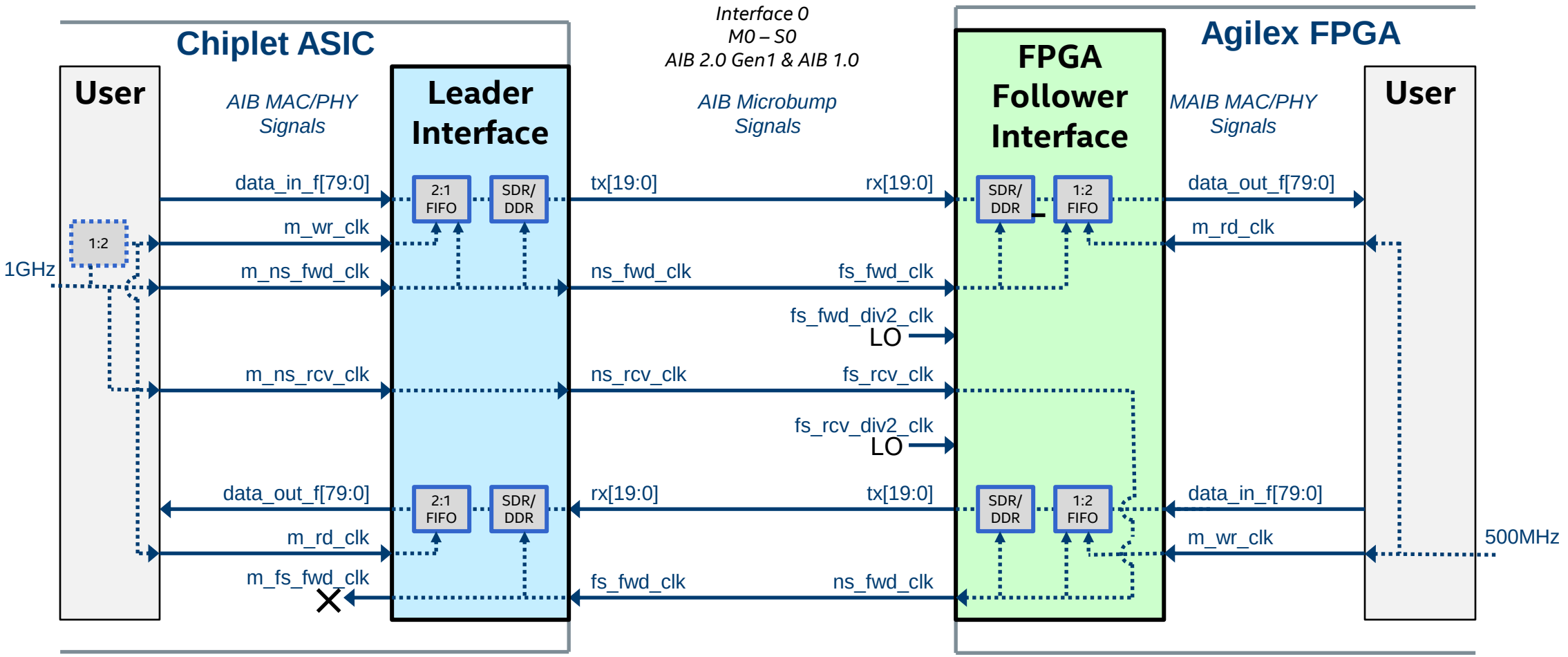
LEGAL DISCLAIMER: Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration. No computer system can be absolutely secure. Check with your system manufacturer or retailer or learn more at intel.com. Software and workloads used in performance tests may be optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information, visit www.intel.com/benchmarks. Results have been estimated based on internal Intel analysis and are provided for informational purposes only. Any difference in system hardware or software design or configuration may affect actual performance. Cost reduction scenarios described are intended as examples of how a given Intel-based product, in the specified circumstances and configurations, may affect future costs and provide cost savings. Circumstances will vary. Intel does not guarantee any costs or cost reduction. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors.

Statements in this document that refer to future plans or expectations are forward-looking statements. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at www.intc.com.

This document contains information on products, services and/or processes in development. All information provided here is subject to change without notice. Contact your Intel representative to obtain the latest forecast, schedule, specifications and roadmaps.

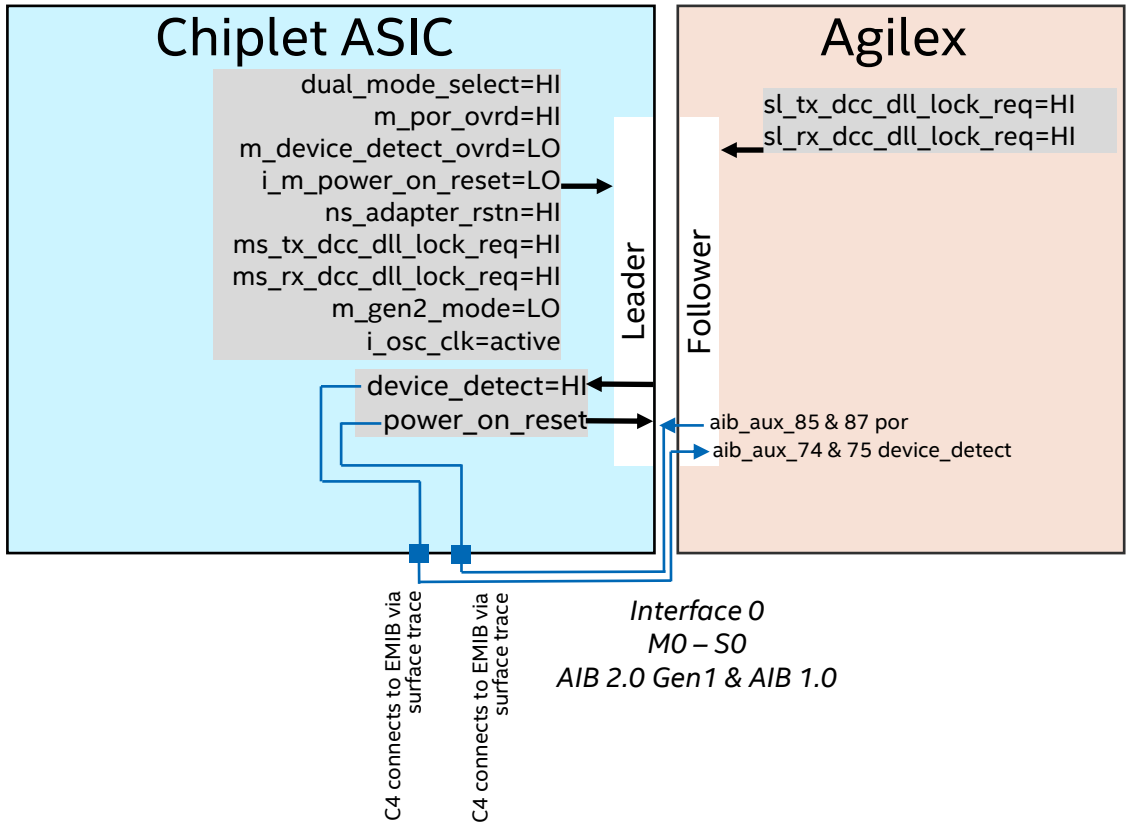
Intel estimated results are based on product specifications. Your costs and results may vary. Intel does not control or audit third-party data. You should consult other sources to evaluate accuracy.

AIB 2.0 in Gen1 Mode, 2:1 FIFO (Half Rate 500MHz) to AIB 1.0 FPGA, 2:1 FIFO (Half Rate 500MHz)

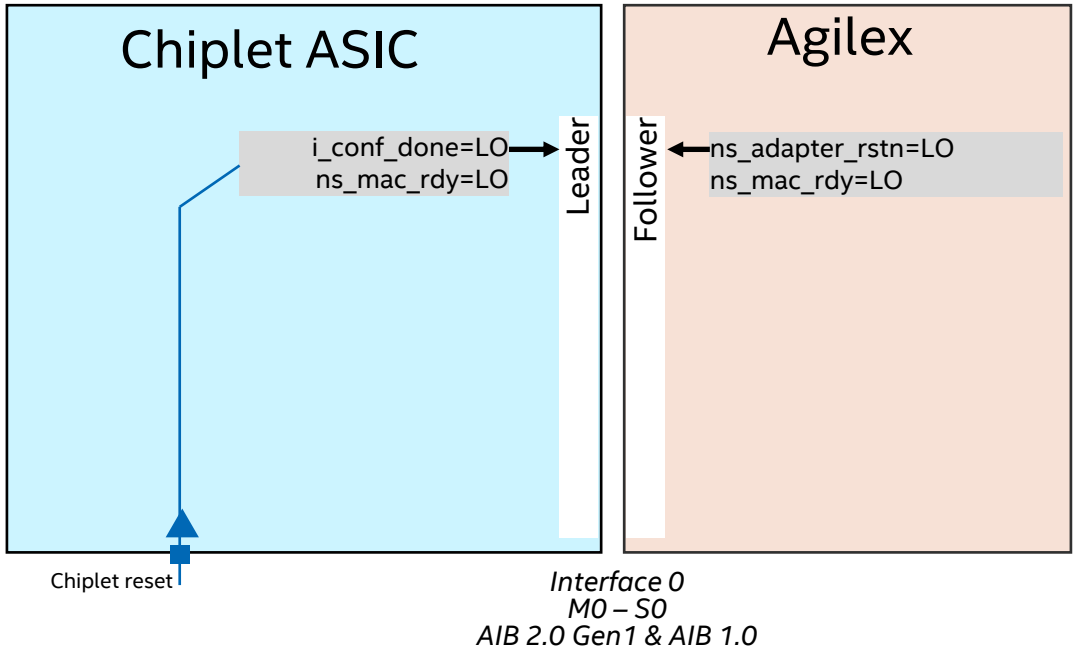


Fixed Settings Determined at Power Up
(does not depend on chiplet or AIB reset)

- These are all static settings, either set by the chiplet application or external resistors
- Since Chiplet ASIC uses C4 bumps for power_on_reset and device_detect, the chiplet does not need to utilize m_por_ovrd and m_device_detect_ovrd. The ovrd AIB inputs are tied inside the ASIC.



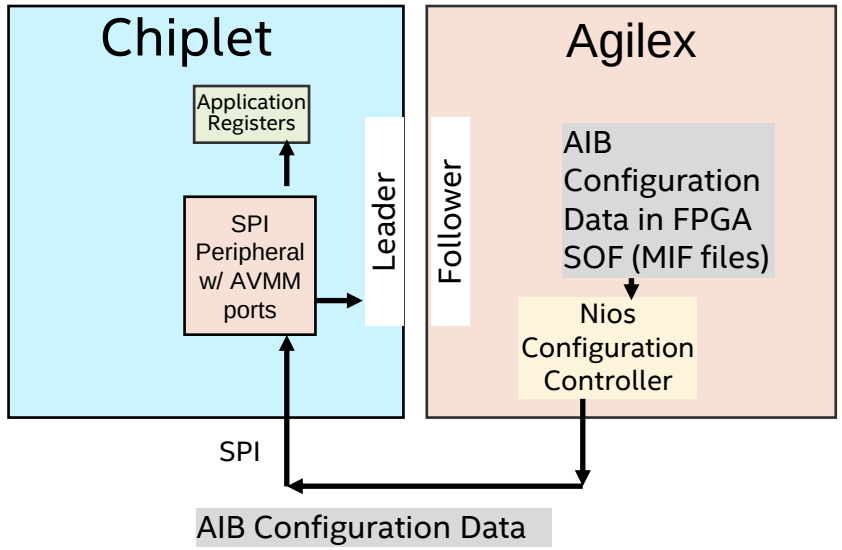
Linked to Chiplet Reset



- i_conf_done signals are controlled by register bits that are reset to 0. See CONF_DONE coming up.
- ns_mac_rdy signals are controlled by the chiplet application, which may take actions based on i_conf_done and may need to wait until, for example, clocks are ready

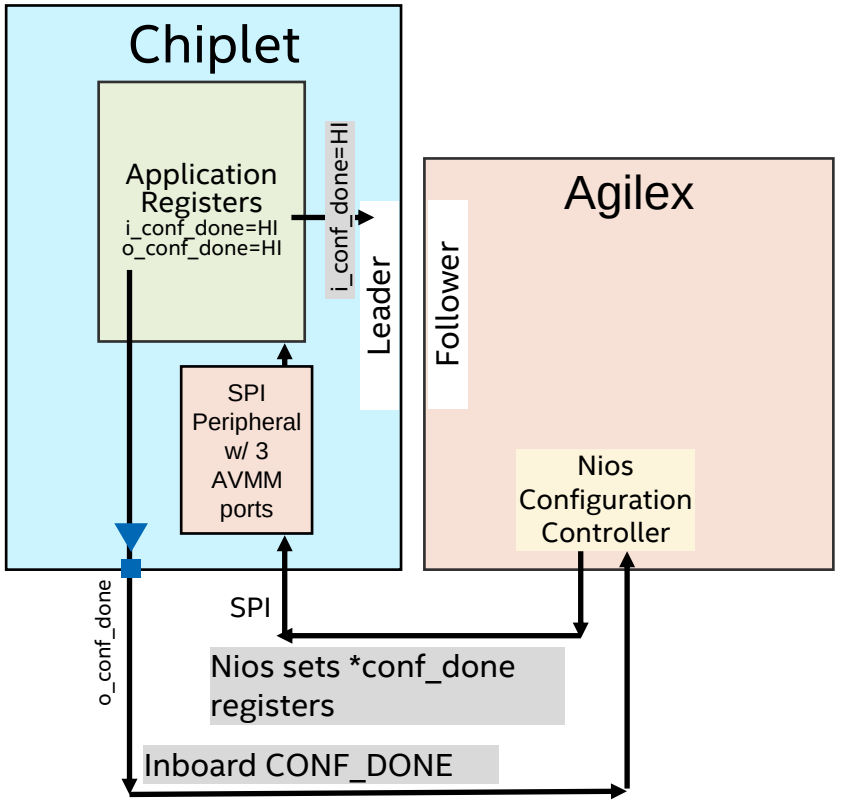
AIB Configuration

Configuration Controller (Typically in FPGA or SoC)
• Chiplet ASIC must ensure the AVMM clock is stable before SPI Follower is brought out of reset**.** • The configuration controller configures all AIB interfaces in an MCP through SPI. • The configuration controller starts using SPI after HI to LO transition on miso. **The HI to LO transition indicates the SPI Follower is out of reset.**



CONF_DONE

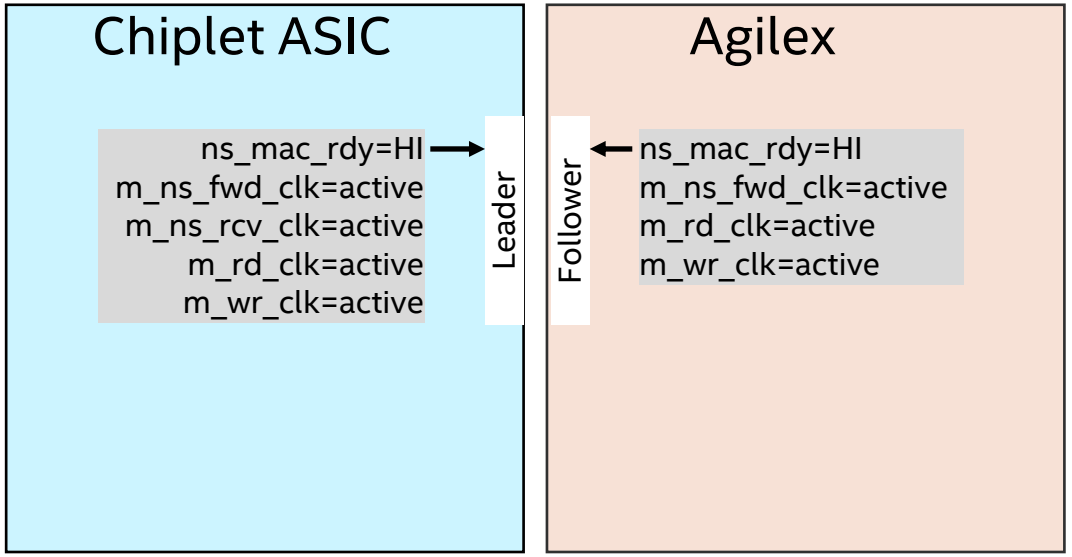
Initialization
• The configuration controller signals the chiplet AIB interface that the configuration is done through a SPI side channel. • The configuration controller sets the Application to PHY signal i_conf_done HI via an application control register



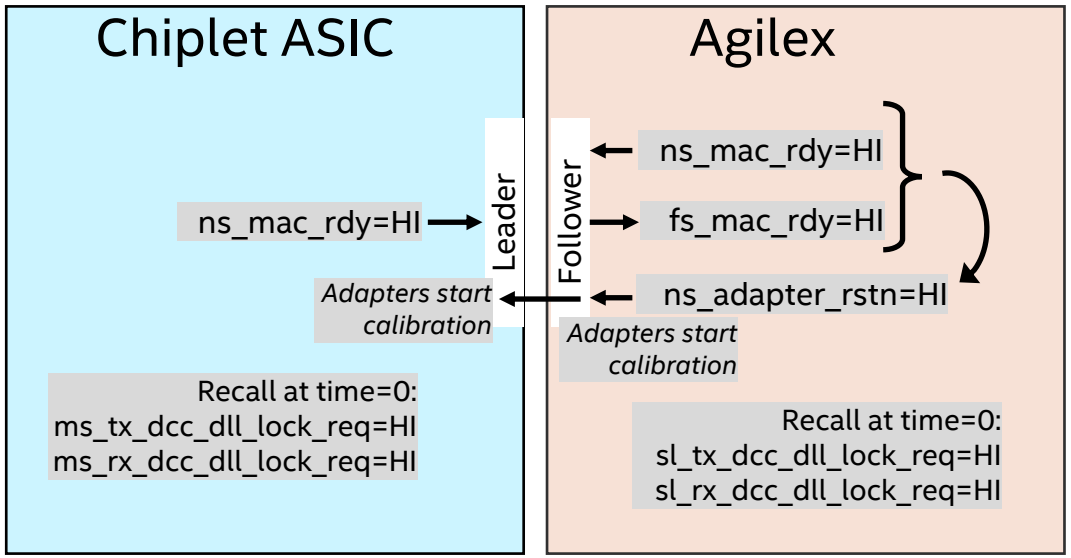
- Since FPGA is in user mode at this time, the MAIB was earlier configured by SOF & SDM/SSM
- Chiplet application *conf_done registers are reset to LO, set HI by the FPGA's configuration controller over SPI

ns_mac_ready

Initialization
• The application brings up all AIB clocks if not done already • Once local clocks are stable, each application MAC sets ns_mac_rdy HI indicating the AIB channel is ready to begin calibration. This action is up to the application which may itself depend on configuration.



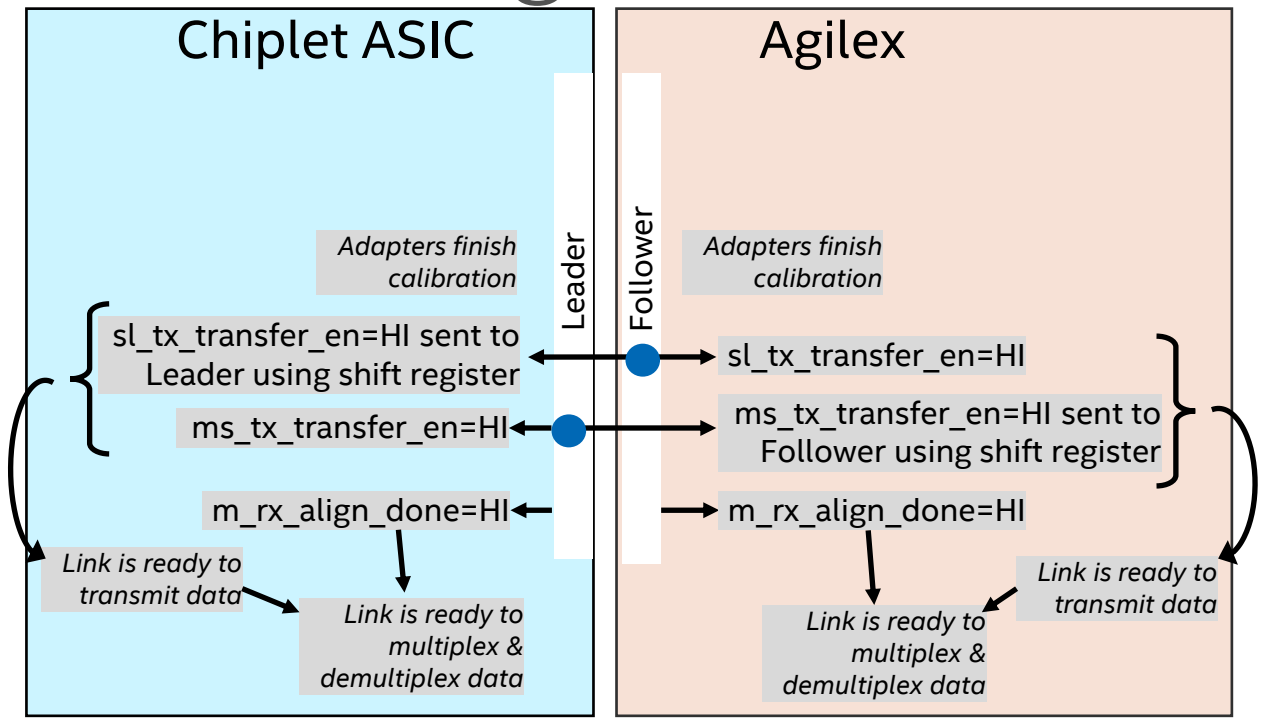
Starting Calibration



- The FPGA application is responsible for controlling ns_adapter_rstn MAC to PHY signals on a per-channel basis

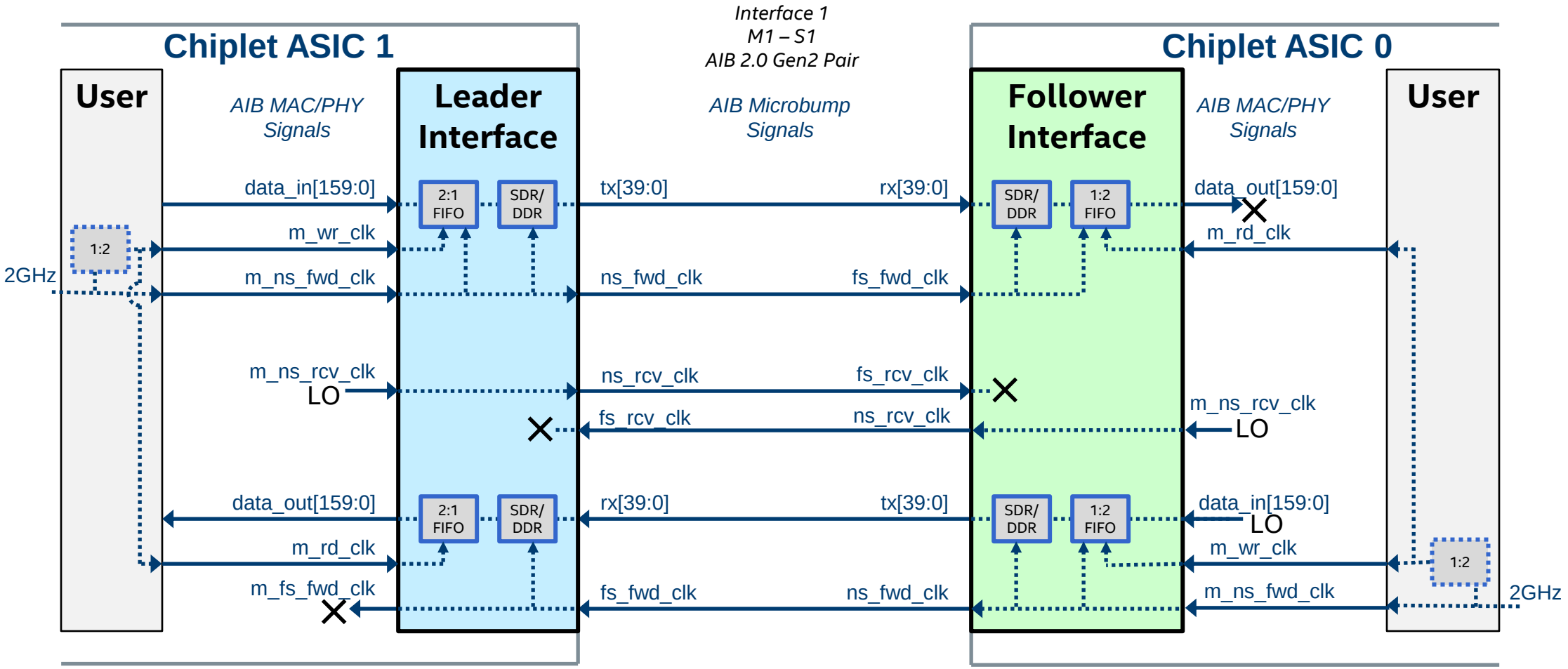
Completing Calibration and Rx Alignment

Common Leader and Follower Initialization
• When both the AIB PHY to MAC signals sl_tx_transfer_en and ms_tx_transfer_en are HI, then the link shall be ready to transmit data. • m_rx_align_done=HI means Rx is aligned to the incoming word marking.



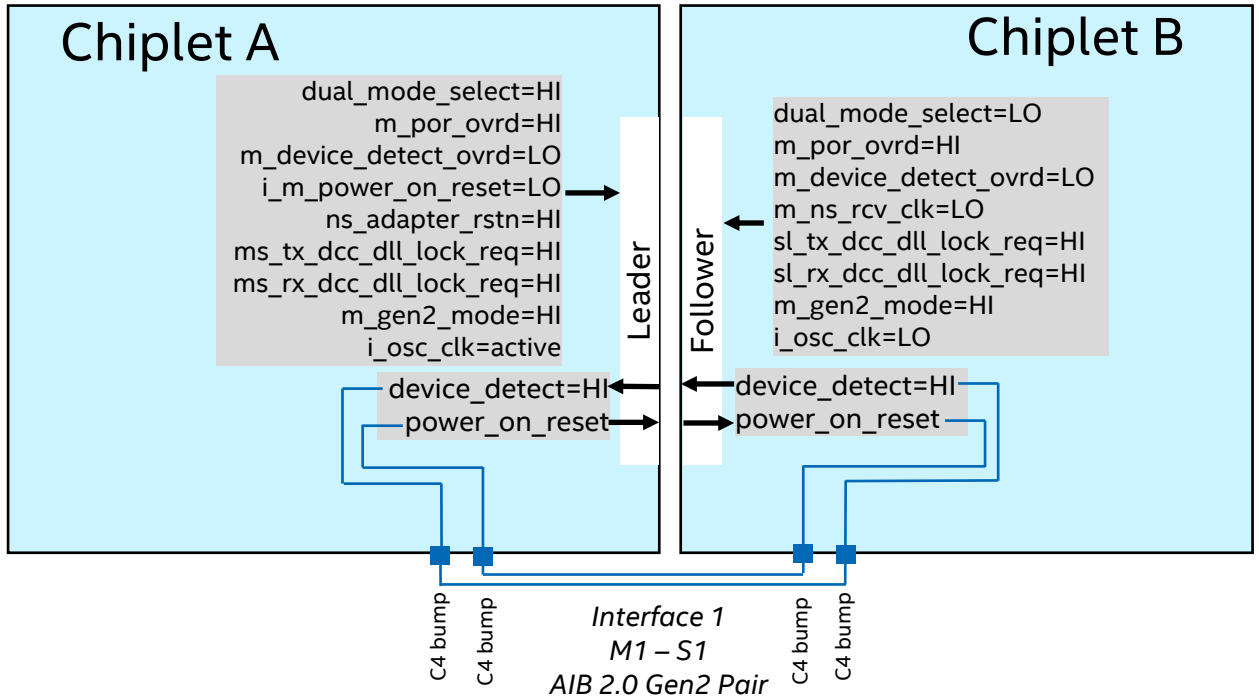
- The application is responsible for reading sl_tx_transfer_en, ms_tx_transfer_en and m_rx_align_done to know when the link is ready.

AIB 2.0 Gen2, 2:1 FIFO (Half Rate 1GHz) to AIB 2.0 Gen2, 2:1 FIFO (Half Rate 1GHz)

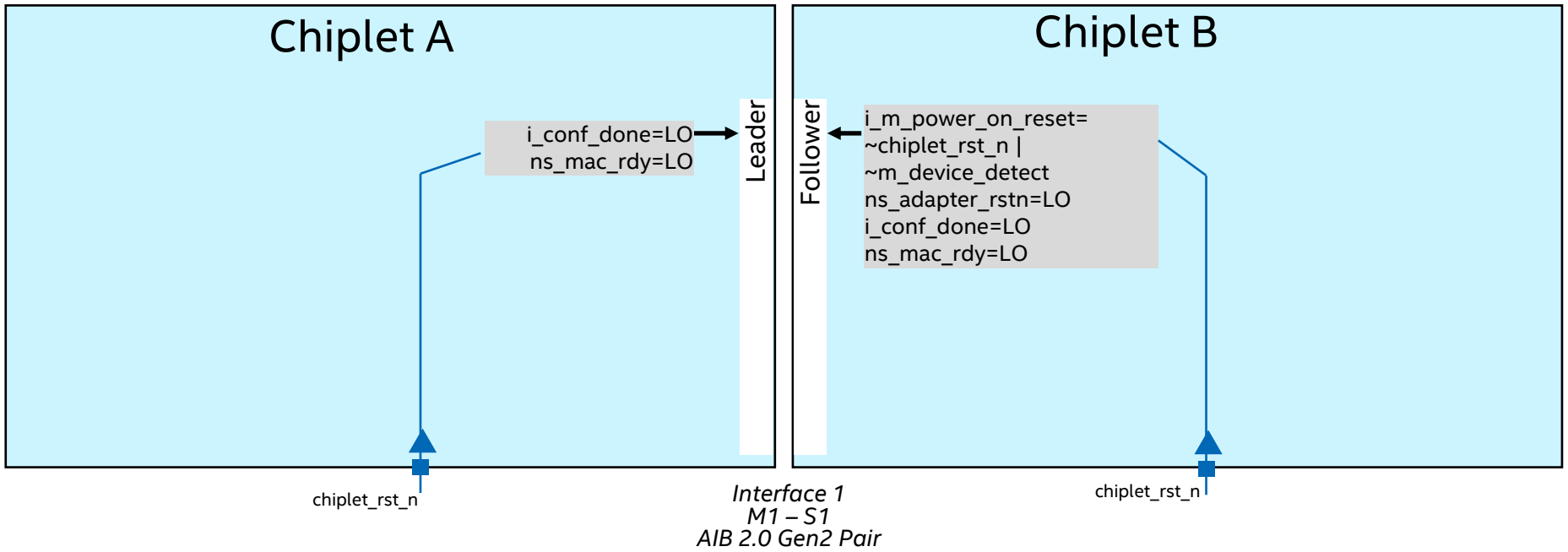


Fixed Settings Determined at Power Up
(does not depend on chiplet or AIB reset)

- These are static settings set by the chiplet application
- Since Chiplet ASIC uses C4 bumps for power_on_reset and device_detect, the chiplet does not need to utilize m_por_ovrd and m_device_detect_ovrd. The ovrd AIB inputs are tied inside each ASIC.



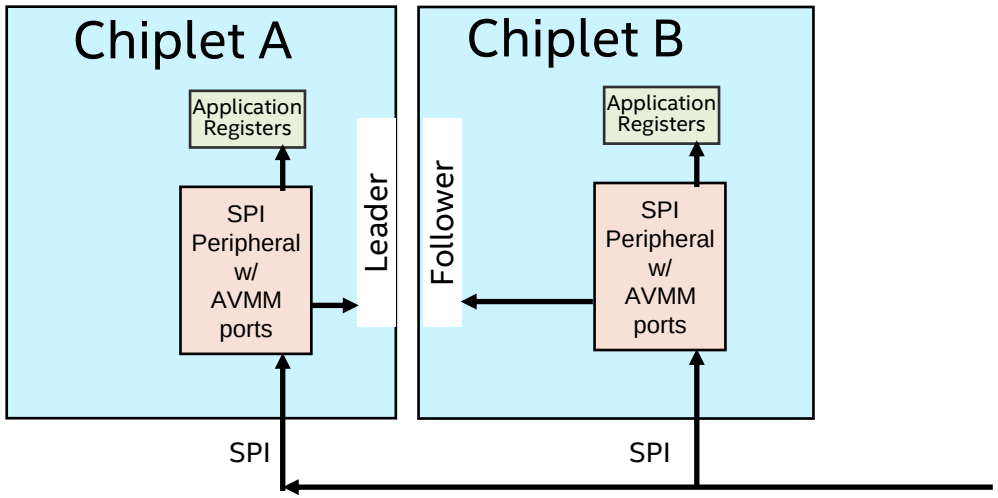
Linked to Chiplet Reset



- i_conf_done signals are controlled by register bits that are reset to 0 by chiplet_reset_n. See CONF_DONE coming up.
- ns_mac_rdy signals are controlled by the chiplet application, which may take actions based on i_conf_done and may need to wait until, for example, clocks are ready

AIB Configuration

Configuration Controller (Typically in FPGA or SoC)
• The chiplet must ensure the AVMM clock is stable before SPI Follower is brought out of reset**.** • The configuration controller configures all AIB interfaces through SPI. • The configuration controller starts using SPI after HI to LO transition on miso. **The HI to LO transition indicates the SPI Follower is out of reset.** • CONF_DONE is performed in the same manner as the Chiplet+FPGA case earlier.



AIB Configuration Data from a configuration controller device (may be an FPGA or one of Chiplet A or B)

ns_mac_ready and Calibration

Initialization
• The application brings up all AIB clocks if not done already • Once local clocks are stable, each application MAC sets ns_mac_rdy HI indicating the AIB channel is ready to begin calibration. This action is up to the application which may itself depend on configuration. • The application is responsible for controlling ns_mac_rdy MAC to PHY signals on a per-channel basis • Starting and completing calibration is done in the same manner as the Chiplet+FPGA case described earlier.