2020 CHIPS Alliance Workshop

The Emergence of the Open Source AIB Chiplet Ecosystem

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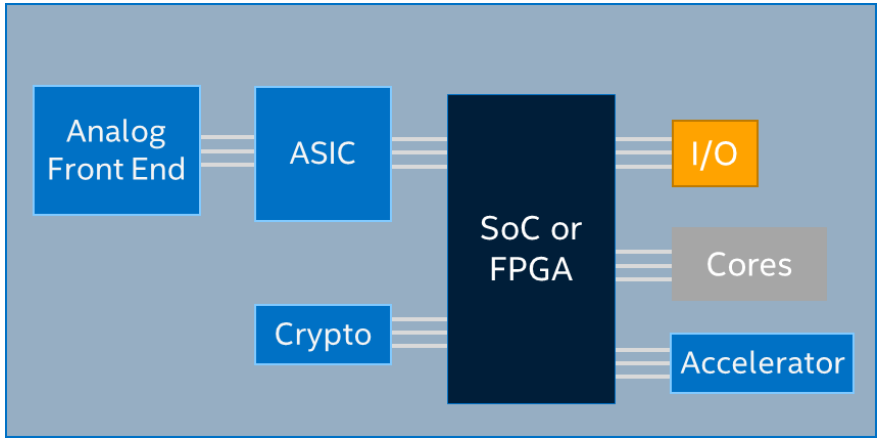
Chiplets on the Rise Recap

- Advanced packaging technology inspired new thinking about SoC microarchitecture
  - Use high die-to-die bandwidth to build a heterogeneous system
- Chiplets enable faster system development serving a broader range of applications
  - Intel E-tile on Stratix 10 achieved FPGA transceiver leadership
- Open source Advanced Interface Bus (AIB) standard encourages a chiplet ecosystem

"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1]."

Gordon E. Moore

1: 3rd Page of Moore's 1965 paper, "Cramming more components onto integrated circuits"



Images: Intel

Open Source Hardware?

- Open source user's point of view, pro and con:
  - "[The CHIPS Alliance is addressing] the problem of high expenses of chipmaking and what can be done in the open source domain to reduce the cost." – *Zvonimir Bandic, Chair of the CHIPS Alliance, Sr. Director at Western Digital*[1]
  - "Replacing proprietary IP license costs with open-source IP licenses will only reduce these [SoC development] costs by ~1%-20%." – *Brucek Khailany, Director of Research at NVidia*[2]
  - **Reuse** to lower the cost of hardware development
- Open source provider's point of view:
  - Enable other companies' silicon to interoperate with my silicon
  - Address an expanded set of customer requirements

Intel FPGA with two Ayar Labs TeraPHY™ optical I/O chiplets

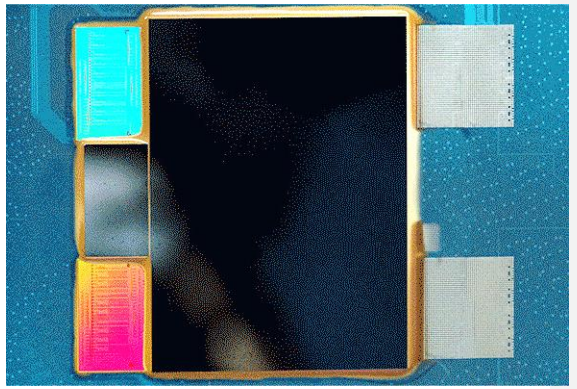


Image: Intel

Fully packaged FPGA with Ayar Labs optical I/O

Image: Ayar Labs, Inc. Used with permission.

1. "Five Minutes with Zvonimir Bandic," Embedded Computing Design, May 2019
2. Khailany, Brucek, "ISSCC 2020 Panel: Open Source Hardware," IEEE International Solid-State Circuits Conference, February 2020

Intel and CHIPS Alliance

- CHIPS Alliance AIB Specification
- CHIPS Alliance AIB PHY Open Source Hardware
- CHIPS Alliance AIB Generator Open Source
  - With Blue Cheetah Analog Design, Inc.
- Excellent alignment with the CHIPS Alliance objectives[1]:

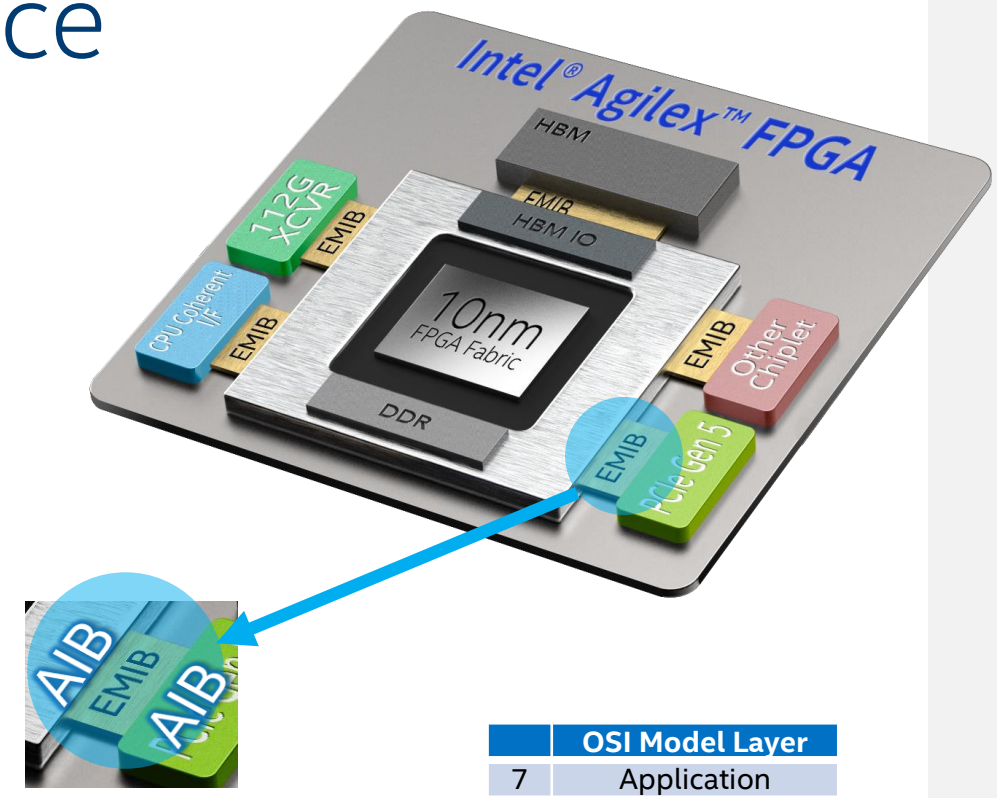
  "The mission of the CHIPS Alliance is to develop high-quality, open source hardware designs relevant to silicon devices and FPGAs."

  "By creating an open and collaborative environment, CHIPS Alliance shares resources to lower the cost of development."

1. Source: chipsalliance.org

AIB Die-to-Die Physical Interface

- Advanced Interface Bus (AIB)
  - Standard chiplet wide parallel physical interface
    - https://github.com/chipsalliance/AIB-specification
  - AIB is a clock-forwarded parallel data transfer like DDR DRAM
  - Advanced Packaging like InFO* or EMIB
  - AIB is PHY level: OSI Layer 1
  - Build protocols like AXI*-4 or CXL* on top of AIB



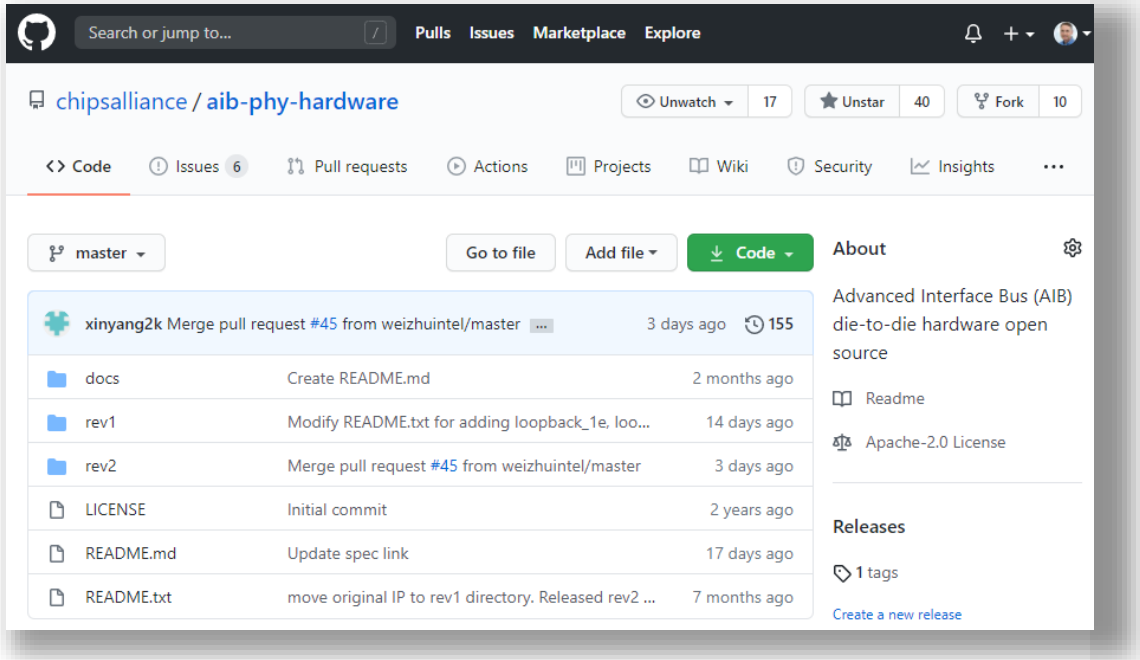
	OSI Model Layer
7	Application
6	Presentation
5	Session
4	Transport
3	Network
2	Data Link
1	Physical

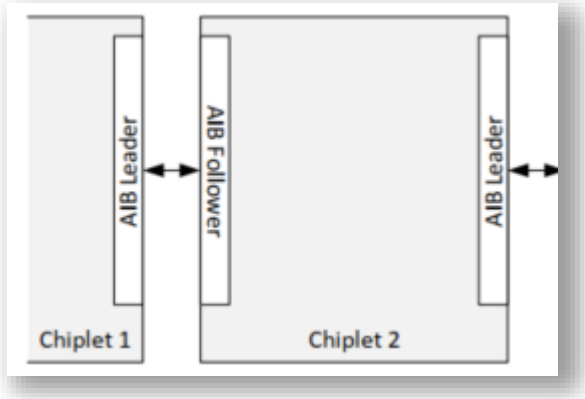
AIB

Images: Intel

AIB PHY Open Source Hardware

- https://github.com/chipsalliance/aib-phy-hardware
  - Source is mostly connectivity from chiplet core to AIB I/Os
  - Modest amount of RTL for DLL and DCC bring-up handshaking
  - Behavioral models of custom cells for IO, DLL, DCC
- **New Addition**: Follower side Open Source code
  - Leader vs. Follower:
    - Differs in bring-up handshaking (only one side can control reset!)
    - Legacy pinout





AIB Leader and Follower

Images: Intel

New: AIB Generator Open Source Hardware

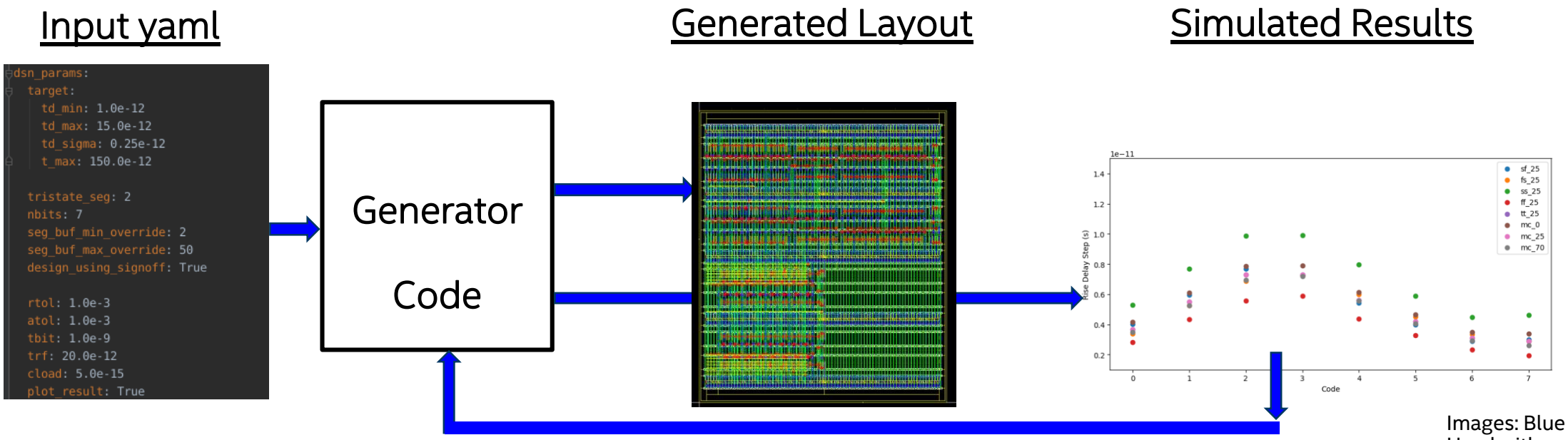
- https://github.com/chipsalliance/aib-phy-generator
  - **Generates the custom cells for IO, DLL, DCC**
  - Builds on the AIB PHY Open Source
- DLL Interpolator Generator Example
  - Delays the input clock to achieve 90 degree offset for data sampling
  - Compensates for PVT through dynamic phase interpolation
  - Usually implemented as custom design in a target process
- Generator abstracts design away from a proprietary process design kit (PDK)!

AIB Custom Cells

```
$ pwd
…/aib-phy-hardware/rev2/rtl/v2_common/ana
$ ls
DIFF_CLK_RCVR.v              aibcr3_dll_interpolator.v
aibcr3_dcc_dlyline64.v       aibcr3_dll_phasedet.v
aibcr3_dcc_helper.v          aibcr3_dlycell_dcc.v
aibcr3_dcc_interpolator.v    aibcr3_dlycell_dll_comb.v
aibcr3_dcc_phasedet.v        aibcr3_frontend.v
aibcr3_dll_dlyline64.v
```

AIB Generator Phase Interpolator Example

- Top-level specifications in yaml:
  - $t_{d,step,min}$, $t_{d,step,max}$, $t_{p,max}$, $s_{td,step}$
  - # of delay steps
- Generator produces netlist, GDS, LIB, LEF, and behavioral model
- All sizing decisions needed to achieve top-level specs are made using feedback from post-layout simulations



Images: Blue Cheetah.
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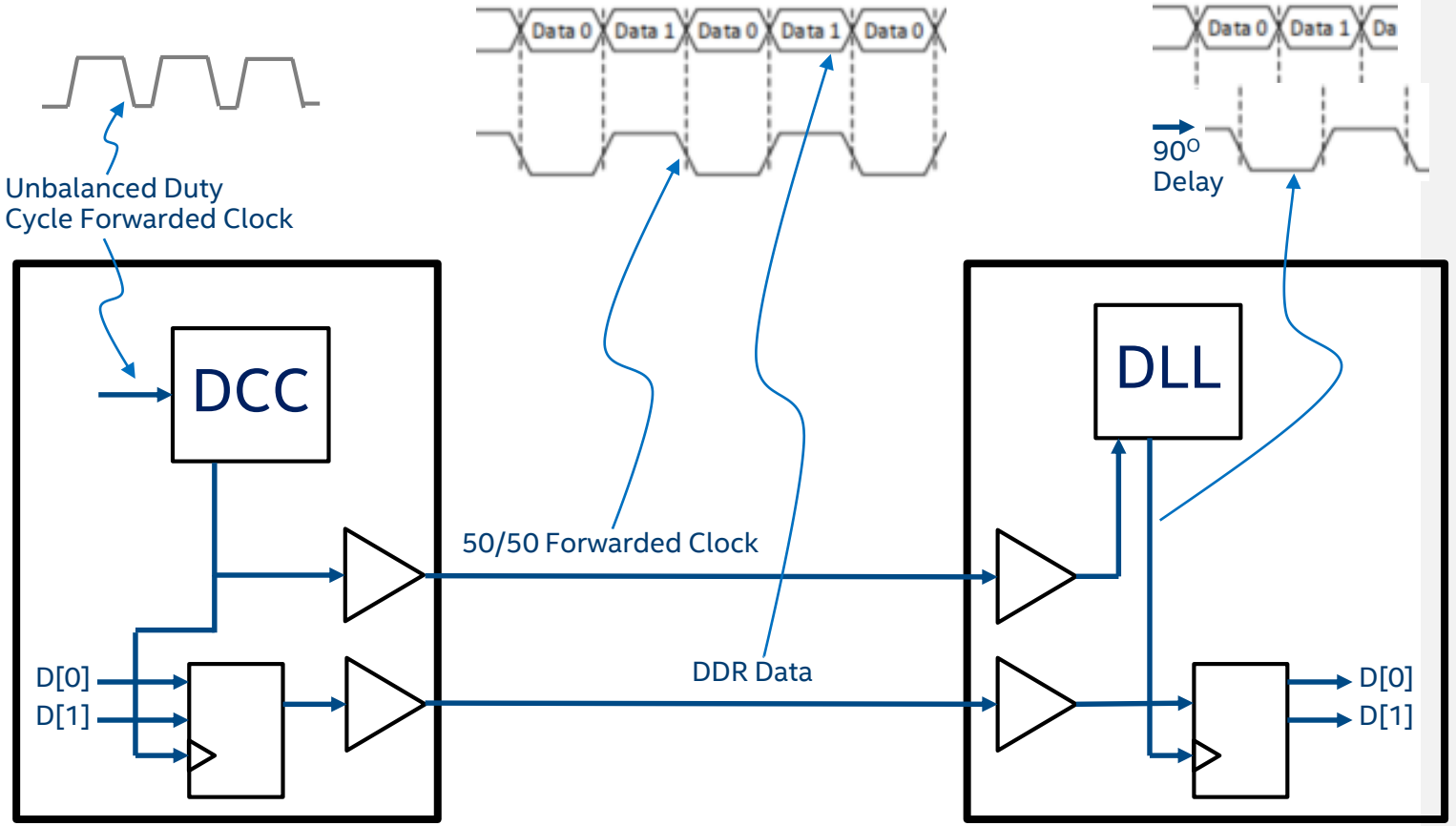
Generated Custom Cells

- Why do we need custom cells, vs. standard cells?
  - IO: ESD and voltage level shifting
  - DLL, DCC: Fine control of clock edges
- Why do we need a DCC?
  - Dynamically compensates for VT to balance the bit periods of DDR transfers
- Why do we need a DLL?
  - Dynamically compensates for VT to center the receive data sampling



Growing AIB Chiplet Portfolio

Device with AIB	Process	Status
Intel® Stratix® 10 FPGA	Intel 14	Production
L-tile 17G SERDES	TSMC 20	Production
H-tile 28G SERDES	TSMC 20	Production
E-tile 56G SERDES	TSMC 16	Production
Intel® Agilex™ FPGA	Intel 10	Sampling
P-tile PCIe Gen4/UPI	TSMC 16	Production
University of Michigan offload ASIC	TSMC 16	Powered up
Jariet EW class ADC/DAC	GF 14	Powered up
Ayar Labs Photonics I	GF 45RFSOI	Powered up
University & IP Test Chip (UMich, Blue Cheetah)	Intel 22	Powered up
Intel® High Performance Computing	TSMC x	In progress
Customer I	Intel 22	In progress
Ayar Labs Photonics II	GF x	In progress
Ayar Labs Photonics III	GF x	In progress
Customer II	Intel 22	In progress
Customer III	Intel 22	In progress
R-tile PCIe Gen5/CXL	Intel x	In progress
F-tile 116G SERDES	Intel x	In progress
Commercial	TSMC x	In progress
University	Intel 22	In progress
Intel® next generation FPGA and eASIC™ devices	Intel x	In progress

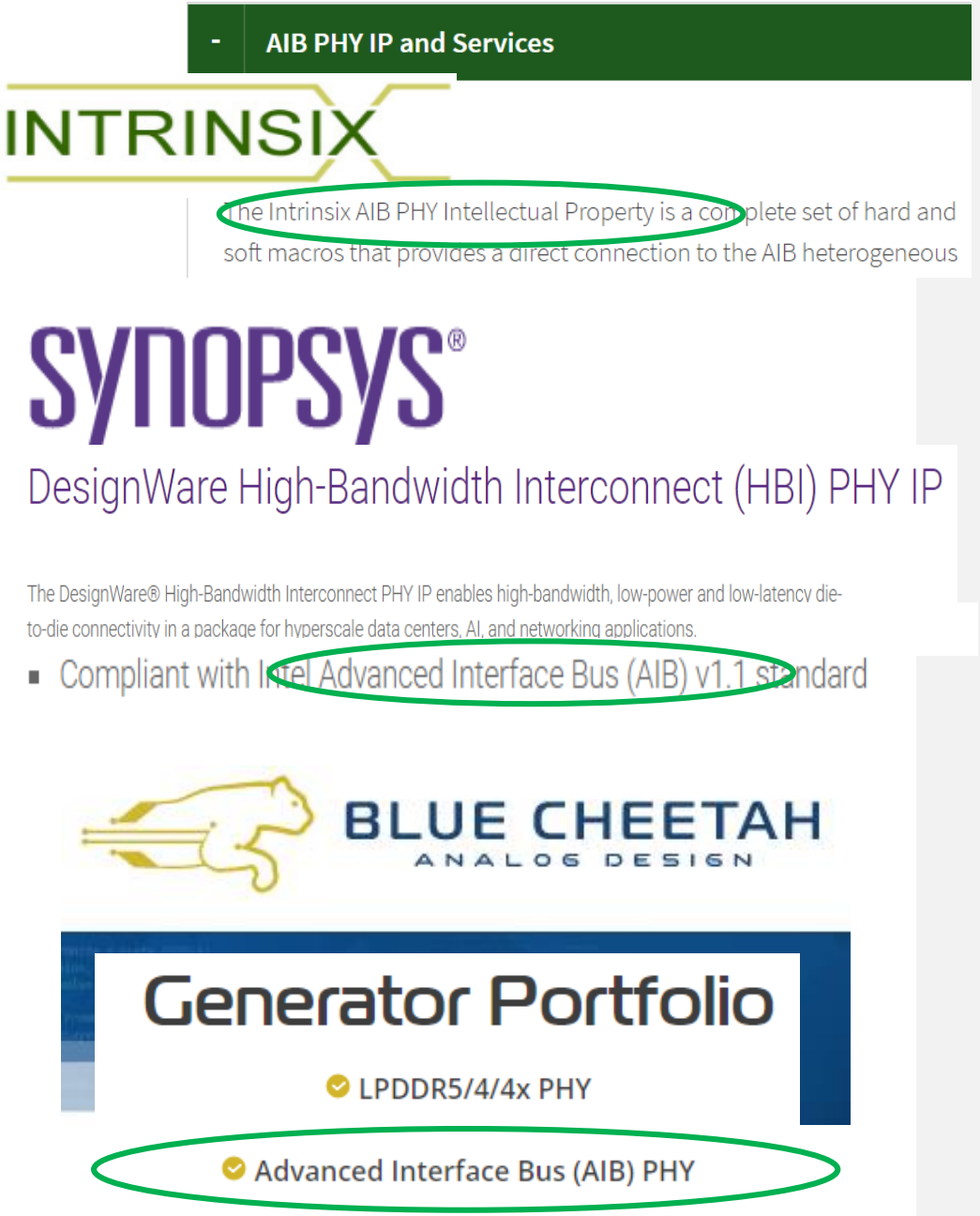
Today

Technology & Foundry Agnostic

- 3 FPGA families
- 6 SERDES chiplets
- 3 Data Converter chiplets
- 3 Optical chiplets
- 2 ASIC compute chiplets
- 3 University research chiplets
- 3 Customer research chiplets
- 1 Intel® eASIC™ chiplet

Chiplet Ecosystem
AIB PHY IP

- *Excellent progress on AIB PHY IP:*
  - AIB PHY Open Source hardware enhancements for ASIC to ASIC link pair
  - AIB IP announced from Intrinsix, Synopsys and Blue Cheetah Analog Design
  - AIB Generator Open Source analog cell design automation to reduce process porting costs



AIB 2.0: A Second Generation Die-to-Die Interconnect

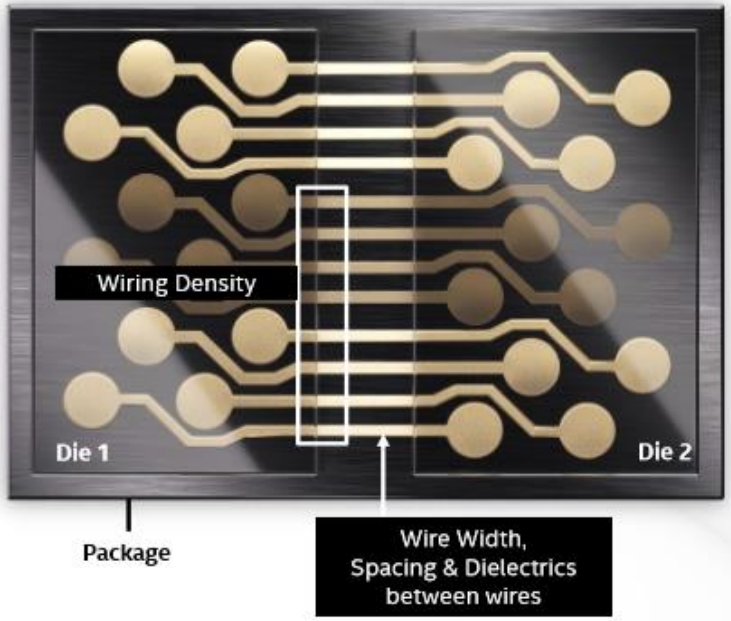
- https://github.com/chipsalliance/AIB-specification

Enabling an Ecosystem

High density die-to-die interconnects

More AIB 2.0 Highlights:

- ***Data Bus Inversion***
- ***Loopback for testability***
- ***Provision for smaller bump pitches***
- ***Many clarifications, e.g. interface reset and testability***



Feature	AIB 1.0	AIB 2.0
Bandwidth/wire (Gbps)	2	Up to 6.4
Bump density (um)	55	55/45/36
Bandwidth/mm shoreline (Gbps/mm)	256	1638
IO Voltage (V)	0.90	0.90/0.40
Energy/bit (pJ/bit)	0.85	0.50
Backward Compatibility	n/a	1.0

AIB Generator available at:
github.com/chipsalliance

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Architecture Day 2020

Images: Intel

Second Generation Chiplet Concepts

- AIB PHY Enhancements: Standards, Open Source Hardware
  - Data Gearboxing
    - *How to reassemble a 320bit word at 500MHz that was sent over a 40bit AIB channel at 4Gbps*
  - Channel Alignment
    - *How to reassemble a wide bus sent over multiple AIB channels*
- Protocols over AIB
  - Logical PHY Interface (LPIF) Adapter for CPU to chiplet application
    - CXL and PCI Express controllers operate on top of LPIF
  - AXI* Streaming and AXI*-4 Read/Write
- Chiplet Security
- Standard chiplet footprint & package for ease of prototyping
- AIB-3D

Conclusion

- First Generation Chiplet Accomplishments
  - Chiplets are extending Moore's Law
  - Chiplets are commercially viable from multiple silicon suppliers
  - Standardization with the AIB interface is enabling an emerging ecosystem of chiplets, IP, design tools and design services
- Starting on Second Generation Chiplets
  - Scale up to die-to-die bandwidth requirements of new wireless and optical systems with AIB 2.0
  - Flow down SoC concepts like security to chiplets
  - Provide a more complete framework of hardware for chiplet developers


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