AIB 2.0 Usage Note

7/13/2022

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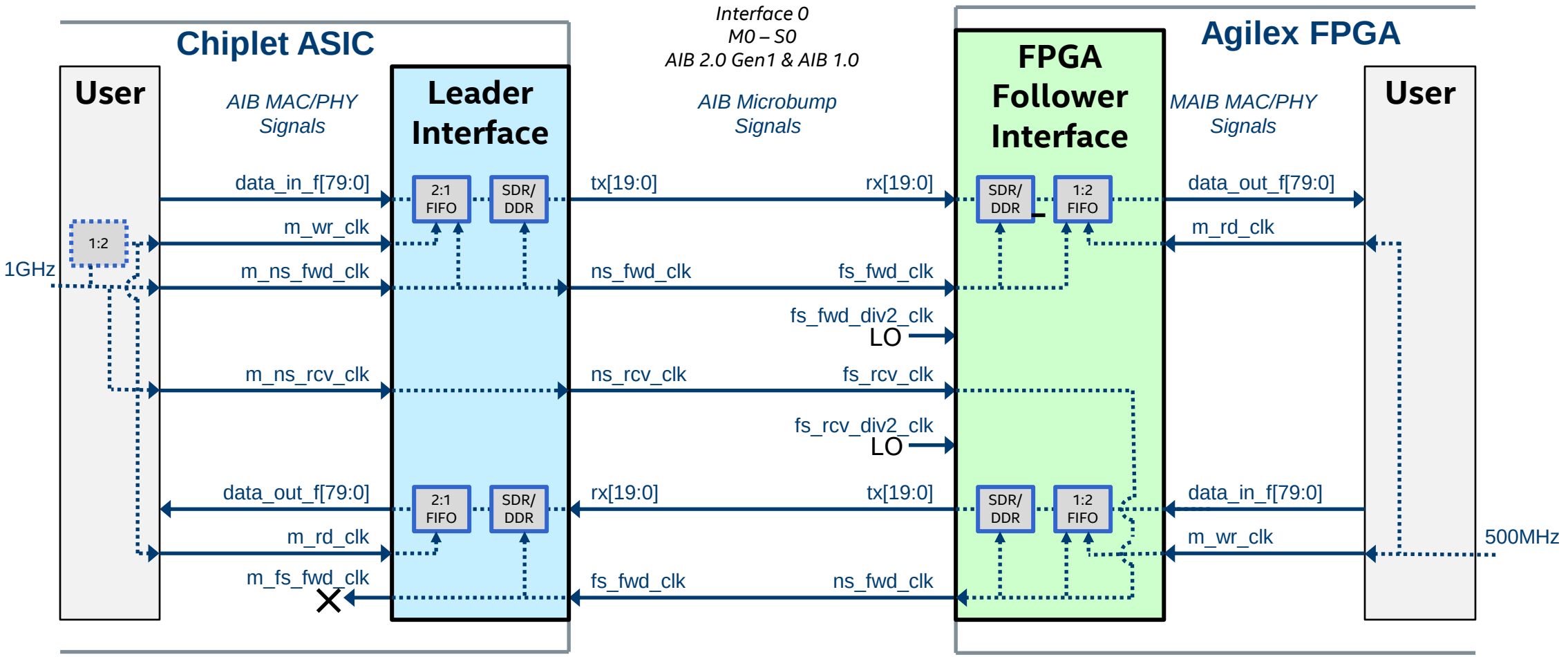
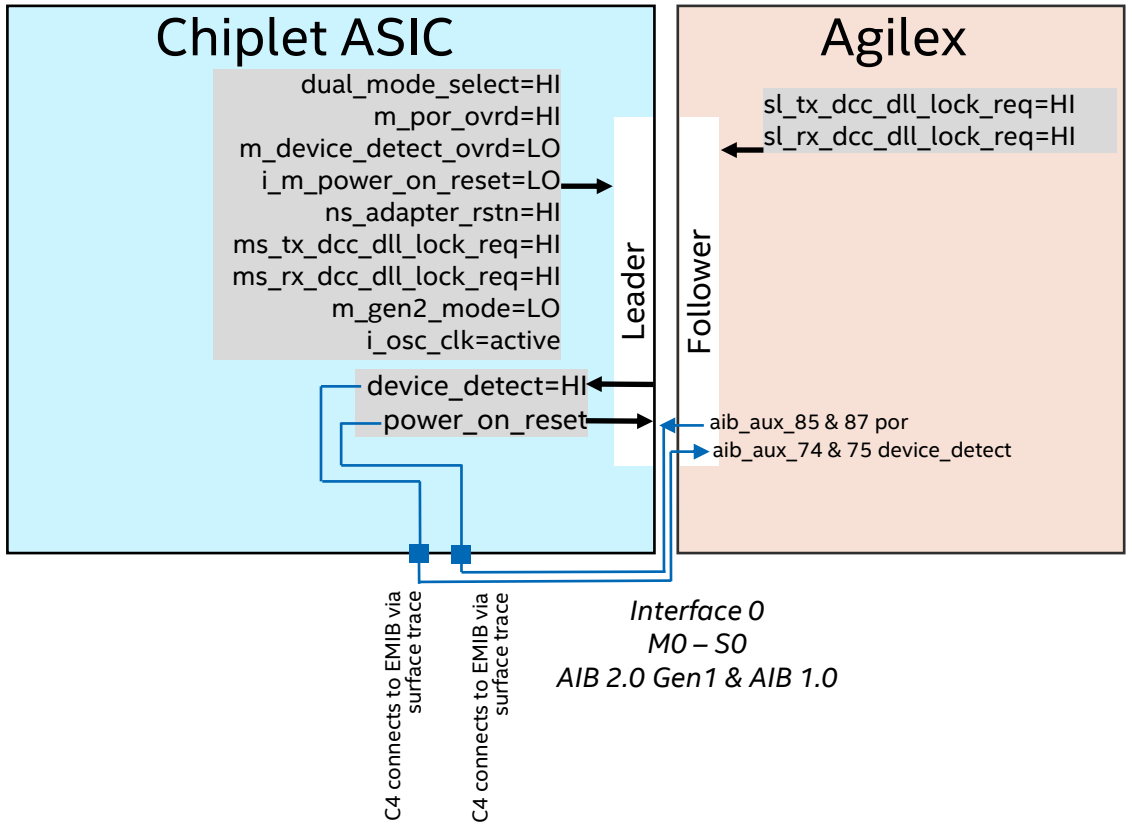
AIB 2.0 in Gen1 Mode, 2:1 FIFO (Half Rate 500MHz) to AIB 1.0 FPGA, 2:1 FIFO (Half Rate 500MHz)



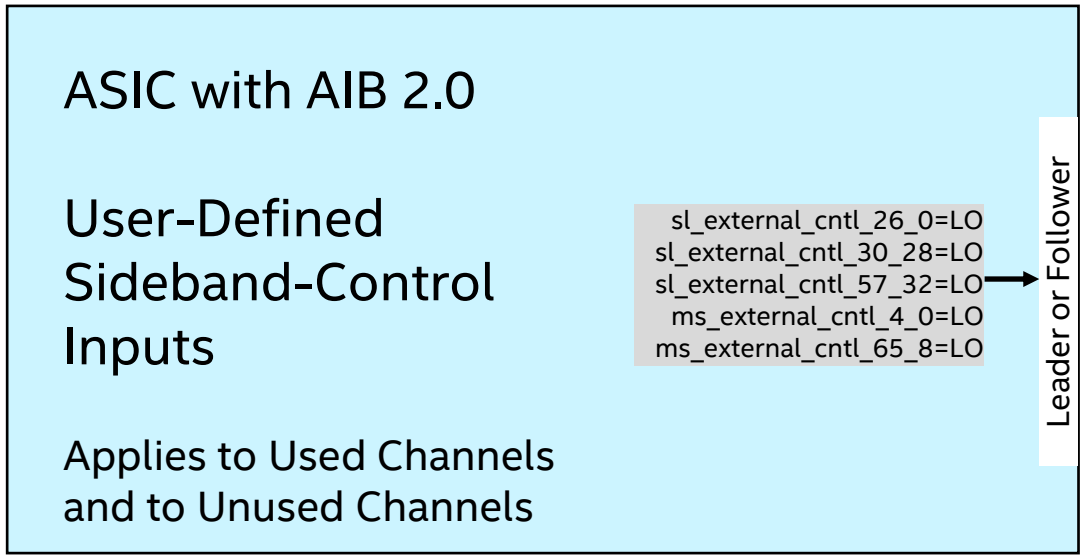
Fixed Settings Determined at Power Up
(these do not depend on chiplet or AIB reset)

- These are all static settings, either set by the chiplet application or external resistors
- Since Chiplet ASIC uses C4 bumps for power_on_reset and device_detect, the chiplet does not need to utilize m_por_ovrd and m_device_detect_ovrd. The ovrd AIB inputs are tied inside the ASIC.



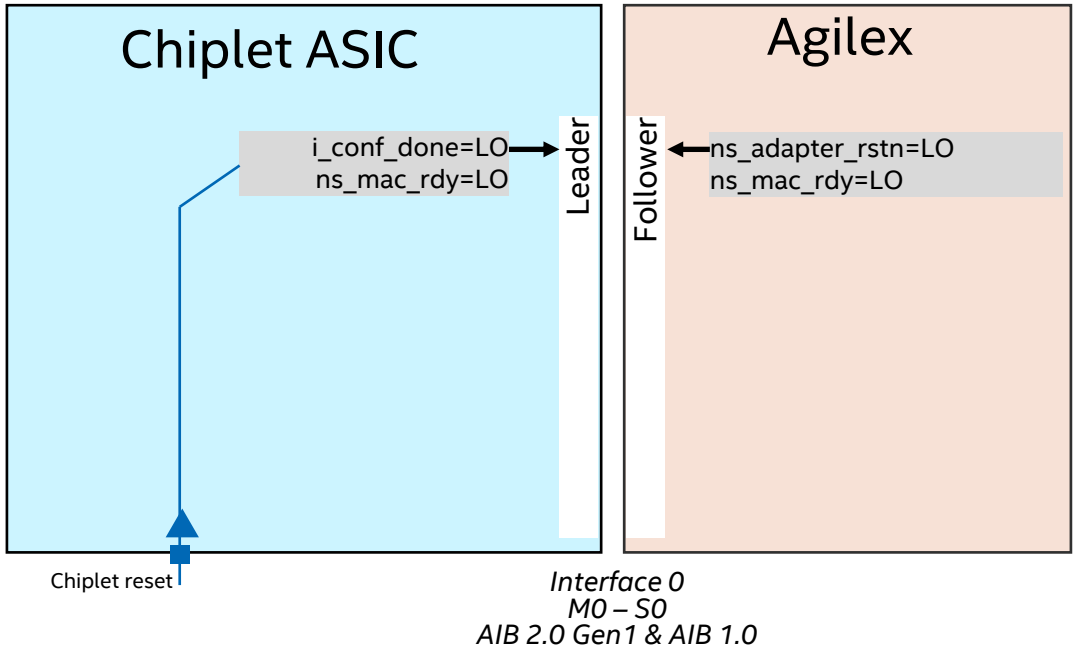
User-Defined Sideband-Control Signals

- The following inputs are User-defined Sideband-Control signals
- For maximal compatibility, do not use these signals
- They should be connected as shown below for both used channels and unused channels



Linked to Chiplet Reset

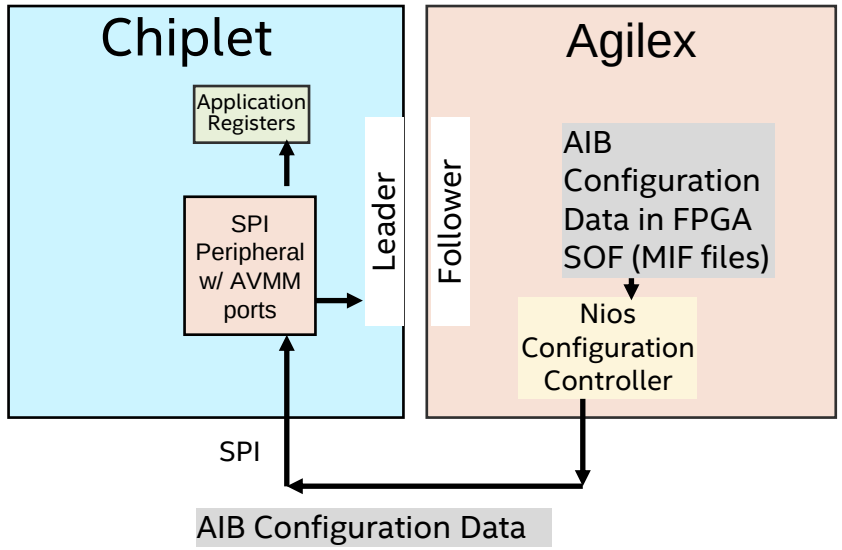
Signal states shown during reset (these are not static)



- i_conf_done signals are controlled by register bits that are reset to 0. See CONF_DONE coming up.
- ns_mac_rdy signals are controlled by the chiplet application, which may take actions based on i_conf_done and may need to wait until, for example, clocks are ready

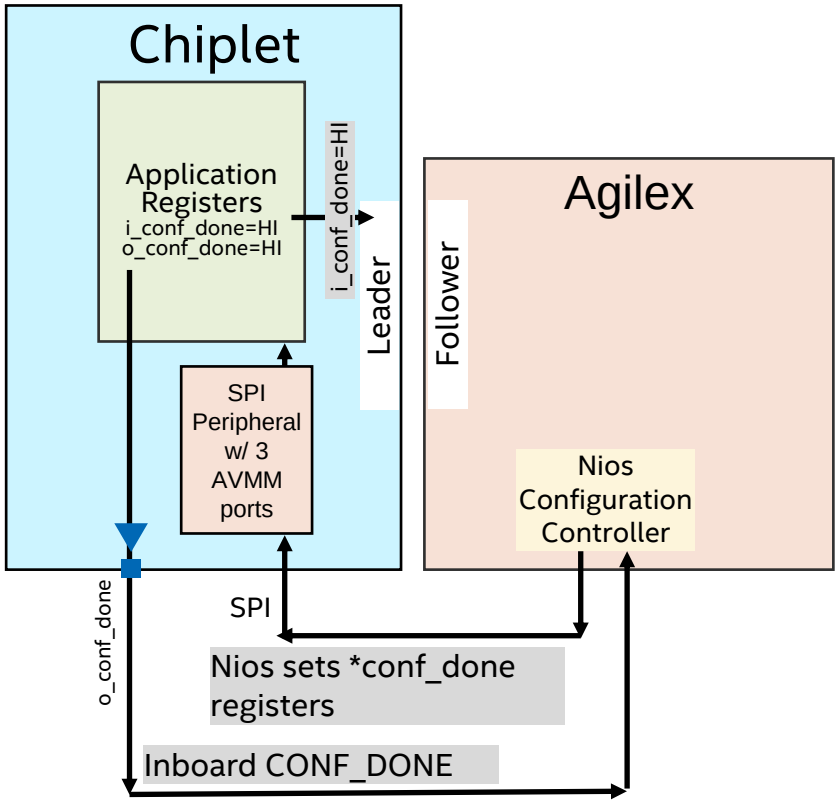
AIB Configuration

Configuration Controller (Typically in FPGA or SoC)
• Chiplet ASIC must ensure the AVMM clock is stable before SPI Follower is brought out of reset**.** • The configuration controller configures all AIB interfaces in an MCP through SPI. • The configuration controller starts using SPI after HI to LO transition on miso. **The HI to LO transition indicates the SPI Follower is out of reset.**



CONF_DONE

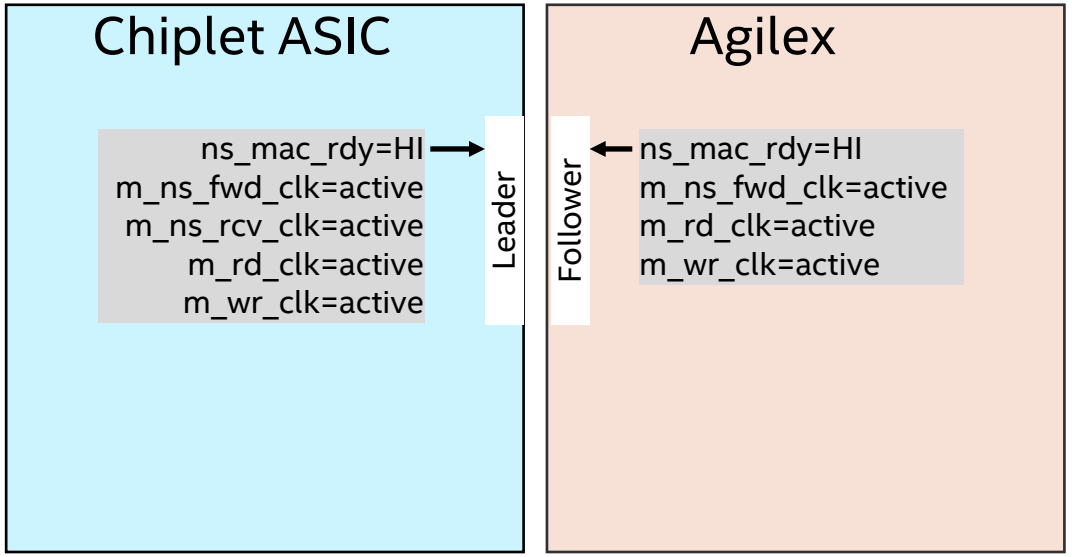
Initialization
• The configuration controller signals the chiplet AIB interface that the configuration is done through a SPI side channel. • The configuration controller sets the Application to PHY signal i_conf_done HI via an application control register



- Since FPGA is in user mode at this time, the MAIB was earlier configured by SOF & SDM/SSM
- Chiplet application *conf_done registers are reset to LO, set HI by the FPGA's configuration controller over SPI

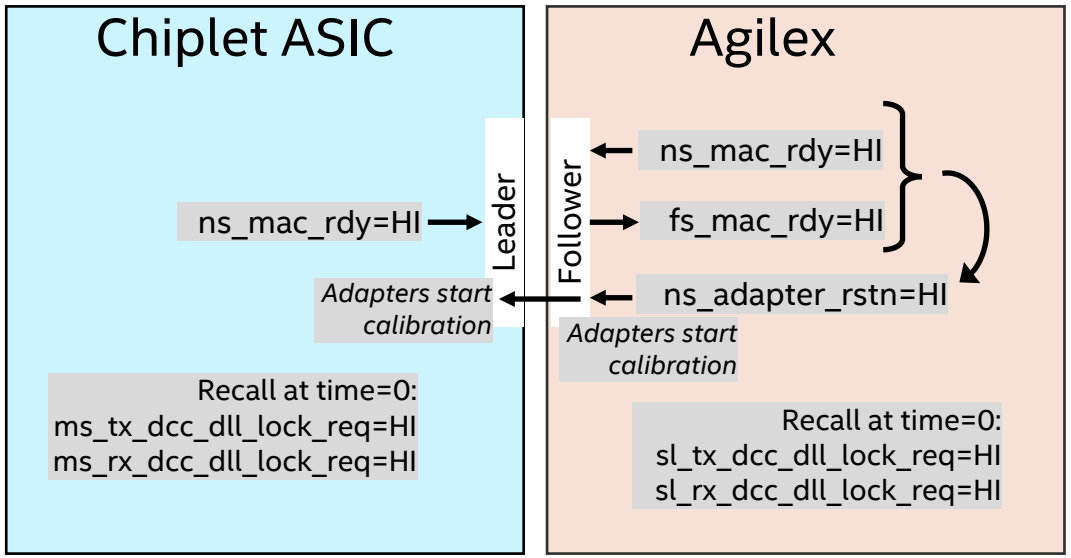
ns_mac_ready

Initialization
• The application brings up all AIB clocks if not done already • Once local clocks are stable, each application MAC sets ns_mac_rdy HI indicating the AIB channel is ready to begin calibration. This action is up to the application which may itself depend on configuration.



- The application is responsible for controlling ns_mac_rdy MAC to PHY signals on a per-channel basis

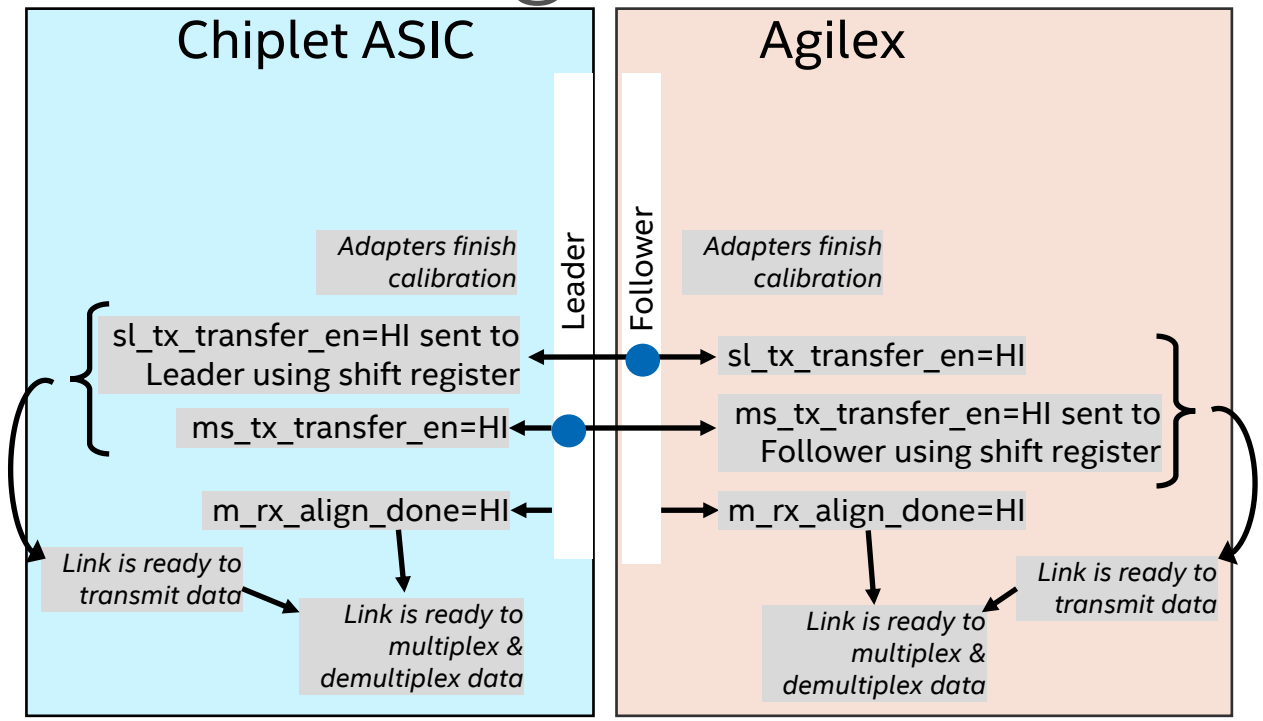
Starting Calibration



- The FPGA application is responsible for controlling ns_adapter_rstn MAC to PHY signals on a per-channel basis

Completing Calibration and Rx Alignment

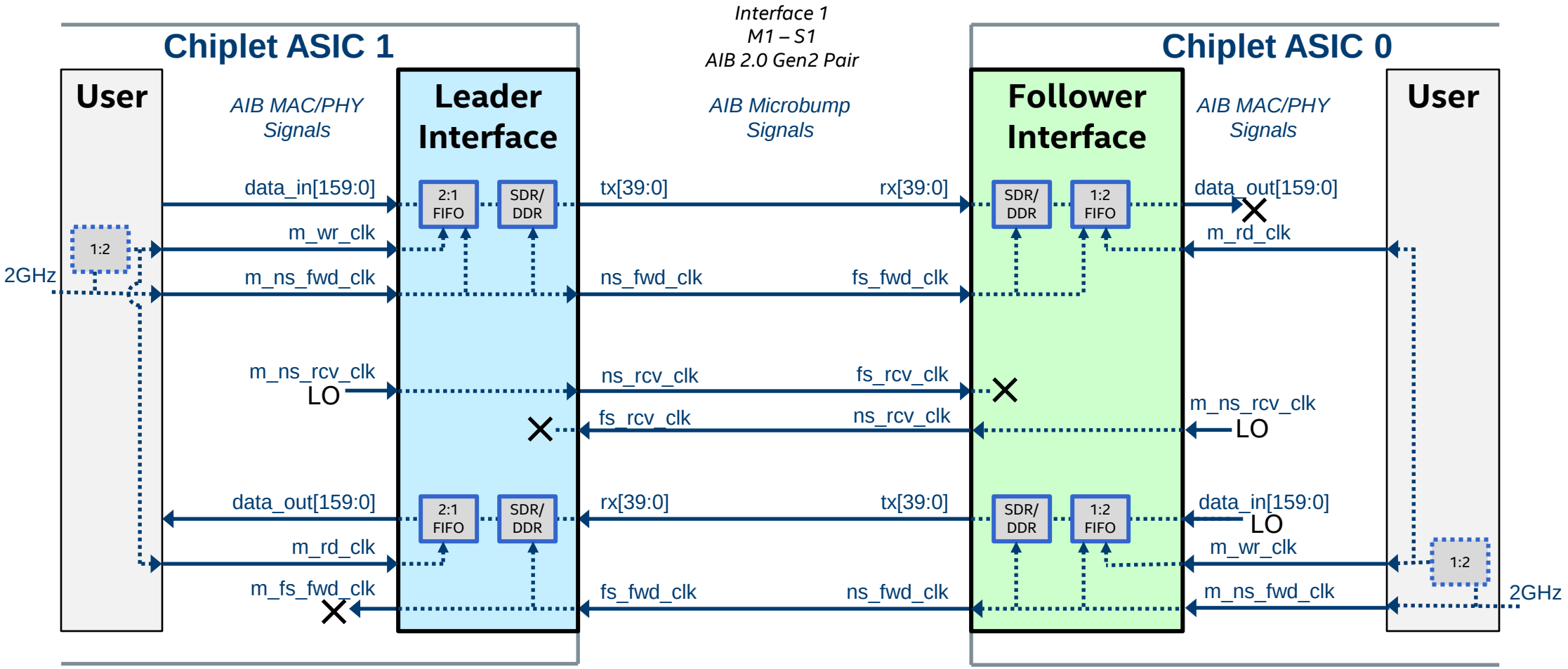
Common Leader and Follower Initialization
• When both the AIB PHY to MAC signals sl_tx_transfer_en and ms_tx_transfer_en are HI, then the link shall be ready to transmit data. • m_rx_align_done=HI means Rx is aligned to the incoming word marking.



- The application is responsible for reading sl_tx_transfer_en, ms_tx_transfer_en and m_rx_align_done to know when the link is ready.
- AXI on AIB Notes, for use of Open Source AXI github.com/chipsalliance/aib-protocols

1. AXI on AIB IP cannot start until the link is ready or it will hang.
2. FPGA as AXI Leader. How does FPGA know Chiplet ASIC is ready?
   sl_tx_transfer_en and ms_tx_transfer_en can be read by the FPGA soft IP from the MAIB. Regarding the Chiplet m_rx_align_done, either the FPGA waits long enough that it can be sure that the Chiplet is aligned, or the FPGA polls a Chiplet register using SPI to read m_rx_align_done for each channel.
3. Chiplet as AXI Leader. How does Chiplet know FPGA MAIB is ready?
   Chiplet will know FPGA MAIB is at rx_align_done because of sideband sl_rx_transfer_en, which in MAIB goes true after the RX FIFO has aligned. This is unspecified MAIB behavior that the Chiplet AIB 2.0 does not perform. We take advantage of this here. ms_tx_transfer_en in turn depends on sl_rx_transfer_en. Chiplet has to wait for ms_tx_transfer_en (and sl_tx_transfer_en) before AXI on AIB TX_ONLINE and RX_ONLINE.

AIB 2.0 Gen2, 2:1 FIFO (Half Rate 1GHz) to AIB 2.0 Gen2, 2:1 FIFO (Half Rate 1GHz)



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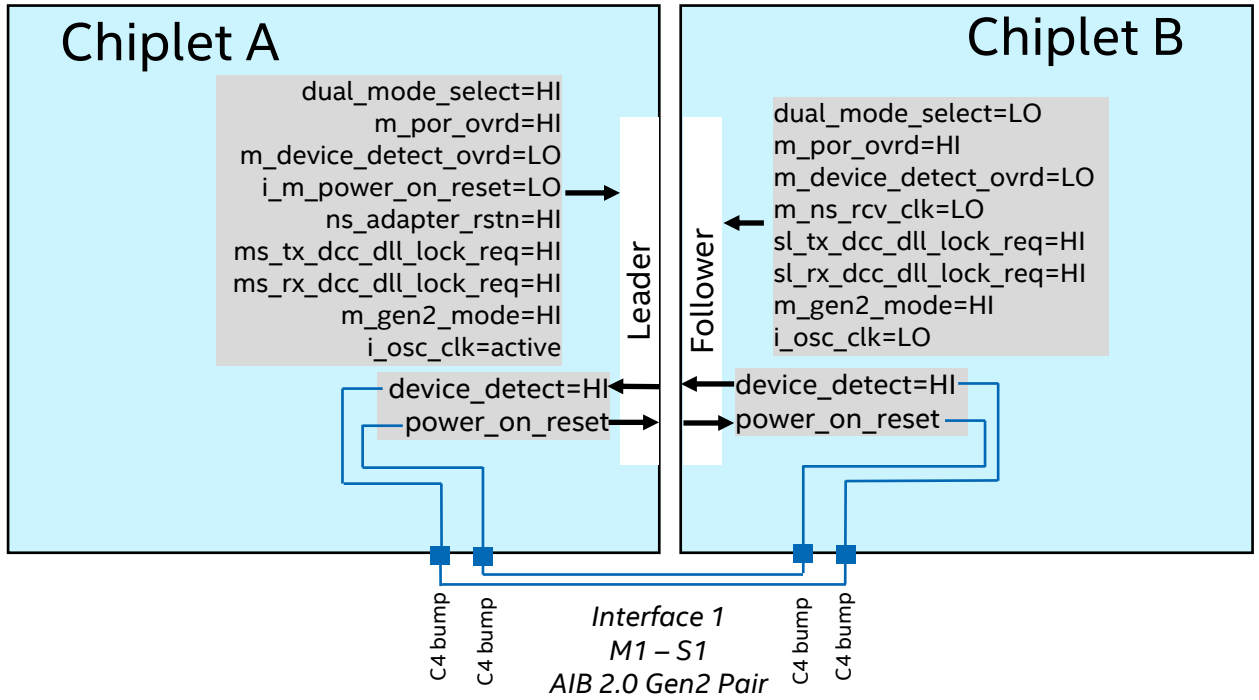
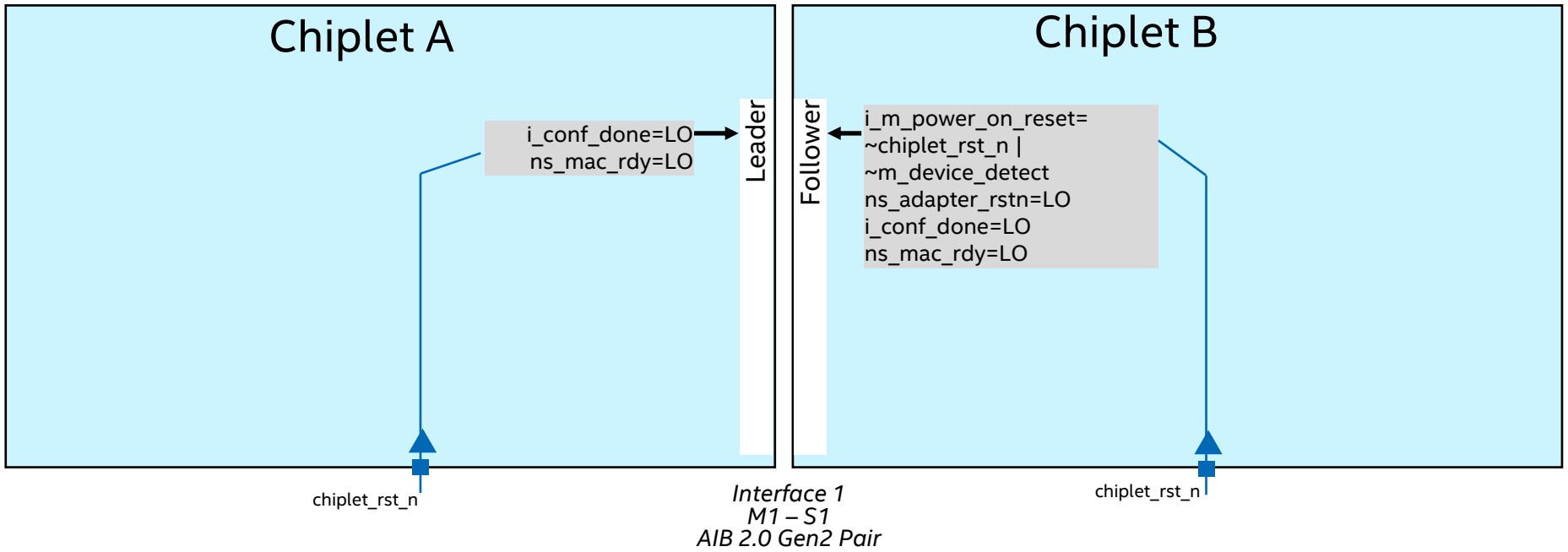


Linked to Chiplet Reset



- i_conf_done signals are controlled by register bits that are reset to 0 by chiplet_reset_n. See CONF_DONE coming up.
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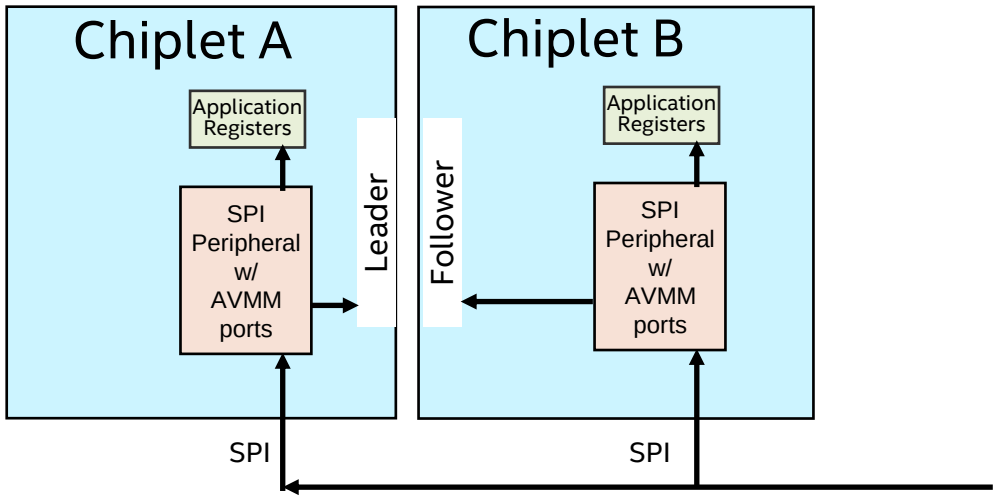

AIB Configuration Data from a configuration controller device (may be an FPGA or one of Chiplet A or B)

ns_mac_ready and Calibration

Initialization
• The application brings up all AIB clocks if not done already • Once local clocks are stable, each application MAC sets ns_mac_rdy HI indicating the AIB channel is ready to begin calibration. This action is up to the application which may itself depend on configuration. • The application is responsible for controlling ns_mac_rdy MAC to PHY signals on a per-channel basis • Starting and completing calibration is done in the same manner as the Chiplet+FPGA case described earlier.