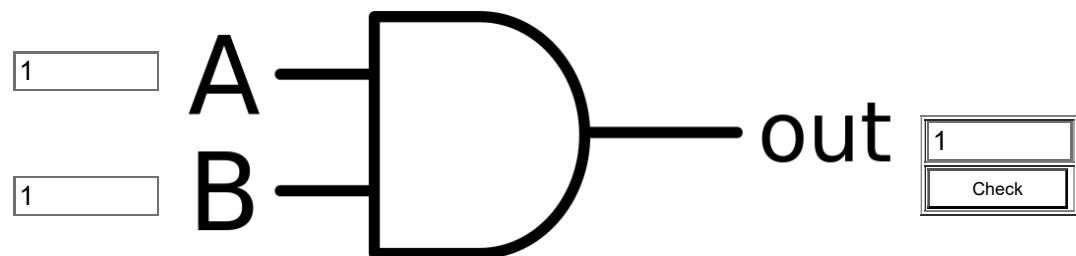


INSTRUCTIONS

Verification of truth table for AND gate



TRUTH TABLE

Print

Serial No.	A	B	Output	Remarks
1	0	0	0	Correct
2	0	1	0	Correct
3	1	0	0	Correct
4	1	1	1	Correct

Reset

INSTRUCTIONS

Verification of truth table for XNOR gate

The circuit diagram shows an XNOR gate with two inputs, A and B, and one output, 'out'. Input A is connected to the top terminal of the gate, and input B is connected to the bottom terminal. The output 'out' is shown as a circle at the end of the gate's output line. To the left of the gate, there are two rectangular input boxes, both containing the number '1'. To the right of the gate, there is a rectangular output box divided into two horizontal sections: the top section contains '1' and the bottom section contains 'Check'.

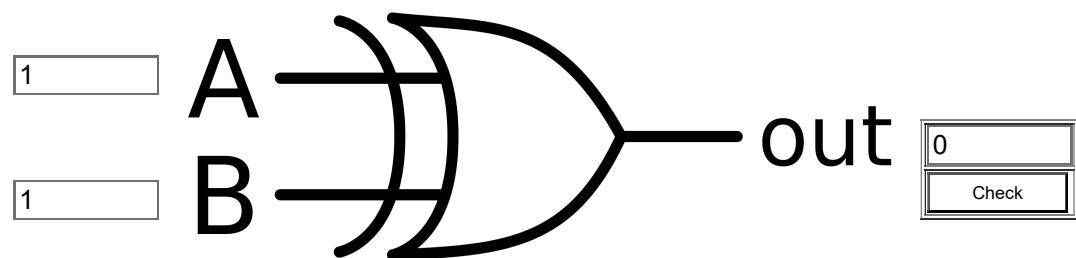
TRUTH TABLE				
Serial No.	A	B	Output	Remarks
1	0	0	1	Correct
2	1	0	0	Correct
3	0	1	0	Correct
4	1	1	1	Correct

Reset

Print

INSTRUCTIONS

Verification of truth table for XOR gate



TRUTH TABLE

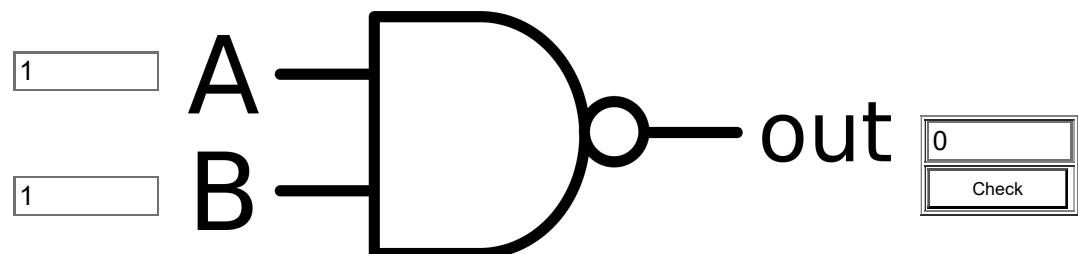
Print

Serial No.	A	B	Output	Remarks
1	0	0	0	Correct
2	1	0	1	Correct
3	0	1	1	Correct
4	1	1	0	Correct

Reset

Instructions

Verification of truth table for NAND gate



TRUTH TABLE

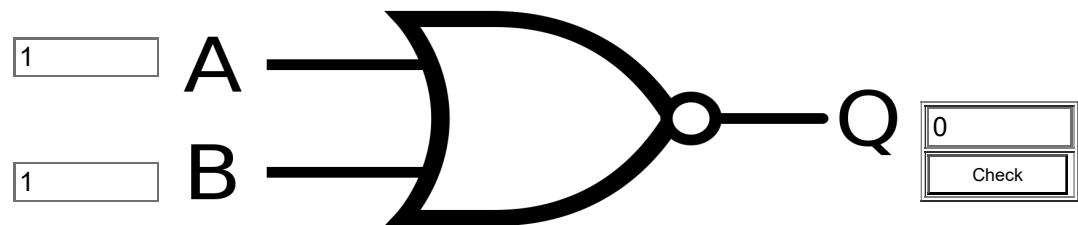
Print

Serial No.	A	B	Output	Remarks
1	0	0	1	Correct
2	1	0	1	Correct
3	0	1	1	Correct
4	1	1	0	Correct

Reset

INSTRUCTIONS

Verification of truth table for NOR gate



TRUTH TABLE

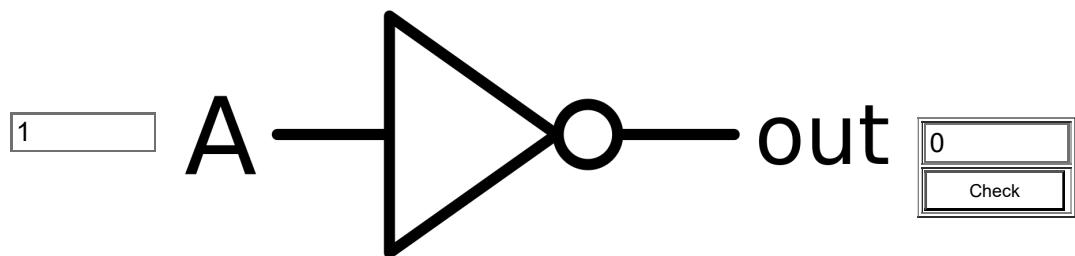
Print

Serial No.	A	B	Output	Remarks
1	0	0	1	Correct
2	1	0	0	Correct
3	0	1	0	Correct
4	1	1	0	Correct

Reset

INSTRUCTIONS

Verification of truth table for NOT gate



TRUTH TABLE

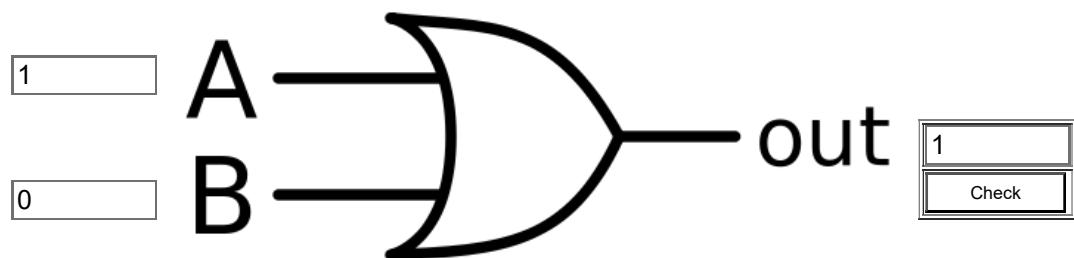
Print

Serial No.	A	Output	Remarks
1	0	1	Correct
2	1	0	Correct

Reset

INSTRUCTIONS

Verification of truth table for OR gate



TRUTH TABLE

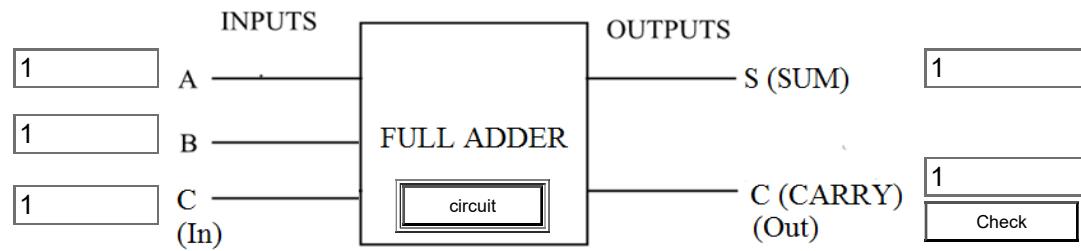
Print

Serial No.	A	B	Output	Remarks
1	0	0	0	Correct
2	0	1	1	Correct
3	1	1	1	Correct
4	1	0	1	Correct

Reset

INSTRUCTIONS

Verification of truth table for FULL ADDER

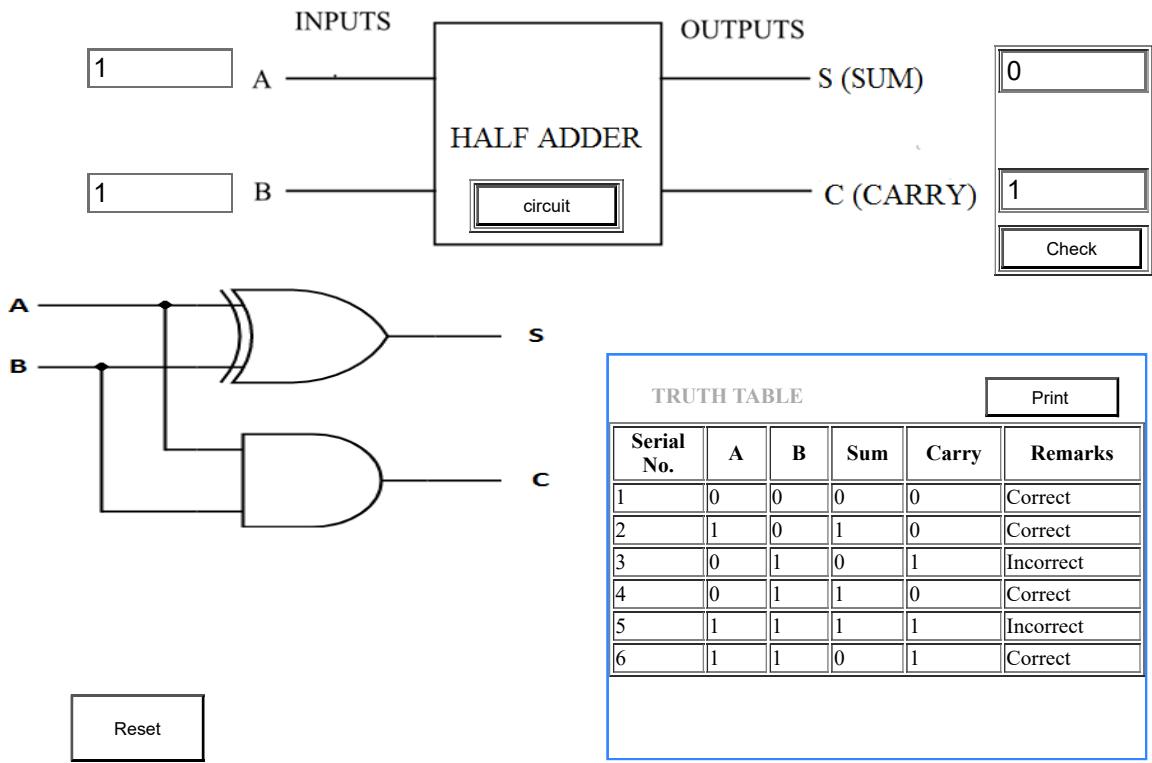


TRUTH TABLE

Serial No.	A	B	C _{in}	Sum	C _{out}	Remarks
1	0	0	0	0	0	Correct
2	0	0	1	1	0	Correct
3	0	1	0	1	0	Correct
4	0	1	1	0	1	Correct
5	1	0	0	1	0	Correct
6	1	0	1	0	1	Correct
7	1	1	0	0	1	Correct
8	1	1	1	1	1	Correct

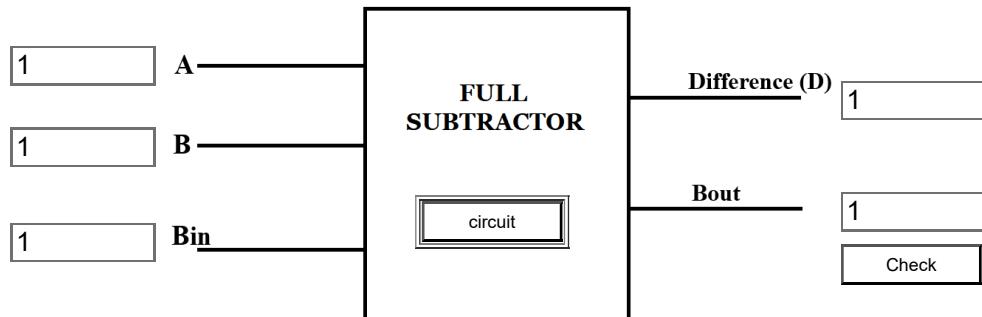
INSTRUCTIONS

Verification of truth table for HALF ADDER



INSTRUCTIONS

Verification of truth table for Full Subtractor Circuit

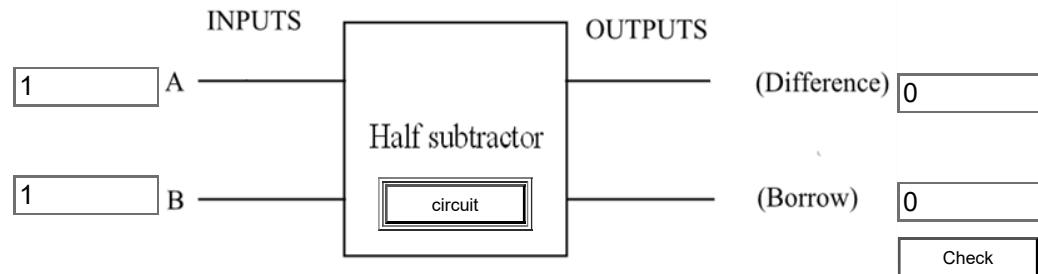


Print

Serial No.	A	B	Bin	D	Bout	Remarks
1	0	0	0	0	0	Correct
2	0	0	1	1	1	Correct
3	0	1	0	1	1	Correct
4	0	1	1	0	1	Correct
5	1	0	0	1	0	Correct
6	1	0	1	0	0	Correct
7	1	1	0	0	0	Correct
8	1	1	1	1	1	Correct

Instructions

Verification of truth table for Half Subtractor Circuit

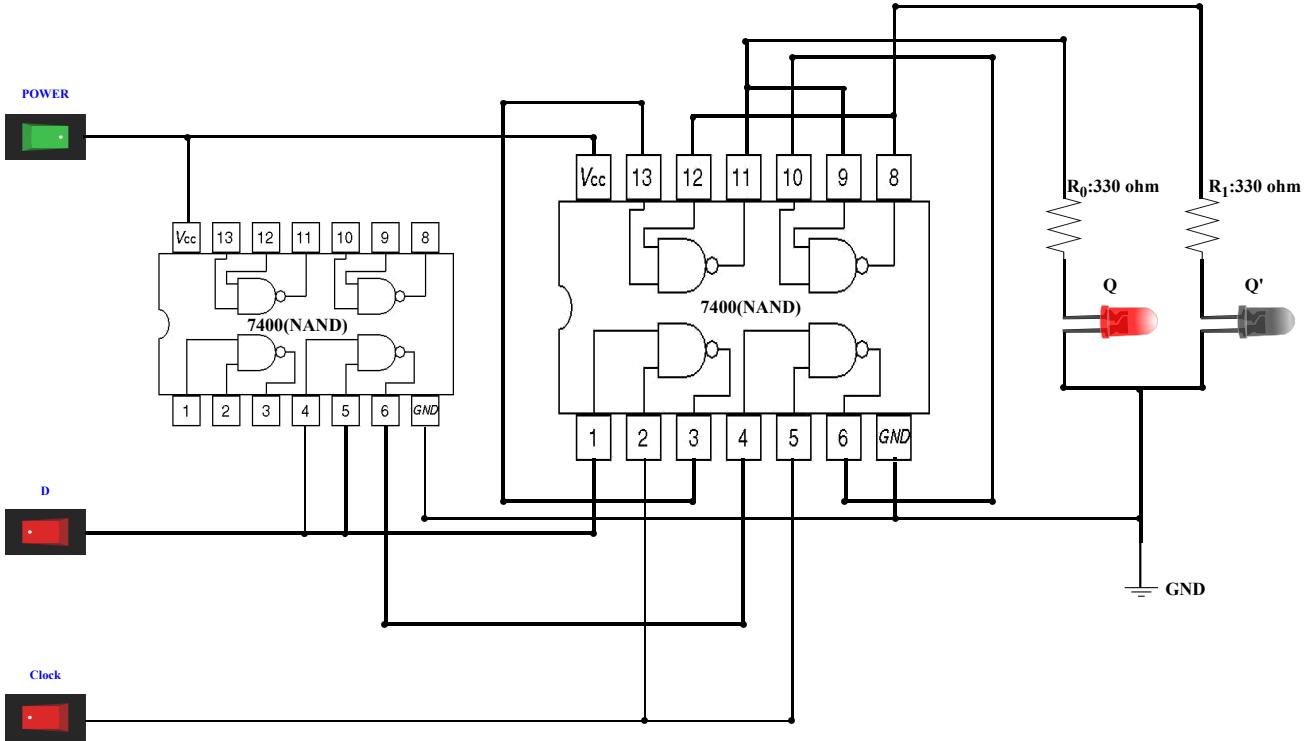


TRUTH TABLE

Serial No.	A	B	Difference	Borrow	Remarks
1	0	0	0	0	Correct
2	0	1	1	1	Correct
3	1	0	1	0	Correct
4	1	1	0	0	Correct

INSTRUCTIONS

Experiment to perform logic of D - Flipflop on kit



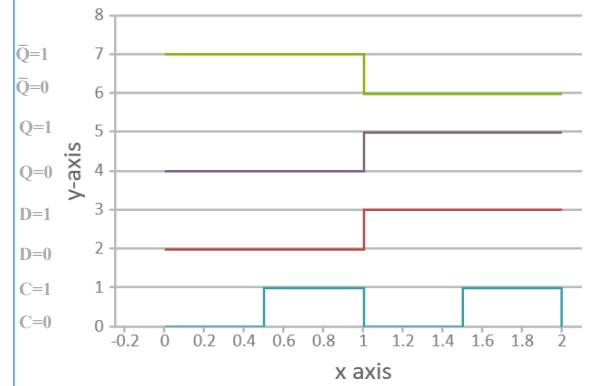
TRUTH TABLE

PRINT

Add

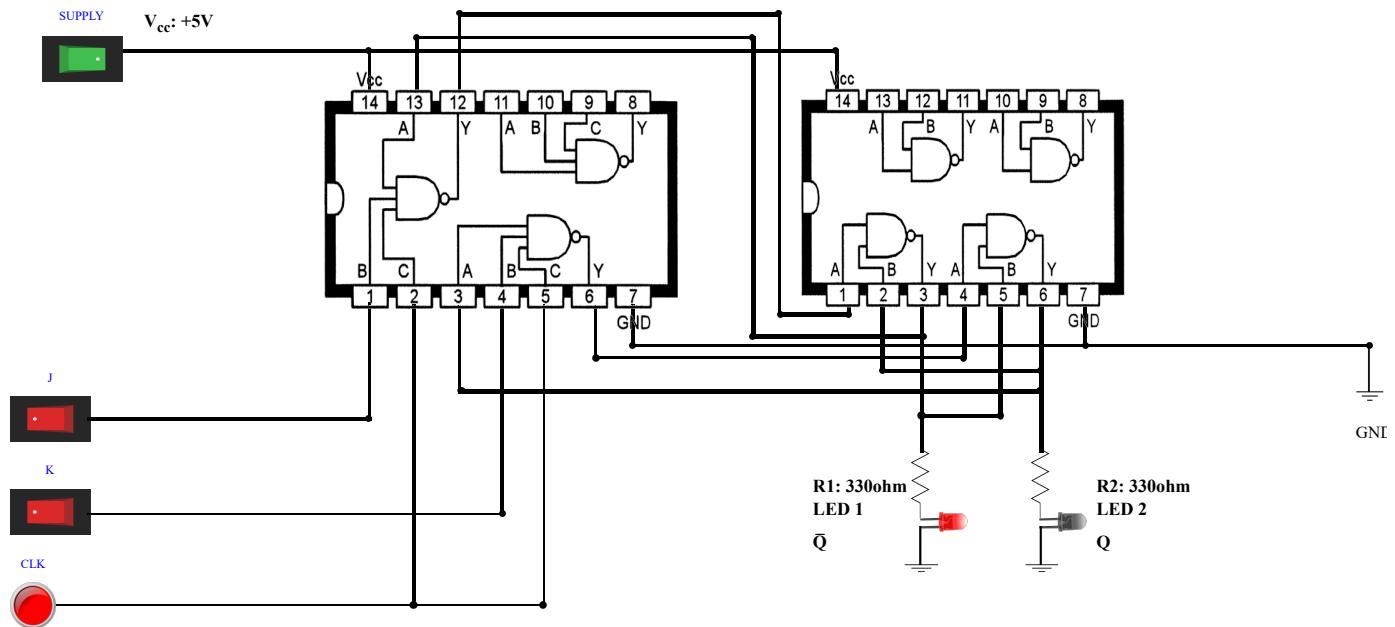
Serial No.	clock	D	$Q(n-1)$	$Q'(n-1)$	Q	Q'	Remark
1	1	0	0	1	0	1	set
2	1	1	0	1	1	0	set

CLOCK DIAGRAM



INSTRUCTIONS

Experiment to perform logic of JK FLIP FLOP on kit



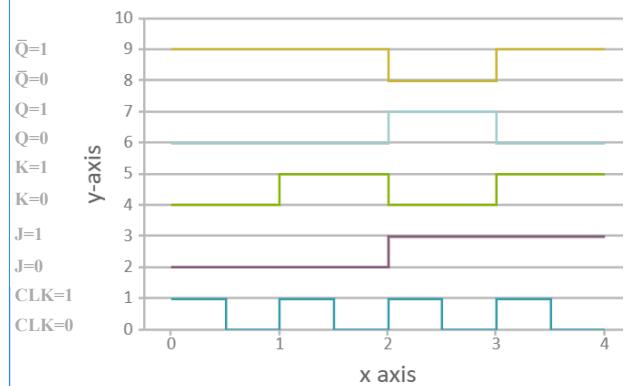
TRUTH TABLE

PRINT

Add

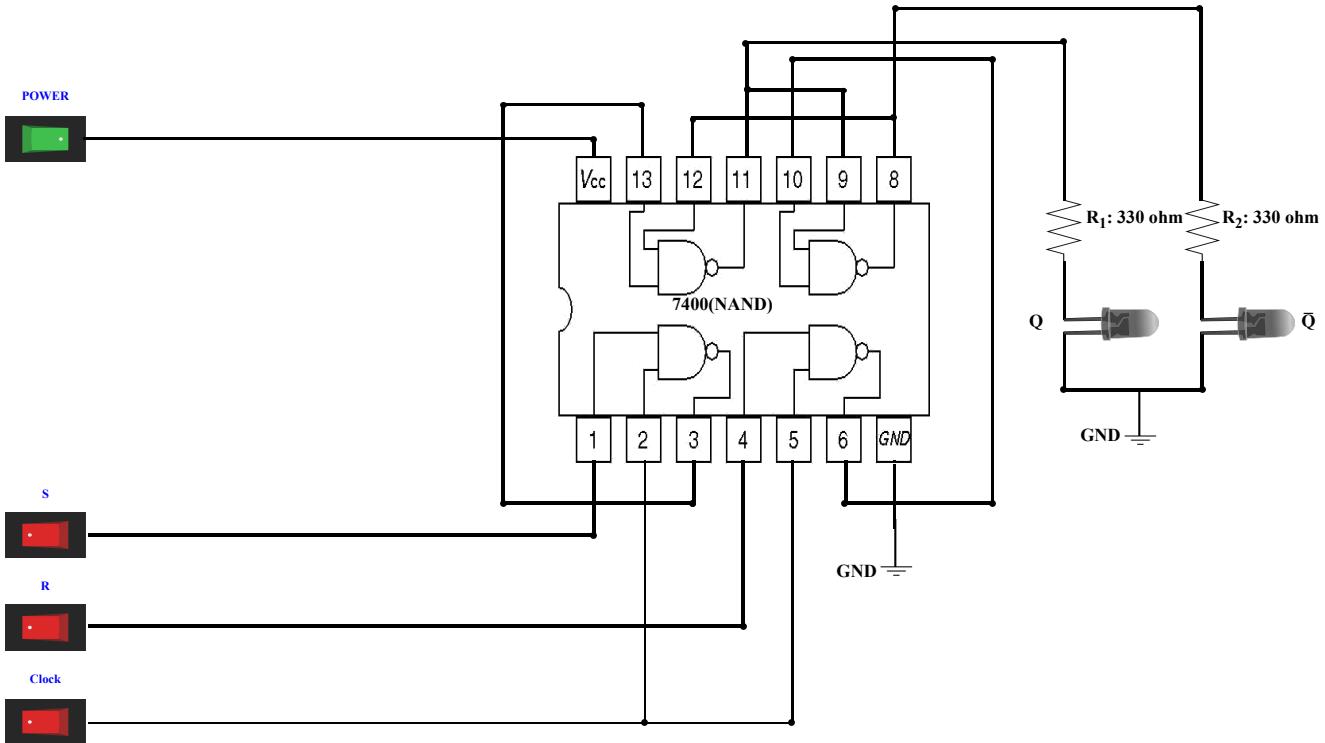
Serial No.	clock	J	K	$Q(n-1)$	$\bar{Q}(n-1)$	Q	\bar{Q}	Remark
1	1	0	0	0	1	0	1	No change
2	1	0	1	0	1	0	1	Reset
3	1	1	0	0	1	1	0	set
4	1	1	1	1	0	0	1	toggle

CLOCK DIAGRAM



INSTRUCTIONS

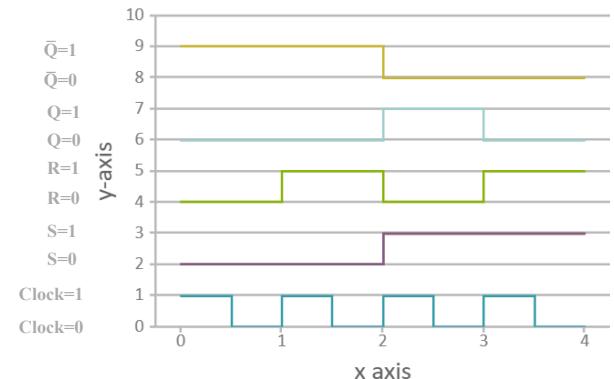
Experiment to perform SR Flip Flop on kit



TRUTH TABLE

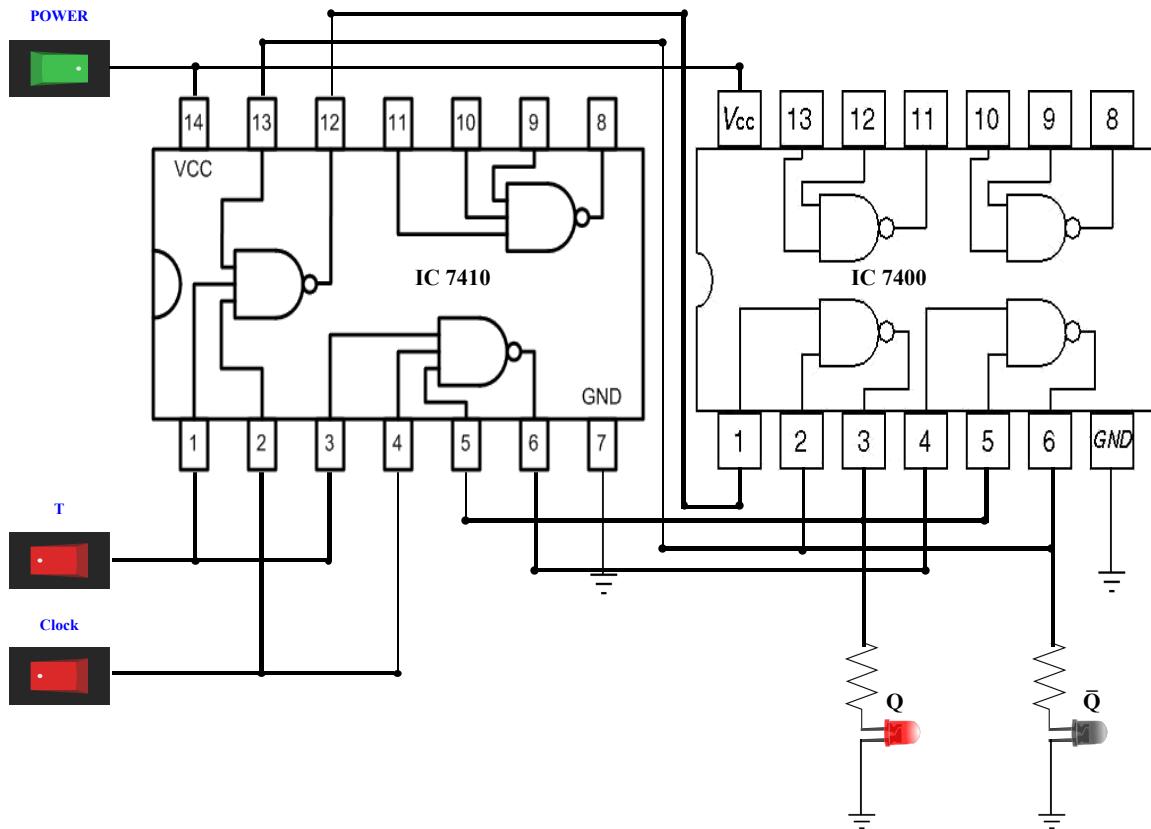
Serial No.	clock	S	R	Q(n-1)	$\bar{Q}(n-1)$	Add		Remark
						Q	\bar{Q}	
1	1	0	0	0	1	0	1	No change
2	1	0	1	0	1	0	1	Reset
3	1	1	0	0	1	1	0	set
4	1	1	1	1	0	0	0	INVALID

CLOCK DIAGRAM



INSTRUCTIONS

Experiment to perform T Flip Flop on kit



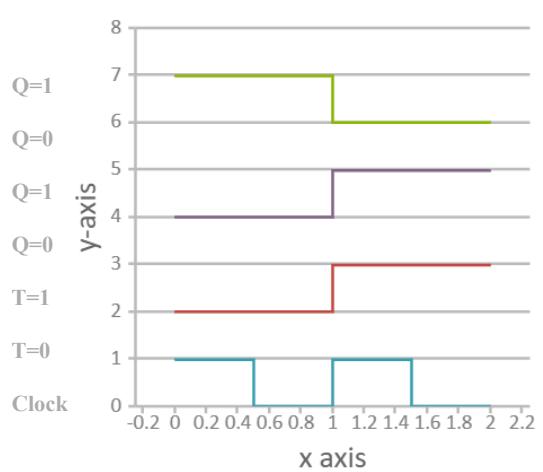
TRUTH TABLE

Add

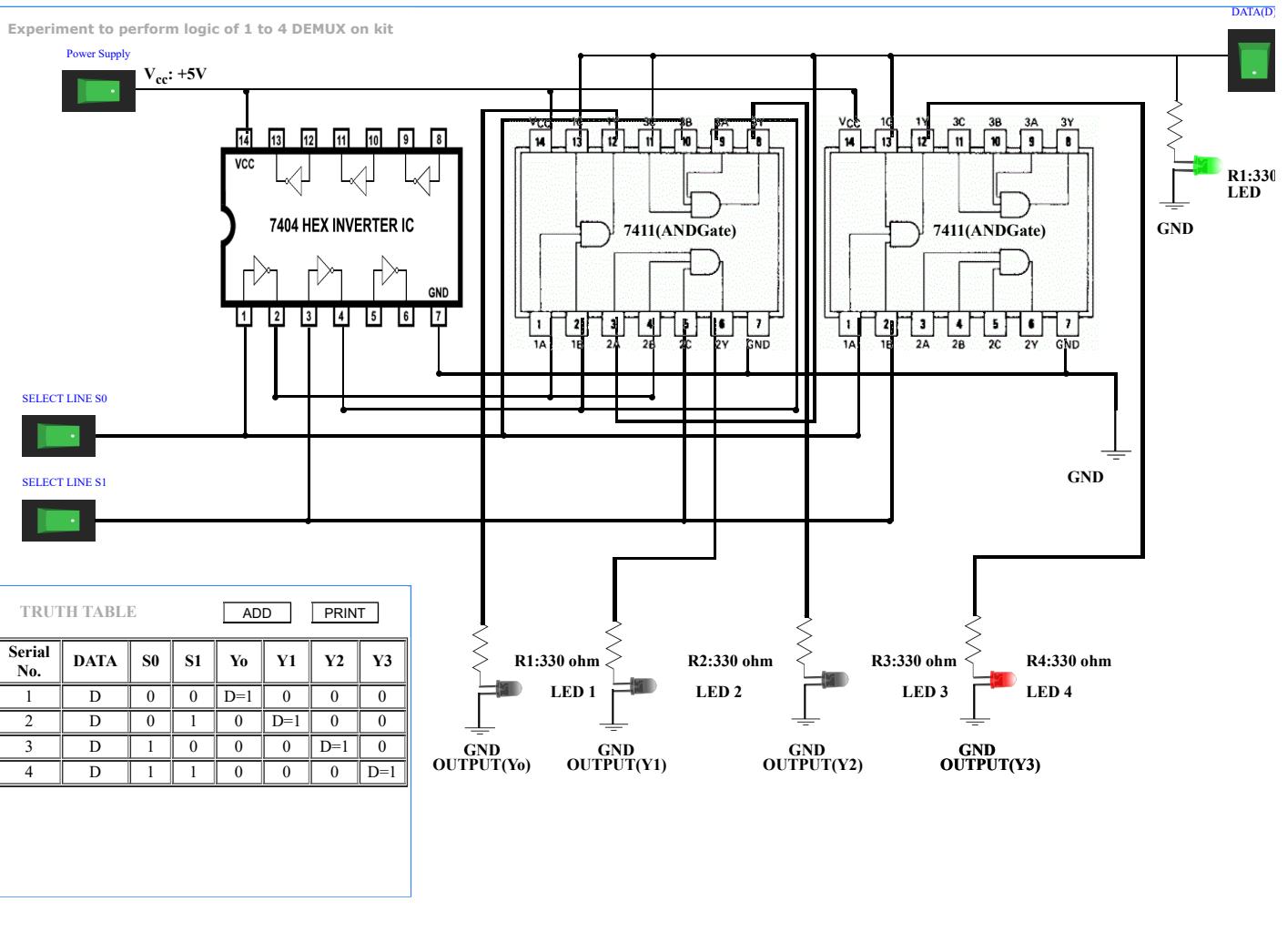
Print

Serial No.	Clock	T	Q_{n-1}	\bar{Q}_{n-1}	Q	\bar{Q}	Remarks
1	1	0	x	x	0	1	No change
2	1	1	0	1	1	0	Toggle

TIMING DIAGRAM

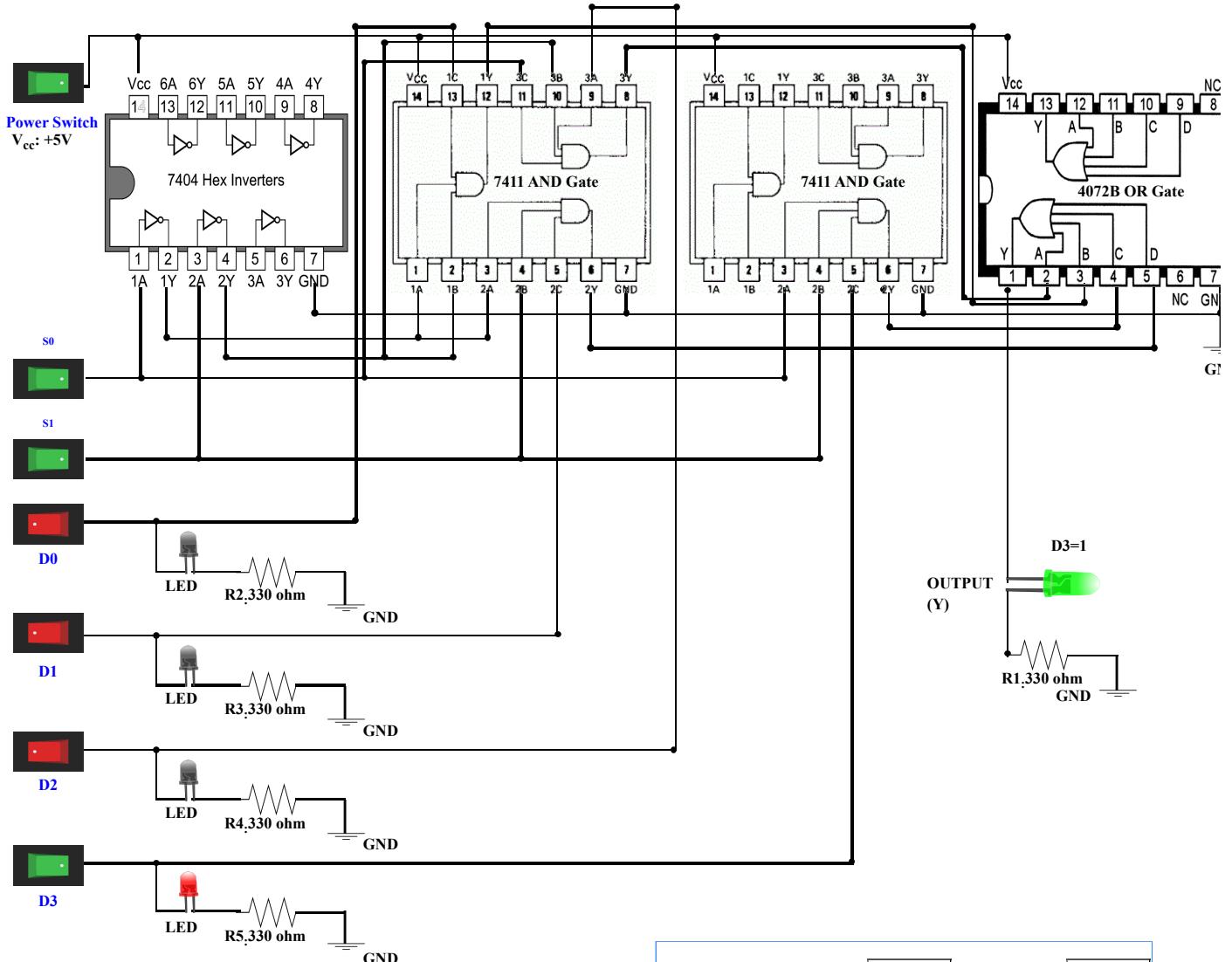


INSTRUCTIONS



INSTRUCTIONS

Experiment to perform logic of 4:1 Multiplexer on kit



TRUTH TABLE

Serial No.	S0	S1	OUTPUT (Y)	OUTPUT VALUE
1	0	0	D0	0
2	0	0	D0	1
3	0	1	D1	1
4	1	0	D2	1
5	1	1	D3	1