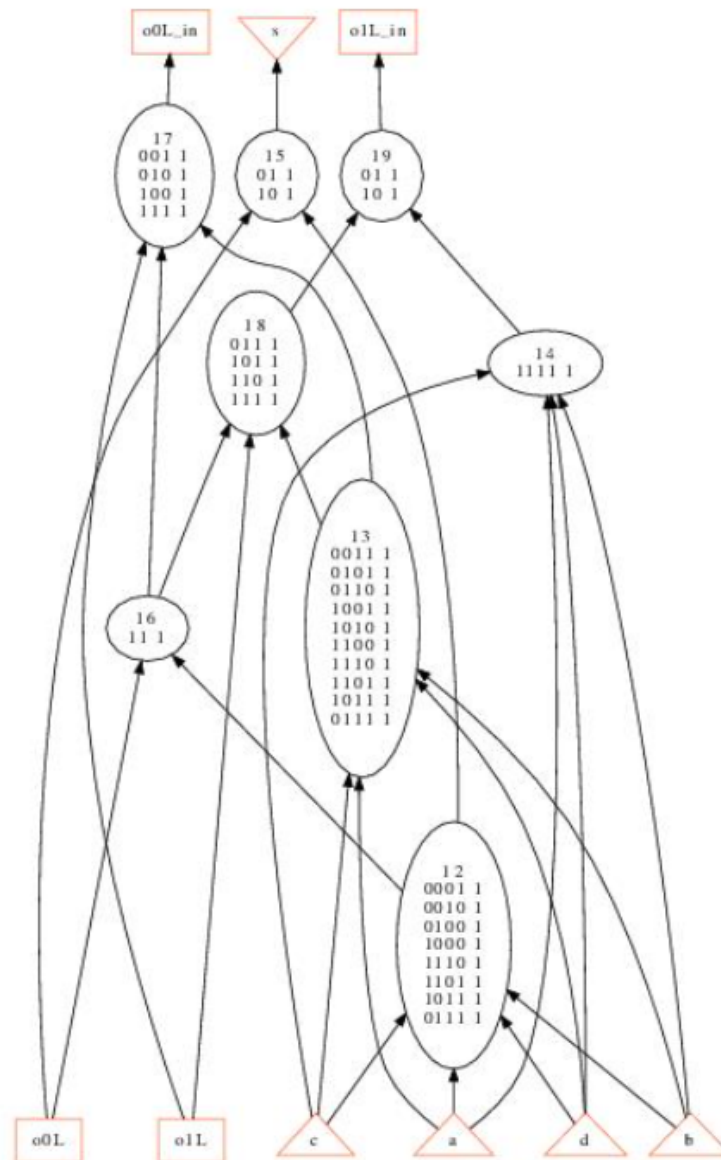


PA1 report

1. results of "show" and "show.bdd -g" after step 3, 5, 7 in Part 1

Network structure visualized by ABC
Benchmark "SERIAL_ADDER". Time was Fri Oct 8 04:24:20 2021.

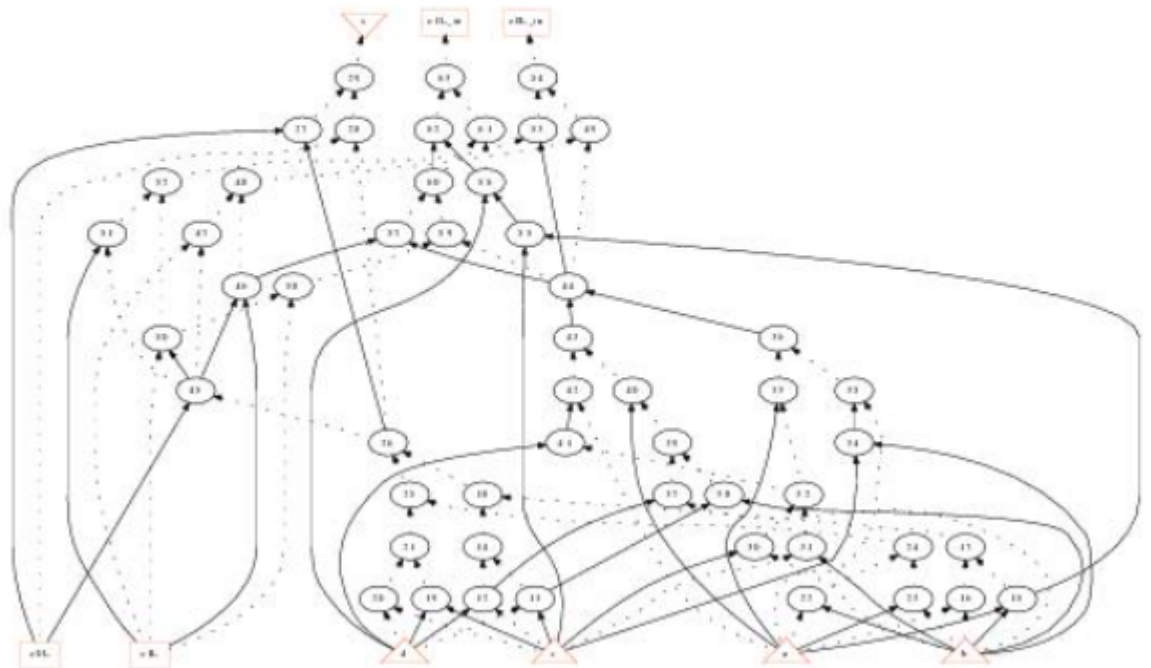
The network contains 8 logic nodes and 2 latches.



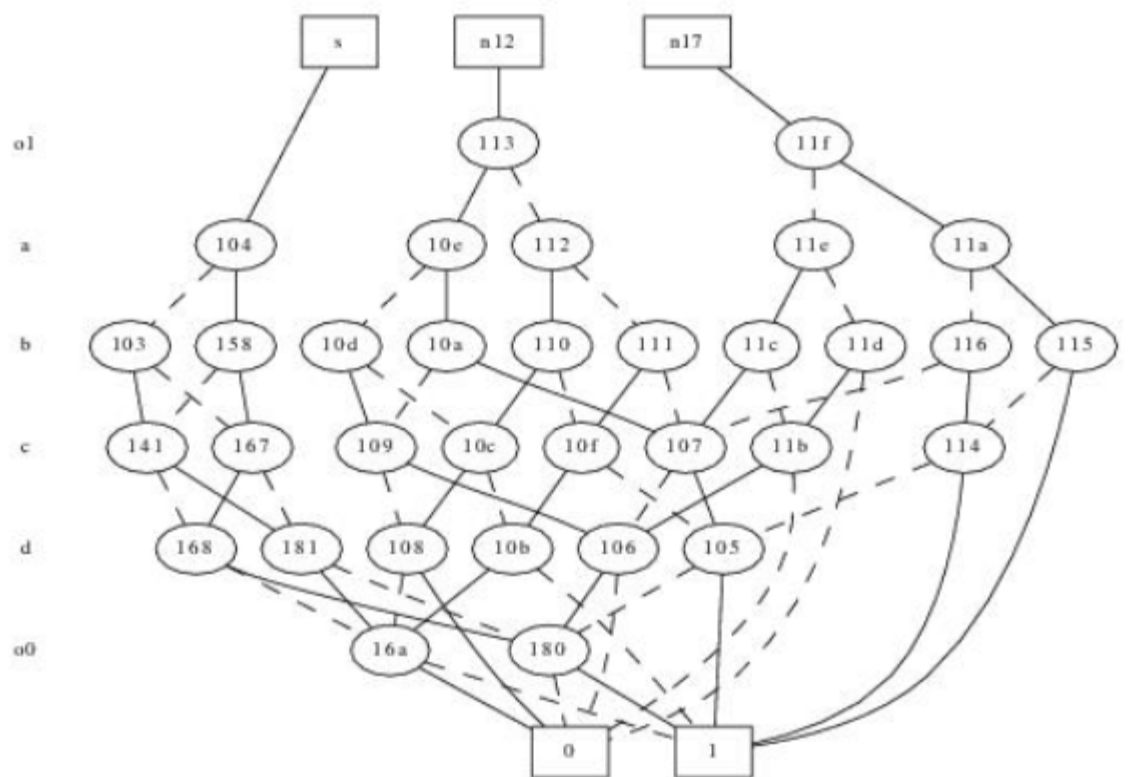
a.

Network structure visualized by ABC
 Benchmark "SERIAL_ADDER". Time was Fri Oct 8 04:34:45 2021.

The network contains 52 logic nodes and 21atches.



b.



c.

2. answers of question (a), (b) in Part 2

a.

```

abc 01> read lsv_fall_2021/pa1/4b_serial_adder.blif
abc 02> ps
SERIAL_ADDER          : i/o = 4/ 1 lat = 2 nd = 8 edge = 24 cube = 32 lev = 4
abc 02> aig
abc 02> ps
SERIAL_ADDER          : i/o = 4/ 1 lat = 2 nd = 8 edge = 24 aig = 57 lev = 4
abc 02> strash
abc 03> ps
SERIAL_ADDER          : i/o = 4/ 1 lat = 2 and = 52 lev = 11
abc 03> |

```

i.

```

abc 03> read lsv_fall_2021/pa1/4b_serial_adder.blif
abc 04> ps
SERIAL_ADDER          : i/o = 4/ 1 lat = 2 nd = 8 edge = 24 cube = 32 lev = 4
abc 04> bdd
abc 04> ps
SERIAL_ADDER          : i/o = 4/ 1 lat = 2 nd = 8 edge = 24 bdd = 27 lev = 4
abc 04> collapse
abc 05> ps
SERIAL_ADDER          : i/o = 4/ 1 lat = 2 nd = 3 edge = 17 bdd = 27 lev = 1
abc 05> |

```

ii.

b. the steps are as follows,

- i. read design.aig
- ii. logic
- iii. print_factor