

# Logic Synthesis and Verification

## Programming Assignment 1

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### List of Files

- `sfa_4num.blif` is the `*.blif` representation of the 4-number serial full adder.
- `b06507027_LSV_PA1_report` is this report.

### 1 [Using ABC]

- (a) The combinational part of the circuit reads 6 inputs:  $a, b, c, d, c_{in}^{(1)}, c_{in}^{(2)}$  and gives 3 outputs:  $s, c_{out}^{(1)}, c_{out}^{(2)}$ , where  $c_{in}^{(1)}, c_{out}^{(1)}$  and  $c_{in}^{(2)}, c_{out}^{(2)}$  are the carry-in/out of the twos and fours digits. Since  $c_{out}^{(2)}c_{out}^{(1)}s$  is the number of 1's in the inputs, we have

$$\begin{aligned} s = 1 &\Leftrightarrow \# \text{ of 1's in the inputs is 1, 3, or 5} \\ c_{out}^{(1)} = 1 &\Leftrightarrow \# \text{ of 1's in the inputs is 2, 3, or 6} \\ c_{out}^{(2)} = 1 &\Leftrightarrow \# \text{ of 1's in the inputs is 4, 5, or 6} \end{aligned}$$

A Python script is used to generate the on-sets via listing permutations of 0's, 1's, and -'s. For example, to list the cubes that covers the case where the number of 1's in the inputs is 2 or 3, we consider all possible permutations of "11000-".

- (b) 3. Figure 1 is the image that command `show` outputs:  
 5. Figure 2 is the image that command `show` outputs after `strash` ing:  
 7. Figure 3 is the image that command `show` outputs after `collapse` ing:

### 2 [ABC Boolean Function Representations]

- (a) 1. As the command `aig` only turn each node into AIG locally, it only affect the internal representation, which can be seen from running `ps`, and when `show` ing the network, the output is still an SOP, albeit optimized. On the other hand, the command `strash` turn the whole circuit into AIG, which when `show` n also outputs an AIG.
2. As in (a), `bdd` has only local effects, while `collapse` turn the whole circuit into a BDD. However, in this case the outputs when running `show_bdd -g` are exactly the same since the command `strash` the circuit implicitly anyway before drawing the BDD (see `src/base/abci/abc.c` Line: 3230).
- (b) A `strash` ed network cannot be turned directly into SOP, but we can first `collapse` it, then the BDD can be turned back into SOP by running `sop`.

Network structure visualized by ABC  
 Benchmark "fa\_4num". Time was Mon Oct 4 19:12:47 2021.

The network contains 3 logic nodes and 2 latches.

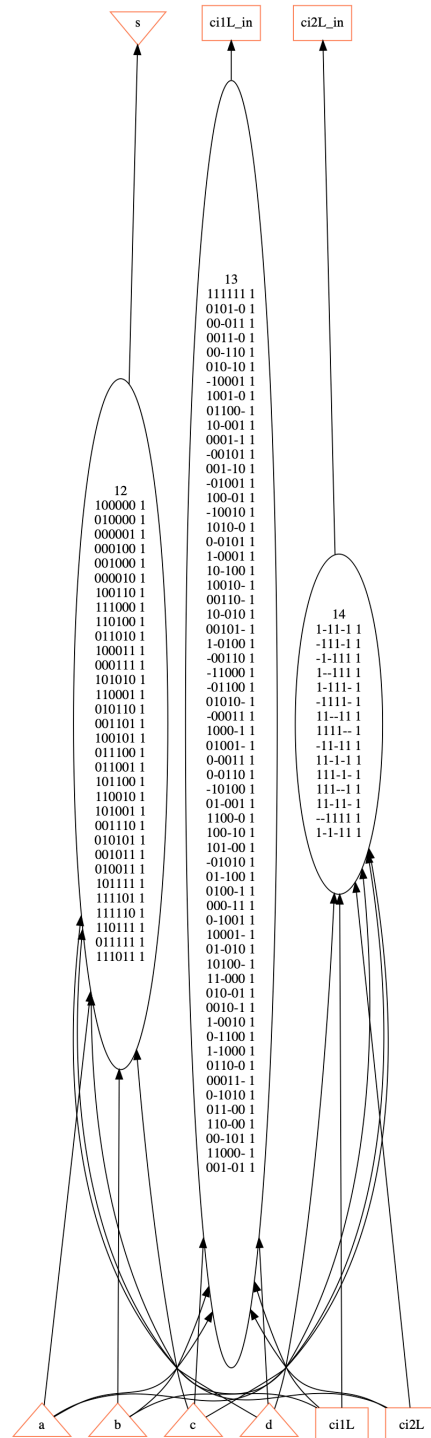


Figure 1: the image that command `show` outputs

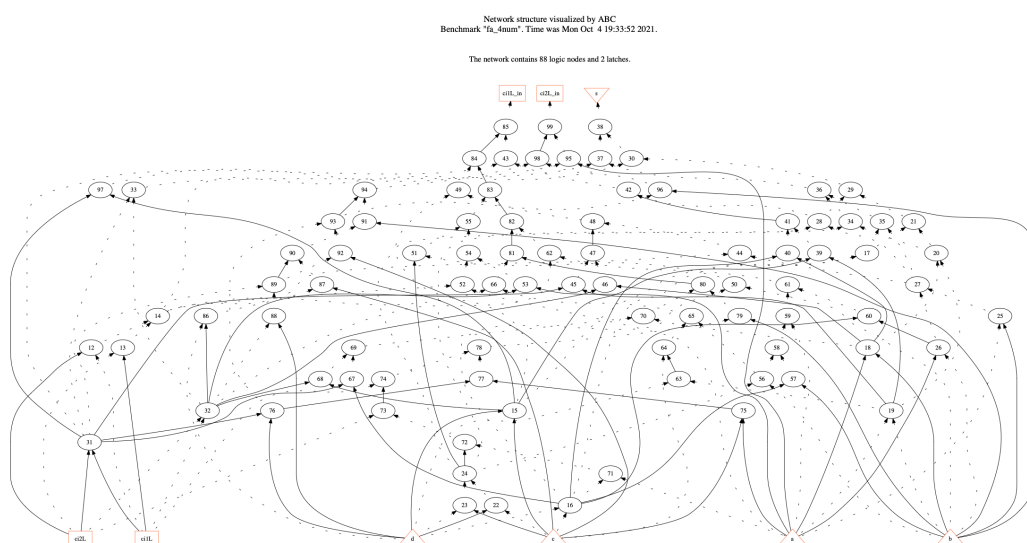


Figure 2: the image that command `show` outputs after `strash` ing

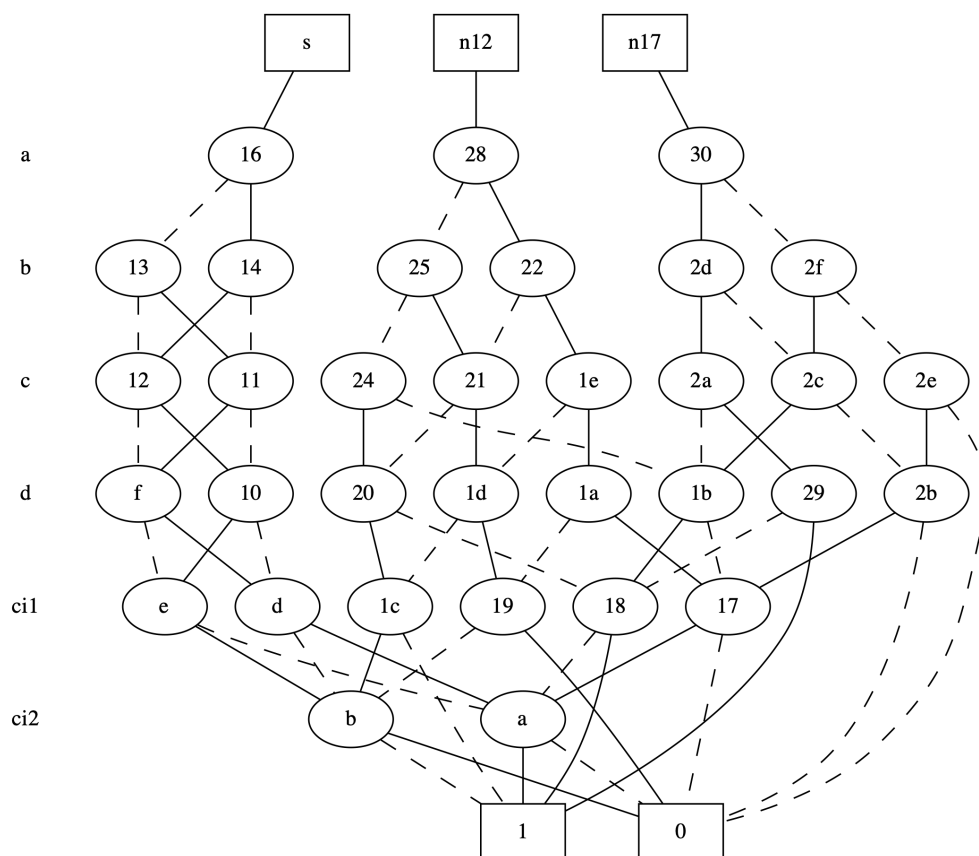


Figure 3: The image that command `show` outputs after `collapse` ing