Logic Synthesis and Verification, Fall SEMESTER, 2023-24 PA1, September 17, 2023

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2 [Using ABC]

- (a) The two-bit unsigned multiplier is written in the file "mul.blif".
- (b) Figures 1. shows the screenshot of the commands. With the given 7 commands, we can obtain another 3 figures, which is the visualization of the network structure(Figure 2), AIG(Figure 3) and BDD(Figure 4), respectively.

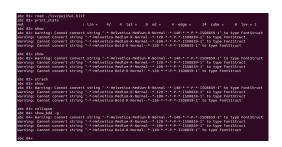


Figure 1: Screenshot of the commands

Network structure visualized by ABC Benchmark "mul". Time was Sun Sep 17 13:05:20 2023

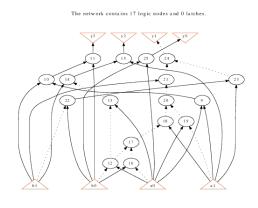


Figure 3: Visualization of AIG

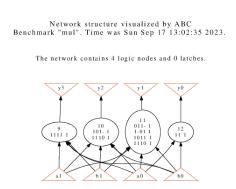


Figure 2: Visualization of network structure

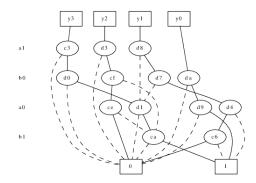


Figure 4: Visualization of BDD

Network structure visualized by ABC
Benchmark "mul". Time was Sun Sep 17 13:13:29 2023

The network contains 4 logic nodes and 0 latches.

Figure 5: logic network in AIG

Network structure visualized by ABC
Benchmark "mul". Time was Sun Sep 17 13:14:06 2023.

The network contains 4 logic nodes and 0 latches.

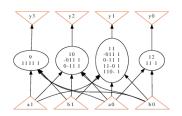


Figure 7: logic network in BDD

Network structure visualized by ABC Benchmark "mul". Time was Sun Sep 17 13:05:20 2023

The network contains 17 logic nodes and 0 latches.

Figure 6: structurally hashed AIG

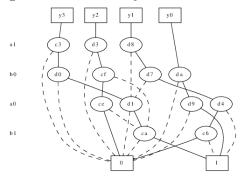


Figure 8: collapsed BDD

- (a) 1. Figure 5. and Figure 6. shows the logic network in AIG and structurally hashed AIG, respectively. From the previous two figures, we may observe that there are differences between two networks since the command "aig" is used to convert logic function of the nodes to AIGs while the command "strash" is to transform the current network into an AIG.
 - 2. Figure 7. and Figure 8. shows the logic network in BDD and collapsed BDD, respectively. Similar to the relation between command "aig" and "strash", the command "bdd" transforms the network to BDD locally while the other one transforms globally.
- (b) Given a structurally hashed AIG, we may use the command "logic" and "show" to visualize the logic network with node function expressed in SOP, which is shown in Figure 9.

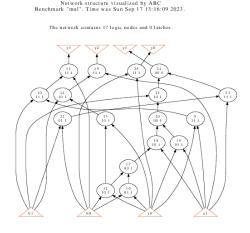


Figure 9: logic network with node function expressed in SOP