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EE M116L Prelab #2

1. Compare a half adder and a full adder in terms of their functionality and architecture.

A half adder is used to generate a carry bit and sum bit when given two input bits: input x and input y. In terms of architecture, we construct it using an AND gate and an XOR gate. The carry bit uses the AND of x and y inputs, while the sum bit uses the XOR of x and y inputs.

Half Adder Truth Table

X	**Y**	**Carry**	**Sum**
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Unfortunately, half adders are incapable of handling three inputs, which may comprise of inputs x, y, and a carry-in bit (that is, the carry bit from the next most significant column). This is where full adders are useful.

A full adder generates a carry-out bit and sum bit when given three input bits: input x, input y, and input carry-in. In terms of architecture, we construct it using two AND gates, two XOR gates, and an OR gate. All three input bits go through the two XOR gates to produce the sum bit, such that a sum of 1 is produced only when exactly one or three inputs are 1. Inputs x and y go through an AND gate while the carry-in bit and the result of (x XOR y) go through the other AND gate. The results of these two AND gates are ORed together to produce the carry-out bit.

Full Adder Truth Table

X	**Y**	**Carry-In**	**Carry-Out**	**Sum**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

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2. Briefly compare a 4-bit serial adder to a 4-bit parallel adder.

A 4-bit serial adder uses shift registers and a full adder circuit. It operates sequentially with operation time dependent on the number of bits being added.

For example, adding 9 (1001) and 11 (1011) follows a process much like:

X	Y	Carry-In	Carry-Out	Sum
1	1	0	1	0
0	1	1	1	0
0	0	1	0	1
1	1	0	1	0
				(1)

As expected, the decimal result is 20. When limited to 4 bits, we only see a decimal value of 4.

In contrast, a 4-bit parallel adder uses parallel load registers and full adder circuits based on the number of bits in adder in order to operate faster; operation time is independent on the number of bits being added. In architecture, a parallel adder is a series of cascaded full adders that pass along the next carry-in bit.

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Serial Adder:

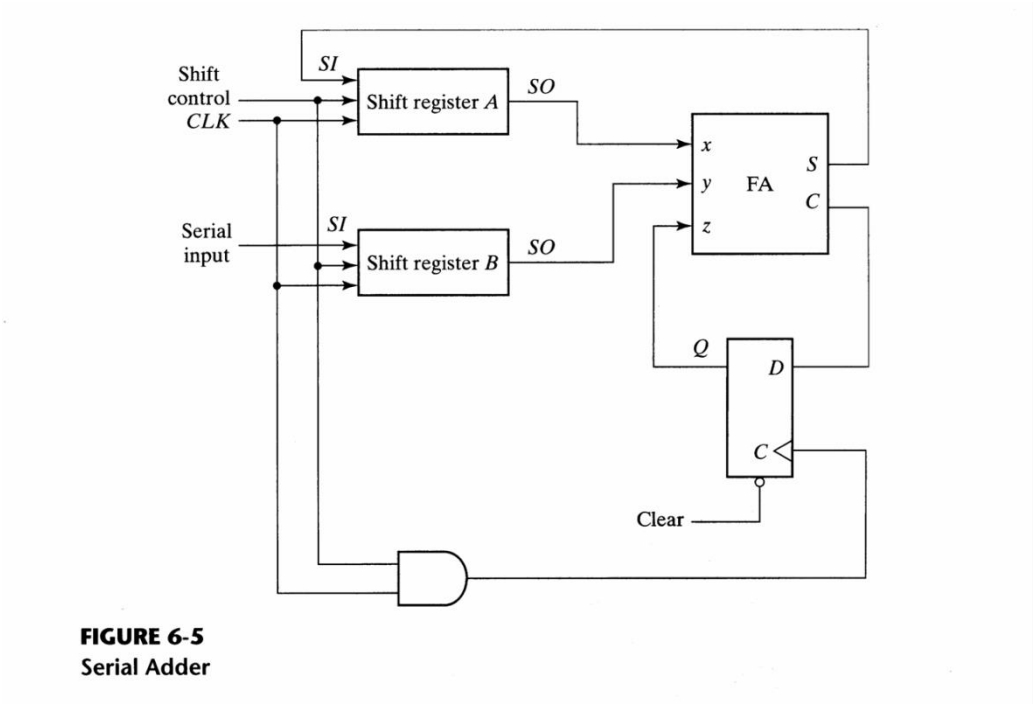
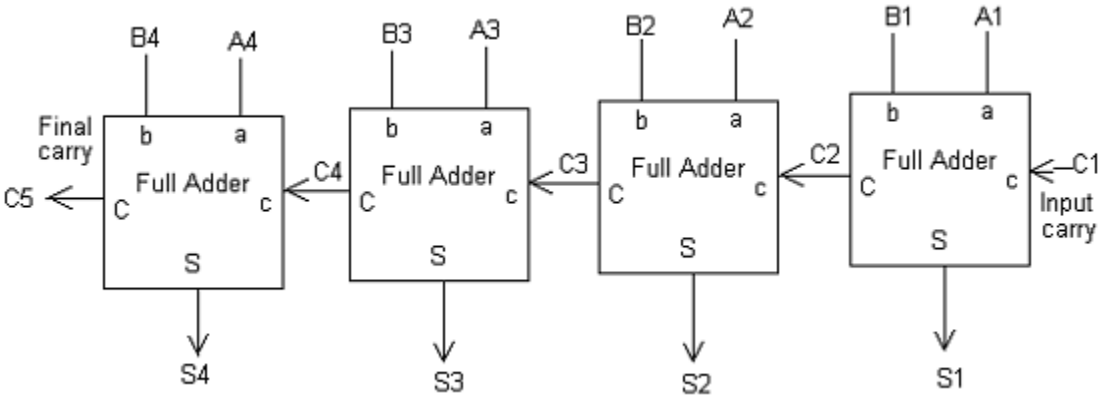


FIGURE 6-5
Serial Adder

Parallel Adder:



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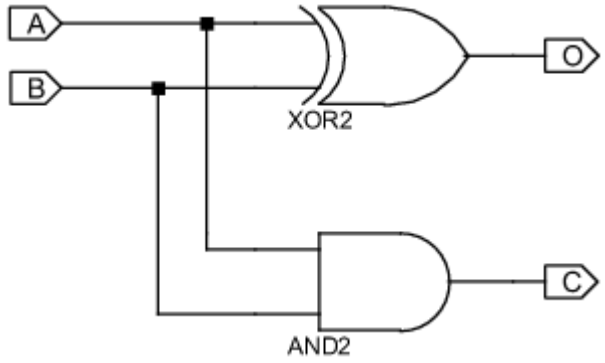
Half Adder:



Full Adder: