CS 152A Syllabus
Computer Science Department, UCLA
Spring 2014

Location: Boelter Hall 3424
Instructor in charge: Lei He (lhe@ee.ucla.edu)

Section #	Time and Days	TA
4	TR 2PM – 3:50PM	Tianheng Tu (116l2014spring@gmail.com)

This lab involves of implementing digital logic designs, and you will find that you will be applying concepts you learned in CS 51A. There will be 6 labs with increasing levels of difficulty. We will be using Spartan-III Xilinx boards and working with the ISE design software to implement designs using schematic and HDL editors.

Specific Objectives of the Course

- Learning how to use discrete components, breadboards, oscilloscopes, voltmeters, datasheets, and instruction manuals
- Being able to design a digital system
- Being able to implement your designs with a schematic editor and VHDL
- Being able to program and use an FPGA
- Being able to work with a partner to produce working, well-designed results

Grading

Quizzes	15%
Participation and Attendance	10%
Final Exam	20%
Laboratory Work (Lab 1-5: 15%, Final Project: 25%)	55%

Lab Work Grading:

Prelab (Graded on effort)	10%
Demo/Correctness	55%
Cleaniness/Tidiness	20%
Writeup (including comments on the lab and your lab experience)	15%

Prelabs

You must prepare a prelab report before each new lab exercise (excluding the first lab exercise). The deadline for the prelab report is the first meeting for that exercise. In the prelab report you should include the preparation work for the lab, such as a circuit design. In addition, you must answer whatever is implicitly or explicitly requested in the lab report. You TA will assign you a grade for the prelab, and ensure that you are on the right track with your design.

Lab Reports
When you are done with your project, inform your TA to demo your work, who will sign your prelab to signify the quality of your demo. Unless specified otherwise, follow this guideline for you lab write-up. (Lab 1, Lab 2, and the final project will have a different format)

- Cover page (names, project # and name, date, TA name, distribution of work)
    - Do not write your name anywhere other than on the cover page
- Schematic files (everything)
    - On each of the schematic files, write at least two sentences to describe what your design methodology was. (You can use arrows to point at modules, etc.)
- VHDL files (if any)
- Prelab with your prelab grade and your demo grade on it

Groups
Each lab group should be made up of two students and each group must submit one lab report. Both group members are expected to make similar contributions. Describe the contribution of each person in the end of your lab report.

Participation
Participation accounts for 10% of your overall course grade. This is evaluated based on your individual contribution to the projects, TAs questions, your overall knowledge of the project (based on project interviews), and the quality of the cleanliness of your work environment. You are expected to keep your work environment clean and leave all supplies in proper working order.

Backup Requirement
Please backup your project onto portable USB memory sticks or floppy disks. The computers are shared among students from all lab sections, so your files can and will be deleted, removed or damaged at any time.

Course Website
You will need to download your laboratory assignment and any other necessary information (such as datasheets and tutorials) from the course website, with the exception of the lab 1 assignment which will be handed out to you. Please check the course website for any important announcements. I would suggest downloading all of the materials on the webpage onto a USB drive and bringing to class with you.

Lab Computers
The lab computers do not have full internet access. You have access only to the xilinx website, which can help you debug your designs. Many students have tried to play with the internet settings to gain full internet access, none have succeeded. Instead they have disabled the license for the modelsim software. Instead, please use the SEASNet or BOL labs to gain access to the internet.

Cheating
Cheating in no form will be tolerated. All students found to be cheating will be reported.

Extra Lab Time
All students from all sections (including electrical engineering sections) may utilize the lab during other CS 152A and EE 116L lab sections. TAs will be happy to help, but priority will be given to students enrolled in that section.

References
1. *Introduction to Digital Systems* by Ercegovac, Lang, and Moreno
2. http://www.xilinx.com
The internet is a good source for quick info, especially for googleing part numbers to get chip datasheets. All material must be properly referenced. Plagiarism will not be tolerated.
3. Check the materials section of the website for additional handouts that will be necessary to complete the labs.