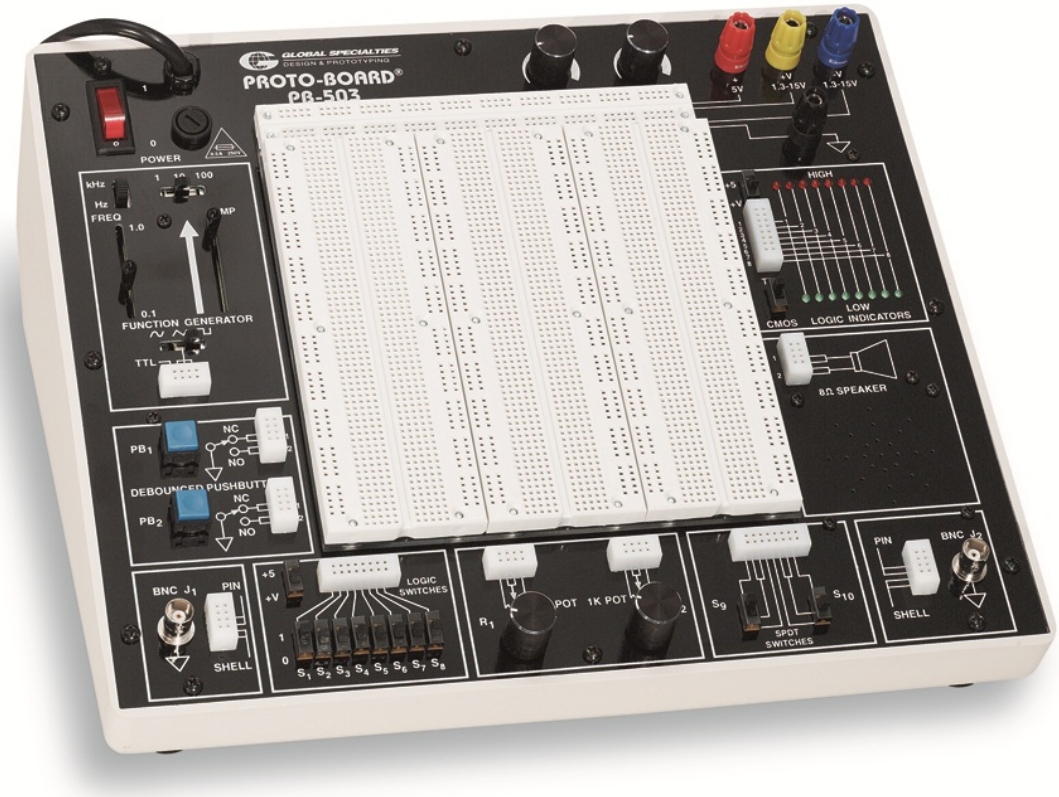
CS M152A
DIGITAL DESIGN LAB



Lab 1 Laboratory Familiarization: The Real World

The purpose of this laboratory assignment is to introduce you to the new devices we will be using throughout the quarter.

CS M152A DIGITAL DESIGN LAB

LABORATORY FAMILIARIZATION: THE REAL WORLD

Introduction

Throughout the quarter, you will be using variations and combinations of the following devices. The goal of this lab is to help you learn how to use them.

- Two-Channel Oscilloscope – when using the Oscilloscope, be sure to set the multiplier on the Probe Wand to 1x.
- 74LS TTL Series Chips (74LS00, 74LS04, 74LS74, 74LS163, 74LS393)
- 74HC00 – CMOS NAND Gate
- 555 Timer
- TTL and CMOS Voltage Levels
- Karnaugh Maps and Boolean Algebra
- Combinational VHDL
- Latches and Flip-Flops
- Simple Sequential and Asynchronous Circuits
- 7-Segment Display
- PB-503 Protoboard– when using the Protoboard, be sure to use the Red Power Supply as your 5V power. This will be your power source for all labs in this class. If this doesn't output 5V, then use the Yellow Power Supply and turn the knob to get it to 5V.

Procedure

This lab is divided into several exercises in order to guide you through the design, construction, and debugging processes. You will be working in groups of two or three for this class, and you will stay in the same groups for the duration of the quarter.

You will be asked to wire circuits for many of the exercises and you will be reusing them, so make sure to save those circuits. Manage your breadboards efficiently so that you can best utilize the space you have available. Before you begin, make sure to read and understand the whole assignment.

For each exercise, be sure to design, build, test, debug, and fix your circuit before continuing on to the next one. Also, be sure to answer all the questions asked in the lab.

You do NOT have to get checked-off on an exercise before proceeding to the next one.

Prelab

Due 1st Session:

1. Do research and write a **brief** report on how to read the coded values of resistors and capacitors.

Due 3rd Session:

1. Draw the architecture of an SR-Latch (not an SR Flip-Flop) and include its truth table.
2. Work on the K-Map of the 7-Segment decoder in Exercise 8.

Exercise 1 – TTL/CMOS Static Electrical Characteristics

The logic values of 1 and 0 are represented by voltage levels in the hardware logic implementation. The voltage levels and other electrical characteristics are not standardized from one logic family to another. We will use both TTL (Transistor-Transistor Logic) and CMOS (Complementary Metal-Oxide Semiconductor) logic. The voltage ranges for the two logic families are not compatible.

In this exercise, you will first measure the electrical characteristics of a TTL gate and of a CMOS gate using the circuit in Figure 1. Wire up this circuit using a 74LS00 integrated circuit chip (IC). **Do not forget to wire power and ground!** These connections are usually omitted from logic diagrams, as the power and ground of the 74LS series are generally the top-right and bottom-left pin, respectively. Typically, the top of the chip has a small semi-circular cutout or a white dot next to pin 1.

Ground the input of the inverter (the first NAND) and measure the output voltage using the oscilloscope. Be sure to be using the voltage markers on the oscilloscope. Connect the input to logic 1 and repeat the measurement.

FIGURE 1: (LEFT) LOGIC LEVEL MEASUREMENT [MEASURE VOLTAGE AT OUT NODE], (RIGHT) POWER SUPPLY WIRING

Next, using a 74HC00, wire up the same circuit and hook VCC to a +5V supply. Perform the same measurements and record your results. Look up the valid input and output voltage ranges using the datasheet for a 74LS00 and a 74HC00 (provided on Courseweb). **For each experiment, do your output values satisfy the range specified in the datasheets?**

Consider interfacing a TTL inverter to a CMOS inverter and vice versa. Look at the IC datasheets for the CMOS and TTL ICs (74HC00 Datasheet has a Table on Page 2, 74LS00 Datasheet has a Table on Page 2). Based on the +5V supply you used, find out the recommended input voltage for HCMOS inputs.

What potential issues could you come across when interfacing TTL and CMOS components? Run the two experiments (interface TTL to CMOS and vice versa) and make voltage measurements.

Exercise 2 – 555 Timer

One way to generate a relatively good clock is to use a 555 Timer IC. Wire the 555 according to Figure 2A. Use the datasheet if necessary.

Typical values for the resistors and capacitors are:

- R1 = 10k
- R2 = 10k
- C = 10nF

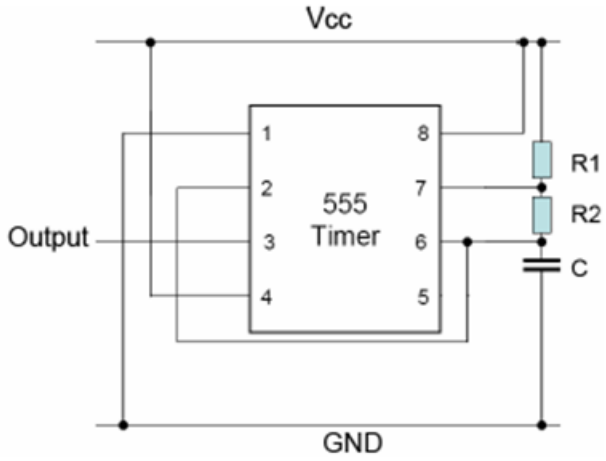


FIGURE 2A - 555 TIMER INTEGRATED CIRCUIT CHIP

FIGURE 2B – POTENTIOMETERS

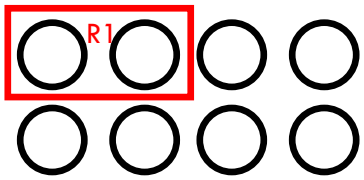


FIGURE 2C - POTENTIOMETER WIRING

You may be provided with different values. Make sure that you indicate the values you use in your report. Also, make sure that you have wired the VCC and GND pins. **What is the frequency of oscillation?**

The duty cycle of any rectangular waveform refers to the percentage of the full cycle that the signal remains at logic 1. If the signal spends half its time at logic 1 and the other half at logic 0, we have a waveform with a 50% duty cycle. This describes a perfect, symmetrical square wave. **What is duty cycle of your clock?**

Now, you will swap out one of the resistors you have been using (R1) and use the potentiometers on the Protoboard. The left potentiometer functions as a resistor with a variable value (1kΩ - 10kΩ). Following Figure 2C, you can connect your wires to the potentiometer and use it as your R1. Make sure that you are still using constant 10kΩ register for R2. Extrapolate this concept and then play with the potentiometer. **What happens as you turn the left potentiometer knob?**

Once you have determined what potentiometer knob's functionality, go ahead and adjust your duty cycle to be 60%. Measure the maximum voltage of the clock then use the TTL IC datasheet to explain why you can use this signal as your clock.

You will be using this 60% duty cycled clock through Exercise 5. We recommend attempting Exercises 2, 3, 4, and 5 during the same lab session.

Exercise 3 – Glitches

Wire up the circuit in Figure 3 using the above clock and 4 NAND gates of a 74LS00. The output GLIT is a purposely glitchy output caused by the circuit. Use the oscilloscope to measure the approximate width of the 'glitch'. **Why is it not possible to measure the width accurately enough?**

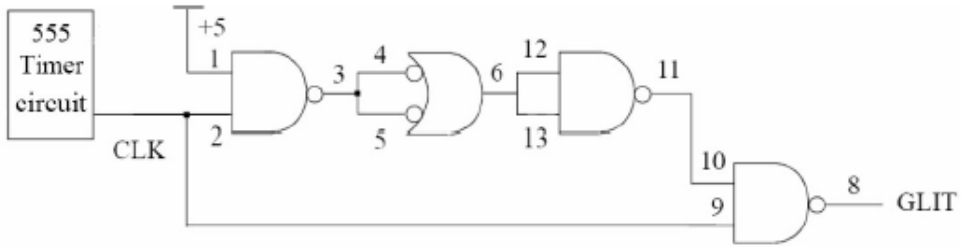


FIGURE 3 - GLITCH MEASUREMENT CIRCUIT (74LS00)

Why does this glitch occur, and what is the lesson learned from this exercise?

Exercise 4 – Asynchronous Counter

Wire up the clock from the previous exercise to a Dual 4-bit Binary Counter, as shown in Figure 4. You do not need to disconnect the previous circuit. In this exercise, we are concerned with how each output bit changes with respect to other bits. Since this counter increments its count every falling edge of the clock, each output bit must have a period twice that of the next significant bit. Because of this characteristic, counters make good clock dividers; if you want a slower frequency clock, it may be helpful to use a counter or a series of counters. Verify the counter's operation using the oscilloscope.

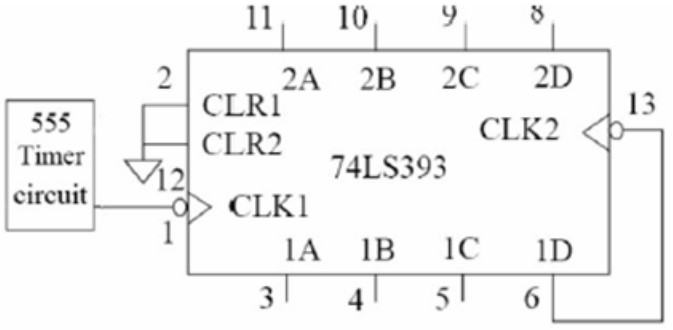


FIGURE 4 - CLOCK AND RIPPLE COUNTER

Exercise 5 – Synchronous Counter

One of the most useful Integrated Circuits of the 74LS series is the 74LS163. This IC is a 4-bit loadable synchronous counter with a synchronous reset.

Wire two 74LS163s so that they are always counting, as shown in Figure 5, connecting any output of your ripple counter (from previous exercise) to its clock input. You can also use the clock generated by the 555 timer. Trigger your scope on the most significant bit (MSB) and verify its operation.

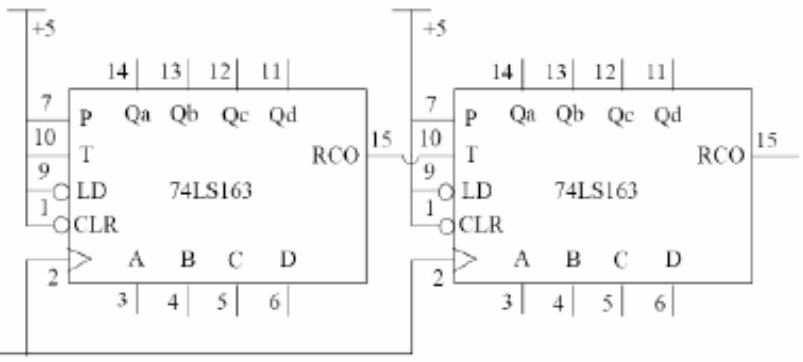


FIGURE 5 - SYNCHRONOUS COUNTER WIRING (RCO OF THE FIRST CHIP IS ONLY CONNECTED TO T)

Explain how RCO output and T input work? A timing diagram may be useful.

Be prepared to comment on the difference between the 74LS163 and the 74LS393 in terms of design, particularly, the differences in area between the two devices. By area, we are asking you to consider how complicated it is to implement the counter. **How many Flip-Flops and how much logic is required to implement each counter?**

Exercise 6 – Ring Oscillator

The 74LS04 is a SSI (Small Scale Integration) IC containing six separate inverter gates. The output pin for the 74LS04 can be found in the manufacturer datasheet. Construct the ring oscillator shown in Figure 6 using a 74LS04 but with **11** inverters instead of 5 inverters. One of the important timing parameters associated with the speed of digital logic gates is the propagation delay. Propagation delay is a measure of how much time is required for a signal to change state. It is measured as the time from the 50% point of the input to the 50% point of the output. It is often cited as the average of the high-to-low and low-to-high delays (corresponding to the two transitions). **Using a timing diagram, explain why this circuit oscillates.**

From this circuit, determine the average propagation delay of a TTL inverter by measuring the period of oscillation by using the time markers on the oscilloscope. If you cannot see the oscillation, play with the trigger of the oscilloscope. You can determine this by determining the number of gates a signal must travel through to complete a full period of oscillation. **What is the frequency of oscillation?** Measure the maximum and minimum voltages of the oscillation.

What should the period of oscillation be with 17 inverters in the ring? Rewire the circuit and measure the period. Comment on the new result. **What are the new values for minimum and maximum voltage?** Compare these values with the case with 11 inverters and comment.

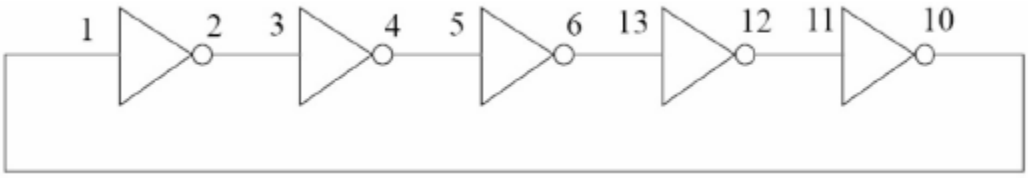


FIGURE 6 - RING OSCILLATOR (USING 74LS04)

Exercise 7 – Set-Reset Latch with NAND Gates

Build a Gated SR-Latch (Figure 7B) using NAND gates. On a 'set', the output Q should be high and $\overline{Q}$ should be low. On a 'reset', the output $\overline{Q}$ should be high and Q should be low. Furthermore, since the latch is gated, it will have an 'Enable' bit as input to specify whether the values for 'S' and 'R' will go through. However, since this is a clocked latch, the output can only change during the clk high phase; it is held at all other times. Explain how the SR latch works and demonstrate the functionality of the built circuit. Be prepared to explain what happens during the case when both S and R are high.

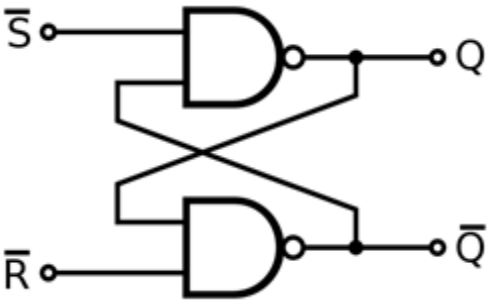


FIGURE 7A - SR LATCH DIAGRAM

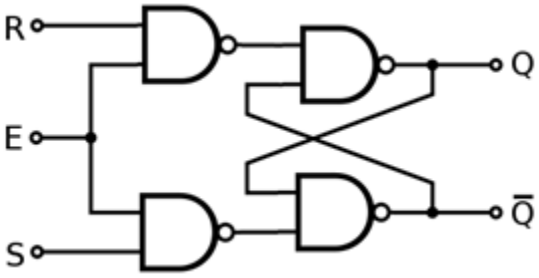


FIGURE 7B - GATED SR LATCH DIAGRAM

Exercise 8 – Writing Combinational VHDL Code

In this exercise, you will be designing a VHDL module that implements combinational logic. This module takes as input a 4-input binary coded decimal and outputs bits that will properly illuminate a 7-Segment display. Figure 7 shows the 10 possible digits.

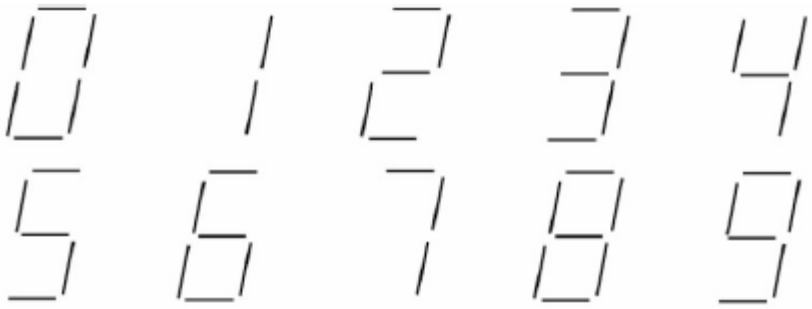


FIGURE 7 - 10 POSSIBLE SEGMENTED DIGITS

Using Karnaugh Maps, design the combinational logic that encodes the 4-bit input to the 7-Segment display. For the FPGA boards used in this class, note that you need to feed logic **0** in order to enable (light up) each segment and logic **1** in order to disable each segment. Fill out each Karnaugh Map, circling either the Minimal Sum of Products (MSP) or Minimal Product of Sums (MPS) in order to simplify your equations. Some segments can use MSP and others can use MPS. Next, program the combinational logic using VHDL. You will be programming this module onto a FPGA. Program the FPGA and appropriately assign pin numbers to switches and the 7-segment LED. Verify its functionality.

To begin this exercise, you will need to follow the directions given in the **Xilinx ISE Quick Tutorial** (provided on Courseweb). This tutorial will outline the process for creating a new project in Xilinx ISE. When you reach to the point of programming the board and creating the (User Constraints File) UCF, refer to pages 18 & 19 of the **Nexys3 Board Reference Manual** for pin assignments.