CSCI 6461 - Design Note for Project Part III

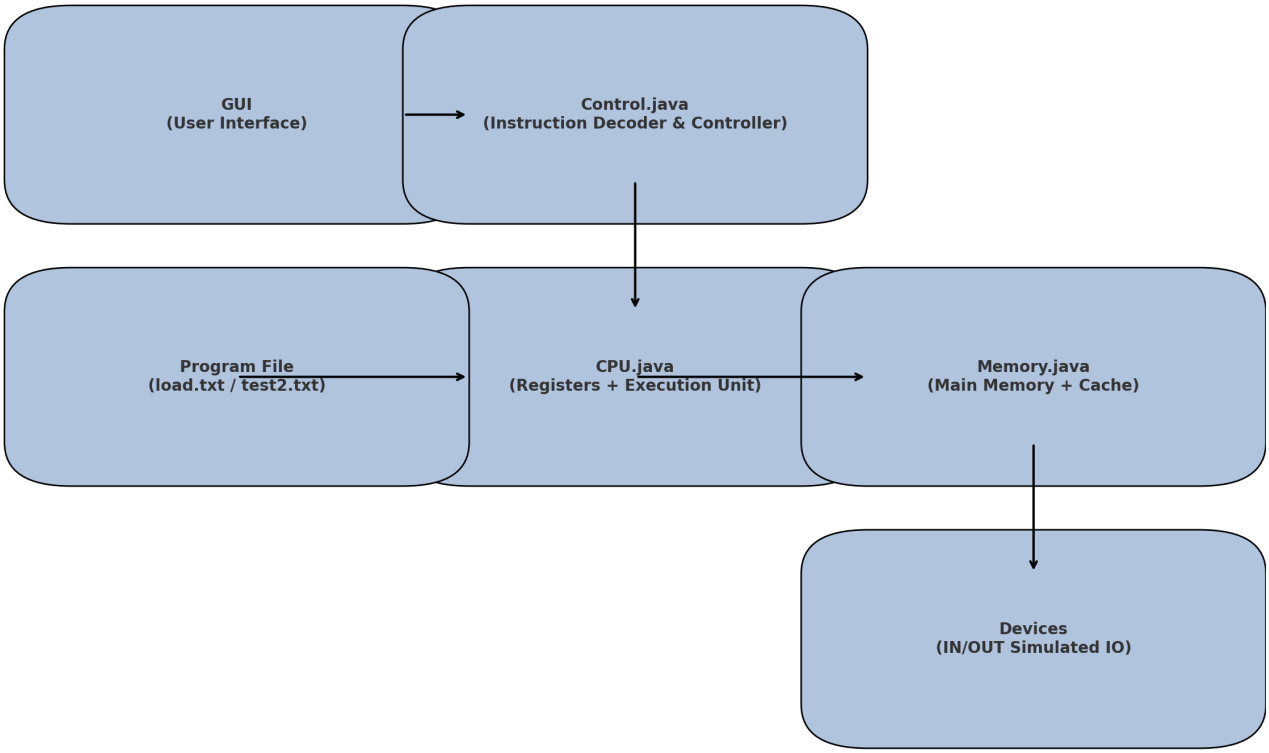
Team: Group 10 Date: April 12, 2025

1. Overview

This document outlines the architectural and functional design of the CSCI 6461 Simulator, focused on the Part III project phase. Part III specifically involves executing all instructions in the ISA, loading program files from disk, and demonstrating complex control flow including machine faults and TRAP handling.

Unlike the user guide, which covers installation and usage, this document focuses on software architecture, data flow, and component interaction.

2. Architecture Diagram



3. Component Breakdown

- GUI.java - Provides the interface for user interaction. Users can load machine code, step through instructions, and observe register/memory states.

- Control.java - Decodes instructions, manages program flow, and interacts with CPU and Memory. Implements instruction parsing, TRAP, and machine fault handling.

- CPU.java - Holds and manipulates registers like PC, IR, MAR, MBR, GPRs, and IXRs. Executes instructions passed by Control.java.

- Memory.java - Simulates main memory and a fully associative FIFO-based cache. All reads/writes from CPU and Control pass through this class.

- Program File (e.g., load.txt) - Contains machine code instructions used to test the simulator, including Program 2 for Part III.

- Devices - Simulated I/O devices like Console Printer and Keyboard, triggered using IN/OUT instructions.

4. Program Execution - Part III

Program 2 implements a paragraph search routine. It loads six sentences from simulated file input, prints them using OUT instructions, then accepts a word from the user and searches for a match using TRR and JZ instructions. Results are printed to output.

The simulator loads this logic via load.txt and executes it using the run/step functionality.

5. Memory Mapping

- Memory[0]: TRAP table base address
- Memory[1]: Machine fault handler address
- Memory[2]: Stores PC during TRAP
- Memory[200+]: Paragraph buffer for Program 2
- Memory[50-55]: Output targets for match reporting

6. Conclusion

This design document outlines the architecture and internal logic of the CSCI 6461 Simulator as applied to Part III. All components integrate successfully to execute the full ISA, including TRAPs and I/O, and Program 2 demonstrates complex instruction chaining and memory interactions.