Cactus Functional Summary and Measurements before Shipment Report

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In the following pages, we provide a summary of the Cactμs detector operation principle and functional characteristics and a short report on the results of spectroscopic measurement performed with the Cactus detector in May 2017, before the shipment to the HASP collaboration colleagues in Sacramento (CA, USA).

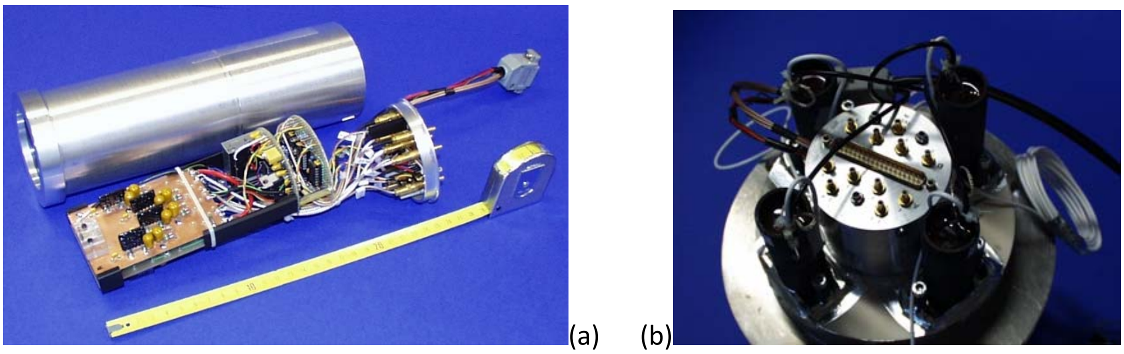
1. Summary of the Cactus detector operating principle and main hardware characteristics

The Cactus detector is composed by two bulk CdTe crystals, in which the anode side is segmented in 4 strips and the cathode is a mono-electrode. Each sensor has been provided by the Acrorad company (Japan). The CdTe sensors have a 10x10x2 mm^3 sensitive volume.

The two crystals are used in PTF irradiation configuration, i.e. with respect to the entrance windows of the Cactus detector container the CdTe sensor collecting electrodes are parallel to the cylinder axis (Figure 1a). Each anodes strip is readout by a charge sensitive preamplifier (CSP) (CLEAR PULSE CP-515-2, see Annex 1 for data sheet)

The two sensors are associated to a code: A1-4 and B1-4. "A" and "B" represent the two sensor units, while the number from 1 to 4 represent the anode strip. This code have a direct correspondence in the 8 radial connectors in the backside of the Cactus cylinder (Figure 1b). Just under the B radial connectors there is a radial connector marked "test-in", which use is specified in the following section. Beside to the "test-in" connector, there are a couple of trimmer that are used to (??) change the HV bias or some threshold (we are trying to reconstruct their use, may be you can also look inside and try to see where these trimmer act)

The two radial marked 1-2 and 3-4 was originally used to readout the four photomultipliers of the plastic anticoincidence. The trimmer between these two connectors was dedicate to the same photomultipliers.



(a) (b)

Figure 1. *(a) The overall Cactus detector system with its light-tight cylindrical container: at left the CdTe sensors containers (one for each side) board including the front-end CSPs; in the centre the DC-DC converter and bias filters; at right the output connectors. The 15 pins grey connector was for Photomultiplier HV bias*

The 37 pins male Canon connector (at centre of the cylinder backside) provide the low voltage bias to the CSP's, the HV bias to the CdTe sensors through an internal EMCO HV DC-DC converter and as output temperature and HV monitor signals (Figure 2).

Conn.	FUNZIONE	Tipo	N° poli
P3	PWER Out per Det & PL + Dig I/O + ANA HK In	D-Shell	37S

Pin #	Funzione	Note
1	+12 EL SW Out	CSP Positive Supply
2	±12 RET ±V_{CSP}	RET CSP Supplies
3	-12 EL SW Out	CSP Negative Supply
4		
~~5~~	~~+24V HV PL SW Out~~	~~Supply HV PL~~
6	RET + 12/+24 HV	RET HV
7	+12V HV Det"A" SW Out	Supply HV Det"A"
8	+12 V HV Det "B" SW out	Supply HV Det "B"
9		
10		
11	TS03 Monitor IN	Monitor Sensore 03 (Pt-2k) Det "A"
12	TS04 Monitor IN	Monitor Sensore 04 (Pt-2k) Det "B"
13	TS 05 Monitor IN	Monitor Sensore 05 (TMP-01)
14	TS 06 Monitor IN	Monitor Sensore 06 (TMP-01)
15	TS 07 Monitor IN	Monitor Sensore 07 (TMP-01)
16	TS 08 Monitor IN	Monitor Sensore 08 (TMP-01)
17		
18	+Vcc(CSP) Monitor IN	Monitor CSP positive supply
19	–Vcc(CSP) Monitor IN	Monitor CSP negative supply
20	+12EL +V_{CSP} SW Out	CSP Positive Supply
21	Ret ±12 RET ±V_{CSP}	RET CSP Supplies
22	-12EL –V_{CSP} SW Out	CSP Negative Supply
23		
~~24~~	~~+24 HV PL SW Out~~	~~Supply HV PL~~
25	RET + 12/+24 HV	RET HV
26	+12V HV Det"A" SW Out	Supply HV Det"A"
27	+12 V HV det"B" SW out	Supply HV Det"B"
28	+5V Dig SW Out	+5 Dig Supply
29	Monitor HV "B" IN	Monitor Voltage HV "B"
30	Monitor HV "A" IN	Monitor Voltage HV "A"
31		
~~32~~	~~PM1&2 IN (TTL)~~	~~Anticoincidence signal from PM1 e PM2~~
~~33~~	~~PM3&4 IN (TTL)~~	~~Anticoincidence signal from PM3 e PM4~~
34	+12V EL SWOut	+12V supply
35	Ret ±12	
36	-12V EL SW Out	-12V Supply
~~37~~	~~Monitor Voltage (HV PL)~~	~~Monitor HV-PL System~~

These are signal in V that are analogic temperature housekeeping Optional (*)

This are analogic monitor of the bias to CSP Optional (*)

This are analogic monitor of the HV CdTe bias Optional(*)

Several of the bias pins are duplicated because the different power board in the Cactus 2001 version.
In the new configuration in the new power board this bias shall be parallelized.

(*) These monitor required a dedicated electronics to be inserted in the data sotred and/or transmitted to ground with TLM

Figure 2. *The pin function of the 37 Pins Canon Connector in the Cactµs cylinder. In the table above, **"IN"** means a signal that comes from the detector system, while **"Out"** is for signals that should be provided to the detector system. The **yellow** highlighted pins are mandatory connections, while the pins crossed with a **red line** are not needed and can be left not wire connected. The **green** and **cyan** highlighted pins refer to monitor signals coming from the voltage monitor associated to detector components bias lines (HV and CSP low voltages) and from temperature sensors situated close to the CdTe sensor and on the front-end electronics board.*

2. "Test-in" signal use in CaCTµS

This section concern a hot issue in the Cactµs operation as a balloon borne payload. The quality and the scientific meaning of the data acquired during a stratospheric flight depends mainly on the stability of sensor channel gains. The gain equalisation can be performed in the lab using radioactive sources in controlled environmental conditions (temperature and humidity). During the flight the gain of each detector channel can drift mainly because of temperature variation and together with other environmental parameters such pressure, humidity, and magnetic field intensity.

In the 2001 flight Cactµs configuration, the gain and offset of each amplification channel was periodically checked during in-flight operations. This operation was performed through double valued voltage signals given to all 8 CSP chains by means of the "Test-in" connector in order to automatically calibrate any amplification channel gain and offset within ~2%.

Because most of the scientific data reliability depends on the equalization of the amplifier chains. Since CACTµS does not have an in-flight radioactive sources calibration system, it was decided to periodically stimulate the amplifier chains (including the detector front-end CSPs) by electrical test pulses (CAL/TEST).

Voltage pulse trains of two pre-definite amplitudes (VG and VOF) were generated under the digital control of independent two DACs and sent to the CSP "test-in" connector. The first amplitude VG, is used to test/calibrate any sensor channel gain, while the second (VOF=VG/k, k~50) was used to check the offset.

The "test-in" double amplitude pulse signal was issued to the detector channels with a constant rate. The generated shaped output signals, after the ADC conversion, were recorded as a "double amplitude pulse signal spectrum" in a dedicated memory.

This test/calibration procedure produce two energy peaks in a multichannel pulse height analysis of the type represented qualitatively in Figure 3. By evaluating the integral counts and the centroid of the peaks defined by the two energy bands $E_a<E(VG)<E_b$ and $E_c<E(VOF)<E_d$, it is possible to operate a correction for offset drifts and gain changes, respectively in order to maintain differences between channels at some percent level.

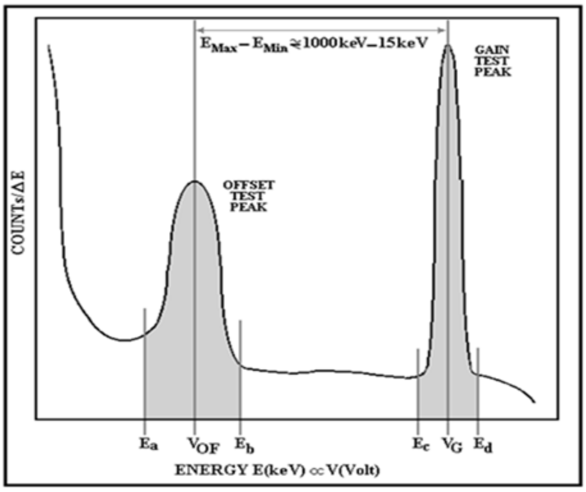


Figure 3. *The Cactus in-flight calibration scheme by using the "Test.in" double amplitude signal.*

Neglecting most of the details of the implementation in the 2001 Cactµs electronics system, the "current" calibration data for the offset-gain equalisation were stored in a dedicated memory (CAL Mem) with the window energy data E_a, E_b, E_c, E_d. The data obtained by the CAL/TEST procedure were compared with the reference ones stored the CAL Mem and used to correct the offset by adding or subtracting to any event signal a voltage amount proportional to the measured drift. The gain changes were compensated by issuing an increase or a decrease of the reference voltage of the ADC proportional to the gain shift detected in the CAL/TEST procedure. The calibration data extracted in the last CAL/TEST procedure were then uploaded in the CAL Mem to represent the reference for the following CAL/TEST.

3. IASF-Bologna Lab last measurements.

Before shipping the Cactus detector system, we made a set of lab measurements with radioactive source (^{137}Cs). We connected the 8 output channels of Cactus to a standard spectroscopic acquisition chain (Ortec research amplifier and Maestro acquisition SW). We performed the measurements setting two different shaping times in the Ortec amplifier: 0.5 and 3 µs. These values were the same used in the Cactus balloon flight in 2001 to readout the CdTe anodes. In the Cactus flight electronics, each anode signal was readout by two shaping amplifiers for 16 channels. The driving idea was to use fast and slow shaped signal to try to compensate the signal for trapping effect mainly due to holes mobility and lifetime characteristics (Auricchio N., et al., IEEE NSS Conf. Record 2015, DOI: 10.1109/NSSMIC.2015.758227).

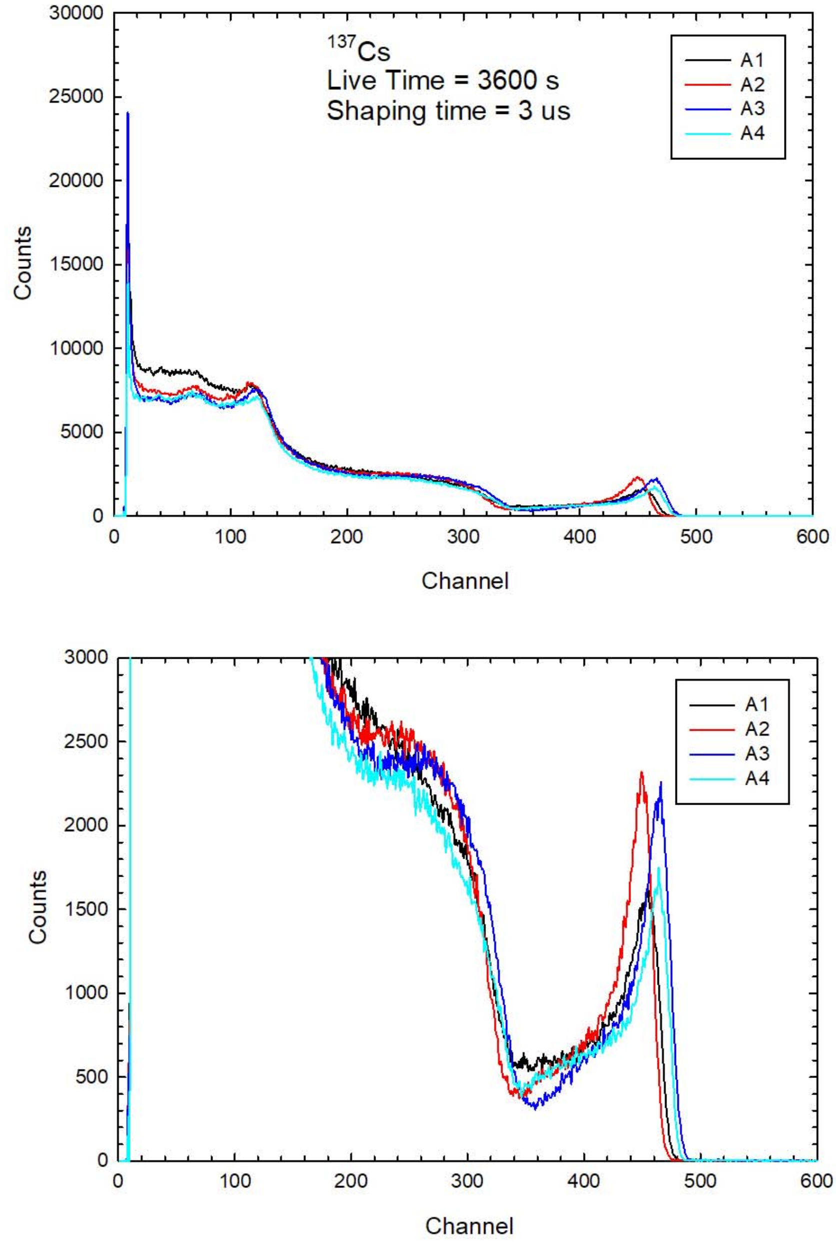


Figure 4*. CdTe sensor A, anode strip 1 to 4, 137Cs spectra obtained using 3 µs shaping and integrated over one hour live time.*

The signals from the 4 anodes of sensor A show a good intrinsic equalisation. The maximum shifting between the 662 keV peaks is of ~15 channels, i.e. ~3.5%. The differences in efficiency between the two anode groups (1, 4) and (2, 3) are mainly due to the fact that 1 and 4 are the external anodes (border effect) of the sensor A. The change, in maximum counting in the ^{137}Cs peak, between the two anodes strip group is ~10%, is also confirmed by the peak integral counts. In fact, the (2,3) anodes group exhibits a peak efficiency that is again ~10% (in average) better than the one measured for (1,4) anode strips group.

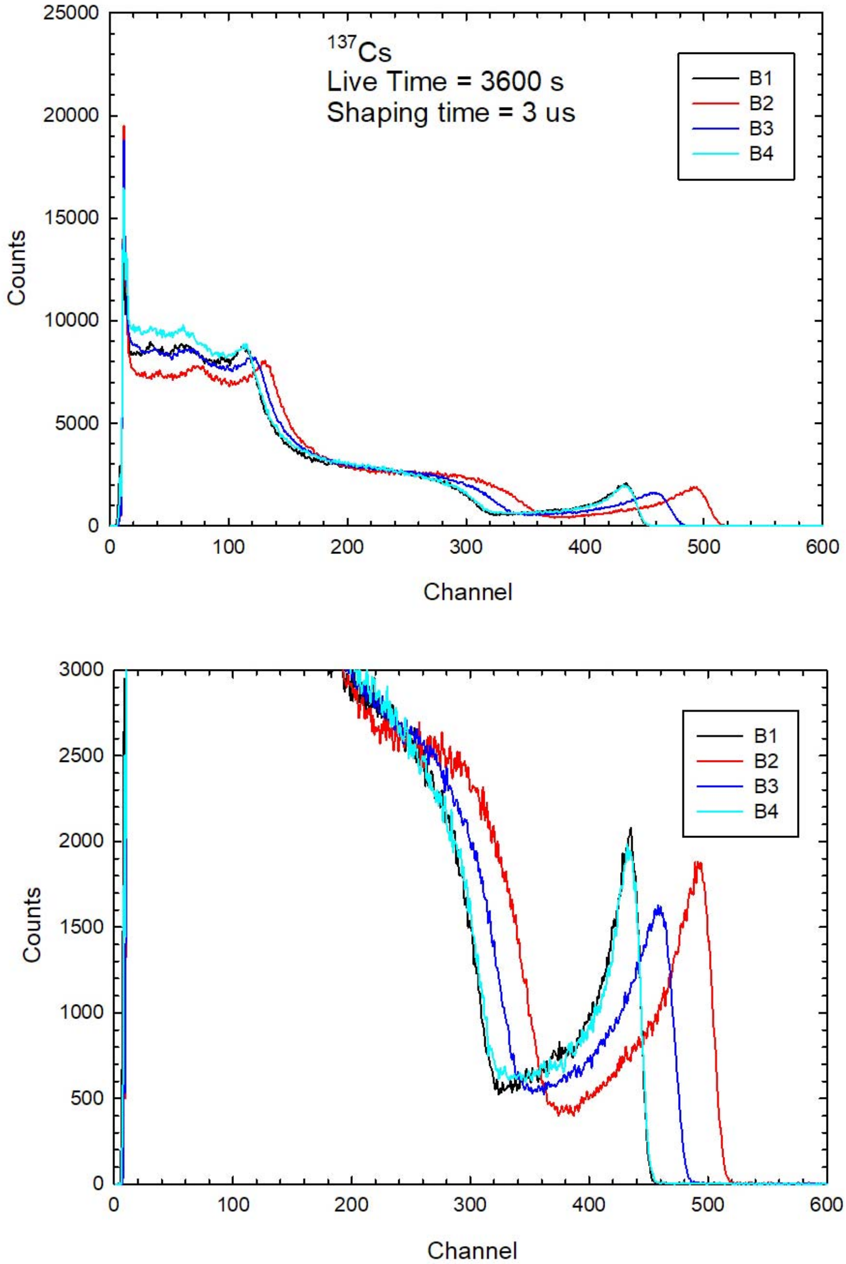
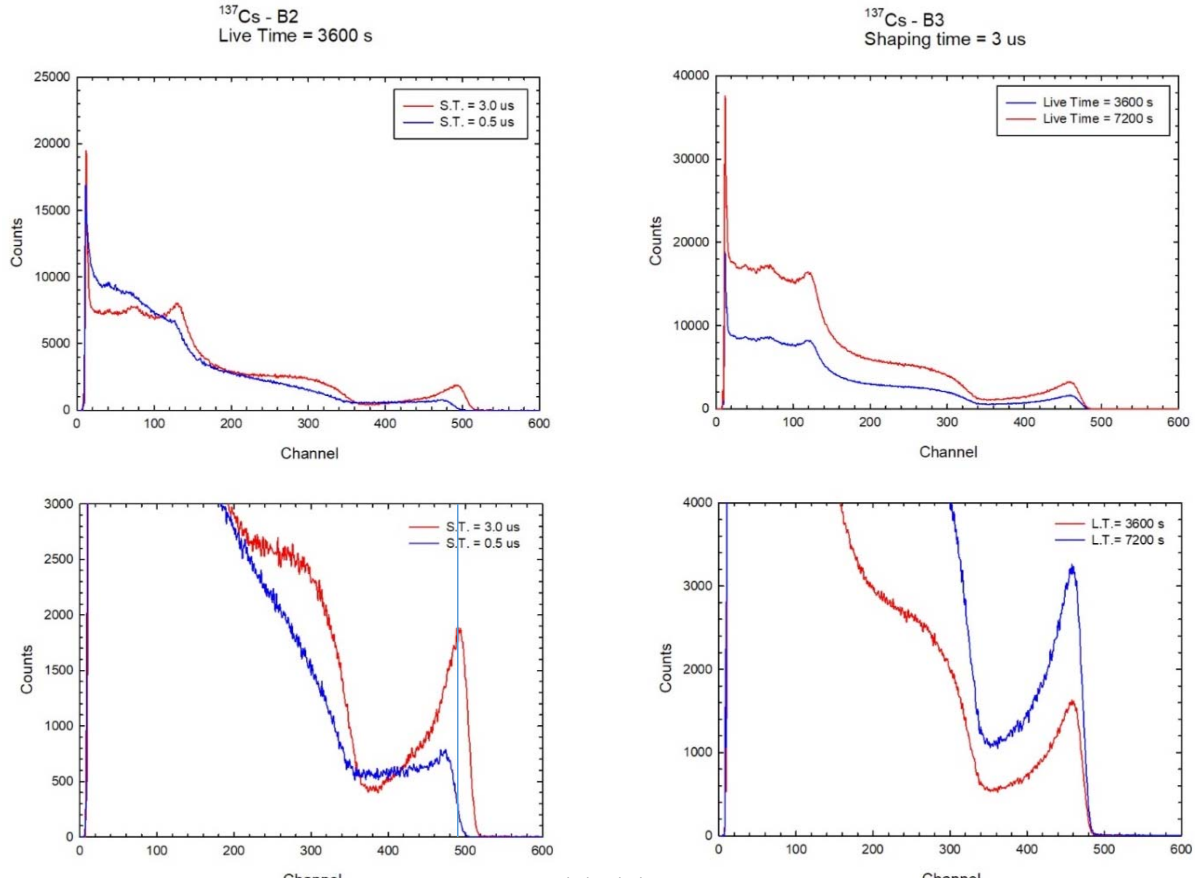


Figure 5. *CdTe sensor B, anode strip 1 to 4, 137Cs spectra obtained using 3 µs shaping and integrated over one hour live time.*

The signals from the 4 anodes of CdTe sensor B exhibit a bad intrinsic overall equalisation. The maximum shifting between the 662 keV peaks is of ~60 channels, i.e. ~14%. In this sensor the two border anodes (1 and 4) are really equalised both in gain (few channel shift for the peak) and in photo peak efficiency (~2% difference), while the two internal anodes (2 and 3) have quite different performance in gain and in photo peak efficiency. The (2,3) anodes have about 8% difference in gain and the photopeak efficiency differs ~5%. Both anodes 2 and 3 have less photo peak efficiency (6%-11%) than 1 and 4 ones. In fact, the differences in photo peak detection efficiency, between all the 4 anodes in sensor B, are of the same order (or slightly smaller) the ones we measured for the CdTe sensor A anode strips set.



(a) (b)

Figure 6. *(a) Anodes (2,3) of the CdTe sensor B: comparison of ^{137}Cs spectra obtained with fast (0.5 µs) and slow (3 µs) signal shaping.*

As stated in section before, in the Cactµs flight configuration each channels (i.e. anode signal) was shaped using two different time (fast and slow) by the amplifier chains. Therefore, we report in Figure 6a the comparison between the ^{137}Cs spectra obtained with sensor B, anode strip 2, setting the shaping time of the Ortec amplifier to 0.5 µs (fast) and 3 µs (slow), respectively. As expected the spectra taken using the "fast" shaping time exhibit a drastic decrease in photo peak efficiency (almost only electrons are collected), while the gain (photo peak channel) does not almost change (~3%). The loss in photo-peak efficiency is ~40% in the case of fast shaping compared to slow shaping.

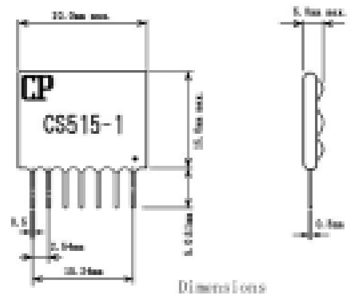
Figure 6b is given only to show the good proportionality with measurement live time of CdTe sensors. This figure compare the 137Cs spectra obtained reading out the anode 3 of the CdTe B sensor with "slow" shaping, but for two live acquisition times (3600 and 7200 s). The photo-peak integral counting ratio between the two measurements is exactly a factor 2 (within the counting statistical errors). The same ratio is confirmed for the total counts in the two spectra.

CLEAR-PULSE

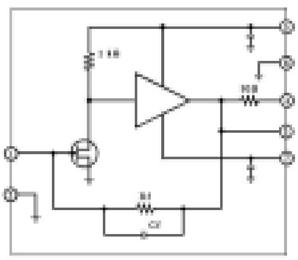
Hybrid IC Charge Sensitive Amplifier

Model CS515-1
CS515-2

Clear Pulse CS515 series Hybrid IC is developed as extended models to CS507 – CS513. CS515 enhances performances of CS507 in many aspects.
One of highlighted changes incorporated to CS515 is compact size that represents 50% reduced face size compared with CS507. This feature provides easier use to those applications, for which compact size is crucial.
Two different models are prepared in terms of feedback resistor/ capacitor combinations.
CS515-1 employs 1000 MΩ/ 1 pF combination that is best fit for CsI (Tl)/ PIN photo-diode scintillator application by reducing pile-up effect with lower time constant.
CS515-2 employs 4700 MΩ/ 0.5 pF combination that is for standard applications such as SSD, CdTe, and PIN photo-diode spectrometers.



Dimensions



Circuit Diagram

Major Specifications

	CS515-1	CS515-2
Charge Sensitivity	1 V/ pico-coulomb *	2 V/ pico-coulomb *
Noise (referred to input)	1.5 Kev (Si) fwhm (at 0 pF) *	1.2 Kev (Si) fwhm (at 0 pF) *
Noise Slope	15 eV/ pF (Si) *	15 eV/ pF (Si) *
Feedback Resistor	1000 MΩ	4700 MΩ
Feedback Capacitance	1 pF	0.5 pF
Output Impedance	Direct-out (less than 1Ω), and 50 Ω	
Power Required	+12 V 8 mA, -12V 3 mA	
Dimensions	7-pin Single-inline type Epoxy-mold 20 (W) x 15 (H) x 5 (D) mm (excluding pins)	

Remark *: At shaping time constant 2 micro-sec

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