DAY 53 – 100 DAYS VERIFICATION CHALLENGE

Topic: AXI Protocol

DAY 53 CHALLENGE:

1. Describe various input & output ports of AXI protocol?
2. Explain functioning of AXI protocol?
3. What is meant by AXI bus?
4. Where is AXI protocol used?
5. What is deadlock in AXI protocol?
6. What is the handshake in AXI?
7. What is AXI ordering?
8. What are the three types of AXI protocols?
9. What is register slice in AXI?
10. What is AXI fifo?
11. How many channels are in AXI protocol? Explain the operation of each channel in detail.
12. What is AXI interrupt controller?
13. Explain the AXI response types?
14. What is fixed burst type?
15. Explain the concept of AXI 4KB boundary condition?
16. Difference between AXI3 and AXI4?
17. What is the difference between AHB and AXI protocol?

Topic : AXI Protocol

Soln① Describe various input & output ports of AXI Protocol ?

- AMBA AXI PROTOCOL Signal

	Signal G	Source	DESCription
1.	AWID	Master	• write address ID.
2.	AWADDR	Master	• write address, The 1st address in a write Burst.
3.	AWLEN	Master	• Boust length, 1-16 transfer in a Boust.
4.	AWSIZE	Master	• Boust Size, 1,2---128 byte per transfer
5.	AWBRUST	Master	• Boust type, Fixed, incrementing or wrapping
6.	AWVALID	Master	• write address/Control valid.
7.	AWREADY	Slave	• write address/Control Accepted.
⑧	WID	Master	• write data ID, must watch AWID.
9.	WDATA	Master	• write data, can be 8,16---1024 bit wide.
10.	WSTRB	master	• write strobe, one strobe for each byte lane
11.	WLAST	master	• Last write transfer in a burst.
12.	WVALID	Master	• write data valid.
13.	WREADY	Slave	• write data accepted.
14	BID	~~master~~ Slave	• write data ID, must match AWID
15.	BRESP	~~master~~ Slave	• write response.
16.	BVALID	Slave	• write response valid.
17.	BREADY	master	• write response accepted
18.	ARID	Master	• Read Address ID
19.	ARADDR	master	• Read address, The 1st address in a read brust.
20.	ARLEN	master	• Boust length, 1-16 transfer in a Boust.
21.	ARSIZE	master	• Boust Size, 1,2---128 byte per transfer
22.	ARBURST	master	• Boust type. fixed incrementing or wrapping
23.	ARVALID	master	• Read address/Control valid.
24.	ARREADY	Slave	• Read address/Control accepted.

write address channel signal

write data channel signals

write Response channel signals

Read Address channel

			• Read data ID.
(25)	RID	slave	• Read data, can be 8, 16 --- 1024 bits wide
26.	RDATA	slave	• Read response
27.	RRESP	slave	• Last read transfer in a Burst.
28.	RLAST	slave	• Read data valid.
29.	RVALID	slave	• Read data accepted.
30.	RREADY	master	

Read data address

Soln ② Explain functioning OF AXI Protocol?

- AXI provides response signaling for both read & write transactions.
- for read transactions, the response information from the Subordinate is signaled on the read data channel using RRSEP (Response sig
- for write transaction, the response information is signaled on the write response channel using BRESP.

Soln ③ what is meant by AXI Bus?

- AXI Bus meant "advanced extensible interface"
- AXI Bus is high performance, point to point, master slave bus with five independent channel for write address, write data, write response, read address, read data used to connect on-chip peripheral circuits (or IP Blocks) to processor cores.
- AXI standard is produced by ARM, and it is open.

Soln ④ where is AXI protocol used?

- AXI protocol is widely used in System on chip designs, particularly in applications that require high speed & low latency data transfer Btw different components.

processor cores, CPU, Automative System etc.

AMBA AXI PROTOCOL

[ADVANCED EXTENSIBLE INTERFACE [AXI]]

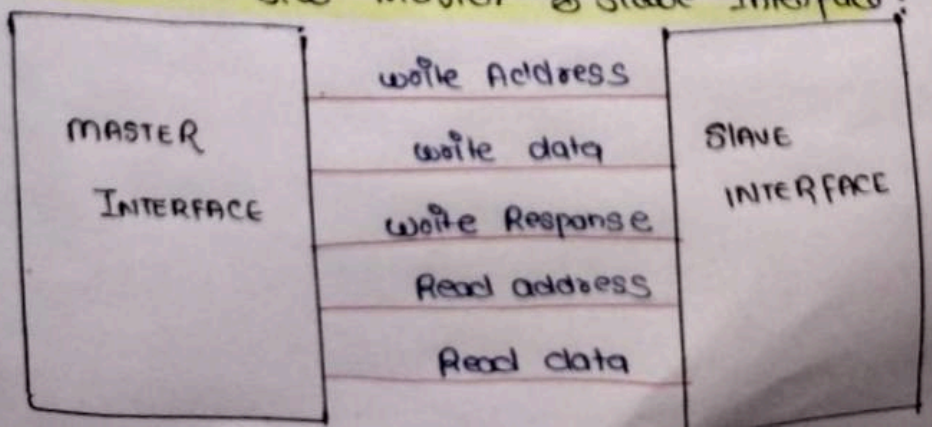
- AXI, the third generation OF AMBA interface AMBA ③ specification.
- its targated high performance. high clk frequency system design & suitable for high speed sub micrometter interconnect.

- **FEATURES OF AXI :-**
  - 5 channel (write address, write data , write response, read data/ response, read address).
  - on chip . point to point communication protocol
  - Burst based transaction with only start address issued.
  - 128 byte data bus width support
  - maximum 256 beat transfer in AXI4 , 16 beat (AXI3).
  - QOS (Quality of support , cache . protection , user support)
  - Separate address and control , data phases.
  - Support for unalgned data transfer using byte strobes.

◉ Burst types :

- The AXI Protocol supports three different burst types that are suitable for.
  1. normal memory access
  2. wrapping cache line bursts
  3. Streaming data to peripheral FIFO locations.

◉ Channel Connection Btw master & slave Interface :



Soln ⑤ what is deadlock in AXI protocol?

- In AXI protocol, deadlock can occur when there are multiple channels dependencies Btw them.
eg: if channel A depends on channel B & channel B depends on channel A.
- A deadlock can occuccen when both channels are trying to transmit data to each other but are unable to do so because of the circular dependencce.

Soln ⑥ what is handshake in AXI? [To complete transfer, valid=1, Redy=1]

- each of five independent channel consist of set of information signals. & uses a two way VALID & READY handshake mechanism. (VALID=1 means valid packet is being transferred).
- handshaking means transmit and receive the data from master and slave signal.
- The VALID signal goes from the source to the destination and Ready (READY) goes from the destination to the source.
- Ready indicate whether slave is ready or not to recive the nxt transction.

Soln ⑦ what is AXI ordering?

- The AXI protocol enable out-of-order transaction completion it gives ID tag to every transaction across the interface.
- The protocol requires the transactions with the same ID tag are completed in order, but transactions with different ID tags can be completed out of order.

Soln ⑧ what are the three types of AXI protocols?

① AXI4 : For high-performance memory-mapped requirements.

② AXI4 lite : For simple, low throughput memory-map communicatio

③ AXI4 stream : for high speed streaming data.

Soln ⑨ what is register slice in AXI ?

- The AXI Register slice can be used to register an AXI interconnect to provide timing isolation (at the cost of clk latency)
- A Register slice can be inserted at most any point in any channel, at the cost of an additional cycle of latency.

Soln ⑩ what is AXI FIFO ?

- The AXI Streaming FIFO Allows memory mapped acess to AXI Streaming interface. The core can be used to interface to the AXI Ethernet without the need to use DMA.
- The principal operation of this core allows the write or read of data packets to or from a device without any concern over the AXI Streaming interface.

Soln ⑪ How many channel are in AXI protocol ? Explain the operation of each channel in detail.

⊙ AXI Consist of five different channels:

① Read address channel
② write address channel
③ Read data channel
④ write data channel
⑤ write Response channel

- write address used to transmit the address / control signal to slave like length, Size of transfers etc.
- write data channel used to transmit the data and recive the response from slave, Read address
- is used to send the master to slave to read the data from slave.

Soln (12) what is AXI interrupt Controller?

- The AXI interrupt controller receives interrupt requests from these peripherals & sends them to the appropriate CPU core to be handled.
- It also manage the priority of interrupts & performs a classification process to determine which interrupts belong to which interrupt handling resource.

Soln (13) Explain the AXI Response types?

- In AXI write and Read Signal response are available.
- during write response separate channel is available whereas during read there is only one channel to send data response.
- every data tranfer has response whereas write response is followed by write transaction is completed.

Soln (14) what is fixed burst type?

- in a fixed burst, the address remains the same for every transfer in the Burst. This Burst type is for repeated access to the same location such as when loading or emptying a peripheral FIFO.

Soln (15) Explain the Concept of AXI 4KB boundary Condition?

- 4KB is the smallest area on AXI slave may occupy in the memory map.
- Therefore, if burst did cross a 4KB boundary, the access could start accesing one slave at the beginng of the burst and then switch to another on the Boundary.

Soln (16) Difference Btw AXI 3 and AXI 4 ?

AXI 3	AXI 4
① AXI 3 support fixed data width of 32, 64 & 128 bits.	① AXI4 retains the support for 32, 64 and 128 bit data width but introduce the capability to use 256 & 512 bit data as well.
② AXI3 does not support QoS	② AXI4 protocol support 4-bit QoS (Quality of Service).

Soln (17) what is the difference Btw AHB and AXI Protocol ?

AMBA AHB	AMBA AXI
① Single channel shared Bus.	① multi°-channel red/write optimized BUS
② A 128 bit bus running at 100MHz.	② A 64 bit bus running at 200MHz.
③ don't have seprate channel	③ Have Seperate channels & Separate handshaking.
④ write strobes are not Supported	④ write Strobe are Supports.