

Ques:6 exaple for \$cast in system Verilog.



```
1 class base_class;
2     function void print();
3         $display("calling from parent class");
4     endfunction
5 endclass
6
7 class child extends base_class;
8     function void print();
9         $display("calling from child class");
10    endfunction
11 endclass
12
13 module tb;
14     base_class base_o;
15     child ch1,ch2;
16     initial begin
17         ch1=new();
18         ch1.print();
19         base_o=new();
20         base_o = ch1;
21         base_o.print();
22         if($cast(ch2,base_o))begin
23             $display("casting is successfull");
24             ch2.print();
25         end
26         else
27             $error("casting is unsuccessfull");
28     end
29 endmodule
```

-timescale 1ns/1ns

Run Options

-voptargs=+acc=npr

Run Time: 10 ms

- ☐ Use run.do Tcl file
- ☐ Use run.bash shell script
- ☐ Open EPWave after run
- ☐ Show output file after run
- ☐ Download files after run

Examples

Community

Log


Share

```
# Loading work.tb(fast)
#
# vsim -voptargs=+acc=npr
# run -all
# calling from child class
# calling from parent class
# casting is successfull
# calling from child class
# exit
# End time: 00:06:45 on Dec 18,2023, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
```

Done

Ques:7 Example for static variable in system Verilog.

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▼ Languages & Libraries

Testbench + Design

SystemVerilog/Verilog ▼

UVM / OVM ?

None ▼

Other Libraries ?

More

testbench.sv

```
1 class sample;
2   static int var1 = 50;
3   static int var2 = 200;
4 endclass
5
6 module tb;
7   initial begin
8     $display("\tsample::var1=%0d",sample::var1);
9     $display("\tsample::var2=%0d",sample::var2);
10  end
11 endmodule
12
13
```

-timescale 1ns/1ns

Run Options ?

-voptargs=+acc=npr

Run Time: 10 ms

☐ Use **run.do** Tcl file

☐ Use **run.bash** shell script

☐ Open **EPWave** after run

☐ Show output file after run

☐ Download files after run

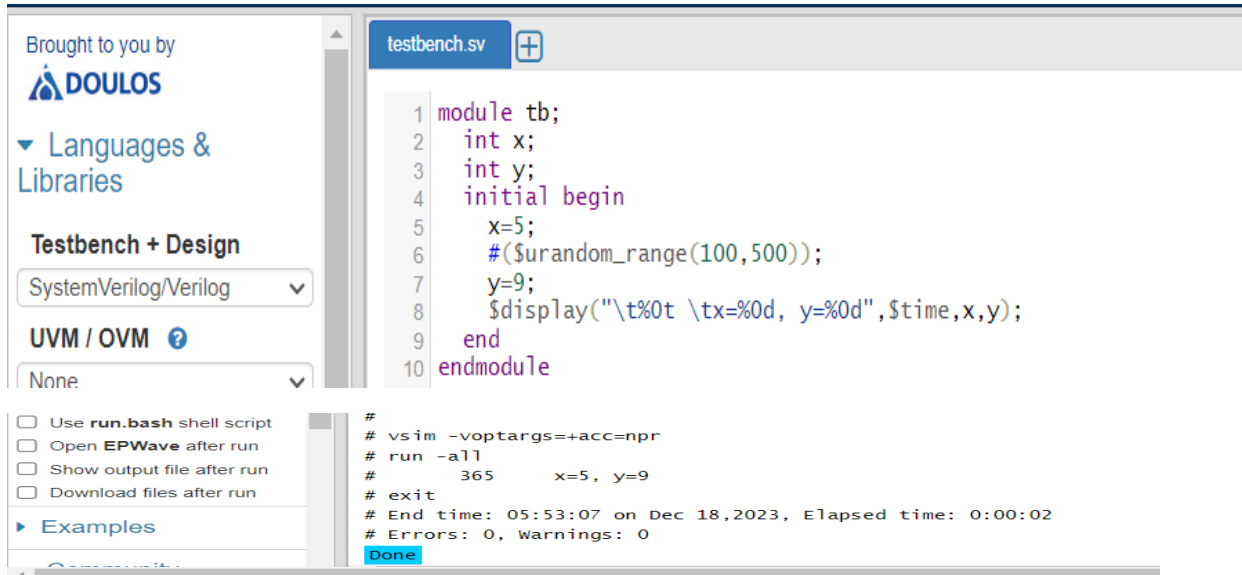
► Examples

Community

Log Share

```
"""
# Loading sv_std.std
# Loading work.testbench_sv_unit(fast)
# Loading work.tb(fast)
#
# vsim -voptargs=+acc=npr
# run -all
#     sample::var1=50
#     sample::var2=200
# exit
# End time: 05:34:48 on Dec 18,2023, Elapsed time: 0:00:01
# Errors: 0, Warnings: 0
Done
```

Ques:15 Write SV code to wait for a random delay in range 100 to 500ns.



Ques:16 Wrie a code to extract 5 elements at a time from a queue.

