

## Day:80

### Topic: System Verilog Trick Codes

#### Ques:1 What is the Problem with below code snippet?

```
/*BusTran b;  
  
    b = new();  
  
    repeat(n)begin  
  
        b.addr = $random();  
  
        $display("Sending addr=%h",b.addr);  
  
        transmit(p);  
  
    end  
  
endtask*/
```

The screenshot displays the Mentor Questa 2021.3 IDE interface. On the left, the 'Languages & Libraries' panel shows 'Testbench + Design' set to 'SystemVerilog/Verilog', 'UVM / OVM' set to 'None', and 'Other Libraries' including 'OVL 2.8.1' and 'SVUnit 2.11'. The 'Compile Options' panel shows 'timescale 1ns/1ns' and 'Run Options' with 'voptargs=+acc=npr'. The 'Run Time' is set to '10 ms'. The main editor shows a file named 'testbench.sv' with the following code:

```
1 class BusTran;  
2     rand bit addr;  
3 endclass  
4  
5 module top;  
6     task generator_example(int n);  
7         BusTran b;  
8         b = new();  
9         repeat(n)begin  
10            b.addr = $random();  
11            $display("Sending addr=%h",b.addr);  
12            transmit(p);  
13        end  
14    endtask  
15  
16 endmodule
```

The bottom panel shows the 'Log' window with the following output:

```
QuestaSim-64 vlog 2021.3 Compiler 2021.07 Jul 13 2021  
Start time: 04:39:03 on Jan 17, 2024  
vlog -mfcu design.sv testbench.sv -work qrun.out/work -csession=incr -writesessionid "+qrun.out/top_dus" -statslog qrun.out/stats_log  
-- Compiling package design_sv_unit  
-- Compiling module top  
** Error: testbench.sv(12): (vlog-2730) Undefined variable: 'p'.  
End time: 04:39:03 on Jan 17, 2024, Elapsed time: 0:00:00  
Errors: 1, Warnings: 0  
child process exited abnormally  
End time: 04:39:03 on Jan 17, 2024, Elapsed time: 0:00:00  
...
```

## Ques:2 Output of Below code

```
/*class constraint_example;
```

```
    rand bit[15:0]a,b,c;
```

```
    constraint c1{0<a<b<c;}*/
```

The screenshot displays the Mentor Questa 2021.3 IDE interface. On the left, the 'Languages & Libraries' panel is visible, showing the 'Testbench + Design' section with 'SystemVerilog/Verilog' selected. Below this, the 'UVM / OVM' section is set to 'None', and the 'Other Libraries' section lists 'OVL 2.8.1' and 'SVUnit 2.11'. The main editor window shows the Verilog code for 'testbench.sv'. The code defines a class 'constraint\_example' with a constraint 'c1' that requires '0 < a < b < c'. The 'top' module instantiates this class and uses the '\$display' function to print the values of 'a', 'b', and 'c'.


```
1 //Output of Below code
2
3 class constraint_example;
4     rand bit[15:0]a,b,c;
5
6     constraint c1{
7         0<a<b<c;
8     }
9 endclass
10 module top;
11     constraint_example e;
12     initial begin
13         e=new();
14         e.randomize();
15         $display("\toutput of code is\n\ta=%0d,\n\tb=%0d,\n\tc=%0d",e.a,e.b,e.c);
16     end
17 endmodule
```

Below the code editor, the 'Log' tab is active, showing the execution output. The output indicates that the code ran successfully with no errors or warnings. The values of 'a', 'b', and 'c' are printed as 57250, 2031, and 48175, respectively. The summary shows 0 errors and 1 warning for the Verilog compilation.

```
#
# run -all
#     Output of code is
#     a=57250,
#     b=2031,
#     c=48175
# exit
# End time: 04:49:24 on Jan 17,2024, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# *** Summary *****
# qrun: Errors: 0, Warnings: 0
# vlog: Errors: 0, Warnings: 1
```

### Ques:3 Output of Below code:

Brought to you by

 DOULOS

▼ Languages & Libraries

Testbench + Design

SystemVerilog/Verilog ▼

UVM / OVM ?

None ▼

Other Libraries ?

None  
OVL 2.8.1  
SVUnit 2.11

☐ Enable TL-Verilog ?

☐ Enable Easier UVM ?

☐ Enable VUnit ?

▼ Tools & Simulators ?

testbench.sv

```
1 //Output of Below code:
2
3 module top;
4     initial begin
5         $display("\t@%0d: start fork...join example",$time);
6         #10 $display("\t@%0d: sequential after #10",$time);
7     fork
8         $display("\t@%0d: parallel start",$time);
9         #50 $display("\t@%0d: parallel after #50",$time);
10        #10 $display("\t@%0d: parallel after #10",$time);
11    begin
12        #30 $display("\t@%0d: sequential after #20",$time);
13        #10 $display("\t@%0d: sequential after #10",$time);
14    end
15    join
16    $display("\t@%0d: after join",$time);
17    #80 $display("\t@%0d: final after #80",$time);
18 end
19 endmodule
```

☐ Enable Easier UVM ?

☐ Enable VUnit ?

▼ Tools & Simulators ?

Mentor Questa 2021.3 ▼

Compile Options ?

-timescale 1ns/1ns

Run Options ?

-voptargs=+acc=npr

Run Time: 10 ms

☐ Use **run.do** Tcl file

☐ Use **run.bash** shell script

☐ Open **EPWave** after run

☐ Show output file after run

☐ Download files after run

Log

Share

```
# run -all
#      @0: start fork...join example
#      @10: sequential after #10
#      @10: parallel start
#      @20: parallel after #10
#      @40: sequential after #20
#      @50: sequential after #10
#      @60: parallel after #50
#      @60: after join
#      @140: final after #80
# exit
# End time: 05:04:59 on Jan 17,2024, Elapsed time: 0:00:00
# Errors: 0, Warnings: 0
# *** Summary *****
#      grun: Errors:    0, Warnings:    0
#      vlog: Errors:    0, Warnings:    0
```

