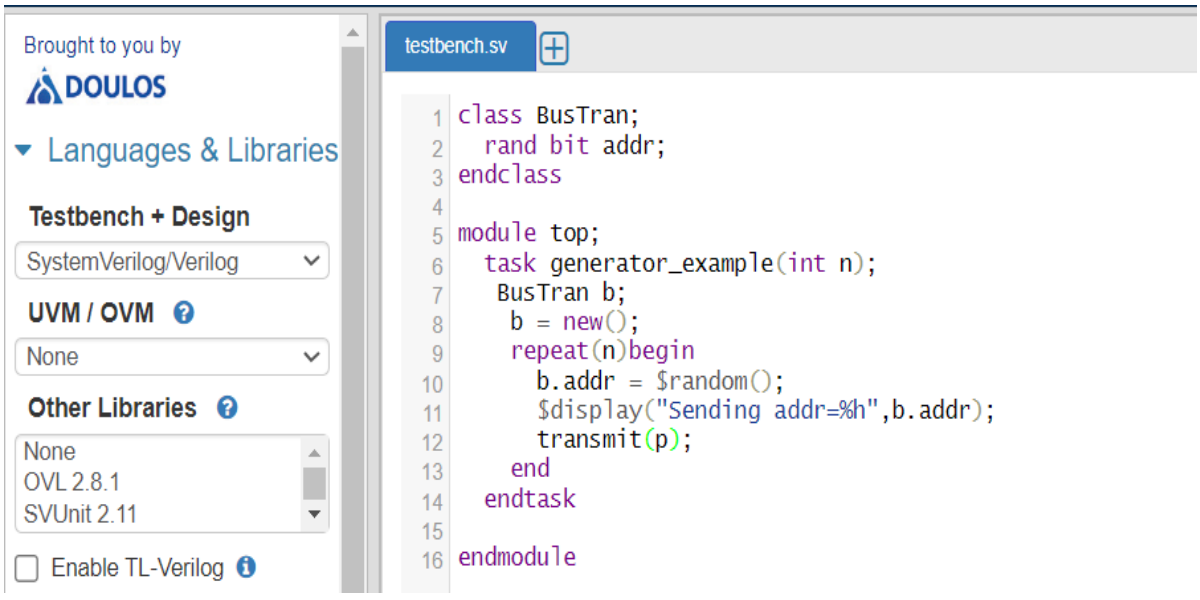
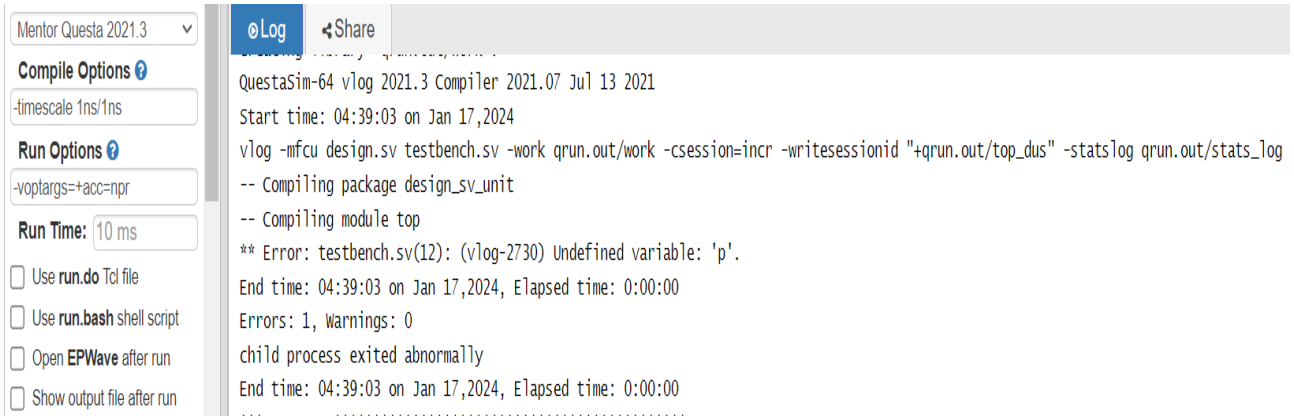
Day:80

Topic: System Verilog Trick Codes

Ques:1 What is the Problem with below code snippet?

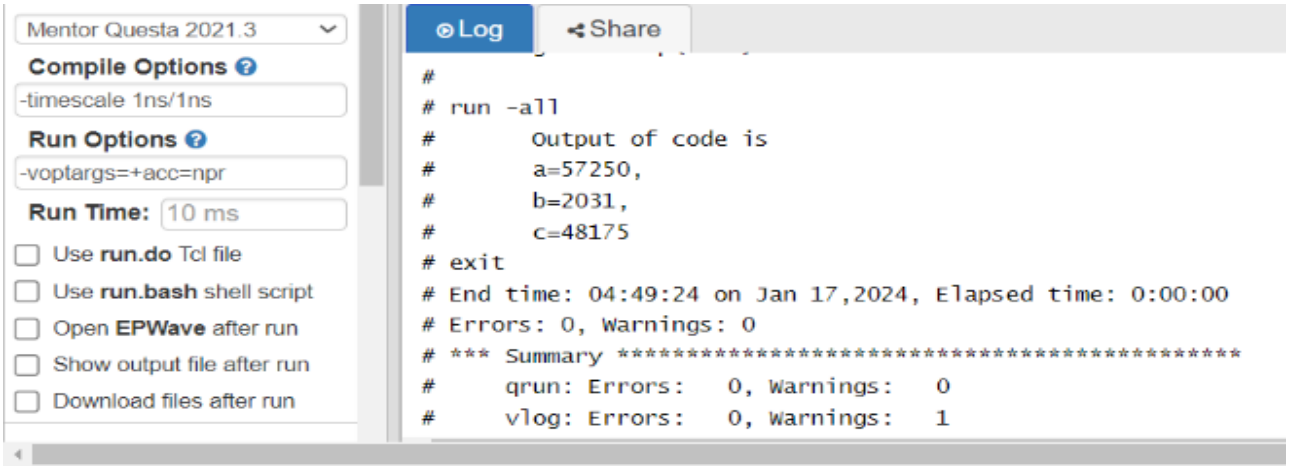
```
/*BusTran b;
    b = new();
    repeat(n)begin
      b.addr = $random();
      $display("Sending addr=%h",b.addr);
      transmit(p);
    end
  endtask*/
```





Ques:2 Output of Below code

```
/*class constraint_example;
  rand bit[15:0]a,b,c;
  constraint c1{0<a<b<c;}*/
```



Ques:3 Output of Below code: