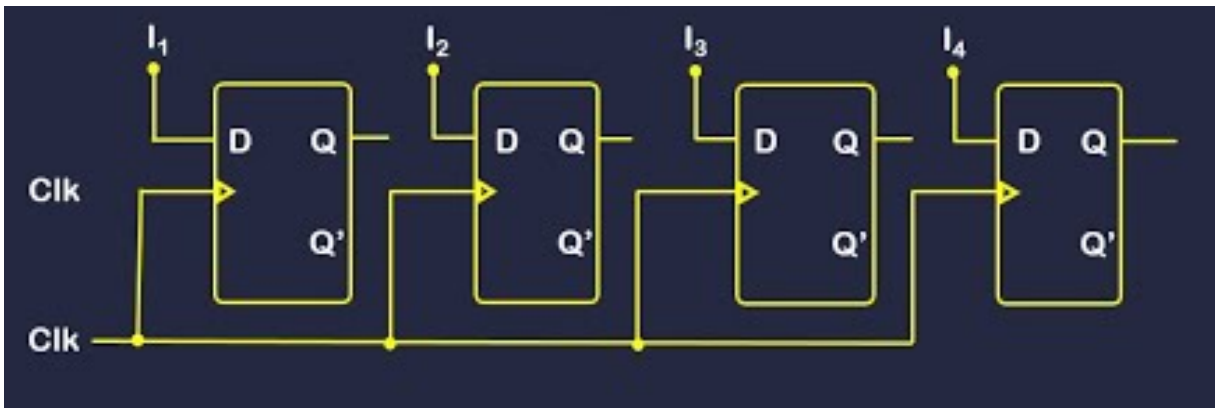


1) 4-bit Synchronous Up counter:

- A four-bit synchronous up counter is a digital circuit that counts in binary from 0000 to 1111 (0 to 15) and increments by 1 for each clock pulse.
- The counter has four flip-flops, one for each bit of the count, and it counts up in a synchronous manner, meaning all the flip-flops change their states simultaneously on the rising edge or falling edge of the clock signal.

Circuit Diagram:



Verilog Code:

```
module four_bit_synchronous_up_counter(clk,rst,count);
input clk,rst;
output reg [3:0]count;
initial
count=0;
always @(posedge clk)
begin
if(rst)
count=0;
else
count=count+1;
end
endmodule
```

Test Bench:

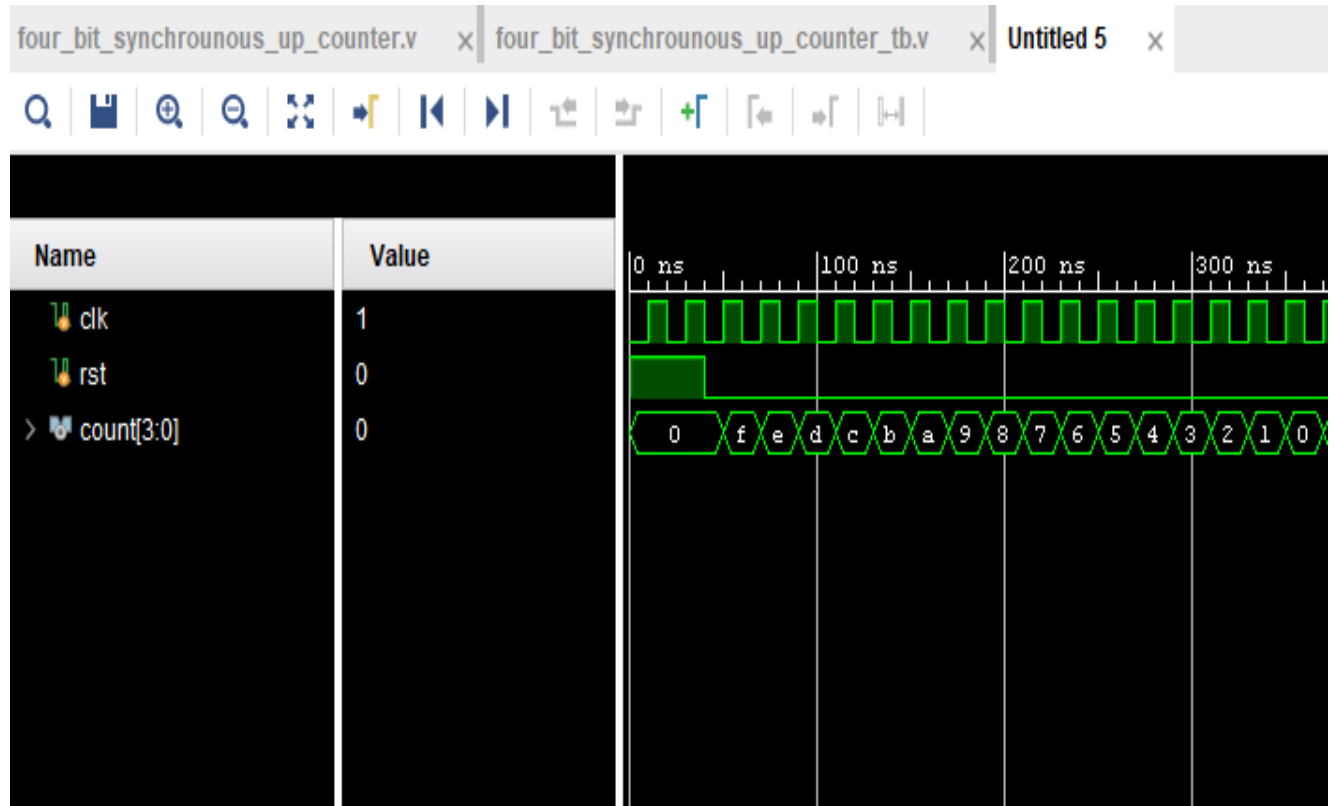
```
module four_bit_synchronous_up_counter_tb();
reg clk,rst;
wire [3:0]count;
four_bit_synchronous_up_counter uut(clk,rst,count);
initial
begin
clk=0;
rst=1;
#40 rst=0;
end
```

```

always
#10 clk=~clk;
initial
#1000 $finish();
endmodule

```

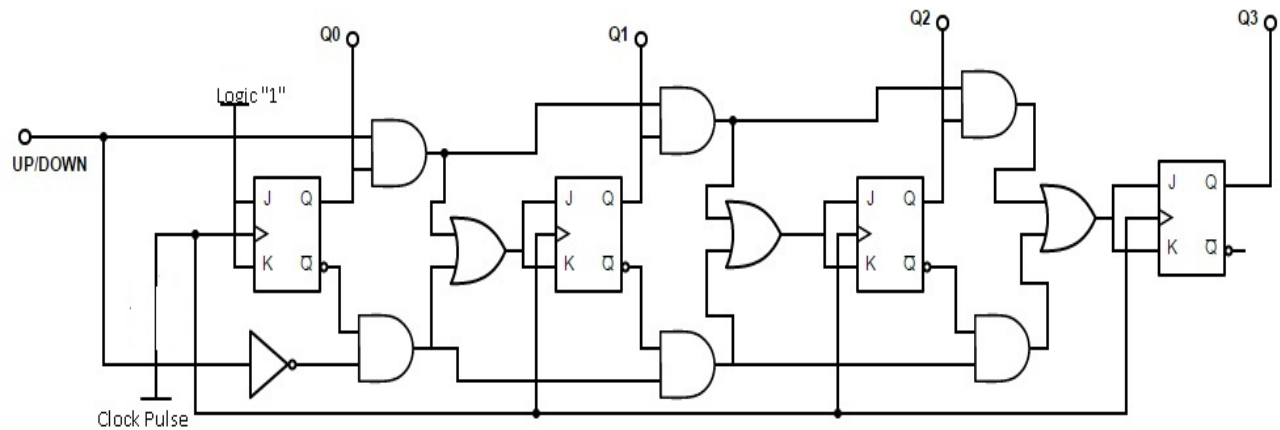
Waveforms:



2)Up/Down Counter:

- An up/down counter is a digital electronic device that can count either up or down depending on the control signal.
- It can increment or decrement its count based on the input signals it receives.
- The control signal (commonly denoted as UP/DOWN) determines the direction of the counting process.
- When it's set to '1', the counter counts up; when set to '0', the counter counts down.

Circuit Diagram:



Verilog Code:

```
module updowncounter(clk,rst,updown,count);
input clk,rst,updown;
output reg [3:0]count;
initial
count=0;
always @(posedge (clk) or posedge (rst))
begin
if (rst==1)
count<=0;
else
if (updown==1)
if (count==15)
count<=0;
else
count<=count+1;
else
if(count==0)
count<=15;
else
count<=count-1;
end
endmodule
```

Test Bench:

```
module updown_tb();
wire [3:0]count;
reg clk,rst,updown;
updowncounter uut(clk,rst,updown,count);
initial
```

```

begin
clk=0;
end
always
begin
#10 clk=~clk;
end
initial
begin
rst=0;
upordown=0;
#300 upordown=1;
#300
rst=1;
upordown=0;
#300
rst=0;
end
initial
#3000 $finish();
endmodule

```

Waveforms:

