Memory Power Tracing on Hybrid Memory Cube

CS5352 Course Project, Fall 2018

Contact

Xi Wang (xi.wang@ttu.edu)

Description

Memory access patterns in data-intensive applications have significant impacts on the performance of HPC. The irregular memory footprints will result in the high miss rate in both cache and Transaction Look-aside Buffer (TLB), which subsequently leads to the high memory access latency and power consumptions.

Targeting at this problem, there are many existing efforts trying to the hide or reduce the memory access latency, such as the dynamic memory coalescing. However, only a few of them investigated the memory power consumptions savings benefited by the memory system optimization, such as the dynamic memory coalescing, prefetching, etc.

Therefore, in this project, we will investigate the impacts of the memory accesses on the power consumptions in an advanced memory devices named hybrid memory cube (HMC). The memory traces with/without the memory coalescing will be provided as the input file and the HMC-Sim simulation infrastructure will be utilized for testing. HMC-Sim is designed to track the memory access latency and power consumptions of HMC based on the provided memory traces. The HMC-Sim also provides the visualization tools that automatically plots the figures and generates the videos.

* This project is a part of the ongoing memory system research and your contribution will be included in the publication, which will benefit your master thesis/project.

Requirements

- Knowledge of C programming
- Knowledge of Memory Systems
- Learn to play with the tool HMC-Sim

References

- http://gc64.org/?page_id=225
- http://gc64.org/?page_id=56
- https://cs.stackexchange.com/questions/18229/what-is-memory-coalescing
- http://delivery.acm.org/10.1145/3230000/3225062/a62-wang.pdf?ip=129.118.162.126&id=3225062&acc=ACTIVE%20SERVICE&key=B63ACEF81C6334F5%2E97433694AFE6D246%2E4D4702B0C3E38B35%2E4D4702B0C3E38B35&__acm__=1538166499_91903d2470e20094d77a9f391162c5ba